Latest Tests performed at DESY Zeuthen with TDC v767 board

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Goal

- Agree in the acquisition mode for the TDCs in BCM1F
- Find out a way to avoid FIFO overflow when data rate is too high
- Give final numbers to get an idea about the possible data loss due to Memory limitations and data transfer bottlenecks in the DAQ setup.

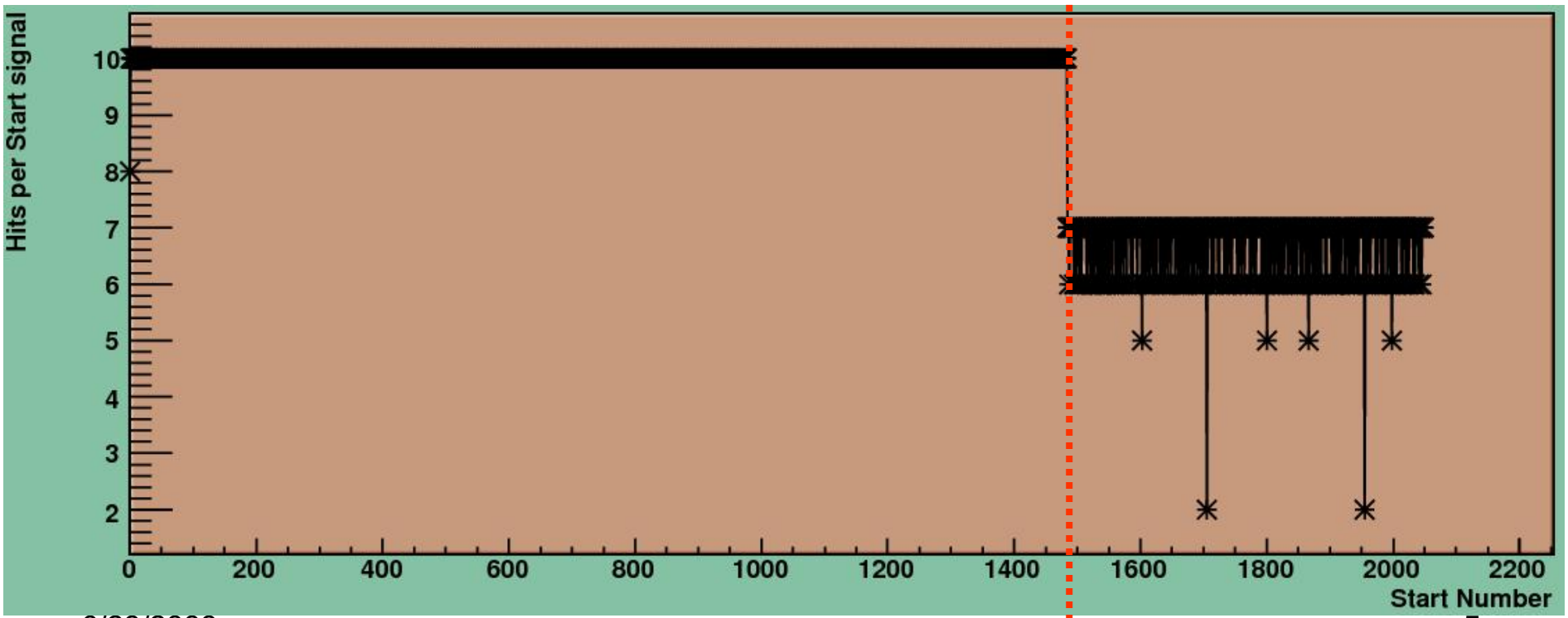
Acquisition Mode

- Continuous Storage seems to be the more convenient since the Hit time information can be given with respect with a given Trigger (orbit Trigger)
- Stop Trigger Matching Mode working fine and ready to be used if neccesary (use of time window)

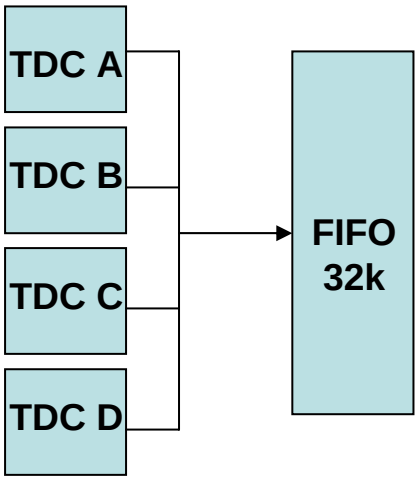
Avoid FIFO overflow

- By VETOing the ouput of the discriminators that feed the TDC board: We loose hits in an orbit but we do not loose sincronization and averaging the data allow us to reconstruct picture for entire orbit
- VETO signals available in TDC board:
  - BUSY→ON if the FIFO if full
  - DREADY→ON if Buffer Almost Full. Disadvantage: misuse of FIFO since at least half of it stays empty. Advantage: some marging to store data until the electric signal vetoes the TDCs input.

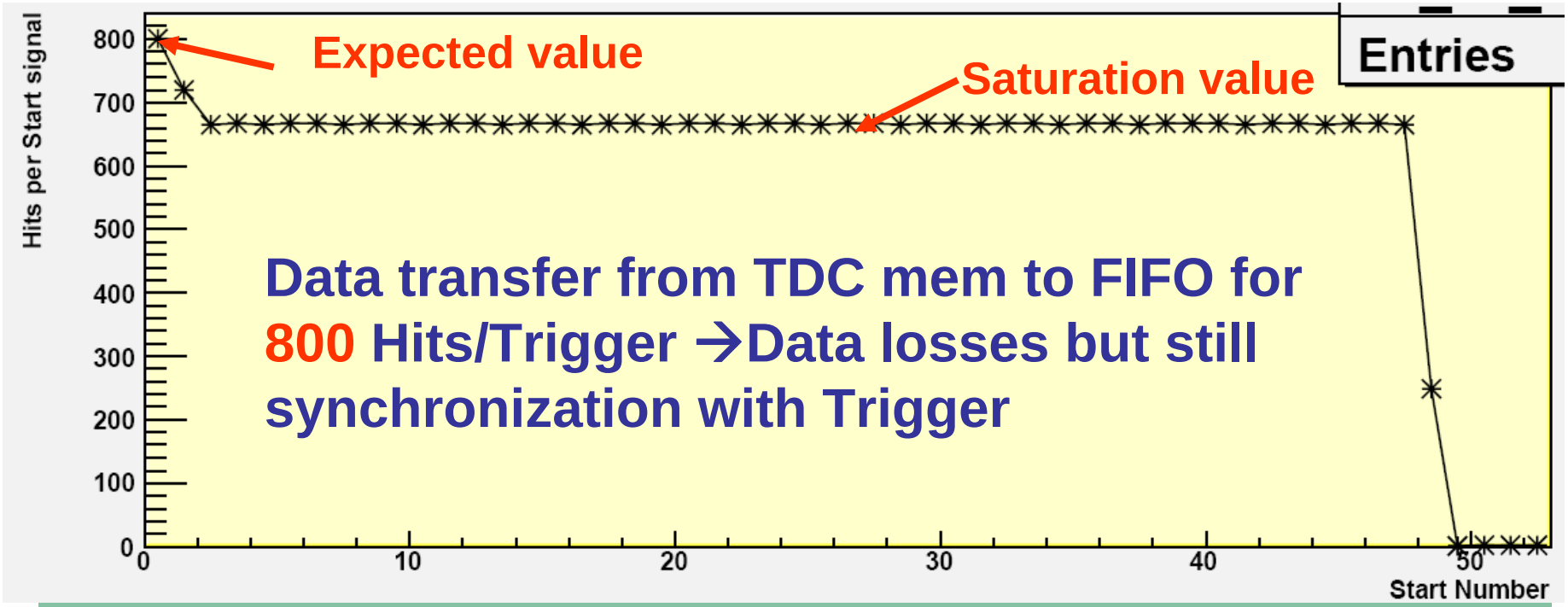
- VETO = DREADY
  - Buffer Almost Full Level=0x3FFF (~16000 half the FIFO size and maximum level allowed)
  - 10 Hits/Trigger

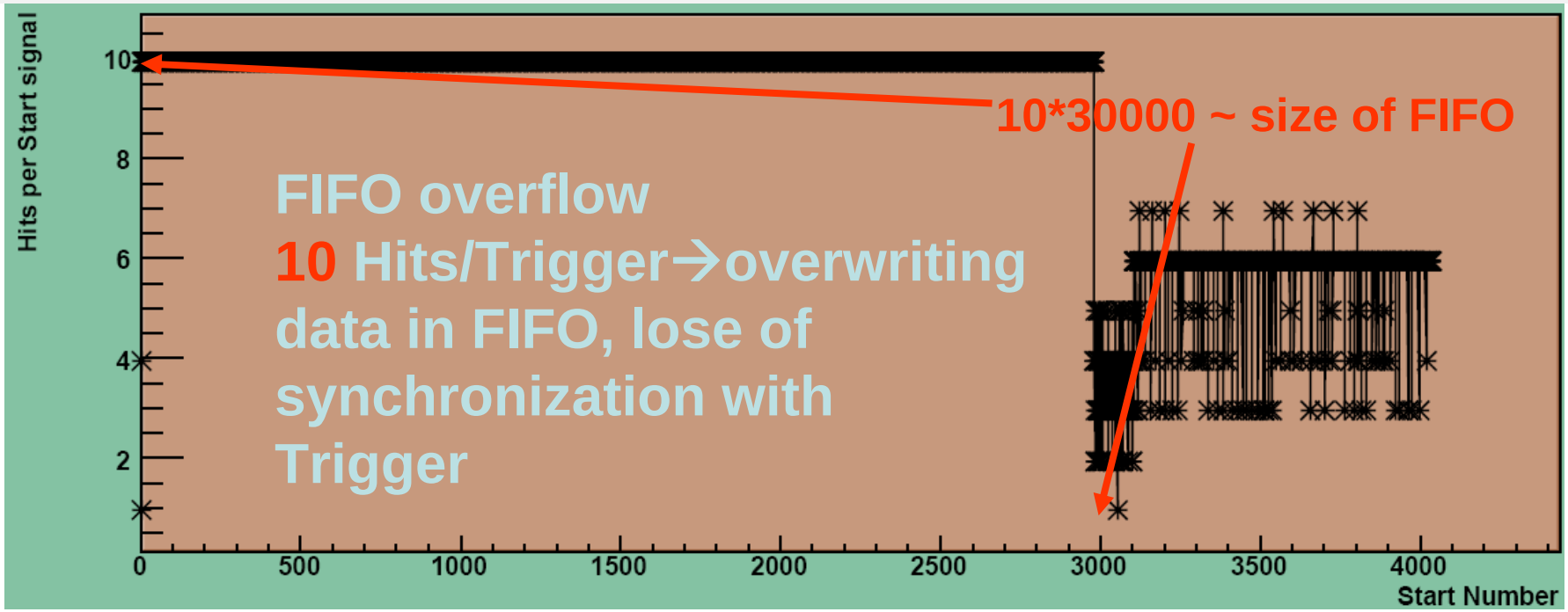


Hit rate limits in the transfer of data from 256 32bit buffer to 32k 32bit FIFO

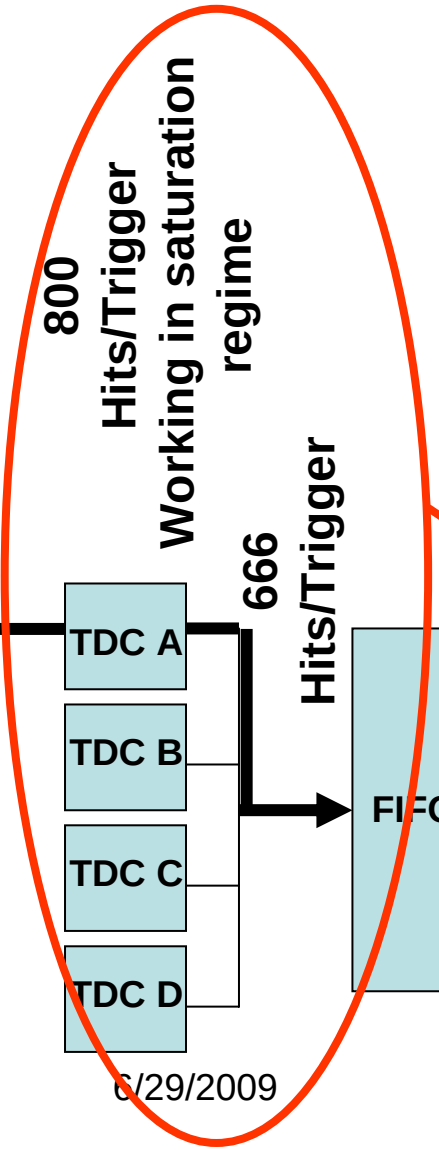


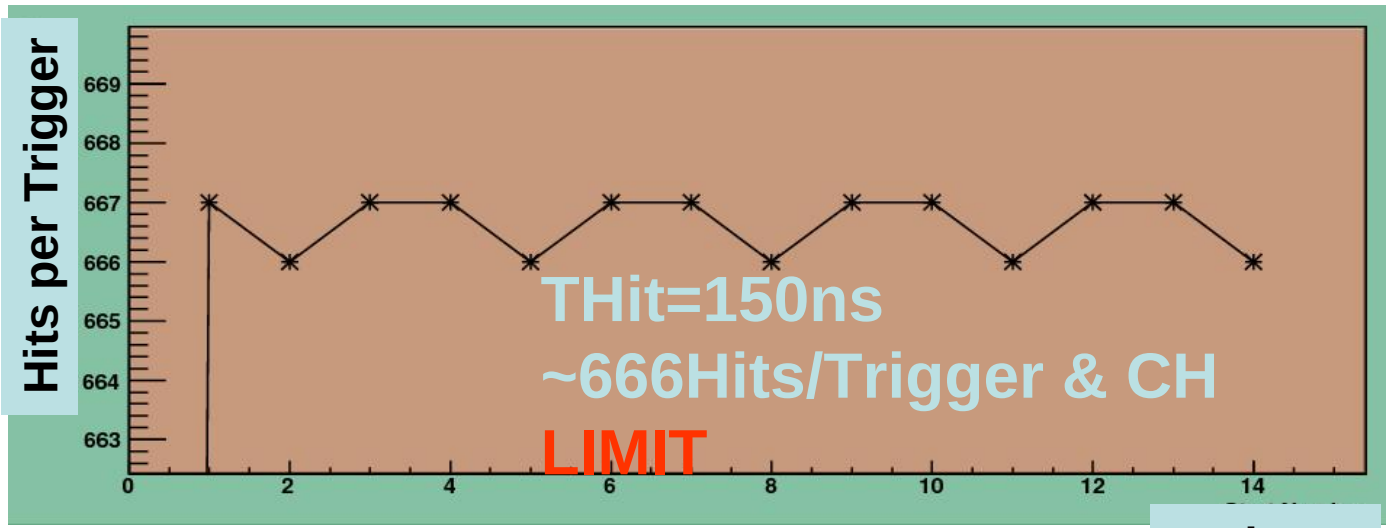
- Tests performed:
  - See hit rate limit with 1 channel in 1 TDC
  - Working above the limit (with data losses, saturation regime) use several CHs in different TDCs and see how the bus deals with the data flowing to the FIFO (common output buffer)

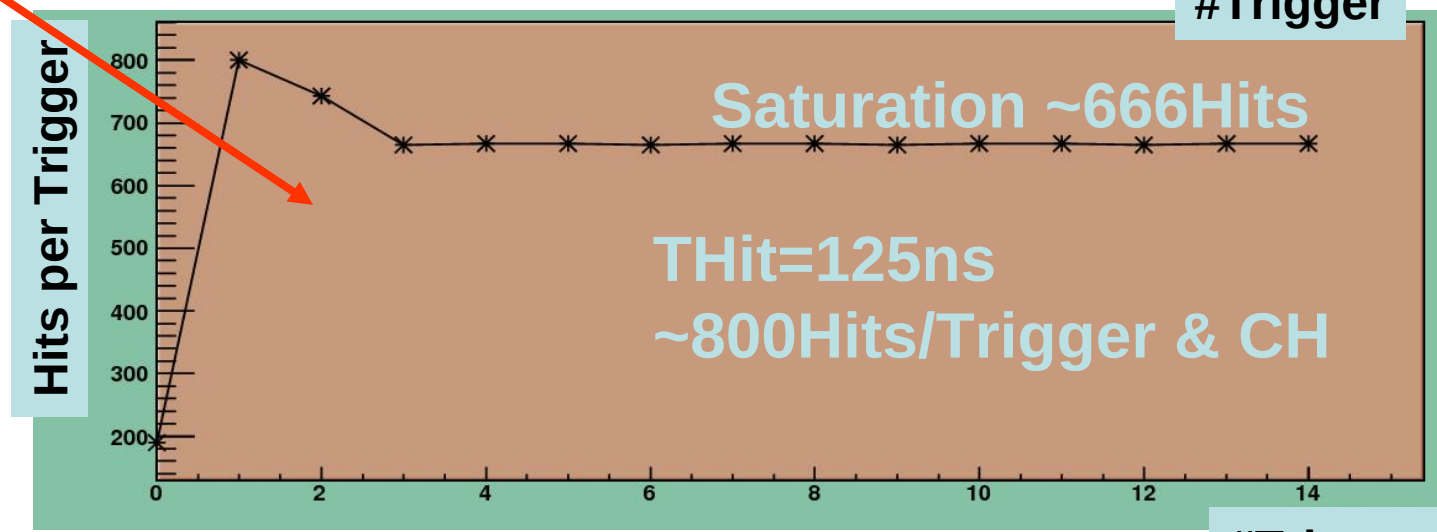

Hits per Start signal
Entries
Expected value
Saturation value
Data transfer from TDC mem to FIFO for
800 Hits/Trigger →Data losses but still
synchronization with Trigger
Start Number


Hits per Start signal
10*30000 ~ size of FIFO
FIFO overflow
10 Hits/Trigger→overwriting
data in FIFO, lose of
synchronization with
Trigger
Start Number

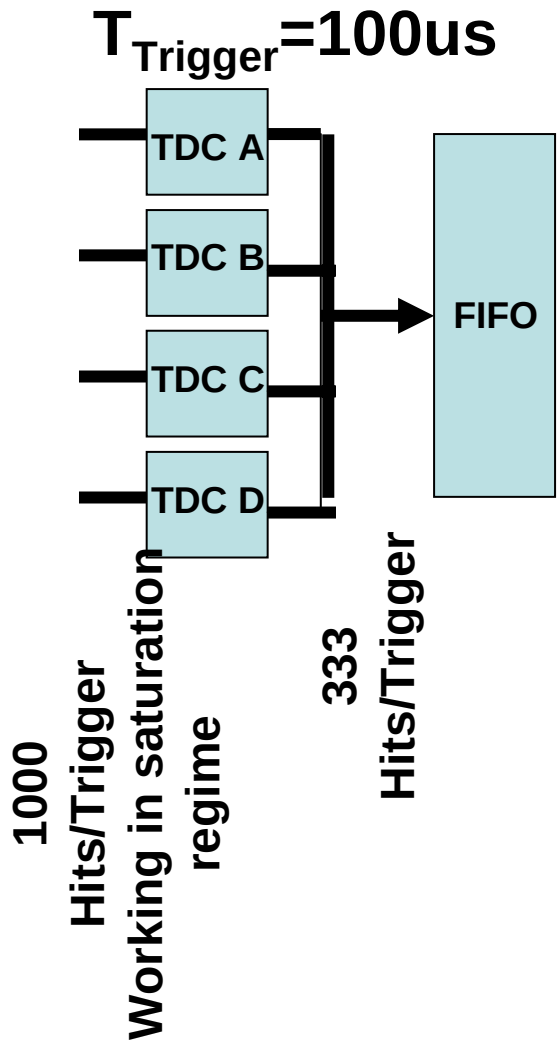
Single channel enabled in 1 TDC

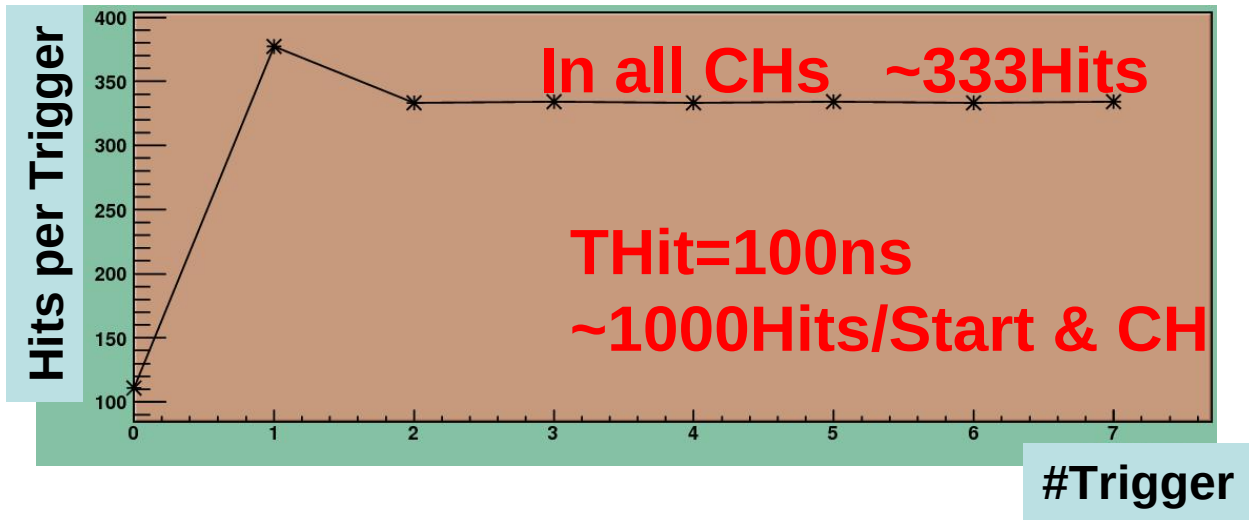






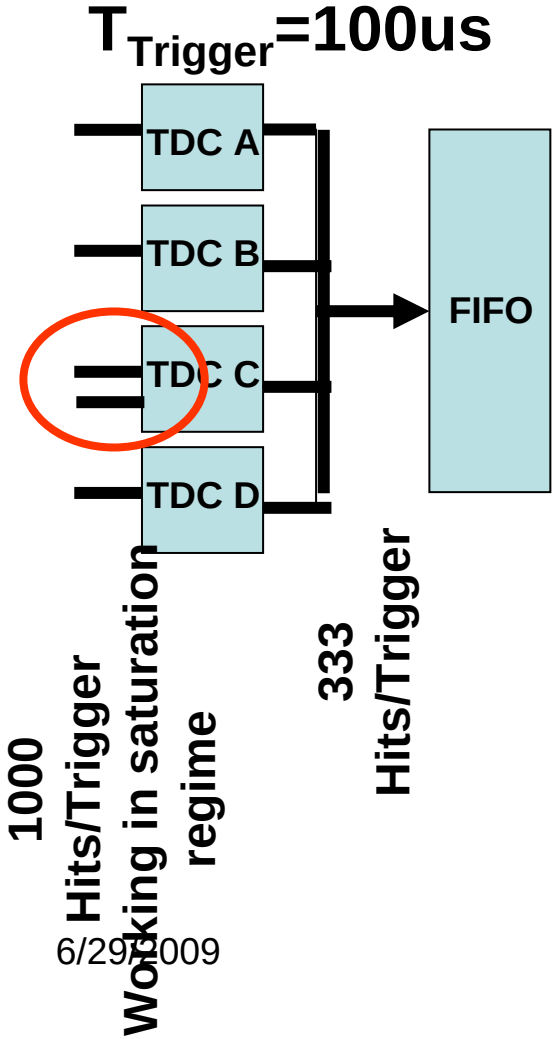
1 channel enabled per TDC

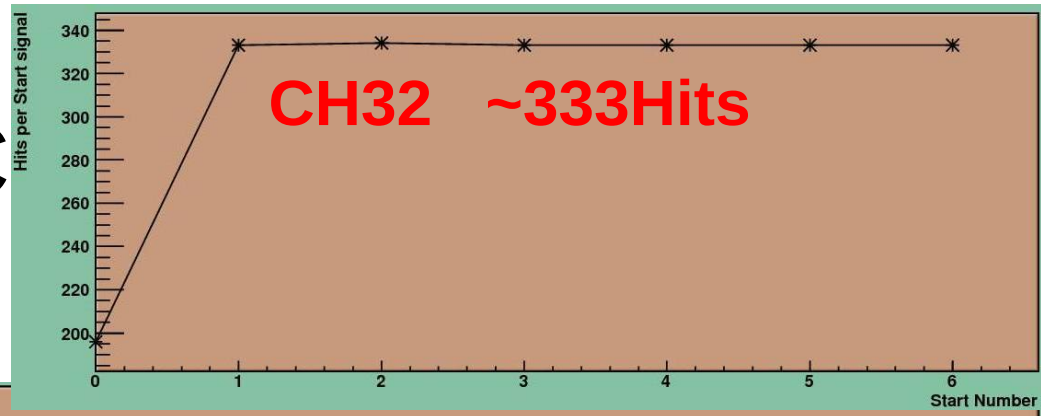


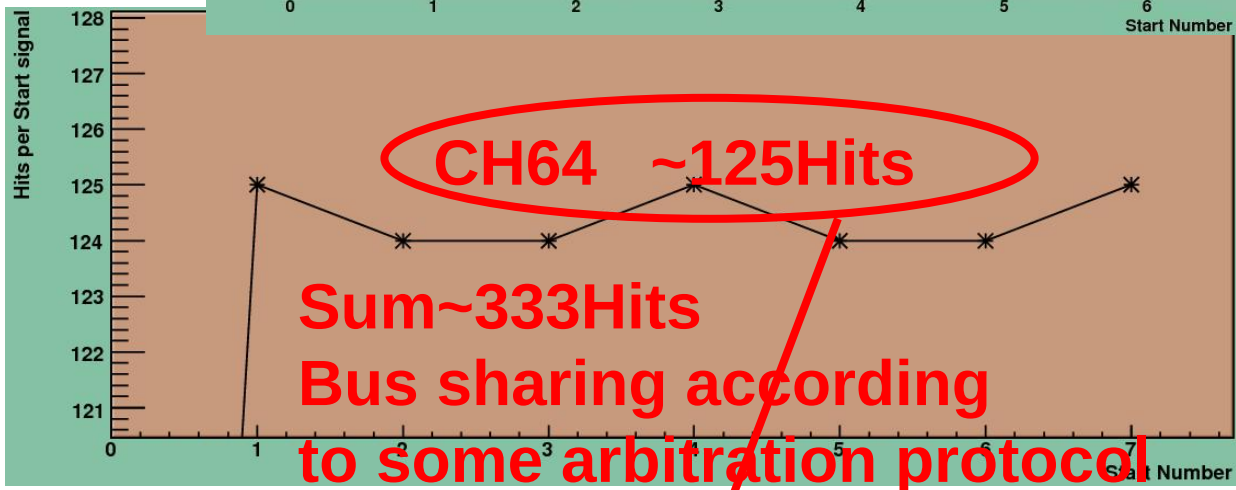


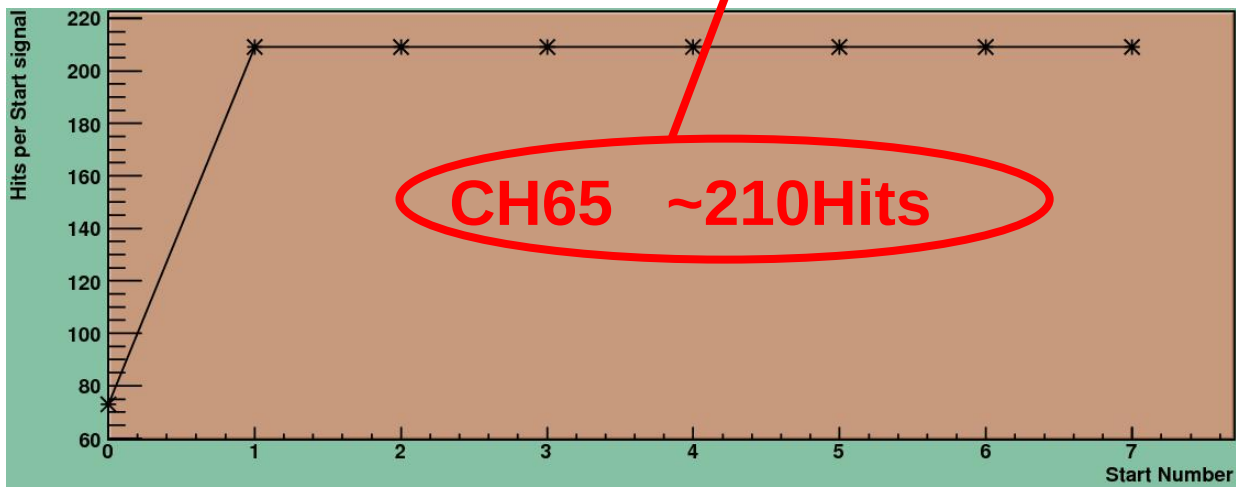
THit~100us/333 Hits = 300ns per chip
Maximum rate when 4 TDCs are working in parallel with a single Channel enabled

2 channels enabled in a TDC 1 in the rest









Still to study

- **Block Transfer mode:** Since it is the fastest way to transfer data we can use this mode to check the VME maximum rate for data transfer.

(In single readout mode, to transfer 32k words through the VME we need around:

32k*100ns (1vme cycle)~4ms)