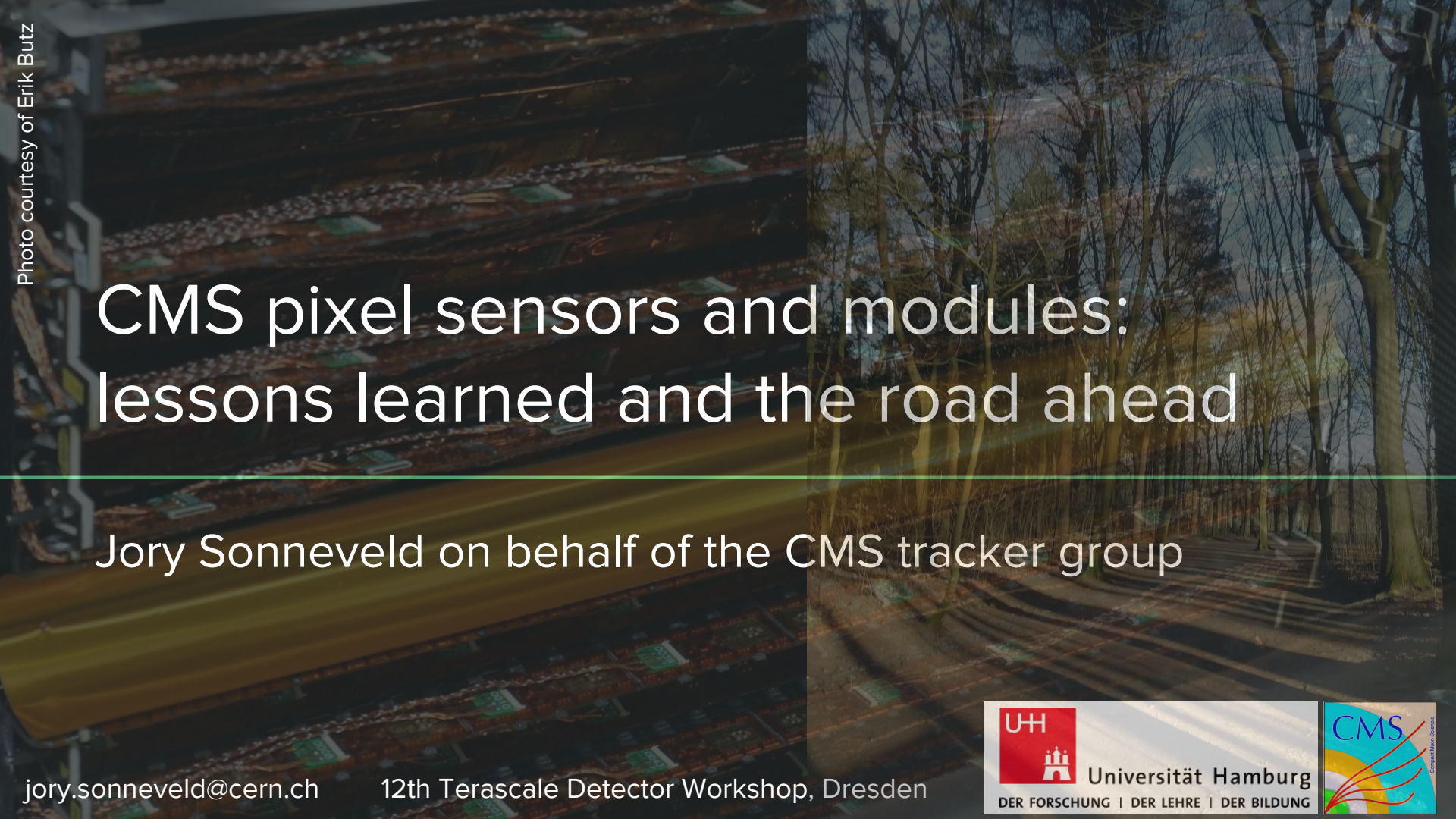


Photo courtesy of Erik Butz

CMS pixel sensors and modules: lessons learned and the road ahead

Jory Sonneveld on behalf of the CMS tracker group

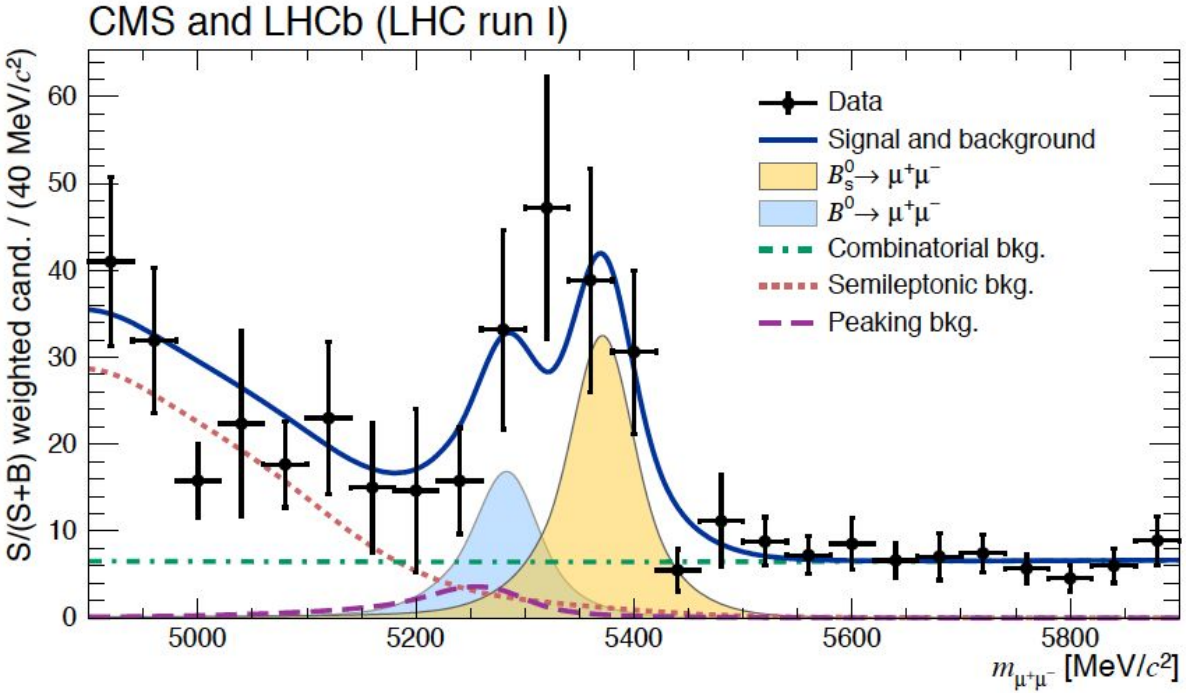
jory.sonneveld@cern.ch

12th Terascale Detector Workshop, Dresden

Universität Hamburg
DER FORSCHUNG | DER LEHRE | DER BILDUNG

High luminosity LHC

High luminosity ➜ high precision

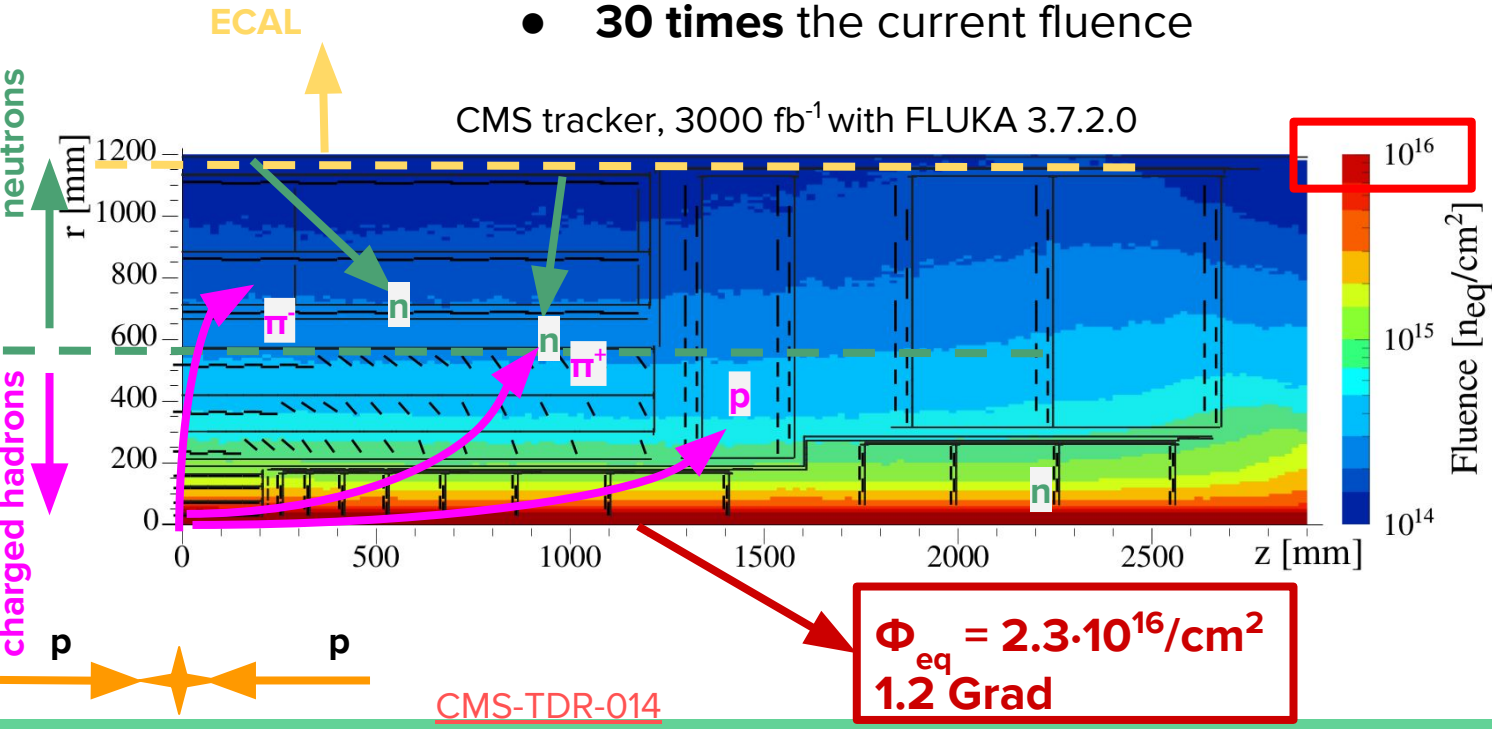


Much better precision for Higgs coupling strengths and measurements like $B_s^0 \to \mu^+\mu^-$

B ➜ μμ measurements are expected to achieve 6.8σ precision

LHC: a challenging environment

- **25 times** the 2017+2018 integrated luminosity
- **30 times** the current fluence



Pileup up to 200 events per bunch crossing at HL-LHC

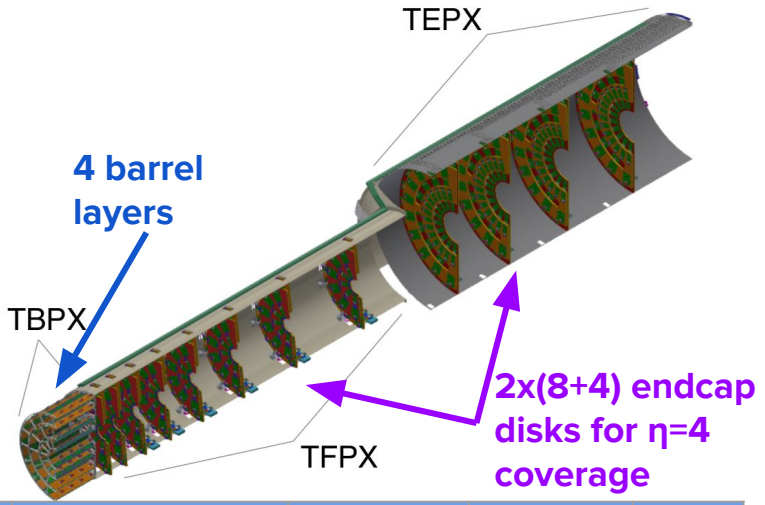
What is needed to cope with these fluences and rates?

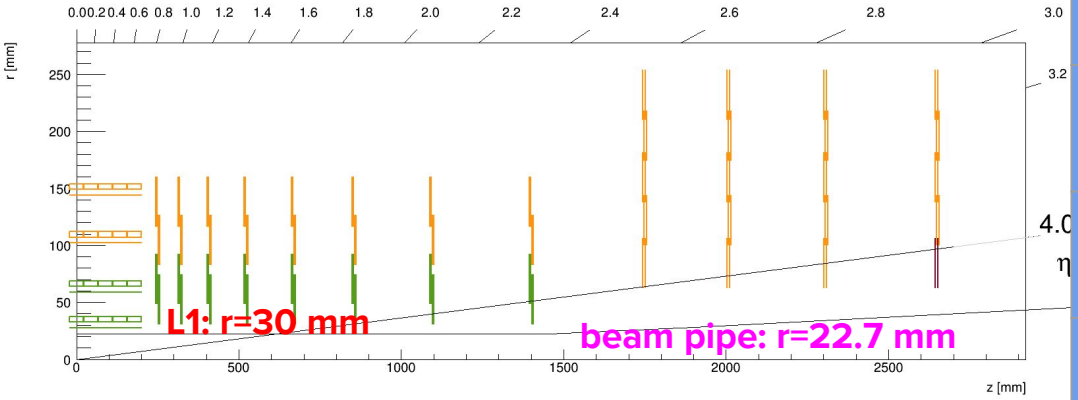
Φ_{eq} = 2.3·10^16/cm^2
1.2 Grad

CMS-TDR-014

CMS phase 2 pixel detector

- Coverage up to η=4 and high-rate capability
- Almost vertical incidence in forward pixel detector
- Serial powering to keep same powering services
- Option to replace L1 after half lifetime
- CO_2 cooling for reduced material





L	Φ_{eq} ·10^{16} /cm^2	now	r [mm]	now
L1	2.3	0.08	30	29
L2	0.5	0.01	61.5	66
L3	0.2	0.001	104.5	109
L4	0.15	0.0005	146.5	160

Fl es as of end 2018, from FLUKA 3.23.1.0

Serial powering: see talk by Matthias Hamer

CMS-TDR-014 CMS pixel phase 2 layout

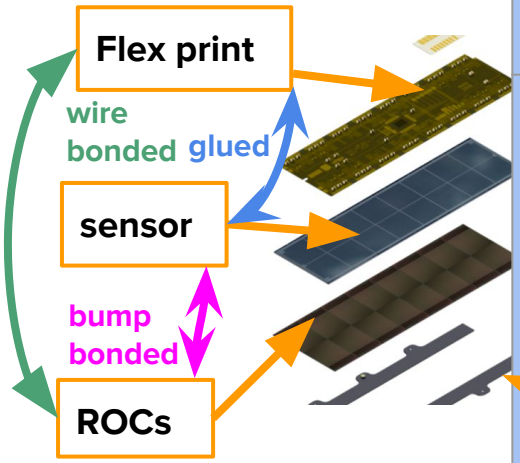
Phase 1 → 2

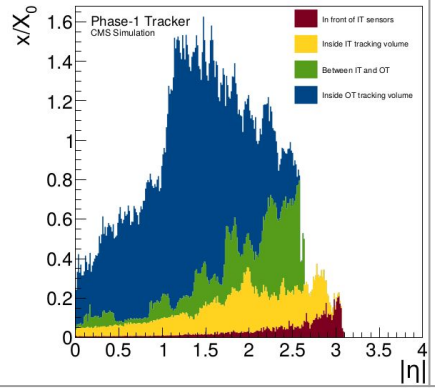
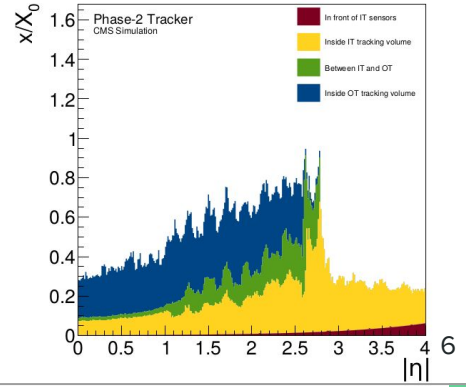
CMS pixel layout

CMS-TDR-011

CMS-TDR-014

Module stacking for both phase 1 and phase 2:



	phase 1 < 2024	phase 2 >= 2024
Disks, layers, reach	4 layers, 3 disks to **η=2.5**	4 layers, 12 disks to **η=4**
Number of pixels	$124 \cdot 10^6$	$1949 \cdot 10^6$
Pixel size	100×150 μm²	100×25 μm², 50×50 μm²
Active silicon area	1.95 m²	4.9 m²
Readout chips	PSI46dig/PROC600 250 nm	RD53B = CROC 65 nm
Number of ROCs	1856 · 16 ROCs	1156 · 2 + 2736 · 4 ROCs
Sensor type	n⁺-n planar 285 μm	n⁺-p planar/3D 100-150 μm
Material budget		

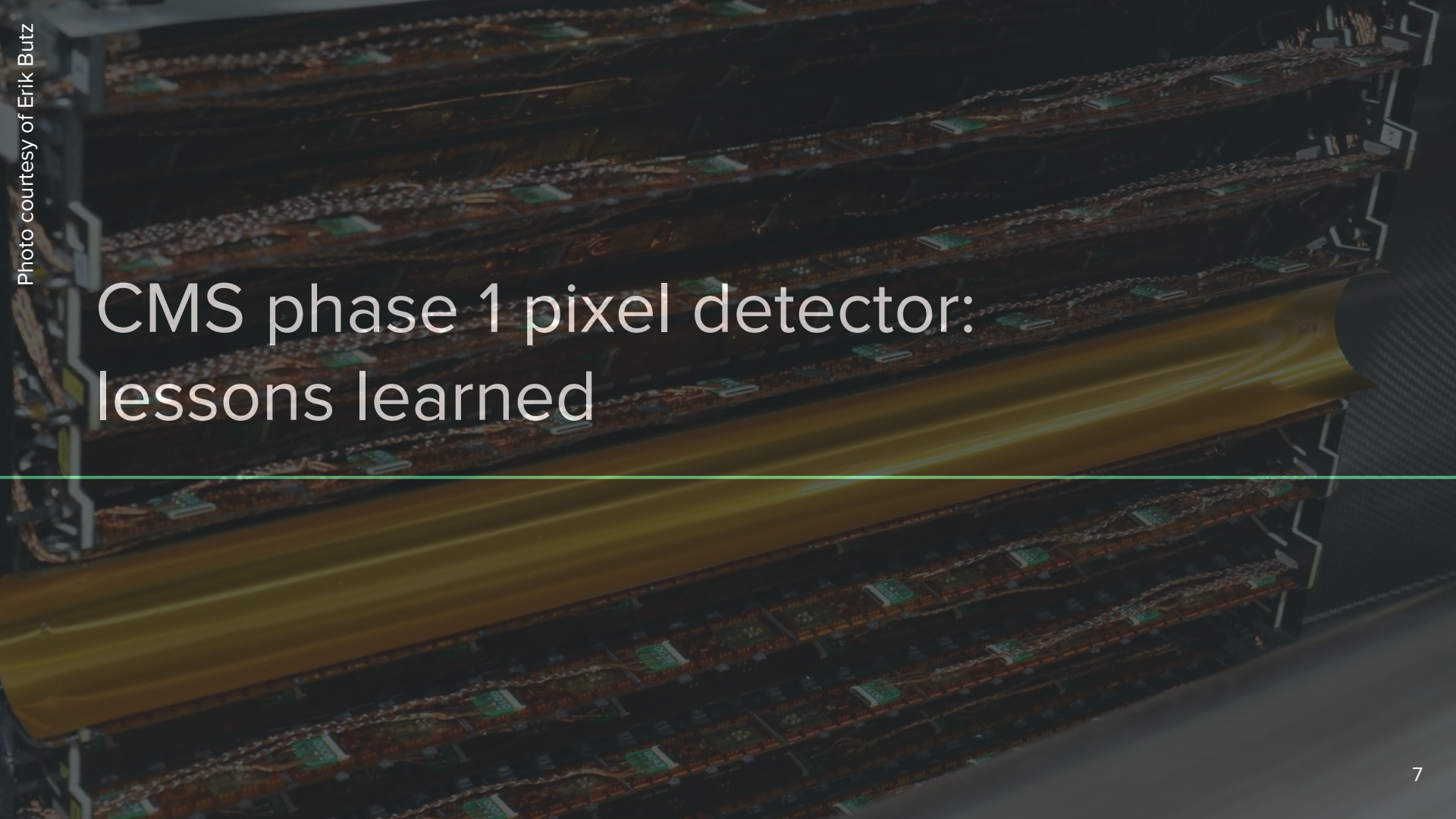


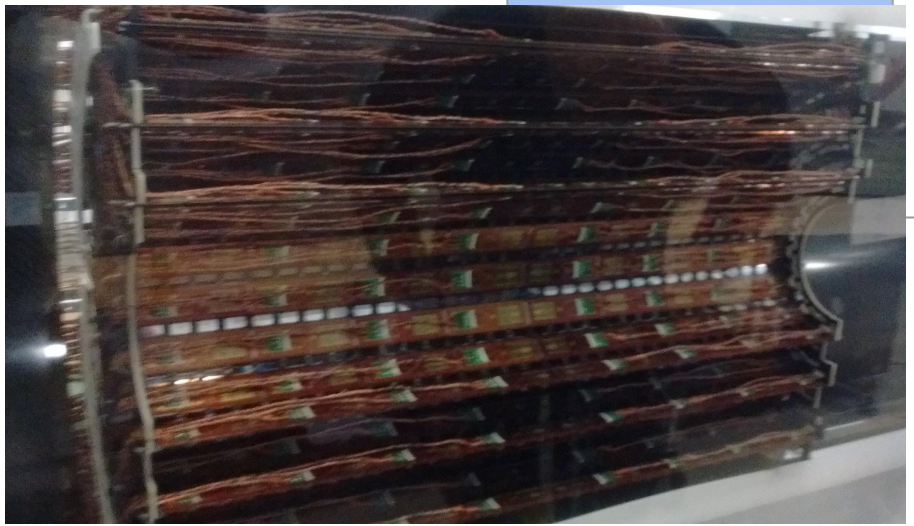
Photo courtesy of Erik Butz

CMS phase 1 pixel detector: lessons learned

Phase 1

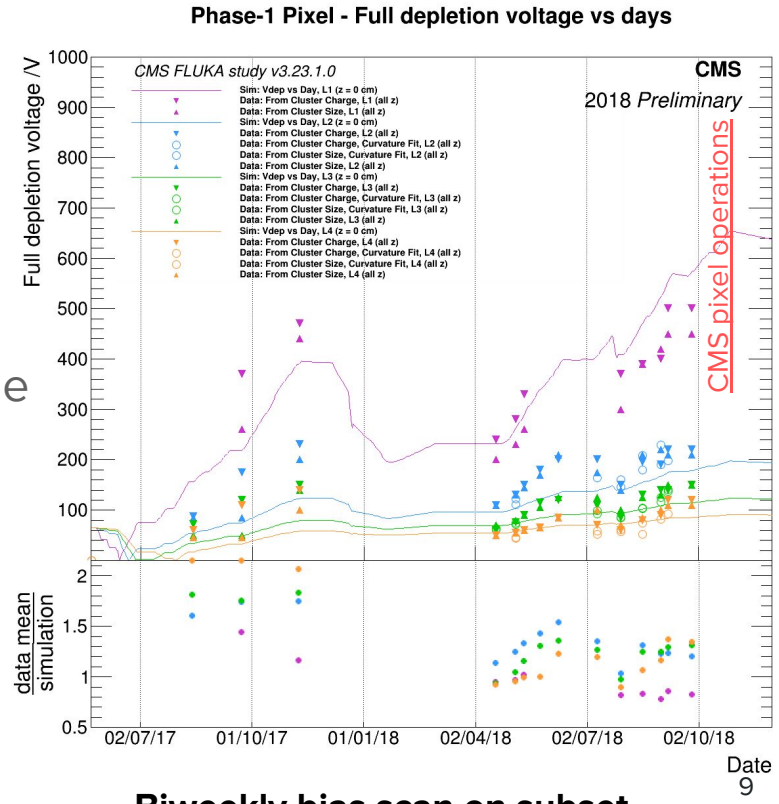
CMS-TDR-011

	phase 1 < 2024	
Number of pixels	$124 \cdot 10^6$	Same cabling as phase 0: ➔ use **DCDC converters** to keep same services: power losses vary ∝ I^2R power use constant ∝ UI
Active silicon area	1.95 m^2	
Number of ROCs	1856 · 16 ROCs	
Sensor type	n^+-n planar 285 µm	
Readout chips	PSI46dig/PROC600 250 nm	**PSI46** known from phase 0: from analog to **digital readout** with column drain **PROC600 new** to deal with high rates with dynamic cluster column drain



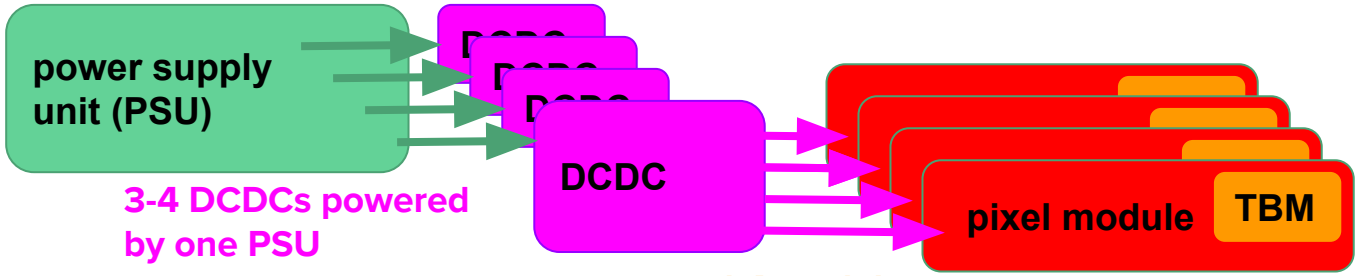
CMS pixel 2017-2018: summary and lessons learned

- Despite many **challenges** like **DCDC failures**, **layer 1 timing and inefficiencies**, pixel detector performed very well in 2017 and 2018
- Good to have **test setups** for example for temperature studies and software testing
- **High and low voltage grouping** ideally the same
- **Monitoring radiation effects** like leakage currents, temperatures, depletion voltages and chip properties very important
- Programming backend with trigger logic and backend for data readout ideally not separated



Biweekly bias scan on subset

Stuck TBMs and malfunctioning DCDCs



3-4 DCDCs powered by one PSU

1-4 modules powered by 1 DCDC

1: token bit manager (TBM)

- 30 single event upsets (SEUs)/fb^{-1} in L1 transistor in TBM latch sets TBM to 'no readout' mode: "**stuck TBMs**"
- recovery only with **power cycle**. Lowest granularity: one **DCDC converter**.

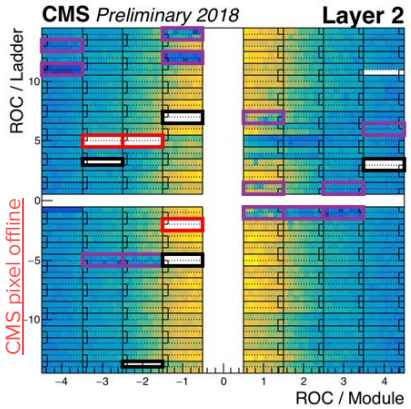
2: irradiated DCDCs stopped functioning in disabled state

- Increased leakage current as a result of one transistor
- 63/1216 at end of 2017 stopped functioning, another 333 had high current

2018: powercycling with PSU. No DCDC broke.

2020+: new DCDCs, new L1 TBMs.

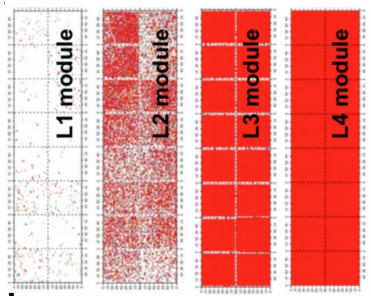
See also talk by Katja Klein



Layer 2 damaged chips

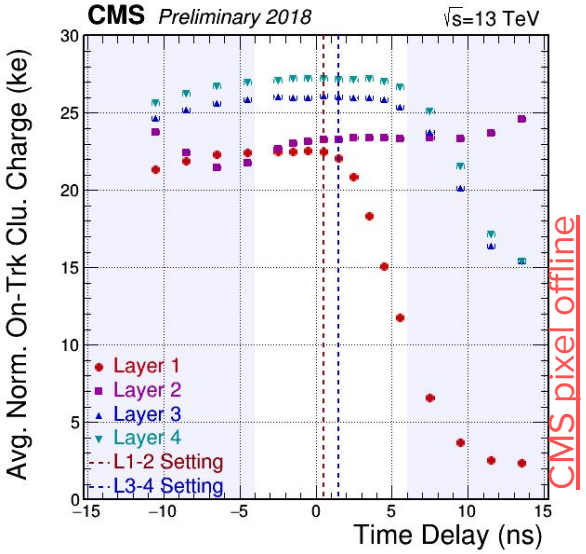
3: readout chips

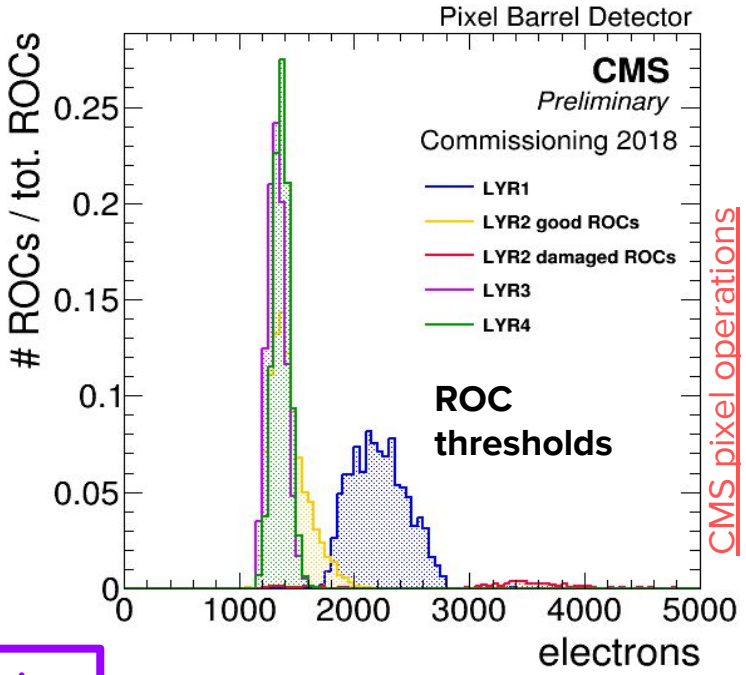
- high and low voltage (HV, LV) grouping not the same
- **HV on, LV off caused chip damage** from sensor leakage current: 8/96 L1 modules lost in 2017



Layer 1 chip PROC600: timing, crosstalk, inefficiency

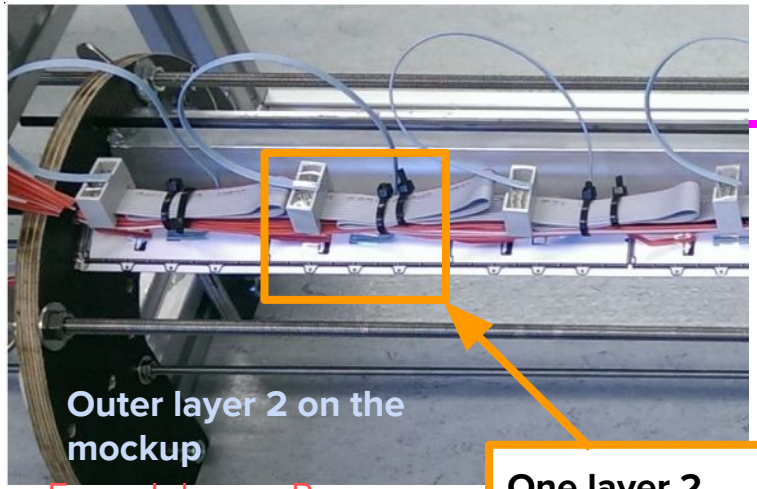
- Layer 1 readout **chip speed very different** from layer 2 ➔ **not enough delay setting granularity**
- **High thresholds** resulting from crosstalk and large timewalk
- **Inefficiency** at high and low rates
- **Reduced dynamic range** as a result of large spread in pedestals





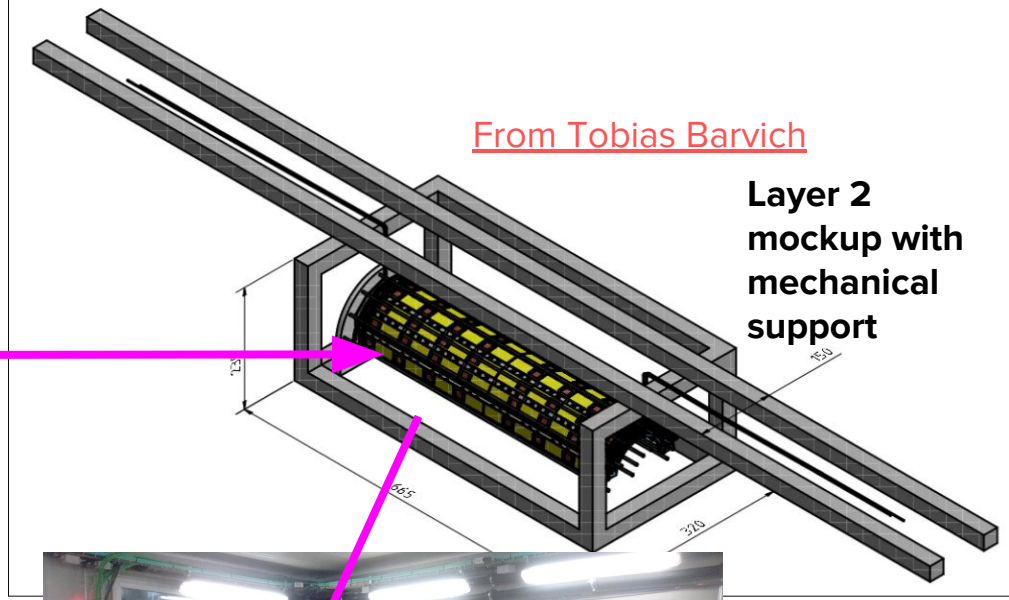
All solved or addressed in next L1 chip version.

Test setup: CO_2 cooling

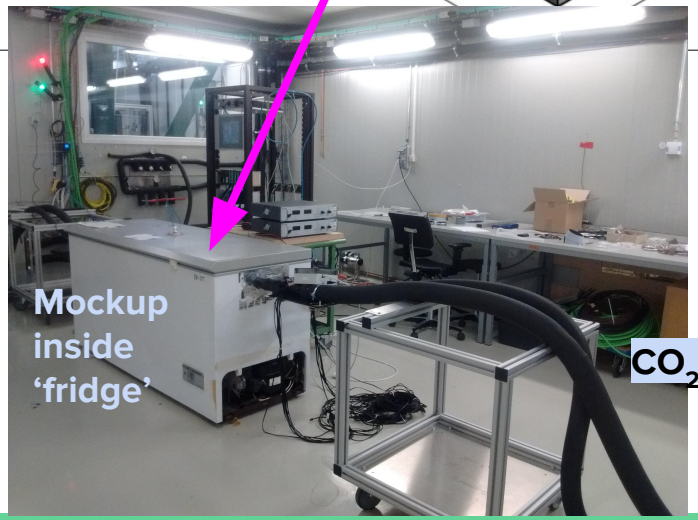


From Johanna Renner

From Tobias Barvich

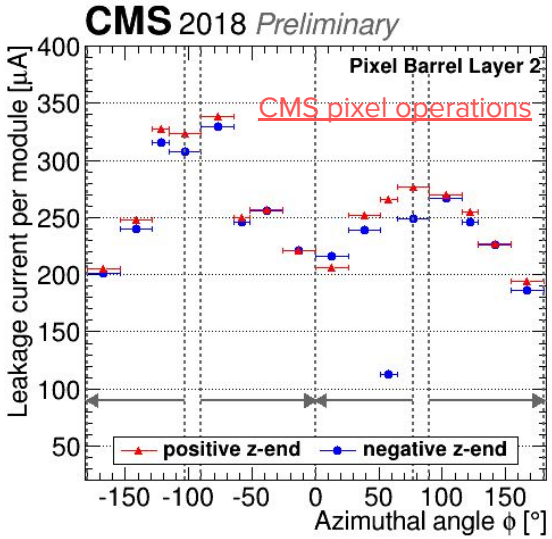


One layer 2 pseudomodule with adjustable heat load

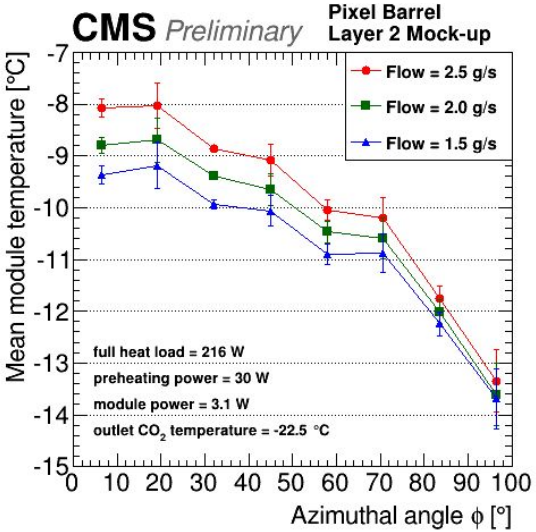


Realistic layer 2 mockup with **adjustable preheating and heat load on pseudo-modules** used to study CO_2 cooling and temperatures.
Flow on CO_2 is adjustable.

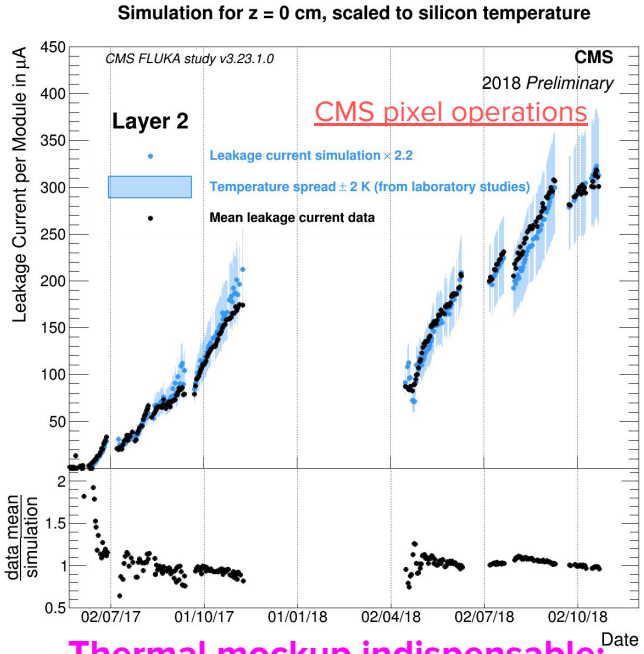
Temperature studies with a mockup of layer 2



Found a **large spread** in high voltage **leakage current** in detector



Mockup temperatures and CO_2 flow change effects **agree well with what is seen in actual detector** layer 2



Thermal mockup indispensable:

➜ temperature modeling is a **large uncertainty** for simulation

➜ **few temperature sensors** in the detector

CMS phase 2 pixel sensors

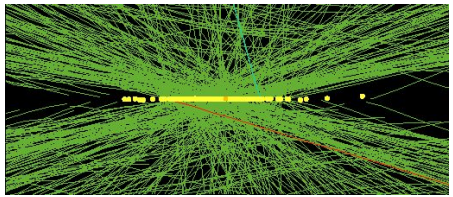
Requirements for CMS pixel phase 2

Must-haves:

- **More radiation hard** ➜ thinner sensors
- **Deal with high rates** ➜ smaller pixels

Wishlist for good physics:

- The best **resolution** ➜ cluster size 2
- Good charge above threshold ➜ good **signal/noise**
- Low enough leakage current ➜ **no thermal runaway**
- **Efficiency** should be ≥ 99%



Event with pileup of 78 in CMS in 2012

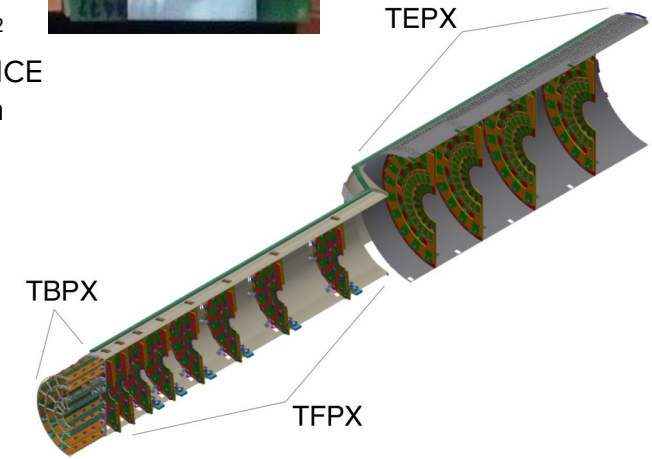
See also talk by Fabian Hügging

Phase 2

CMS pixel layout
CMS-TDR-014

		phase 2 >= 2024
Disks, layers, reach		4 layers, 12 disks to **η=4**
Number of pixels		$1949 \cdot 10^6$
Pixel size	**two options**	100x25 μm^2, 50x50 μm^2
Readout chips	See also talk by Tomasz Hemperek	RD53B=CROC 65 nm CMS version of RD53A (by end 2019)
Sensors	**two type options thickness range:**	**n-p planar or 3D for L1 100-150 µm**

FBK planar 50x50, bias dot, 100 µm, $\Phi_{eq} = 5 \cdot 10^{15}/cm^2$ (Ka), on RICE irradiation card

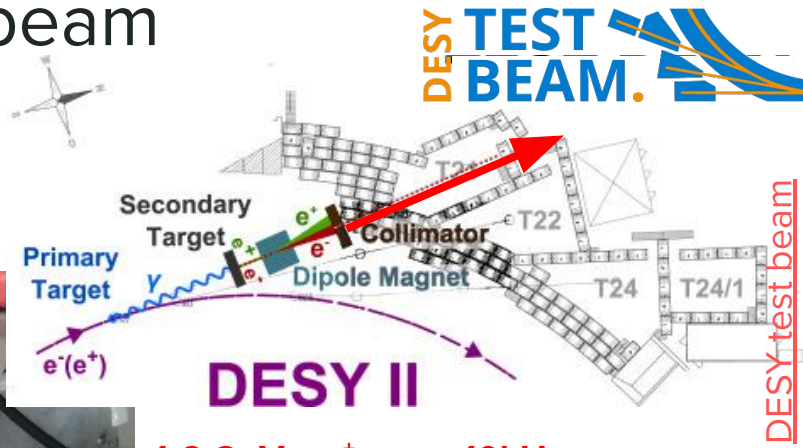


Focus in this talk

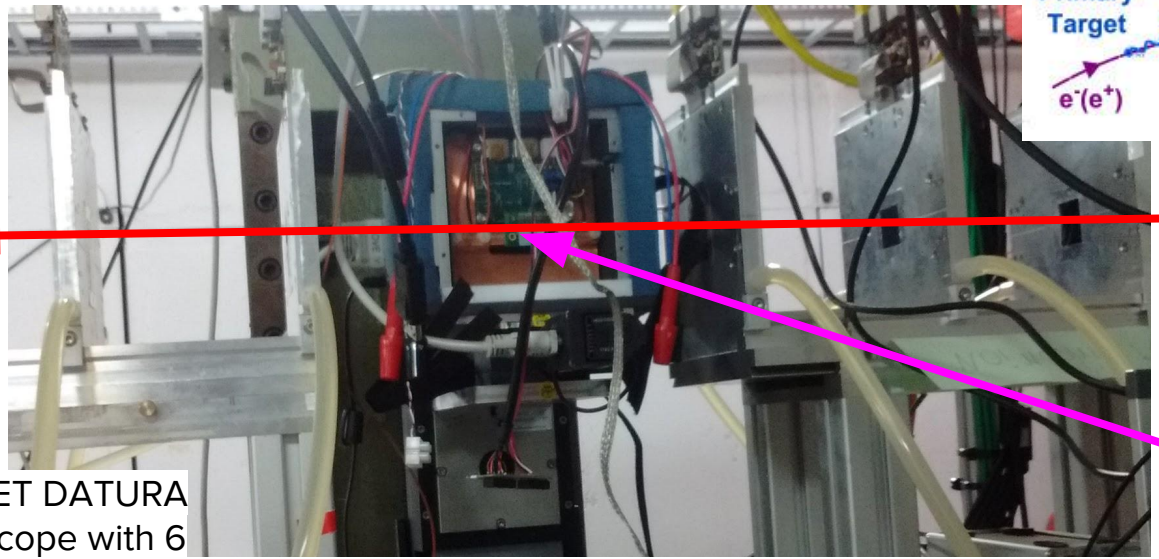
- How thick should the sensor be?
- What dimensions should the pixels have?
- Do we use 3D or planar sensors?

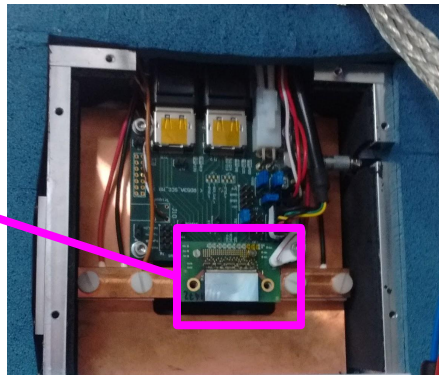
Sensor characterization at test beam

Tests of CMS phase 2 planar and 3D sensors on RD53A or ROC4SENS (R&D) chip



1-6 GeV e^-e^+ up to 10kHz





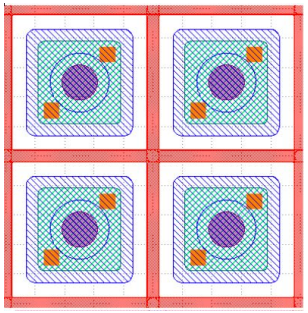
EUDET DATURA telescope with 6 MIMOSA26 (MAPS for ILC, 50 µm thick, 18.4 µm^2) planes with resolution of 5.7 µm

See also talk by Simon Spannagel

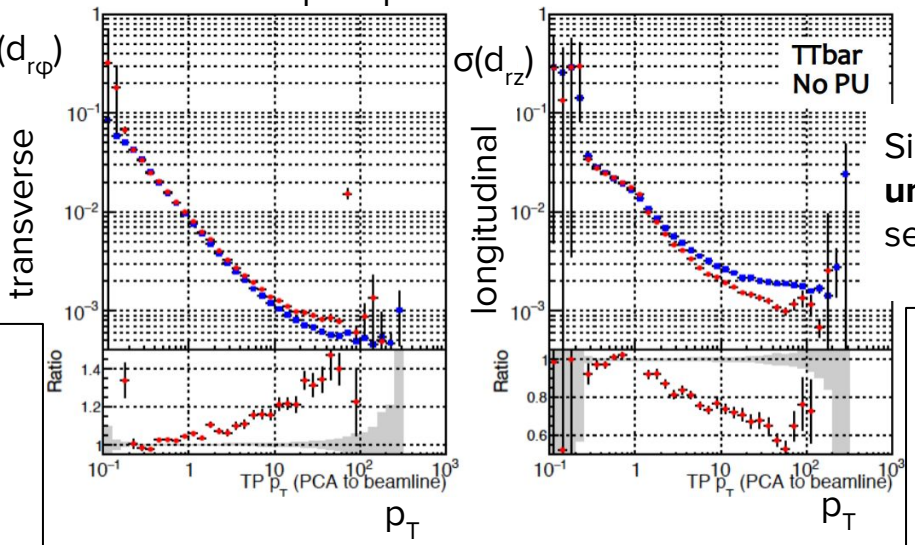
Pixel cell dimensions

- Phase 2 pixel cell size must be ⅛ of phase 1 pixel size 150×100 μm^2
- 25×100 μm^2 or 50×50 μm^2 are both good

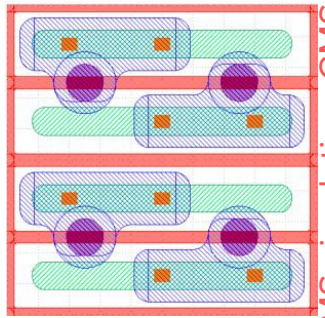
From Jörn Schwandt



impact parameter resolution



Simulation for **unirradiated** sensors



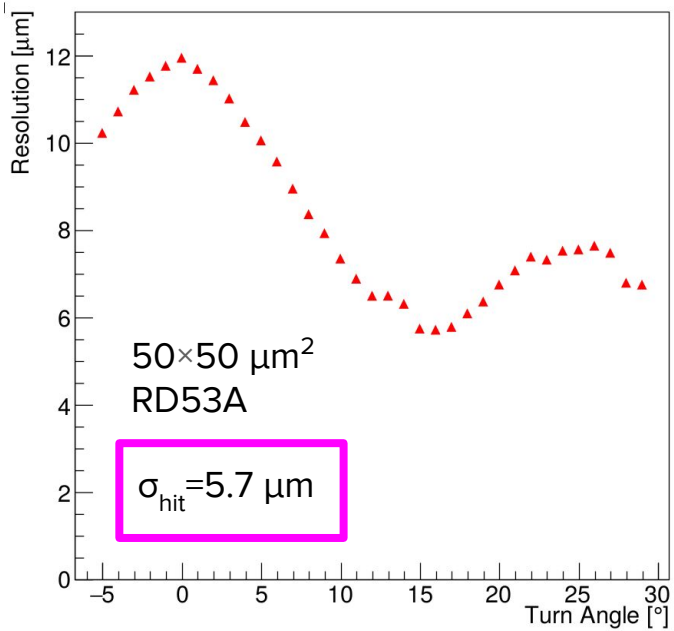
From CMS simulation, CMS-TDR-014

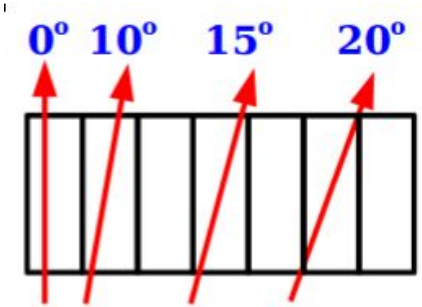
50×50 μm^2
✔ Good primary vertex discrimination
✘ Long clusters at barrel edges can break up

25×100 μm^2
✔ Good impact parameter resolution in barrel and p_T, good resolution in endcaps
✘ Some cross talk seen: under investigation

Pixel cell dimensions and resolution

- 25×100 µm^2 or 50×50 µm^2: charge sharing different
- **Best resolution: cluster size of 2**





2 pixel charge sharing for 18°

Optimal charge sharing at an angle atan(pitch/depth):

- **50×50 µm^2:** atan(50/150) = 18.4°
- **25×100 µm^2:** atan(25/150) = 9.5°

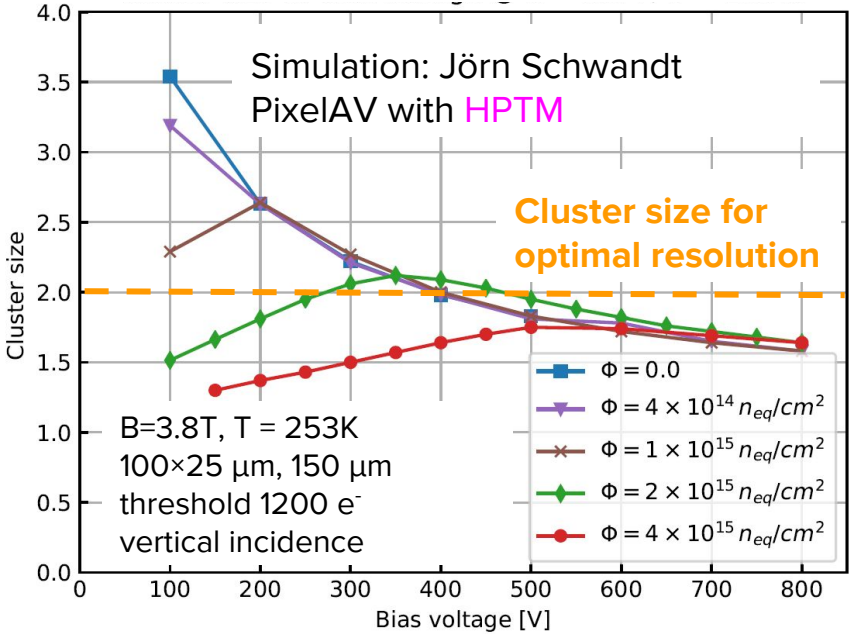
  ➜ increase E-field with higher bias

Compare with Lorentz angle:

≃21° in 3.8T in unirradiated sensors

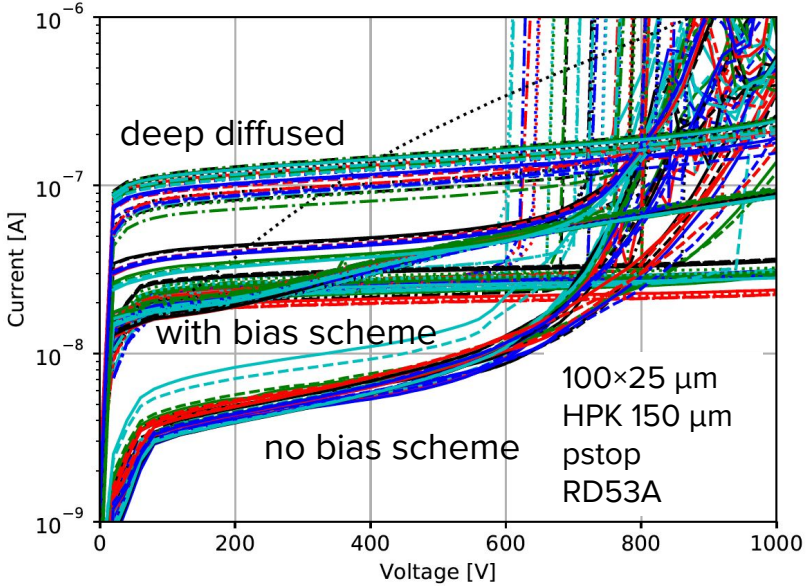
Bias voltage requirements

Cluster size vs bias voltage



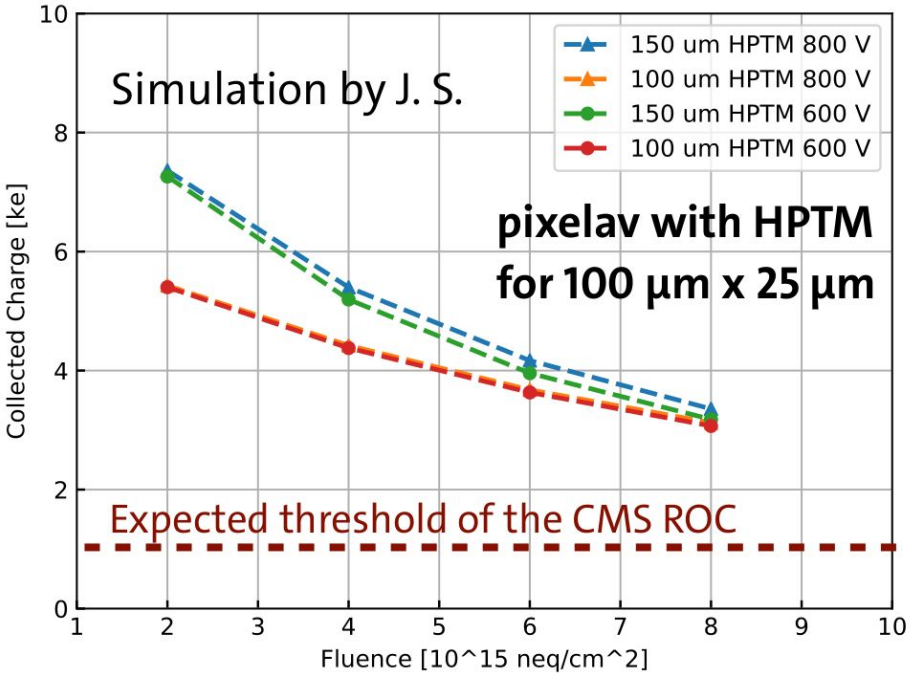
400V needed for optimal resolution

IV curve



Breakdown **only at 600V** before irradiation

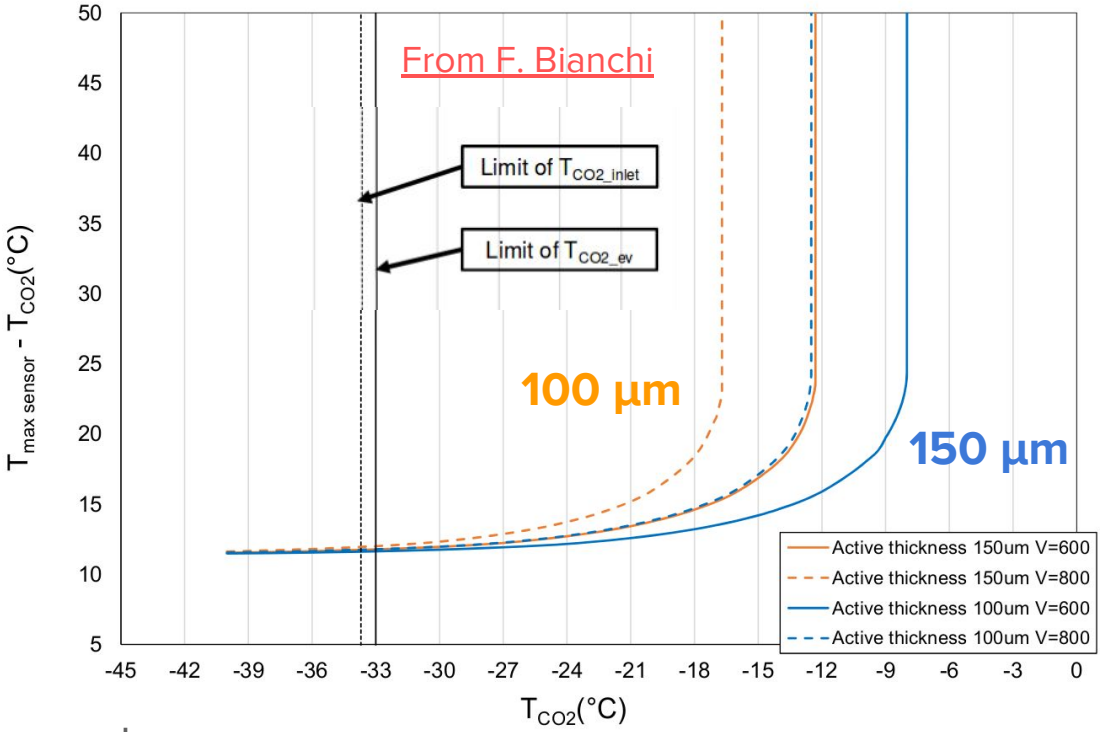
Signal/noise and sensor thickness



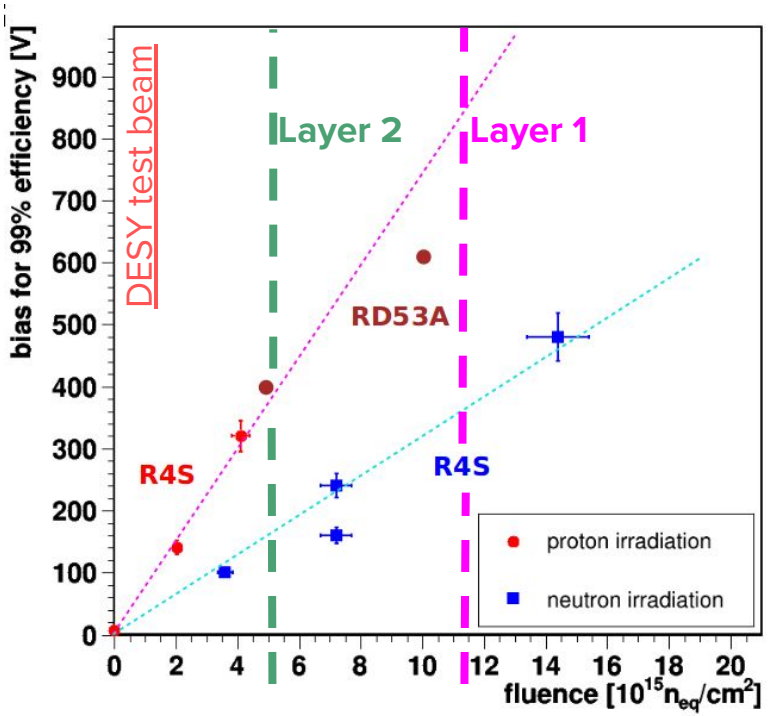
- Hamburg Pentatrap Model (HPTM) used for simulation
- Not much gain in going thinner up to $\Phi_{eq} = 8 \cdot 10^{15}/cm^2$
- Signal/threshold > 3 at $\Phi_{eq} = 8 \cdot 10^{15}/cm^2$
- Thicker sensors have more leakage current: will there be thermal runaway?

Sensor thickness and thermal runaway

- Model of layer 2 material to study thermal runaway
- Both 150 µm and 100 µm start increasing at -30 °C
- 150 µm has higher temperatures but cooling down to -33 °C suffices
- -22 °C is very close to thermal runaway
- sensor should be -20 °C
- Assumed is a total layer 2 fluence at 3000 fb^{-1} of $\Phi_{eq}=5\cdot10^{15}/cm^2$



Required efficiency



To require a tracking efficiency > 99.99%:

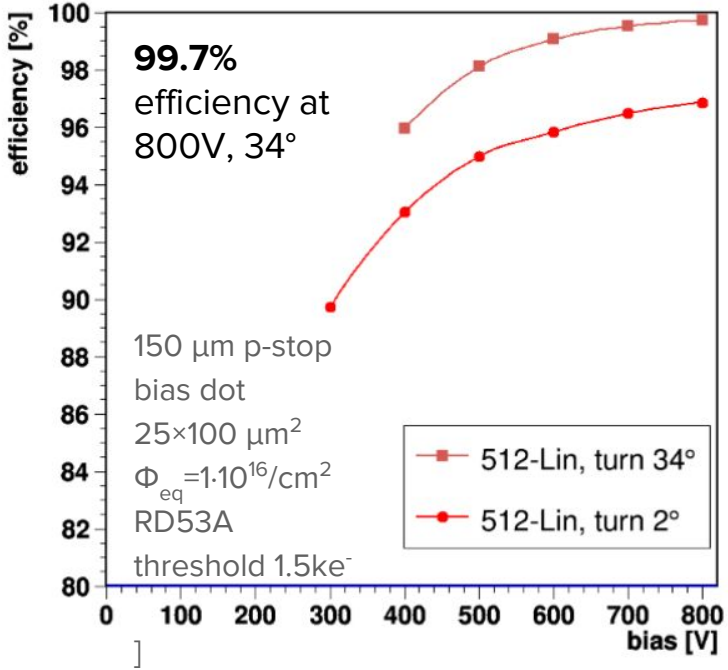
➔ 3 of 5 hits with 97% efficiency (ATLAS)

➔ 3 of 4 hits with 99% efficiency (CMS)

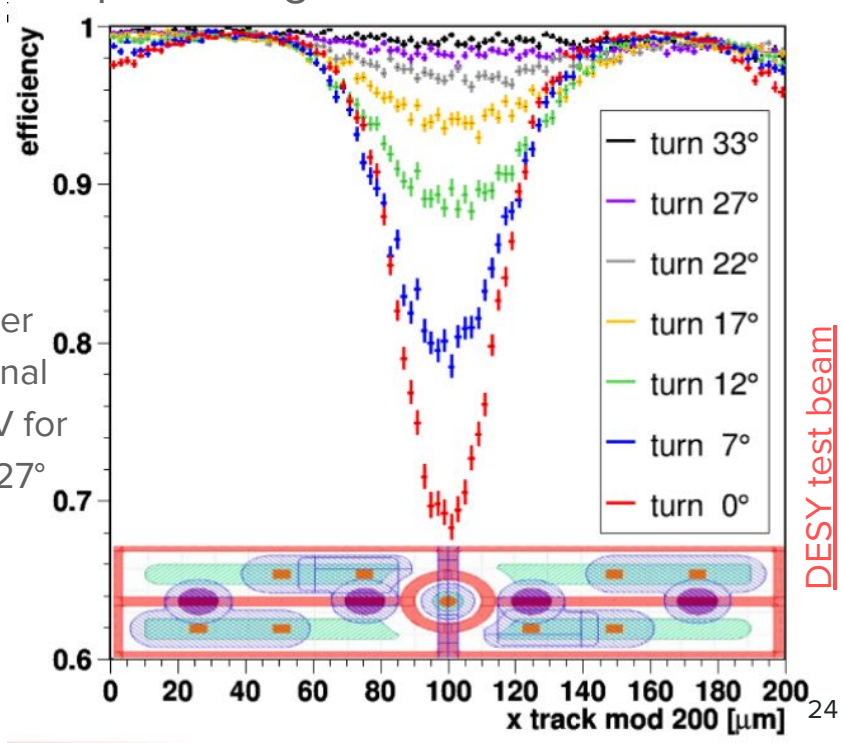
- For fluences up to $\Phi_{eq} = 5 \cdot 10^{15}/cm^2$ **99% efficiency achieved at ≃400V**
  ➔ good for L2-L4 and half-lifetime L1
- For fluences up to $\Phi_{eq} = 1 \cdot 10^{16}/cm^2$ **99% efficiency achieved at ≃600V**

With or without bias dot?

- Bias dot necessary for sensor test before bump bonding
- Reduced efficiency with bias dot at 0°



Efficiency > 99% reachable for inner layer at half nominal fluence and 800V for inclined tracks > 27°



DESY test beam

Conclusions for 150 µm planar sensors

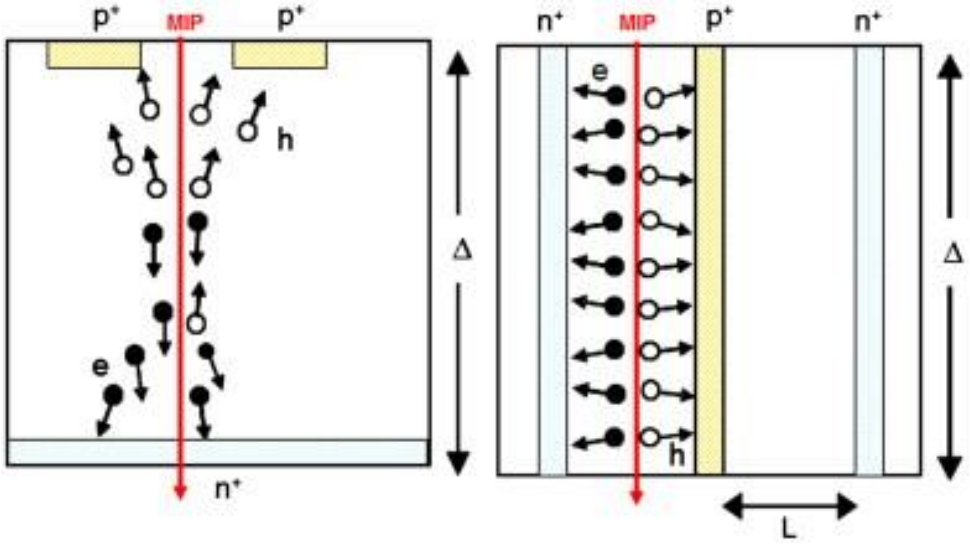
- **Efficiency > 99%** for fluences up to $\Phi_{eq}=5\cdot10^{15}/cm^2$ with a bias voltage < 500V
- **Signal/noise > 3** for a threshold of 1200e^- and a bias voltage below breakdown
- **No thermal runaway** with foreseen CO_2 cooling temperature of -33 °C
- Up to layer 1 half fluence efficiency of 99% reached with a bias voltage of 800V

- This sensor is a possible layer 1 half-lifetime alternative to **3D sensor design**

3D sensors

3D sensors

planar 3D

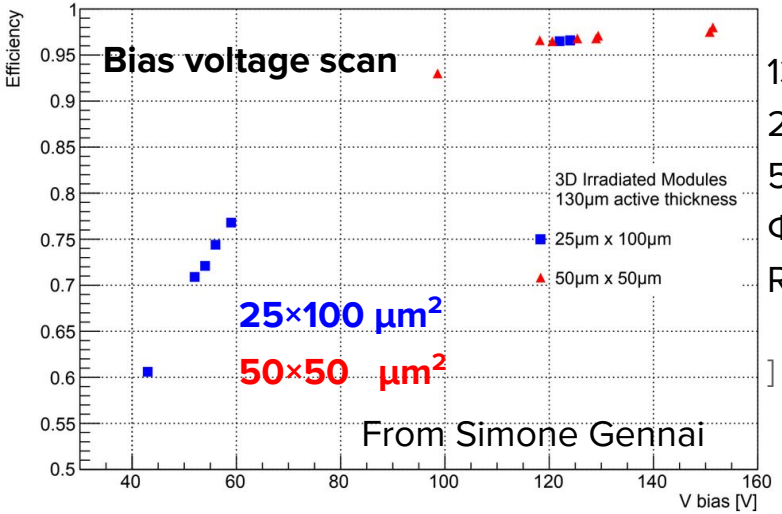


- Substrate thickness Δ and electrode distance L decoupled: promising for radiation hardness
- Lower chance of trapping
- Reduced depletion voltage: O(10) V
- Fast charge collection
- Option for innermost layer of CMS

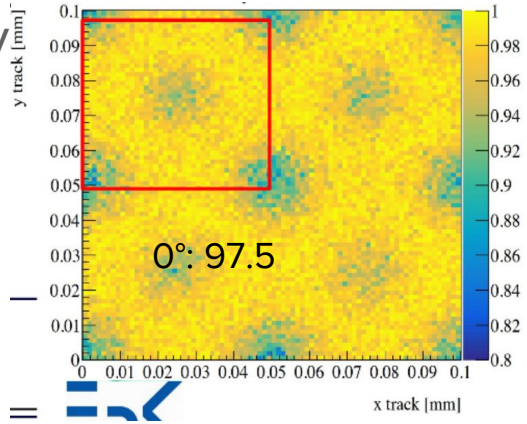
From Da Vía et. al.

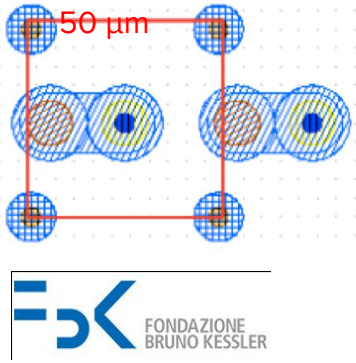
3D sensor results

- 97% efficiency for bias voltages < 200V after half layer 1 expected fluence at 0°

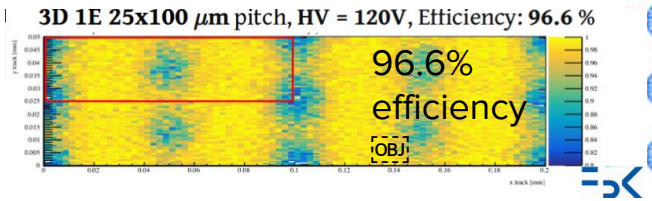


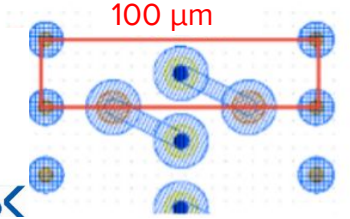
130 µm
25×100 µm²
50×50 µm²
Φ_{eq}=1·10¹⁶/cm² (CERN)
RD53A, threshold 1.4ke⁻





Designs from Marco Meschini



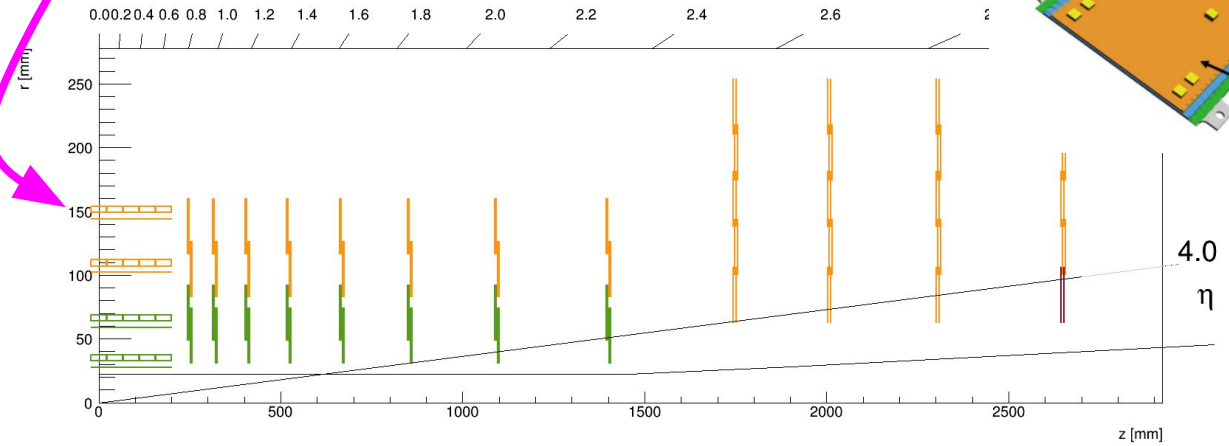


From Jordi Duarte Campderros and Andrea García Alonso

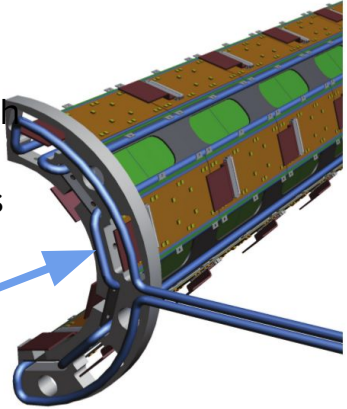
CMS phase 2 pixel modules

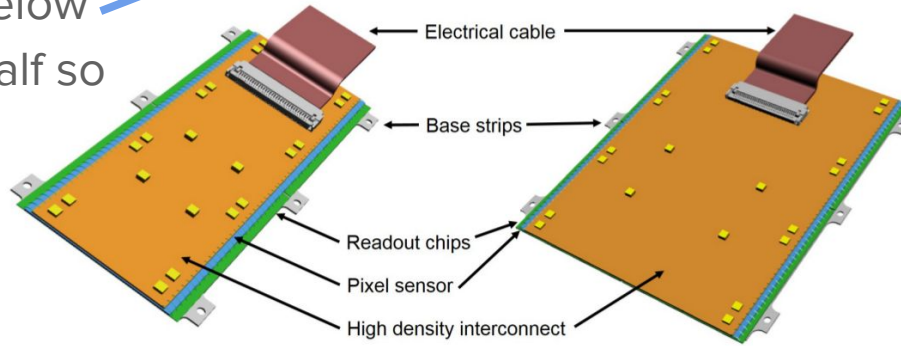
Module structure

- **2x2 chip modules at larger radius**, **1x2 chips on one sensor closer to the beam pipe**
- Modules on ladders with **CO^2 cooling** below
- **4 and 5 modules** resp. on each barrel half so that η=0 is covered



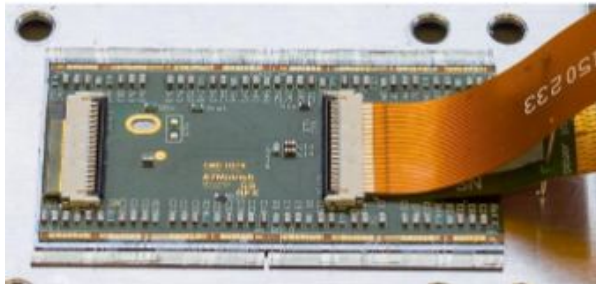
inner layer with 1x2 modules





1x2 **2x2**

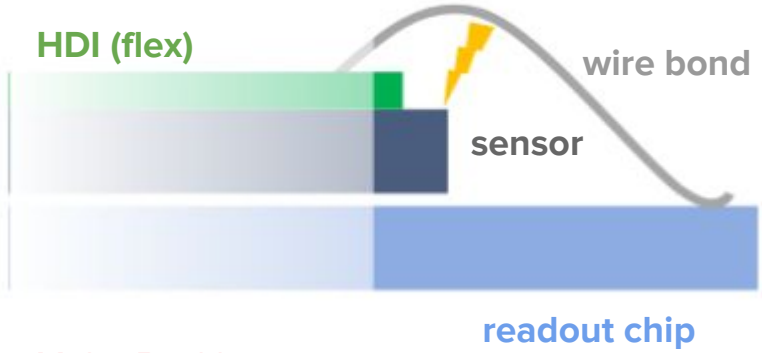
Flex: high density interconnect

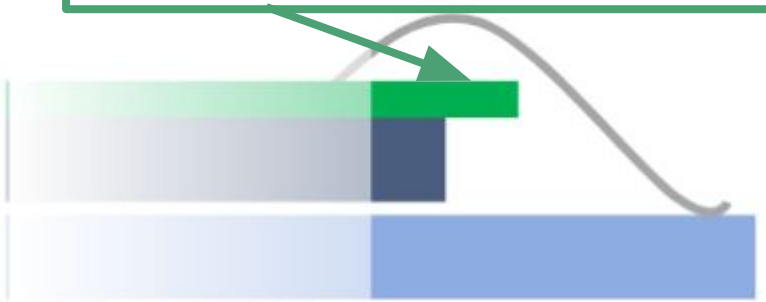


- Transfers data
- Provides clock, trigger, control signals
- Provides power for ROCs
- L2 module power consumption 5.43W
- Prototypes tested up to 1000V

phase 1: n^+-n, HV is on backside with guard rings, usually isolated and not on sensor edges
phase 2: n^+-p, HV on all-metal backside, also **on sensor edges.** HDI copper layers **thin**, pitch **small**!

Protection against glue coverage of HDI pads and increased spark protection





From Malte Backhaus

Increased wire bond pad size from 500 µm to 750 µm
Added overhang of 100 µm in wire bond sides

The road ahead

Phase 1

September 2020: Start replacement of phase 1 layer 1

Early 2021: Start LHC run 3

Phase 2

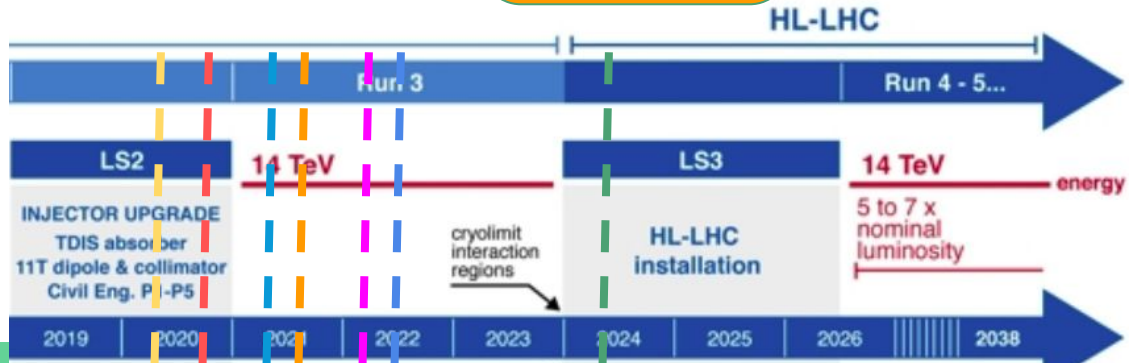
August 2020: Sensor qualification: start production

September 2021: CROC=RD53B qualification

Early 2022: Final CROC Preproduction of final sensor

June 2022: Prepro-duction of final module

June 2024: Finish module production



Summary

CMS phase 1:

- Successful commissioning of CMS phase 1 pixel detector since start of 2017
- Pixel detector running according to predictions
- Layer 1 will be exchanged this long shutdown
- The entire detector will be replaced in the next long shutdown 3

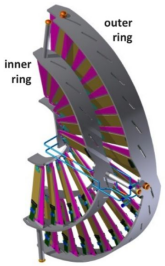
CMS phase 2:

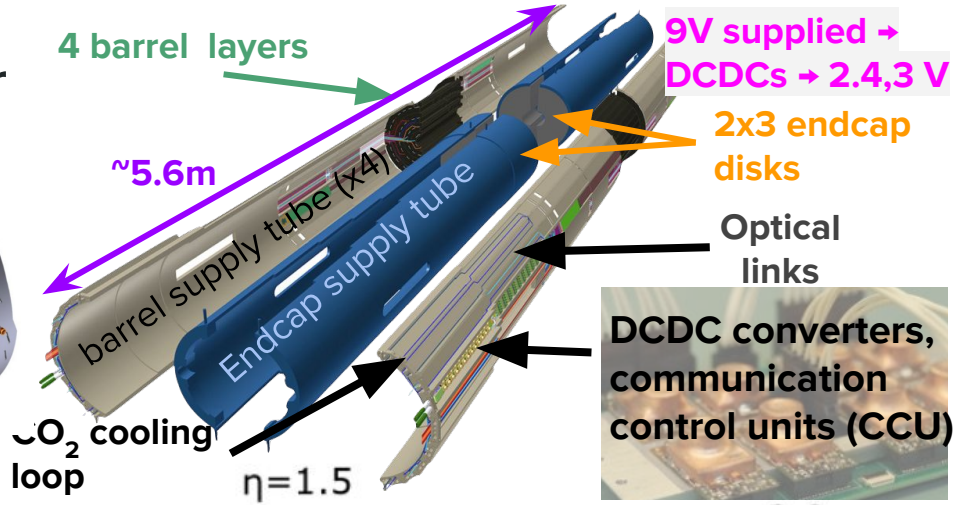
- R&D for pixel sensors and modules is well advanced
- Sensor designs fulfilling requirements are characterized:
  - 150um thick planar up to layer 2
  - 150 um thick 3D or alternatively planar for layer 1 up to half the nominal fluence
- Module design advancing

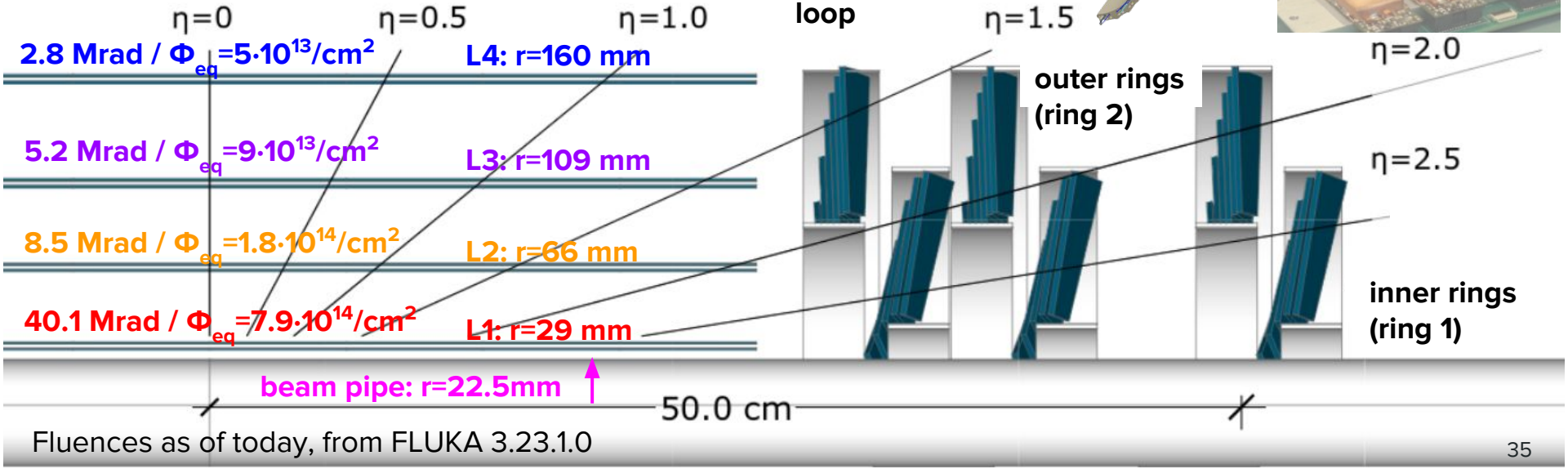
Additional material

CMS phase 1 pixel detector

- 4 hit coverage and high-rate capability
- Turbine-like structure for endcap disks for optimal resolution
- CO_2 cooling for reduced material
- DCDC converters to keep same powering services → 9 V supplied
- Uniform module design throughout

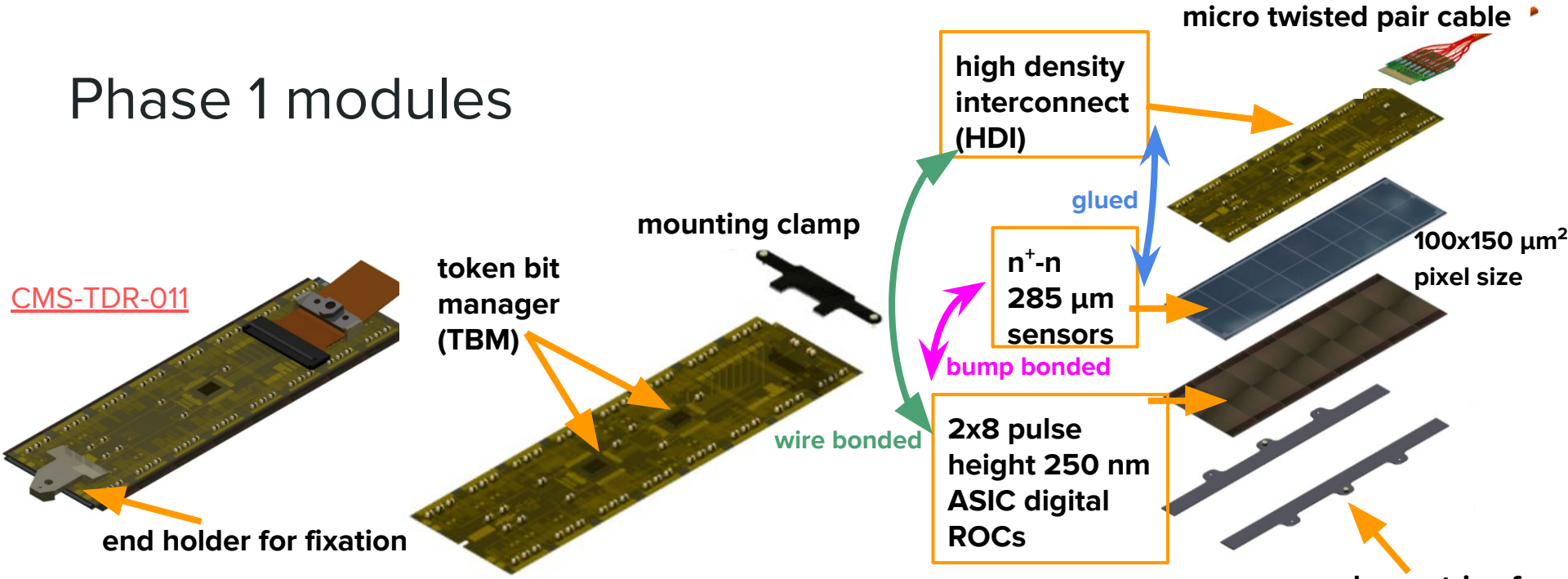






Fluences as of today, from FLUKA 3.23.1.0

Phase 1 modules



Endcap disks 1-3

- 672 modules
- 40-100 MHz/cm^2
- PSI46dig: column drain
- 2 TBM readout channels
- Functions up to 150 Mrad

Barrel layer 1

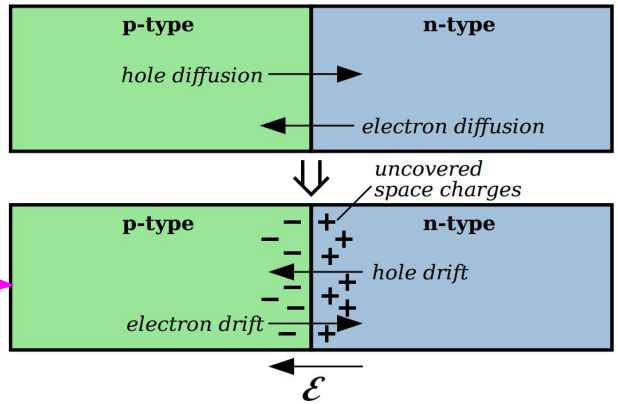
- 96 modules
- 580 MHz/cm^2
- PROC600: dynamic cluster column drain
- 8 TBM readout channels
- Functions up to 480 Mrad

Barrel layer 2-4

- 1088 modules
- 40-100 MHz/cm^2
- PSI46dig: column drain
- 2 TBM readout channels (L3,L4) / 4 TBM readout channels (L2)
- Functions up to 150 Mrad

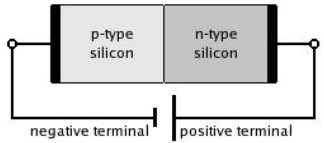
From TheNoise

n^+-p sensors

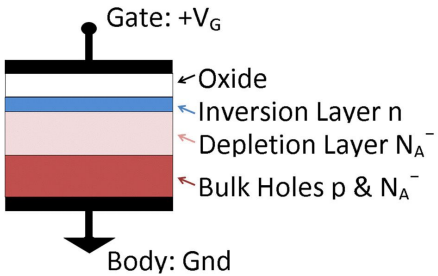


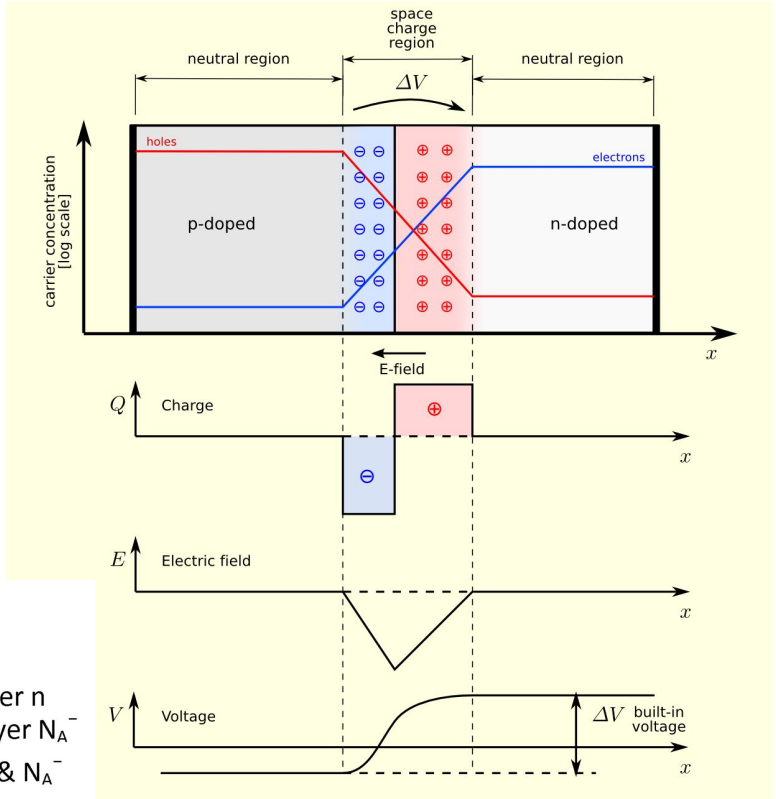
Before diffusion

In equilibrium



-400V



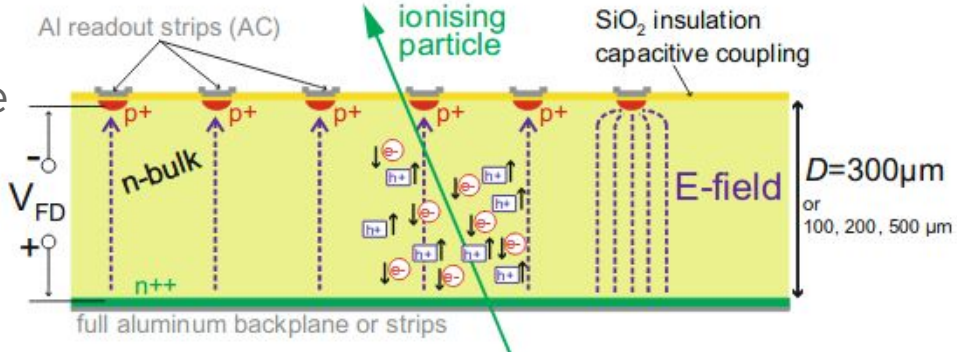


Reverse bias: negative voltage applied p-side with respect to n-side

Effects from radiation damage

Effects from radiation damage can be challenging in operation of detectors as well as for physics:

- Increasing leakage currents
- Charge accumulation in silicon oxide layers
- Single event upsets, in readout only
- Decreasing signal-to-noise ratios
- Changing depletion voltages
- Radiation induced activation of components



Ideal signal detection with a p^+-n silicon sensor

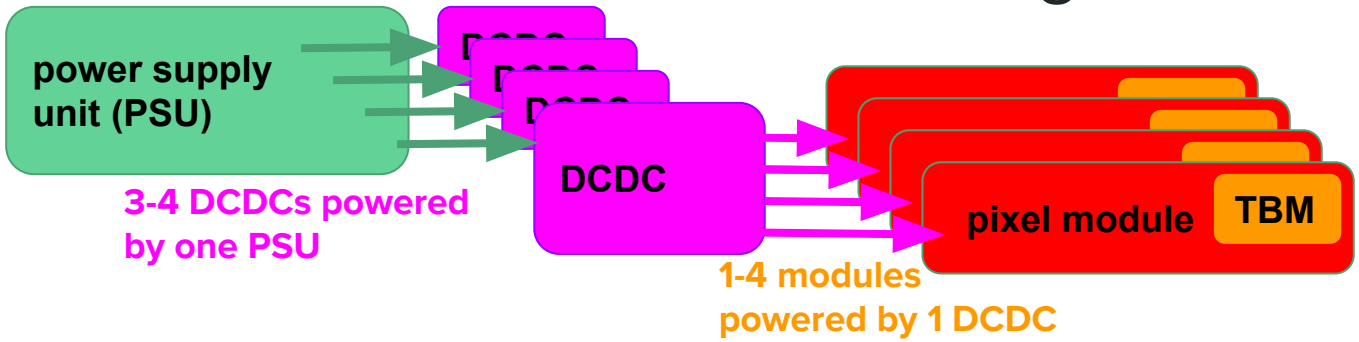
From Michael Moll

From Frank Hartmann

2020+: new DCDCs, new L1 TBMs.

See also talk by Katja Klein

Stuck TBMs and malfunctioning DCDCs

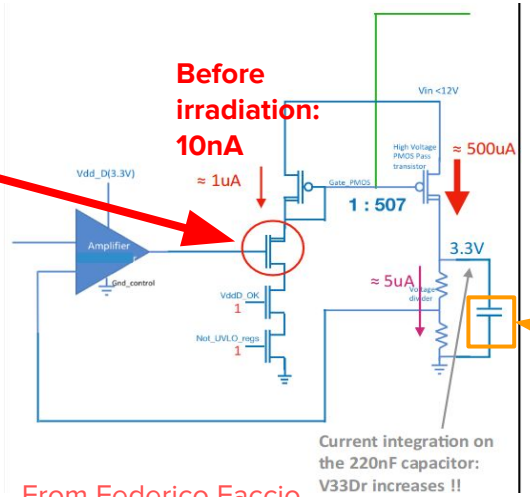


1: token bit manager (TBM)

- $30/fb^{-1}$ in L1 transistor in TBM latch sets TBM to 'no readout' mode: "**stuck TBMs**"
- recovery only with **power cycle**. Lowest granularity: one **DCDC converter**.

2: irradiated DCDCs stopped functioning in disabled state

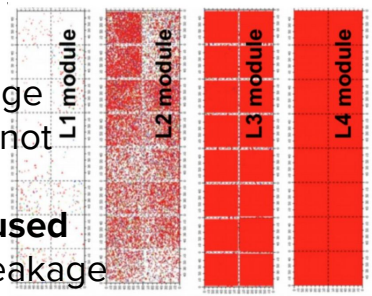
- Increased leakage current as a result of **one transistor**
- 63/1216 at end of 2017 stopped functioning
- 333/1216 in 2017 found to have high current



From Federico Faccio

3: readout chips

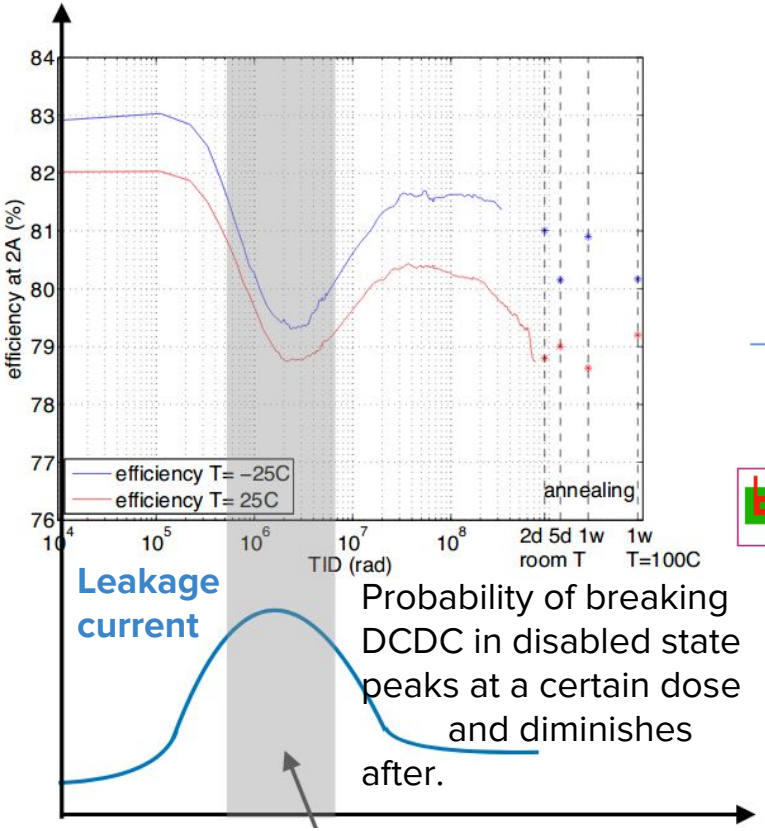
- high and low voltage (HV, LV) granularity not the same
- **HV on, LV off caused chip damage** from leakage current: 8/96 L1 modules lost in 2017



Leakage current causes capacitor to charge up in disabled state

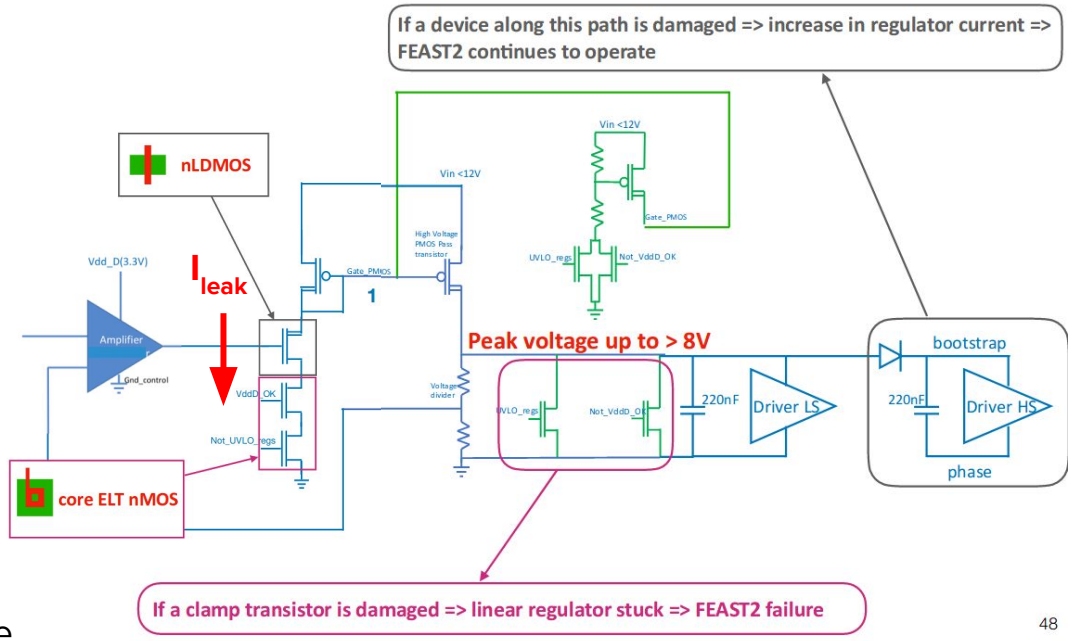
2018: powercycling with PSU. No DCDC broke.

DCDC malfunctioning



Probability of breaking DCDC in disabled state peaks at a certain dose and diminishes after.

Enclosed layout (ELT) vs linear transistors ➜ can 'cut' leakage current path by adding ELT in series



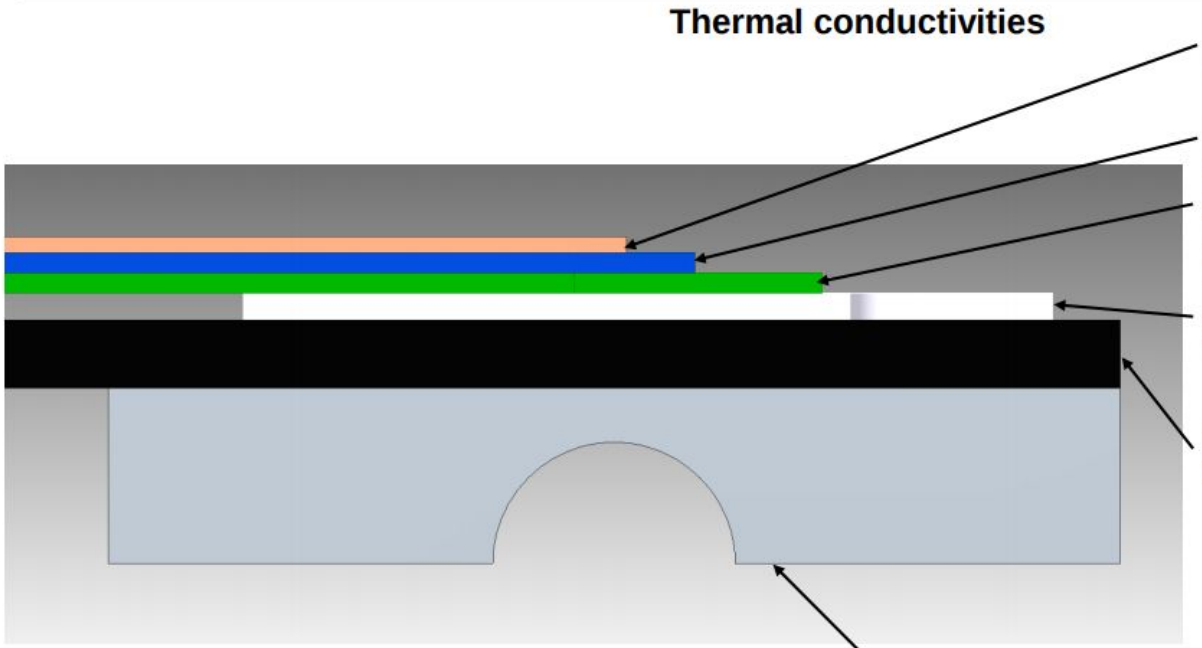
Capacitor charges up in disabled state and causes spikes beyond 3.3V

From Federico Faccio

Planar sensor types

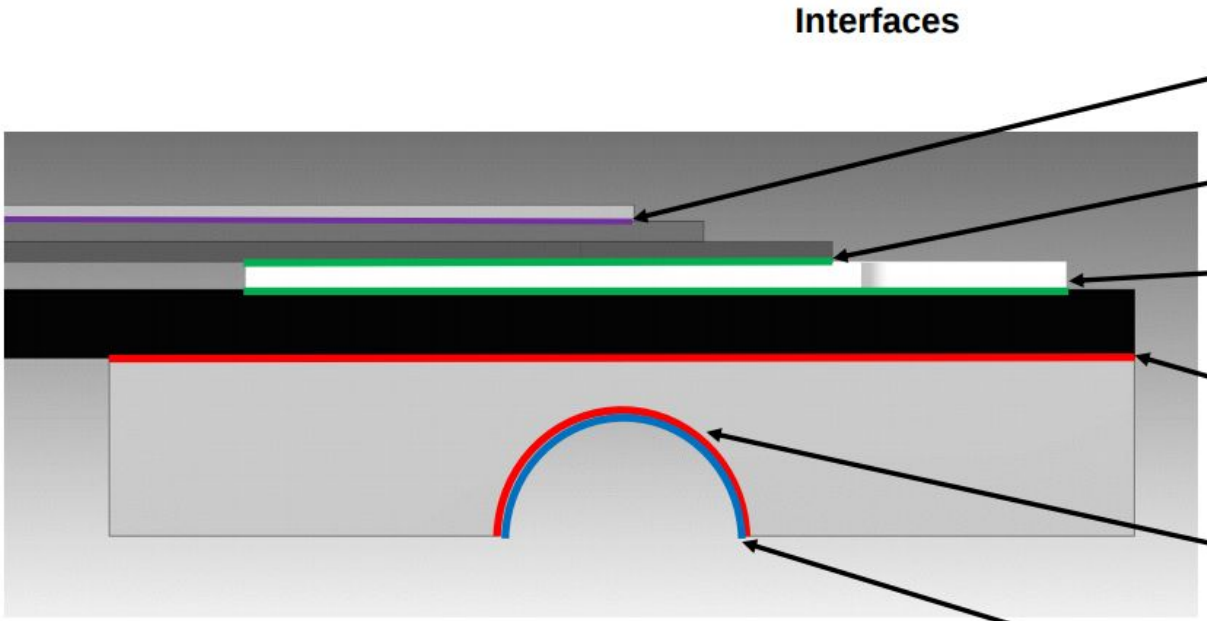
- **HPK** 6” n^+-p with 150 µm active thickness
  - resistivity 1 to 5 kΩ·cm
  - **p-stop** and p-spray isolation
  - common punchthrough and no bias
- INFN **FBK** 6” n^+-p with 100 and 130 µm active thickness
  - resistivity > 3 kΩ·cm
  - p-spray isolation
  - temporary metal for sensor testing
  - active edge/slim edge designs

Thermal runaway model: thermal conductivities



From F. Bianchi

Thermal runaway model: interfaces



From F. Bianchi

Sensor leakage current

- Thicker sensors have more leakage current
- 2nA/pixel reached
- Phase 1: 11nA/pixel, projection: 22nA/pixel
- RD53A requires ≤ 9 nA/pixel