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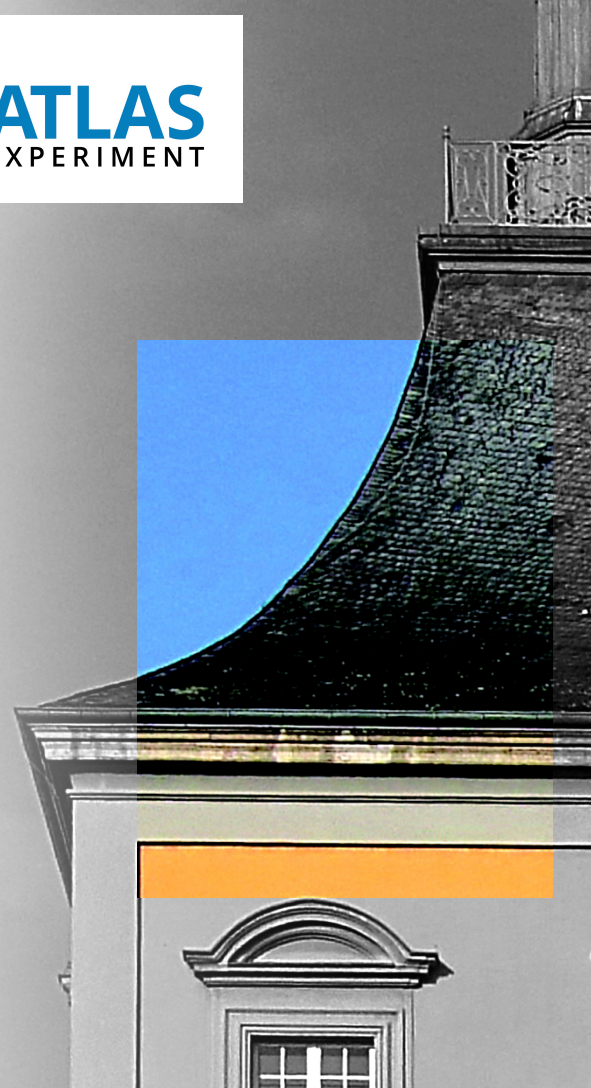
SI LAB Silizium Labor Bonn

ATLAS ITk

ATLAS EXPERIMENT



# ATLAS PIXEL SENSOR DESIGN AND MODULES

12TH TERASCALE DETECTOR WORKSHOP
DRESDEN, MARCH 13 -15, 2019

FABIAN HÜGGING, UNIVERSITY OF BONN
ON BEHALF OF THE ATLAS ITK COLLABORATION

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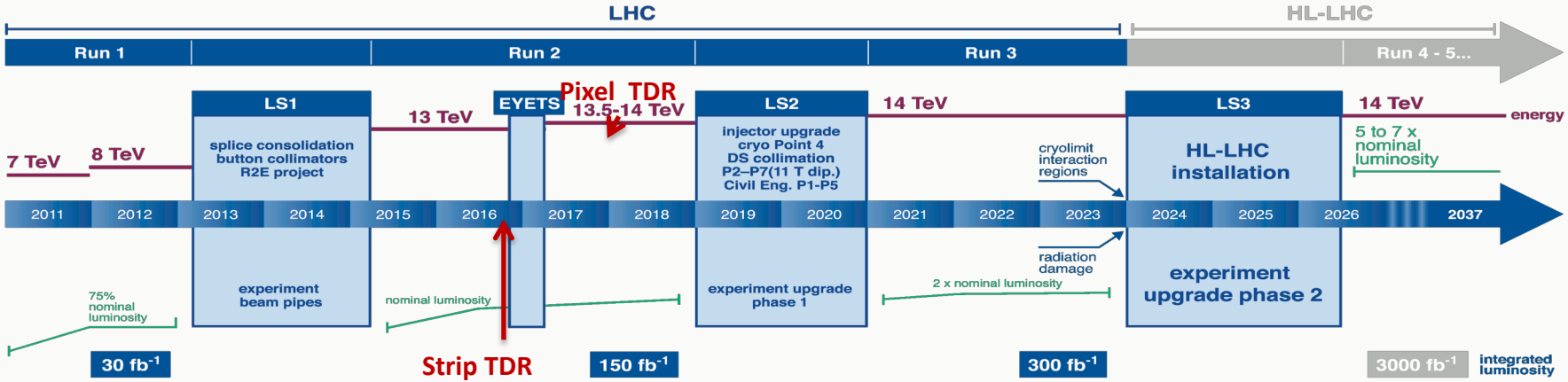
# OUTLINE

- Introduction
  - HL-LHC schedule
  - Requirements
  - Layout of the Phase 2 ATLAS Pixel Detector
- The ATLAS ITk Pixel Detector for HL-LHC
  - Pixel Modules
    - Bump Bonding
    - Module Assembly
  - Pixel Sensors
    - Planar
    - 3D
    - Passive CMOS
- Conclusions

# HL-LHC SCHEDULE




The LHC will be upgraded to the High Luminosity-LHC (HL-LHC) to produce up to 4000 $fb^{-1}$ of integrated luminosity until 2035

- benefits precision measurements in many physics channels
- allows studies of rare processes

# ITK PIXEL DETECTOR REQUIREMENTS

**Instantaneous luminosity**
$1*10^{34}$ $cm^{-2}s^{-1}$ → 5-7.5*$10^{34}$ $cm^{-2}s^{-1}$
**pp interactions per crossing**
23 → 200

**Integrated luminosity**
300 $fb^{-1}$ → 3000 - 4000 $fb^{-1}$
**→ 2*$10^{16}$ MeV $n_{eq}$ /$cm^2$**

**Occupancy (pile-up)**

**Data rate**

**Radiation damage**

**Finer segmentation**

- Smaller channels
- More channels
  → All silicon inner tracker with strips and pixels

**Faster readout & more storage**

- Upgraded readout (ASICs & faster triggers)
- Enhance data purity
  → Track trigger

**Increase radiation hardness**

- New sensor & FE designs
- Exchangeable detector layers
- New CMOS technologies and designs

Simulated HL-LHC event, 200 reconstructed vertices

# ITK PIXEL DETECTOR REQUIREMENTS

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$1*10^{34}$ cm$^{-2}$s$^{-1}$ → 5-7.5*$10^{34}$ cm$^{-2}$s$^{-1}$
**pp interactions per crossing**
23 → 200

**Integrated luminosity**
300 fb$^{-1}$ → 3000 - 4000 fb$^{-1}$
**→ 2*$10^{16}$ MeV $n_{eq}$ /cm²**

**Keep the material low**
- Lightweight support structures with optimized design
- New powering concepts to reduce material of services
- Low material modules: thin sensors and chips

**Occupancy (pile-up)**

**Radiation damage**

**Finer segmentation**
- Smaller channels
- More channels
  → All silicon inner tracker with strips and pixels

**storage**
- Upgraded readout (ASICs & faster triggers)
- Enhance data purity
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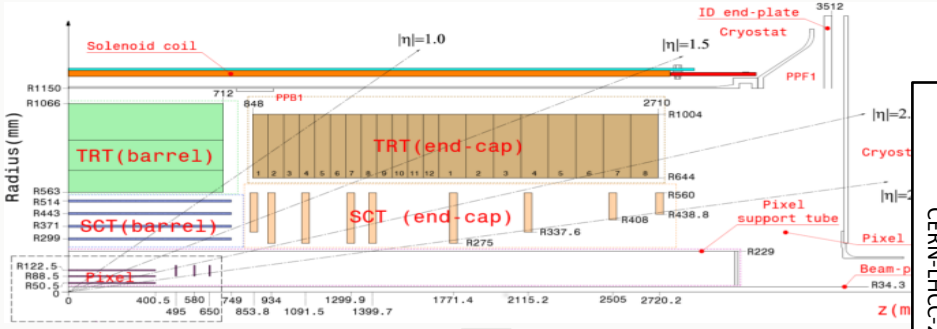
**Increase radiation hardness**
- New sensor & FE designs
- Exchangeable detector layers
- New CMOS technologies and designs

Simulated HL-LHC event, 200 reconstructed vertices

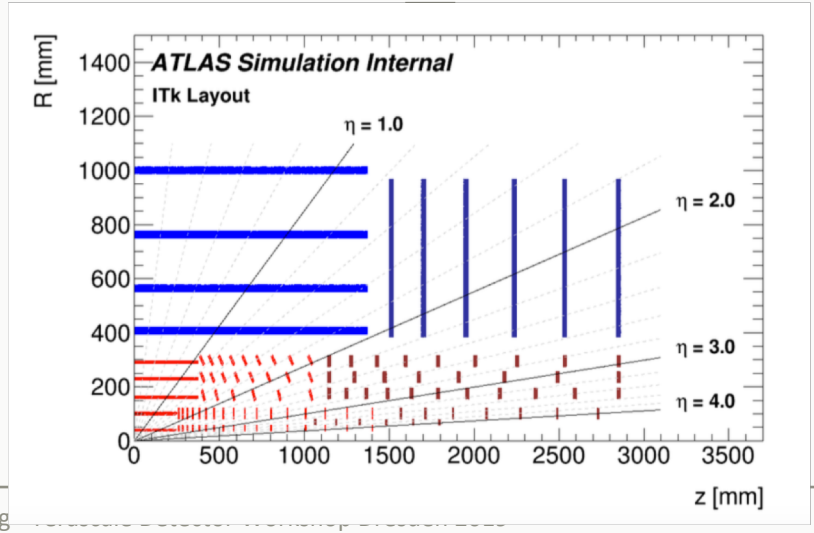
# ITK PIXEL DETECTOR LAYOUT

Design goal:

- ITk should provide the same performance as the current detector, but in harsher environment of the HL-LHC



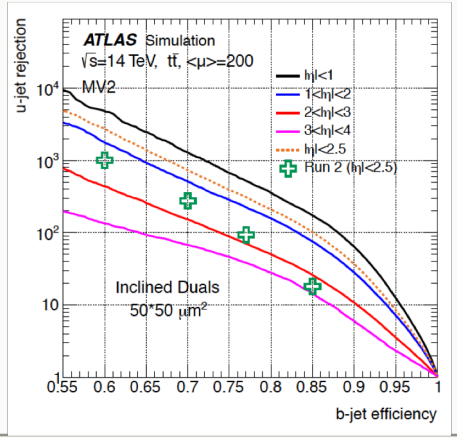

- All silicon design
- η coverage increased from 2.5 to 4
- 5 pixel barrel layers and 5 pixel rings
- 10,000 modules with 13 $m^2$ of pixel detectors
- Design of the pixel part has been finalized: inclined layout optimization

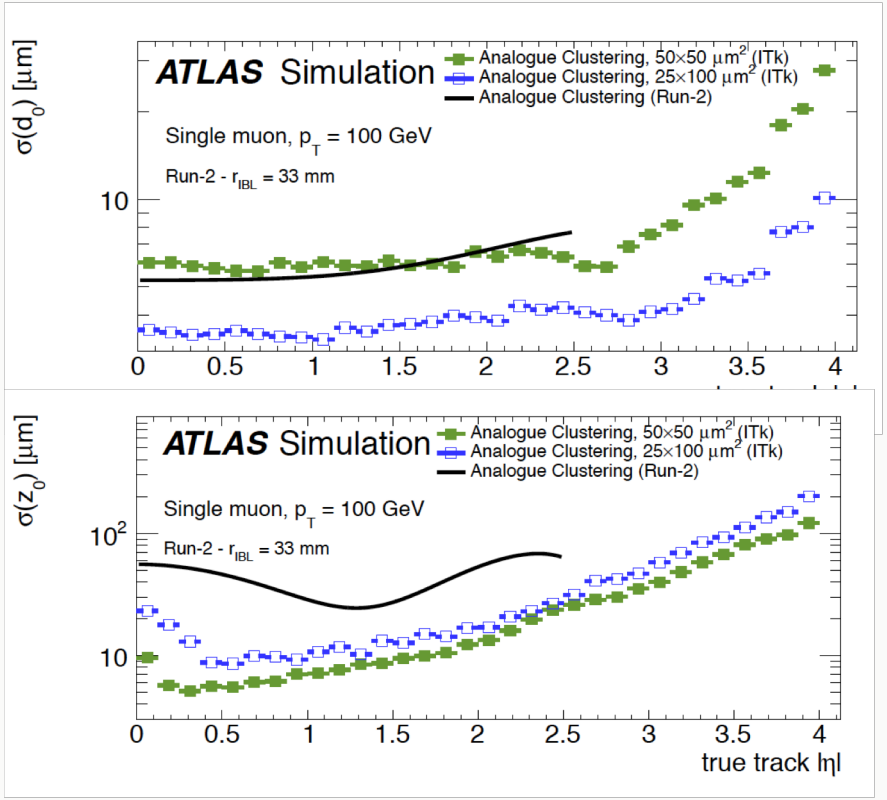



Technical Design Report for the ATLAS Inner Tracker Strip Detector
CERN-LHCC-2017-004. ATLAS-TDR-025, April 2017

# ITK PERFORMANCE

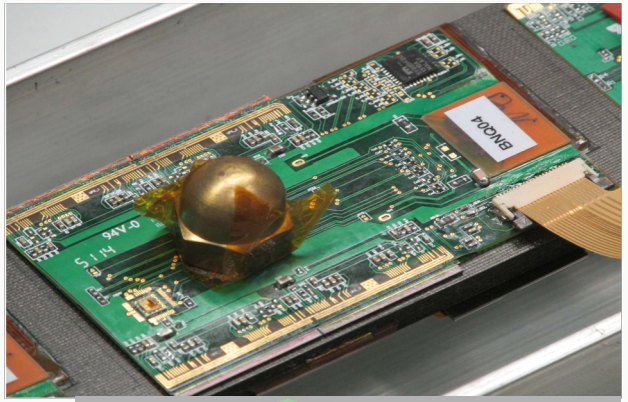
- Tracking resolution and particle identification performance comparable to or better than in Run-2, even with μ~200, for ITk Inclined layout
- Shows that our reconstruction algorithms are performing well in this challenging environment, and proper choices have been made in terms of optimal layout geometry

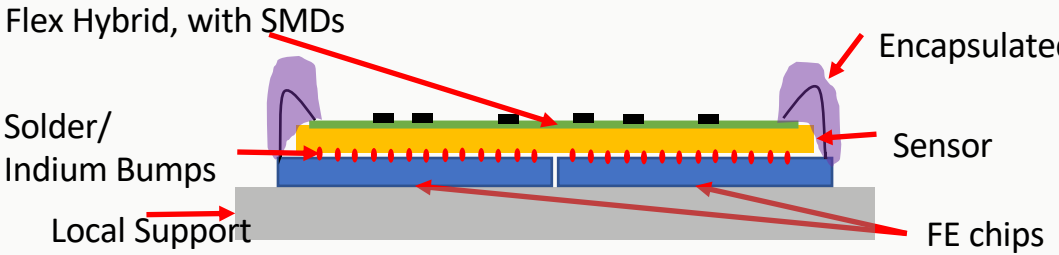


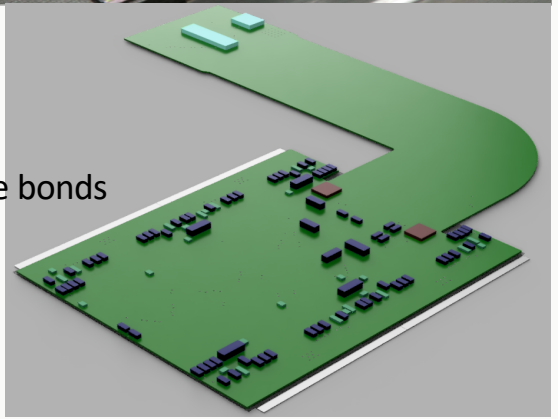



# PIXEL MODULE ASSEMBLY

- Basic building block is the pixel module:
  - bare module assembly consisting of sensor and FE-chip(s)
  - flex hybrid for interconnection of data power line to the local support services
  - Connection between FE, sensors and flex is done via wire-bonds
- For ITk about 10,000 modules are needed (quad- and single chip modules)

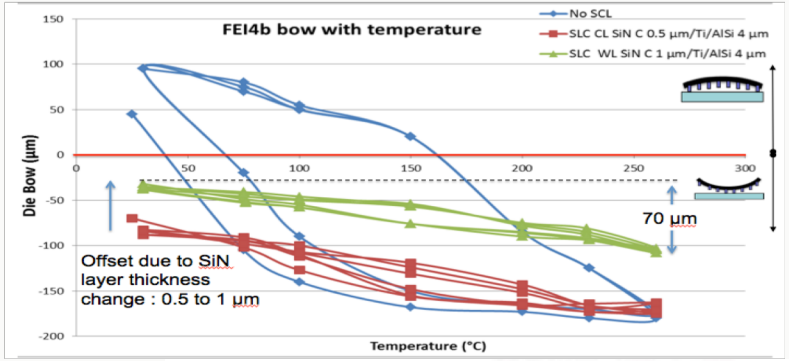


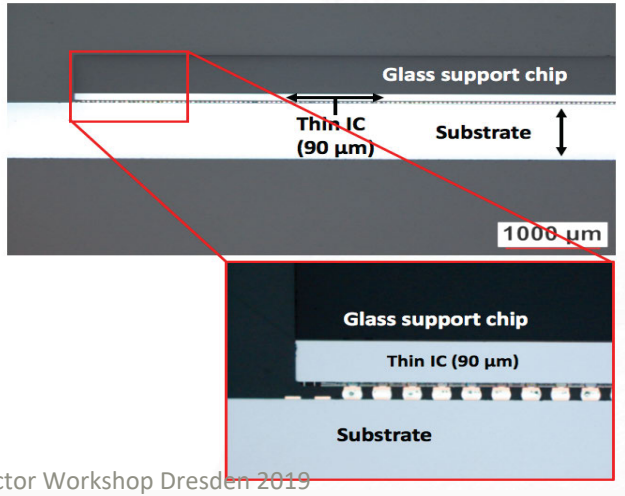


# PIXEL MODULES: BUMP BONDING

- Technology and requirements similar to ATLAS IBL, but
  - huge increase in volume → high production rate required
  - 12,000 modules in two years yield in peak flip-chip rate of 50 modules/day
  - Share the load: progress with several vendors (SnAg or In)
- Technical challenges:
  - assembly of thin devices:
    - sensor as thin as 100µm
    - FE chip 150µm or below → chip bow during reflow
  - Wafer sizes: 300mm FE, 150…200mm sensors
  - bump denisty of 400 bump per $cm^2$ at 50µm pitch
  - smaller inter-chip spacing



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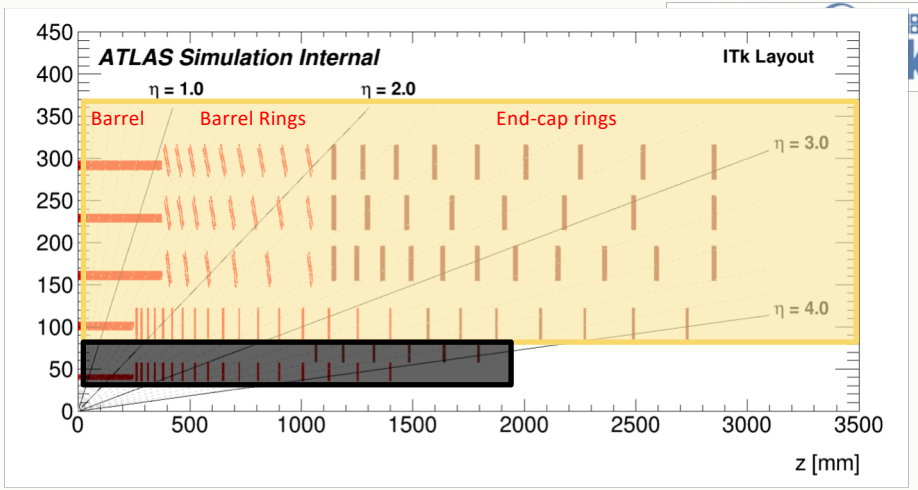
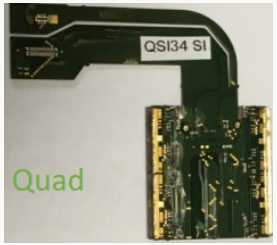
# MODULE TYPES

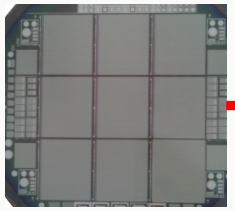
- **Quad modules** are used in all the Outer System sections (Barrel, Barrel Rings and Rings) and in the Inner System Layer 1.
- **Single modules** (with 3D sensors) are used in the Inner System Layer 0.
- As part of the finalization of the design (FDR in 2020), an effort is in progress to minimize the number of module variations.
- In particular, it could be possible to use the same module type in the Outer System and ECs, using only different connection tails.



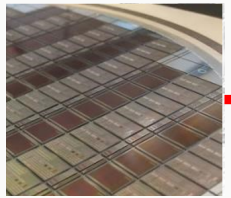




| Layer/Ring | Single | Quads |
|---|---|---|
| Layer 0 | 1064 | |
| Layer 1 | | 920 |
| Layer 2-4 | | 4472 |
| Ring 0 | 336 | |
| Ring 1 | | 280 |
| Ring 2-4 | | 2344 |

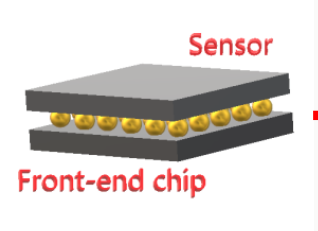
# PRODUCTION STEPS



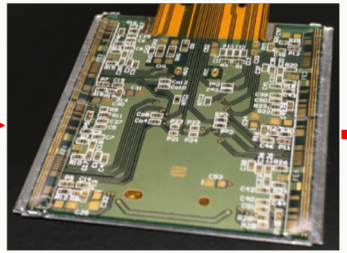
Sensor



FE chip




Bare Module



Assembled Module

Module Loaded on Local Support

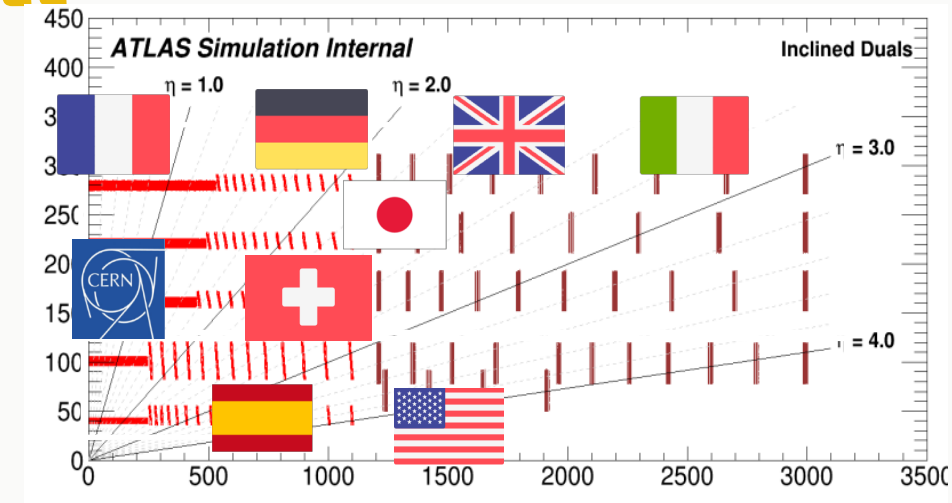
Hybridization

Module Assembly

Module Loading

# PRODUCTION MODEL

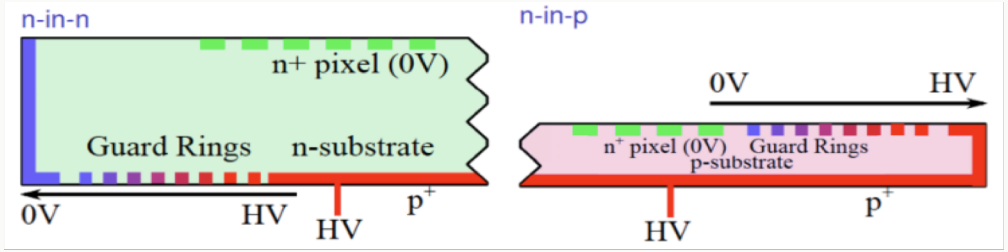
- Module production will be performed in **9 clusters worldwide.**
- There will be some specialization, but **each cluster will produce several types.**
- **200 modules/week** needed in production.
- Loading will be performed in 9 centers, but more then 9 loading lines are needed.
- The outer barrel will be assembled at CERN.
- The inner system will be shipped in complete quadrants from US and assembled at CERN.
- The end-caps will be shipped from UK and Italy.

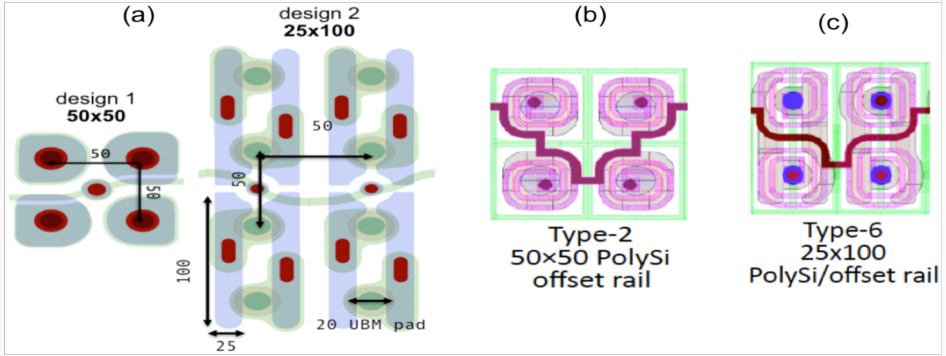



| Activity | Number of clusters |
|---|---|
| Module assembly | 9 |
| Module QA/QC | ~15 |
| Module loading | 9 |
| Integration | 4 |

# PLANAR PIXEL SENSORS

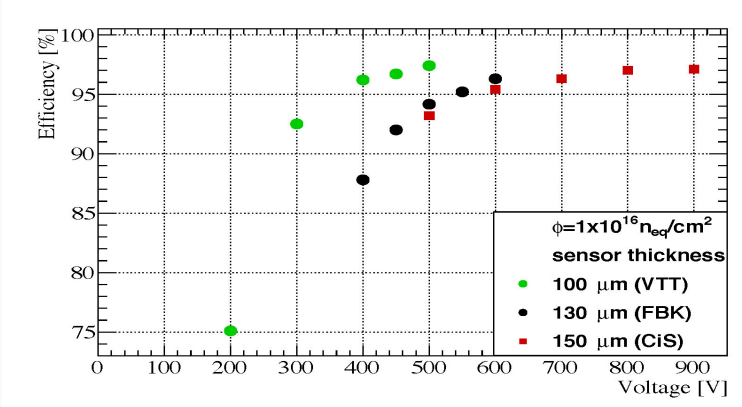
- Planar sensor technology
  - well understood and proven
  - n-in-p compared to current n-in-n → HV insulation on sensor or chip needed
  - for large areas: outer layers and quad assemblies → high yields and low costs
  - Small pixel size of 50x50 µm$^2$ or 25x100 µm$^2$
    - → mitigate effects of charge losses due to punch-through bias grid or bias rails
    - → polysilicon bias resistor helps here but usually also increase the noise
  - thin sensors with 100 (L1/R1) & 150 µm (L2/R2-L4/R4) → dealing with small signals (few ke$^-$) after high radiation fluences while keeping the power dissipation low

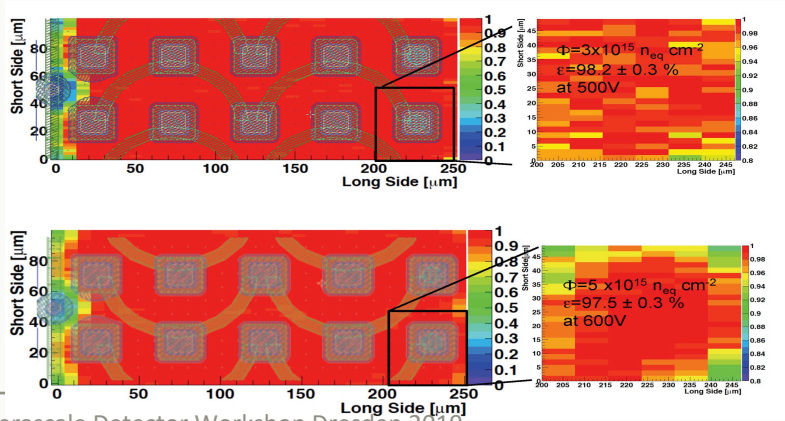


# PLANAR PIXEL SENSORS

- Test of hit efficiency with FE-I4 compatible sensors of different vendors and thickness at $10^{16}$ MeV $n_{eq}/cm^2$:
  - 97% hit efficiency is achieved
  - for thinner sensors this efficiency is already reached at lower bias voltages between 400 - 500 V
- $50x50\ \mu m^2$ pixel cells has been tested with a modified sensor design w/o bias structures to extrapolate the performance expected with RD53



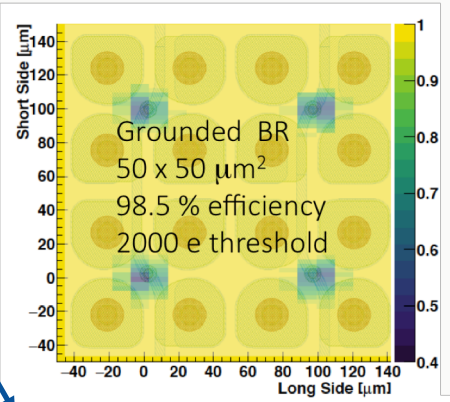



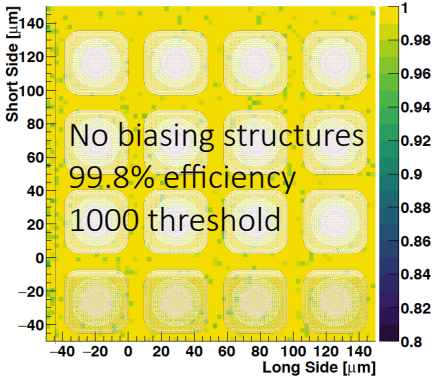
# PLANAR SENSORS WITH RD53A

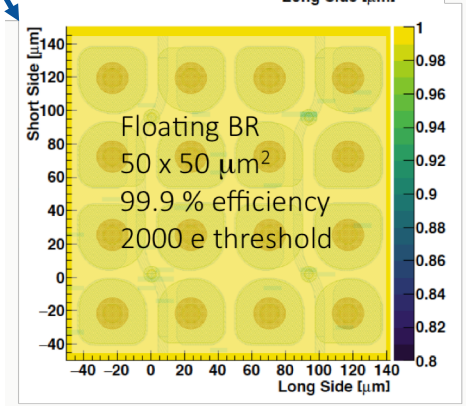
- Effect of biasing structure for 50 x 50 µm² pixel cell design, unirradiated:
  - Clear efficiency drop in bias dot area for grounded biasing structure
  - For floating biasing structure similar high efficiency everywhere as for design without biasing structure
  - Established a new pixel design (“split design”) which allows the grounding of the n-ring around the matrix while the bias grid is still floating → high efficiency also at the edge pixel
- For 25 x 100 µm² pixel cell design the effect of the floating BR is not as high as for 50 x 50 → still see a small efficiency loss in the bias dot area

150 µm thick sensors, 50 V bias, with PT and floating BR

100 µm thick sensors, 50 V bias, w/o biasing structures

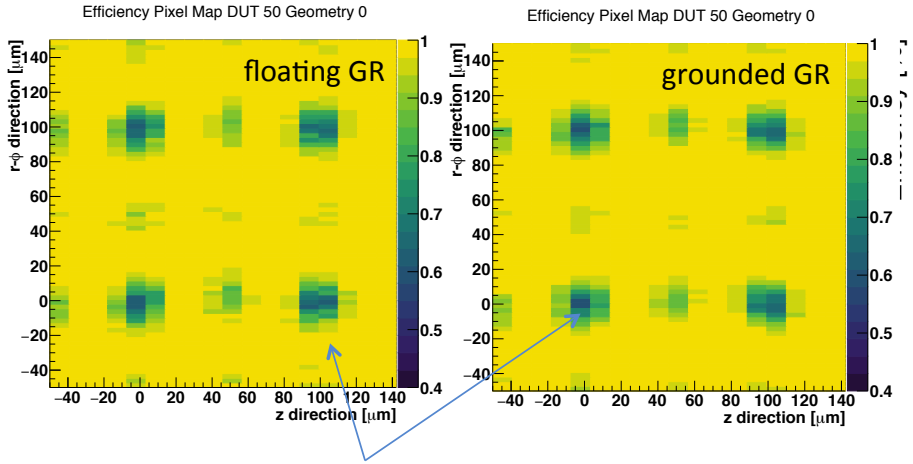


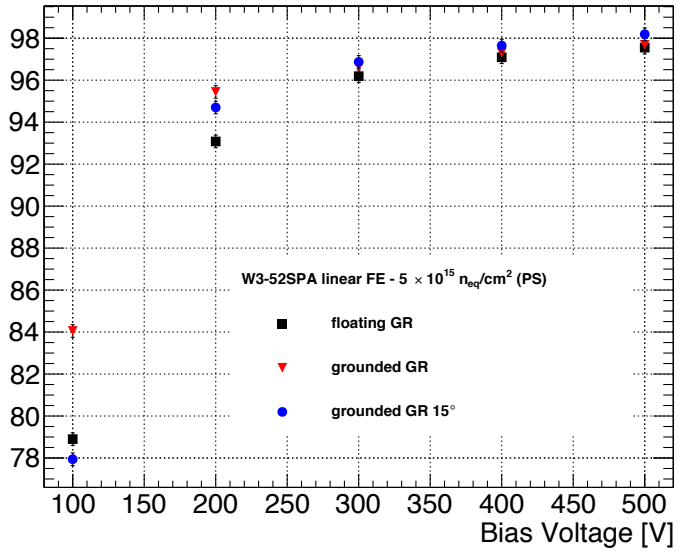
# IRRADIATED PLANAR SENSORS WITH RD53A

- Efficiency of the „split design“ sensor irradiated to 5x10$^{15}$ $n_{eq}$/cm$^2$ with 50 x 50 µm$^2$ pixel cell
- High efficiency of about 98% at 500 V is reached even with a biasing structure - spec is 97%
- Effect of the floating BR is vanishing w.r.t. sensors w/o biasing structure which shows 99% efficiency at 500 V



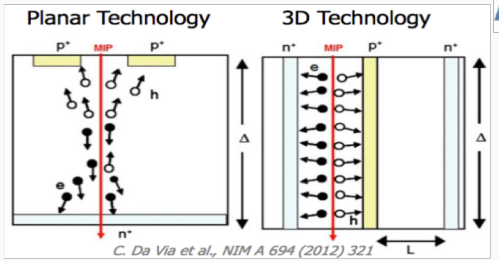

Very similar effect of PT dots with the two different configuration of the ring implant potential

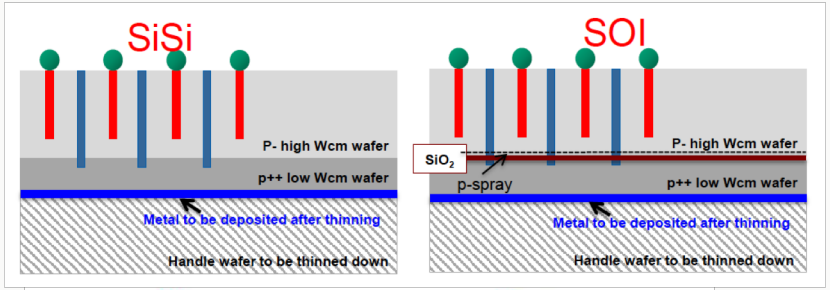
100 µm thick sensor, Threshold ~1100 e-

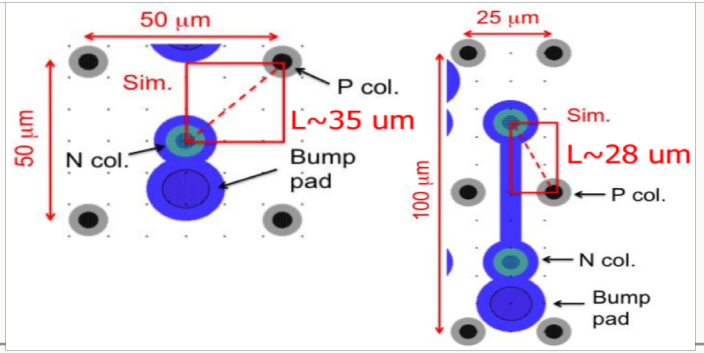


# 3D PIXEL SENSORS

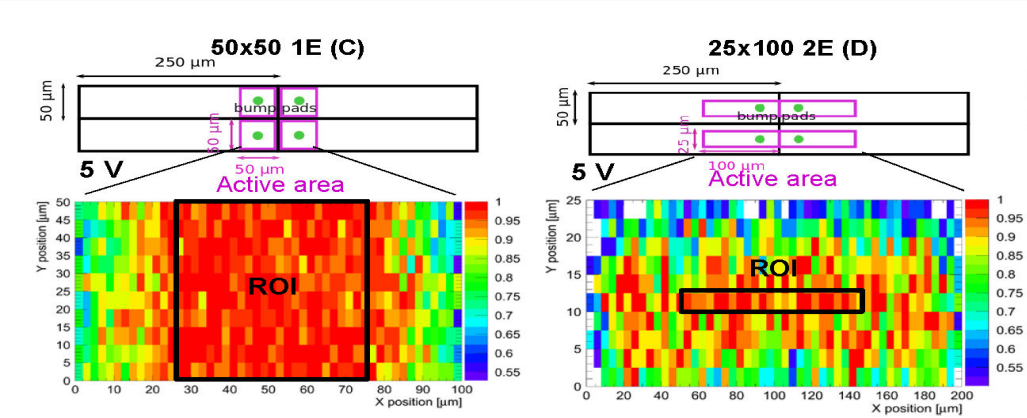
- 3D sensor technology is the baseline for the innermost layer (L0/R0) due to the advantages in radiation tolerance
- 3D sensors are successfully used inside the ATLAS IBL
- Main challenges for the usage inside ATLAS ITk:
  - smaller pixel (50x50 or 25x100 µm$^2$) are more demanding with the column electrodes
  - yield improvements
  - thinner sensors to optimize signals and hits per track: 150µm active thickness on 100µm support wafer needed for process

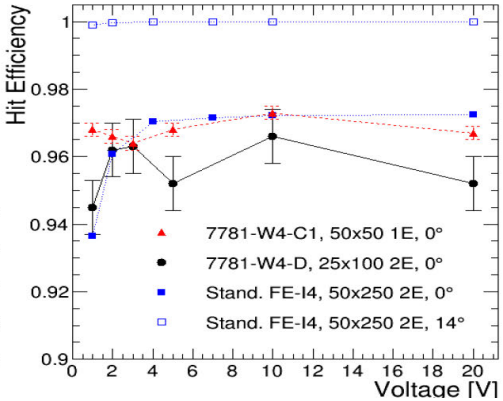


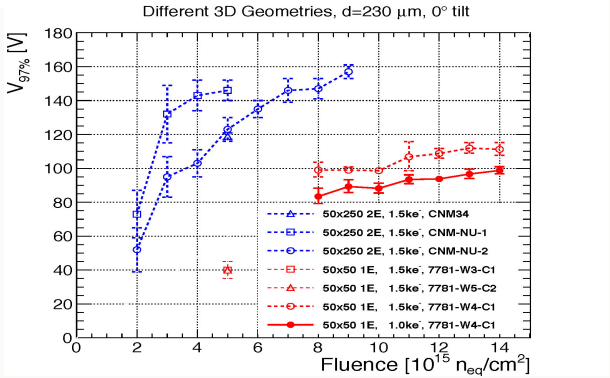



# 3D PIXEL SENSORS



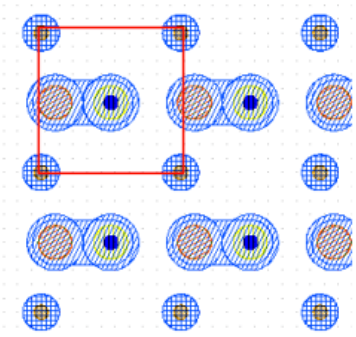

- Small pitch sensors have been investigated with FE-I4 chip before and after irradiation:
  - hit efficiencies of 97% could be achieved at moderate bias up $1.4*10^{16}$ MeV $n_{eq}/cm^2$
  - good uniformities inside the pixel for both pixel sizes
  - $50x50\mu m^2$ pixel size is preferred



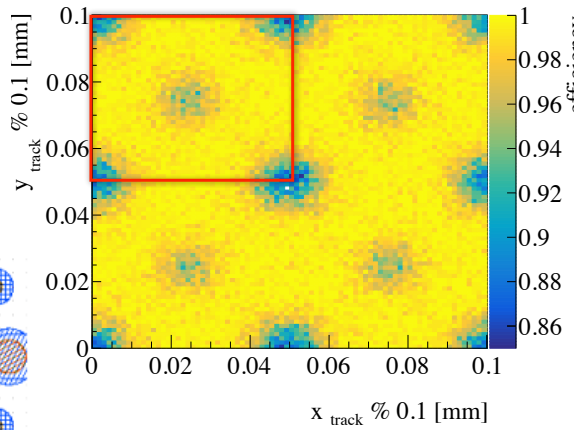
# 3D SENSORS WITH RD53A

- 3D FBK sensor with 130 µm active thickness and 50 x 50 µm$^2$ pixel cell design

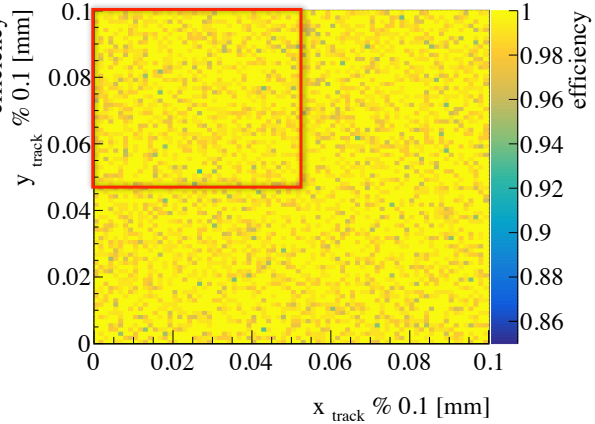
w91 x1y3



3D 50x50, Bias = **14 V**
0 deg tilt, Eff=98.6%

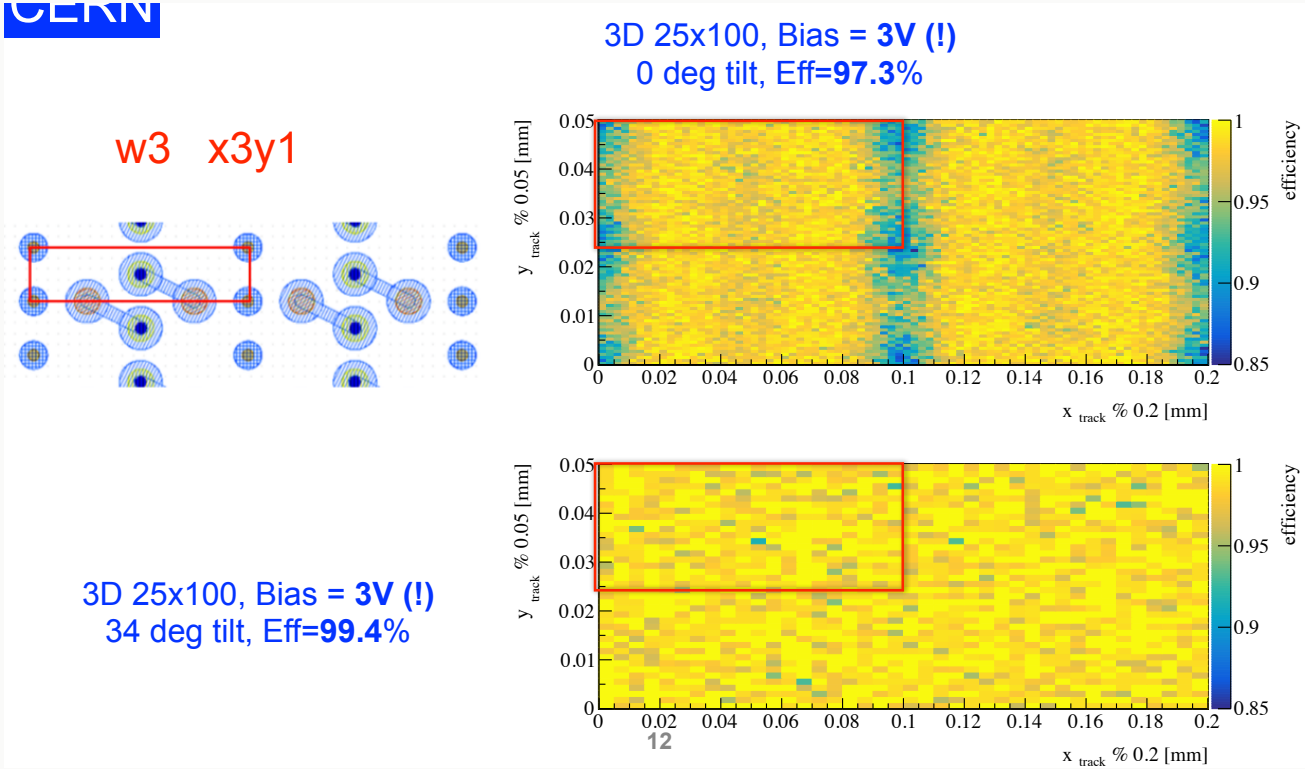



3D 50x50, Bias = **34 V**
34 deg tilt, Eff=99.3%



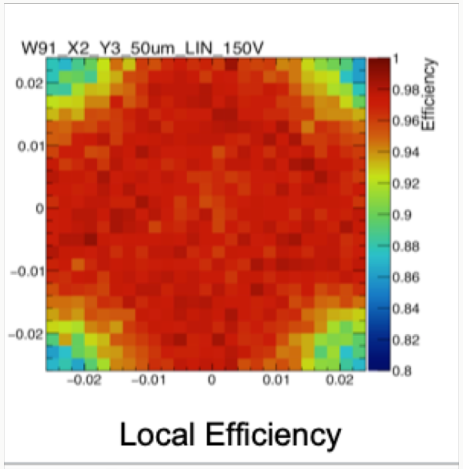
# 3D SENSORS WITH RD53A

- 3D FBK sensor with 130 µm active thickness and 25 x 100 µm$^2$ pixel cell design



# IRRADIATED 3D SENSORS WITH RD53A

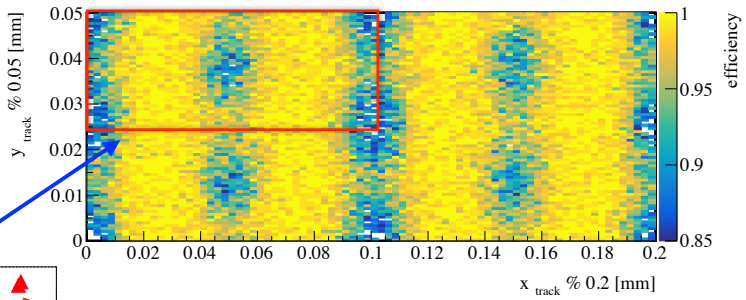
- 3D FBK sensors with 130 µm active thickness irradiated to ~1x10$^{16}$ $n_{eq}$/cm$^2$
- Efficiencies between 96.5 – 97.5 % w/o tilting and for 120 – 150 V bias
- Still some uncertainties about fluence

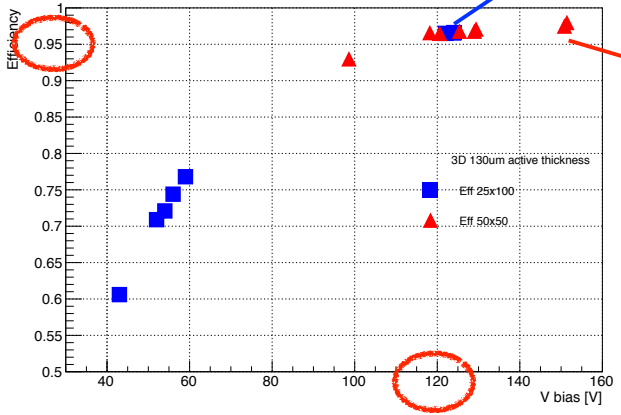


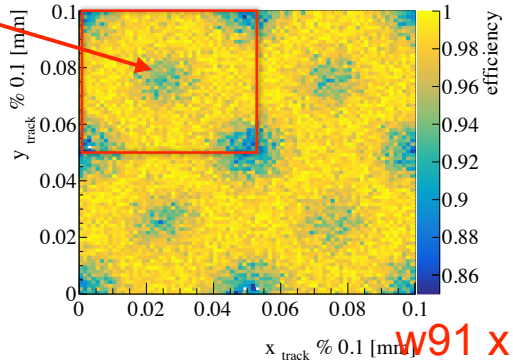

CERN

w3 x3y2

Irradiated Modules



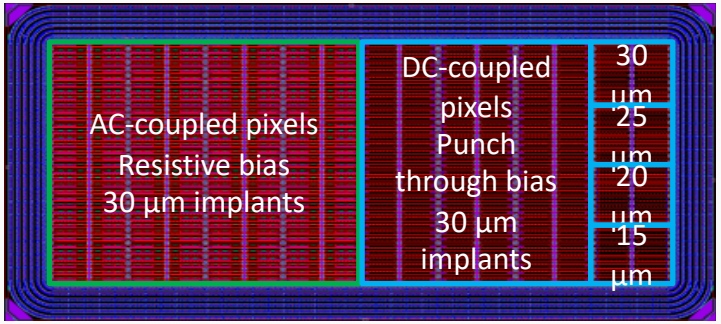



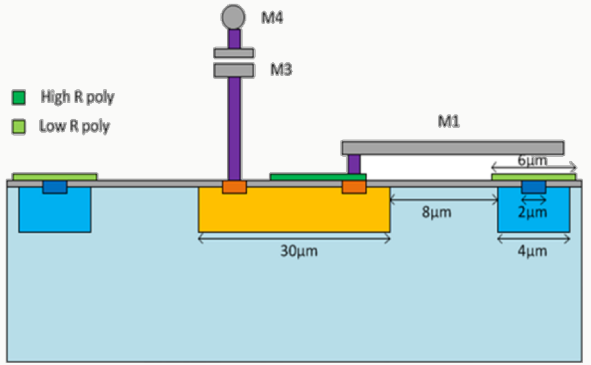

w91 x1y3

# PASSIVE CMOS PLANAR SENSOR

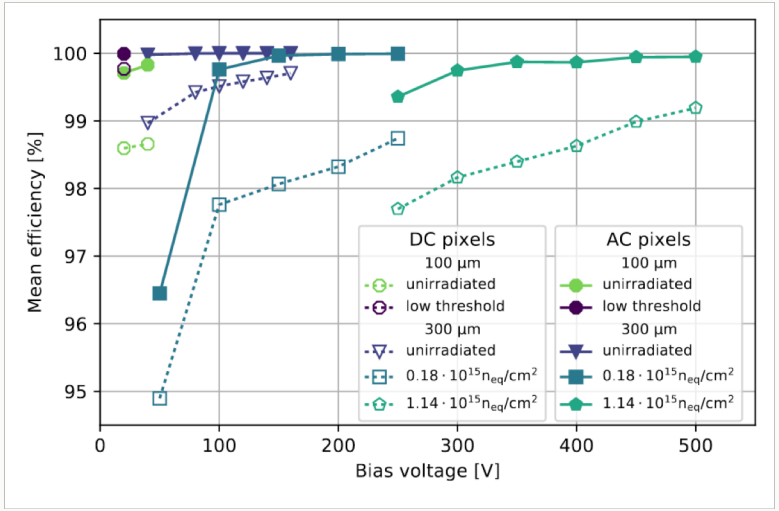
LFoundry 150 nm CMOS technology

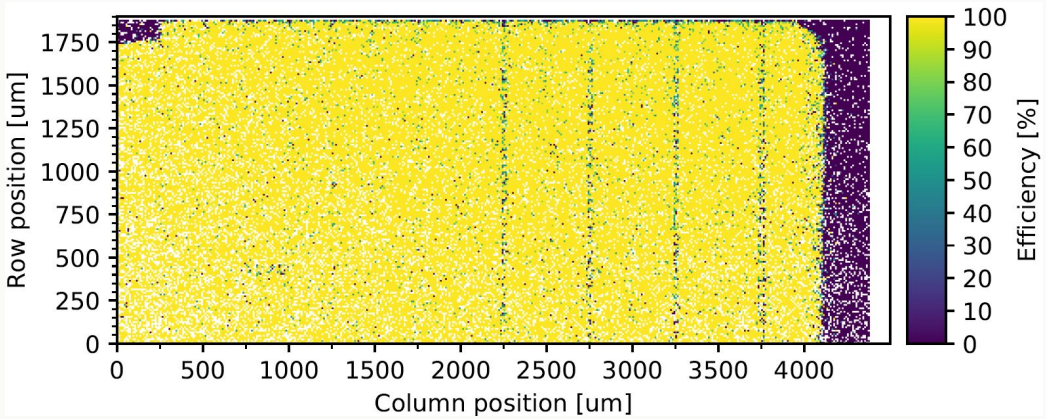
- 2kΩcm p-type material, CZ 8’’
- Passive pixel, i.e collecting node w/o electronic
- 100/300µm thick, backside processed
- Bump bonded to ATLAS FE-I4
- Pixel size: 50 µm x 250 µm
- Matrix size: 16 x 36 (1.8 x 4 $mm^2$)
- Standard DC-coupled pixel Implant size variation
- AC-coupled pixels: 15 MΩ polysilicion resistor / 3 pF MIM capacitor



# PASSIVE CMOS SENSORS WITH FE-I4




CERN SPS 120 GeV/c pions, Mimosa26 telescope
ATLAS FE-I4 time reference plane

D.-L. Pohl, T. Hemperek et. al.
JINST 12 (2017) P06020

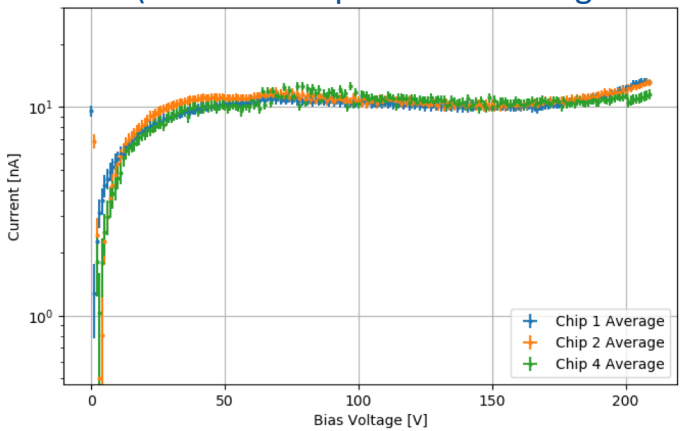
- Very good efficiency of > 99.9% before and after irradiation to 1.1 x $10^{15}$ $n_{eq}/cm^2$ esp. for AC-coupled pixel (no biasing structure)
- DC-coupled pixel show expected efficiency loss at bias dots → 99.1% efficiency at 500 V

**→ CMOS foundries can do good planar sensors (8")**

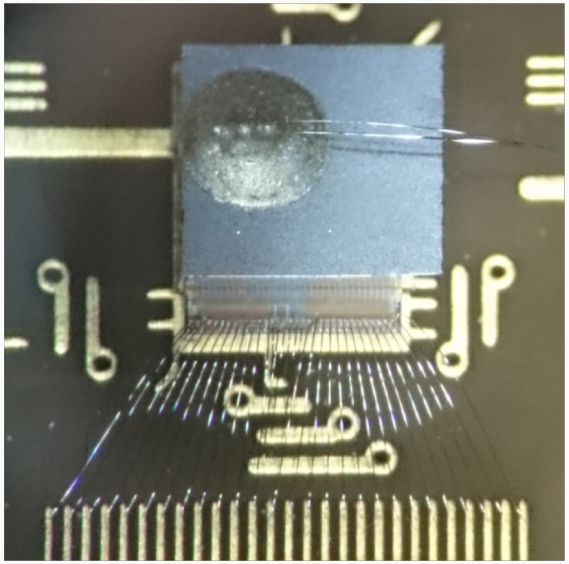
**→ Development is ongoing as planar sensor option for the ATLAS ITk hybrid pixel detector**

# LFOUNDRY PASSIVE CMOS SENSOR 50 X 50 PIXEL DESIGN

- 50 x 50 um² (Pixel geometry of future ATLAS Pixel detector)
- 64 x 64 pixels (~ 4 x 4 mm²)
- No bias grid, DC coupled pixels
- Bump bonded to FE-65p2 (predecessor of ATLAS/CMS pixel prototypes)
- Break down: > 200 V (> 200 um depletion assuming 2 kOhm-cm, p-type):

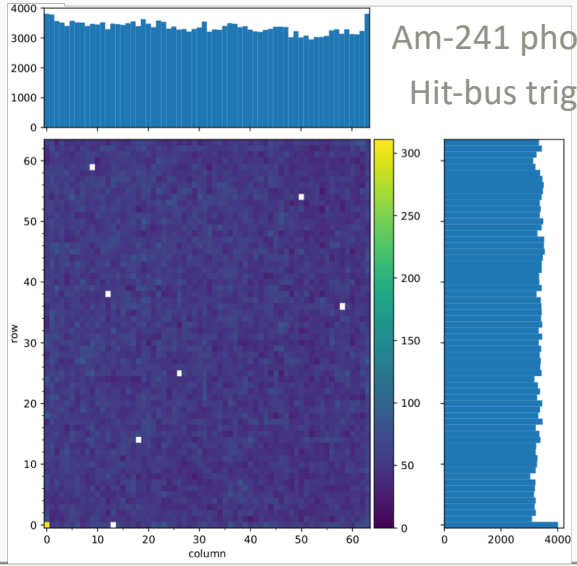



LF sensor w/o backside processing
Backside contact with conductive glue



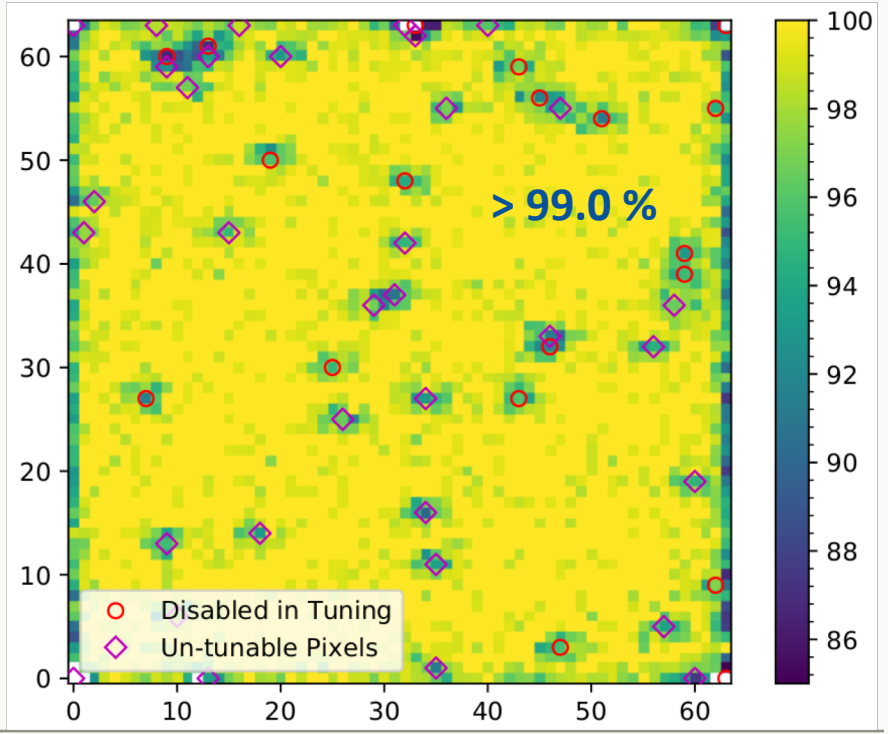
# LFOUNDRY PASSIVE CMOS SENSOR SMALL PIXEL DESIGN

- Sensor illuminated with $^{241}$Am photons
- Only 8/4096: < 0.2% give bad signal, likely FE related
- Fine-pitch bump bonding works (IZM Berlin)




Hit efficiency in test beam

Threshold: ~1 ke
Charge: ~ 10 ke



# CONCLUSIONS

- ATLAS ITk Pixel project is making good progress in a lot areas:
  - ATLAS ITk Phase 2 Pixel Detector module and sensor design has reached maturity:
  - Sensor technologies are far advanced and verified with RD53A
    - Thin planar sensors are fulfilling specs and can be used everywhere probably even in the innermost layer as backup solution
    - Biasing structures allowing sensor testing prior to hybridization introduce significant efficiency losses after irradiation and maybe discarded for the final sensor design
    - 3D sensor design for small pixel is ready and shows good performance up to $10^{16}$ $n_{eq}/cm^2$ with clear advantages in terms of power dissipation
    - 3d sensor design clearly favors a 50 x 50 $\mu m^2$ pixel cell
- We will have a final design within the next 2 years and enter pre-prodution afterwards