DC-DC Powering in LHC Phase-1 and Phase-2 Tracker Upgrades

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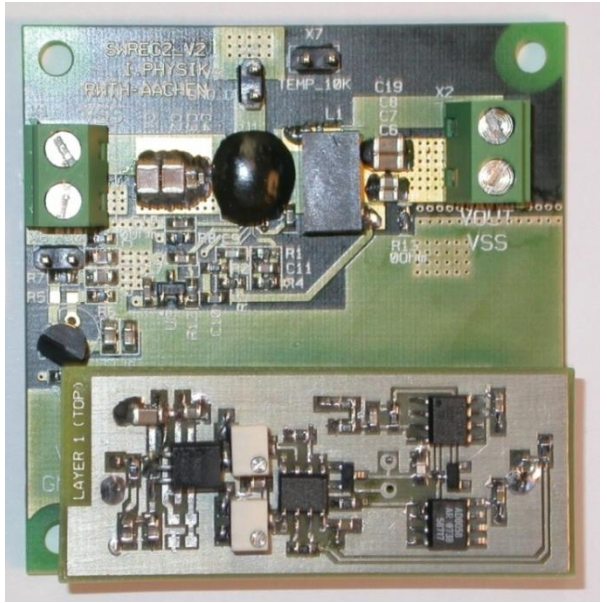
A Bit of History

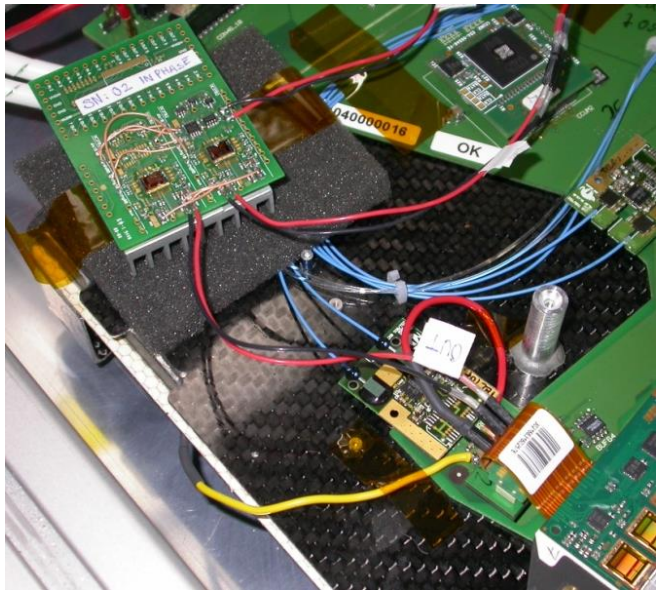
- **In ~2007, DC-DC conversion powering schemes were proposed for the power-hungry Phase-2 trackers**
  - Less voltage drop on cables (~I)
  - Less ohmic losses on cables (~I^2)
  - Less material needed in supply cables
- **CERN started to develop rad.-tolerant and magnetic-field tolerant DC-DC converters**
  - Berkeley worked on charge-pumps
  - Yale proposed commercial DC-DC converters
  - Only CERN DC-DC converter survived
- **In direct competition with serial powering**
  - Years of discussion in ATLAS and CMS!
- **Many people were (very) sceptical:**
  - Switching devices → noise on power lines
  - Air-core inductor → electro-magnetic emissions
  - Bulky → adds material in the active volume
  - Radiation-tolerance, SEUs, etc.

input current ≈ output current x (V_{out}/V_{in})

Early prototypes

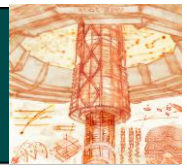


CERN, SWREG2, 2008



LBL, charge pump, 2008

The Situation Today



- Widely accepted in HEP as a viable powering scheme
- Serial powering only used in Phase-2 pixel detectors (where space constraints are inhibitive and material is most critical)

Experiment	Sub-detector	What	Where	DC-DC converter
CMS	Outer Tracker	Strip modules, LpGBT, VTRx+	FE	CERN
	Phase-1 pixel	Pixel modules	PP	CERN
	Phase-2 pixel	LpGBT, VTRx+	PP	CERN
	Endcap calorimeter	Silicon modules, LpGBT, VTRx+	PP or FE	CERN or commercial
	Barrel calorimeter	Crystal ADC	FE	CERN
	Muon system (GEM)	Chambers	FE	CERN
	Timing detector	Readout, LpGBt, VTRx+	FE	CERN
ATLAS	Strips	Strip modules, LpGBT, VTRx	FE	CERN
	Tile calorimeter	Electronics	PP	Commercial
	Liquid argon calorimeter	Electronics	FE	Commercial
	Muon micromegas	GBTx, VTRx	FE	CERN
LHCb	Velo	Pixel modules, GBTx	PP	CERN
	Fiber tracker	Fiber modules, GBTx, FPGA	FE	CERN
ALICE	Pixels	Pixel modules	FE	CERN
Belle 2	SVD	Silicon modules	PP	CERN

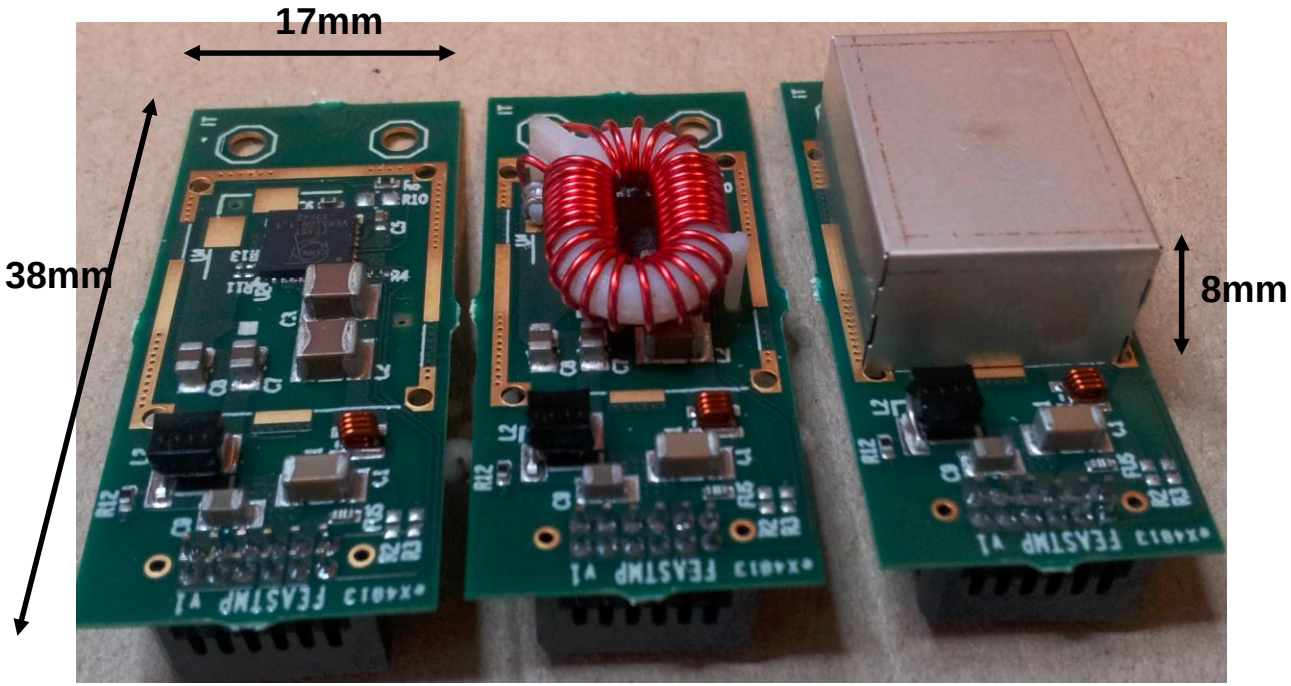
FE = front-end
PP = patch panel

Not exhaustive!

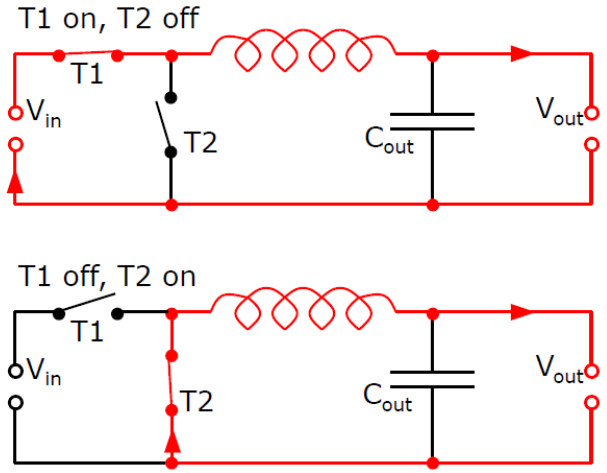
Lot‘s of simplification, not necessarily correct, treat with care!

CERN DC-DC Converters

- DC-DC converters were developed from scratch:
  choice of topology (“buck“), technology (I3T80 automotive), ...
- Both chips (mostly used by trackers) and full modules (basically everybody else) are sold
- FEAST2.x available; bPOL12V and bPOL2V5 are under development for Phase-2 trackers



CERN FEASTMP modules



FEAST2.x specifications and features	
Input voltage	5-12V
Output current	4A max (needs cooling)
Switching frequency	1.5 – 2.0 MHz
Efficiency	Typically 80-85% for 2-3A and V_{in} = 10V
Protection features	Over-temperature, over-current, under-voltage
Remote control & monitoring	Power good bit; output voltage delivery can be enabled/disabled
Radiation levels	200 Mrad TID, 5 x $10^{14} n_{eq}/cm^2$

https://project-dcdc.web.cern.ch/project-dcdc/

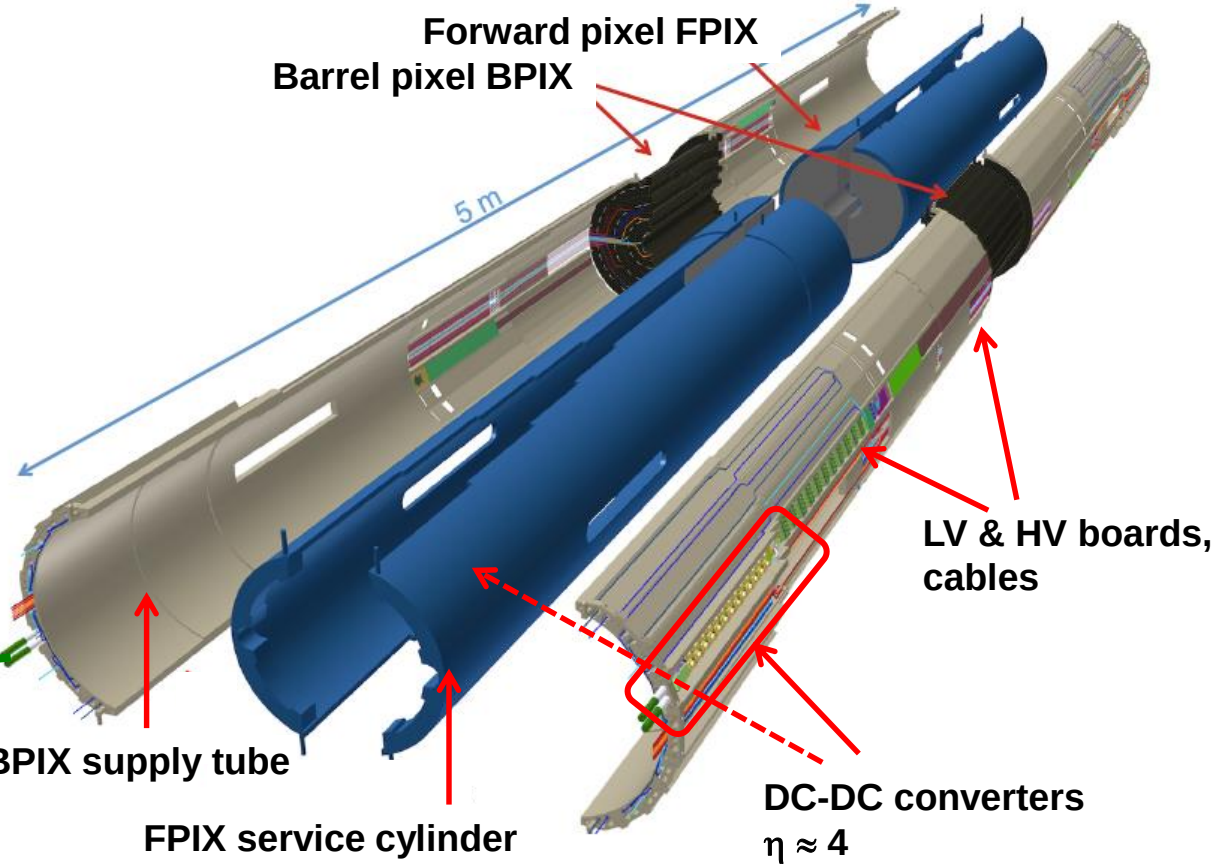
CMS Phase-1 Pixel Detector

Power System Overview

- Phase-1 pixel detector needs twice the power of original detector → with direct powering, new power supplies & cables needed
- In 2009 it was decided to move to a DC-DC conversion powering scheme; requirements fitted well with FEAST specs
- DC-DC converters are about 1-2m away from pixel modules, at $\eta \approx 4$ (outside tracking volume)

CAEN A4603 power supplies
Modified for DC-DC conversion

Multiservice cables
43m + 5m + 0.5m

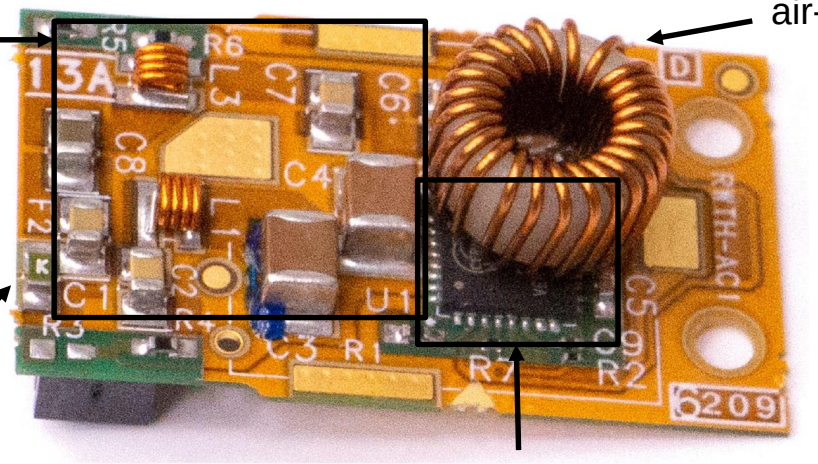


Pixel DC-DC Converters

- Dedicated modules were developed: optimized for our needs (e.g. geometry), and allowed to do R&D and early prototyping
- Custom 2-layer PCBs (inspired by CERN design), shields, inductors
- 3 Flavours: output voltage of 2.4V (analogue domain of pixel chip), 3.3V and 3.5V (digital domain; depending on layer)

Basically **noise filters** at input and output

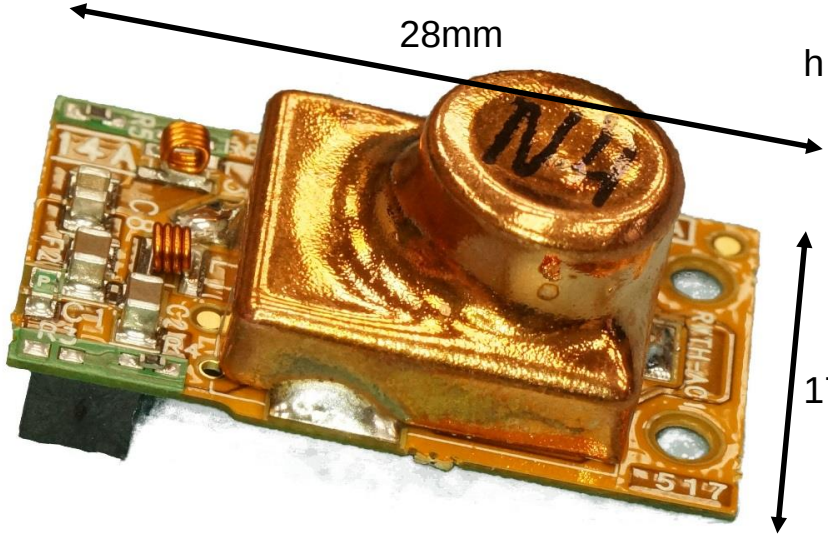
450nH toroidal air-core **inductor**



Fuse at input to protect from shorts (several DC-DCs in parallel)

FEAST2 chip

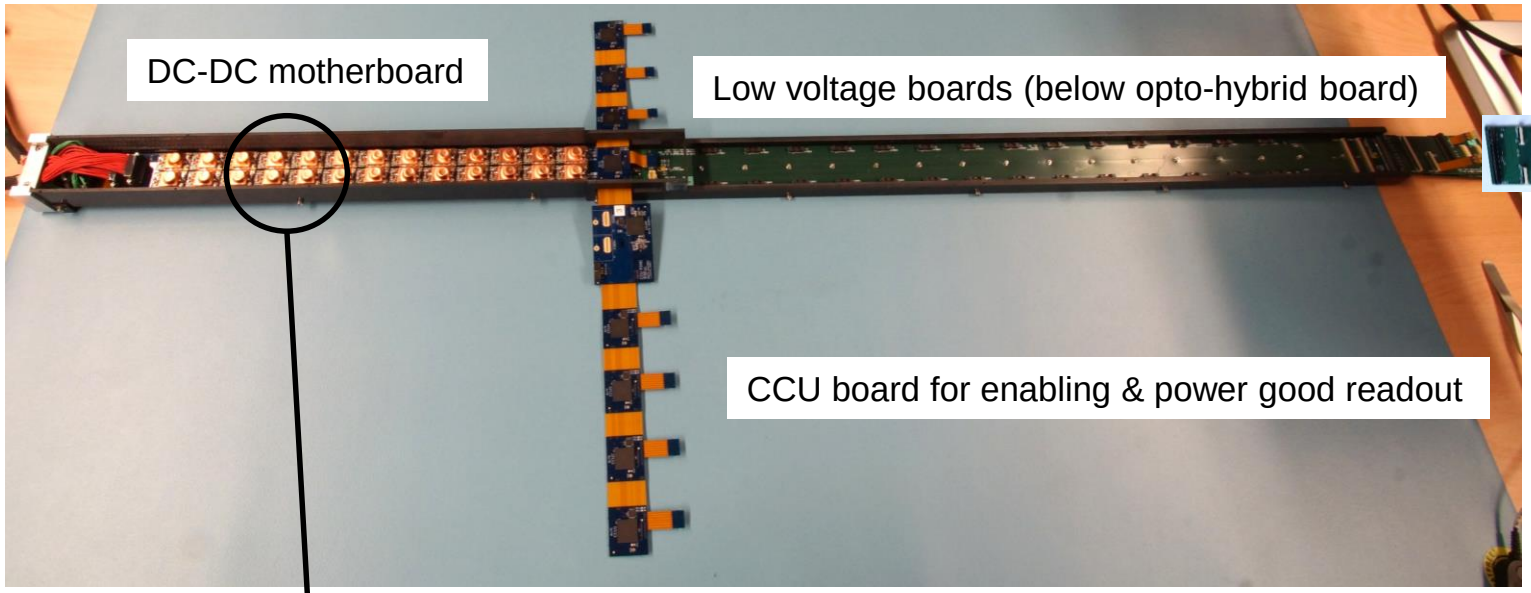
RWTH Aachen



Shield
- Plastic body with 60µm copper
- Shape needed due to space constrains

System Implementation (Example: BPIX)

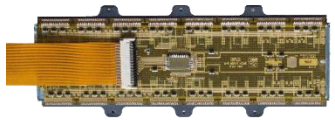
- Pairs of DC-DC converters (analogue + digital) power 1-4 pixel modules in parallel (I_{out} ranges from 0.5A to 2.4A)
- Up to 7 pairs of DC-DC converters are powered in parallel from one PS channel

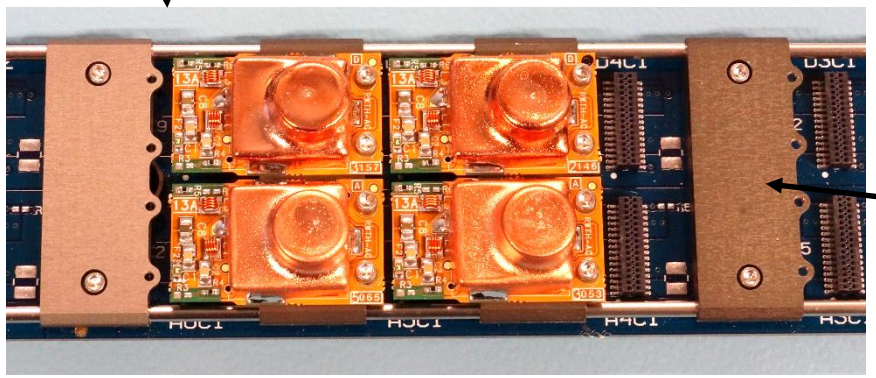


Low mass module cable (1m)

Connector boards

Pixel module(s)





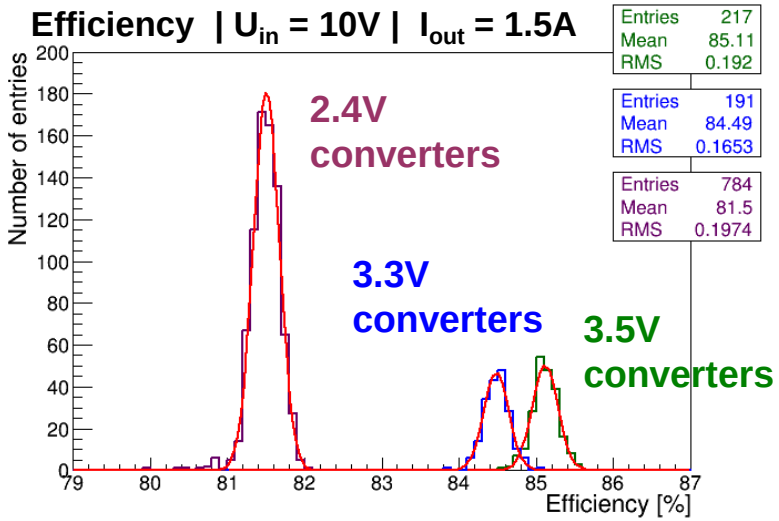
← CO_2 cooling pipes

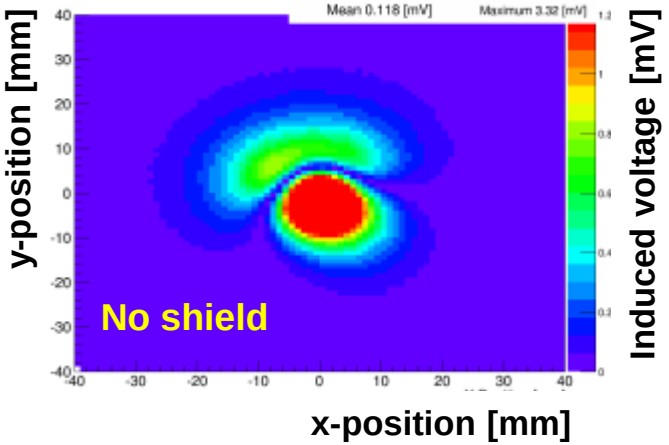
Aluminum cooling bridges

- There are 32 such sectors in BPIX
- Biggest challenge in the end:
  1-2m distance to load, but no sensing → large, load dependent, voltage drops

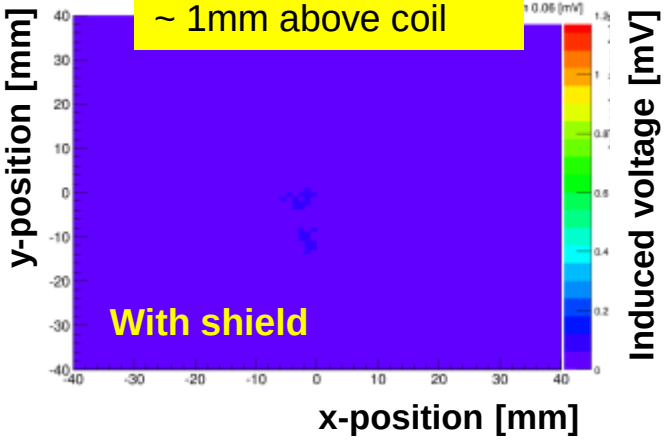
Stand-alone Performance

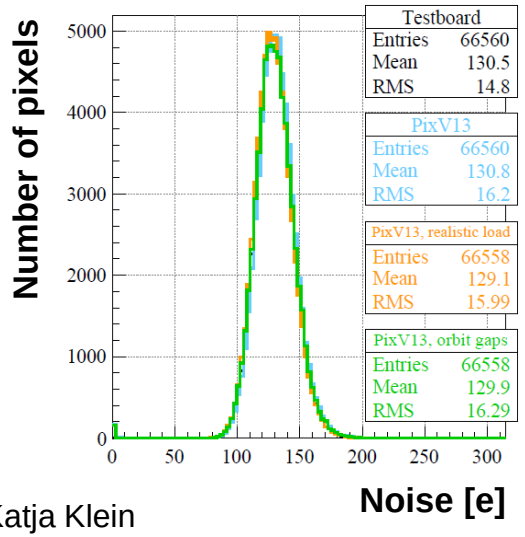
- **Several years of intense R&D and prototyping in pixel community, few examples shown**

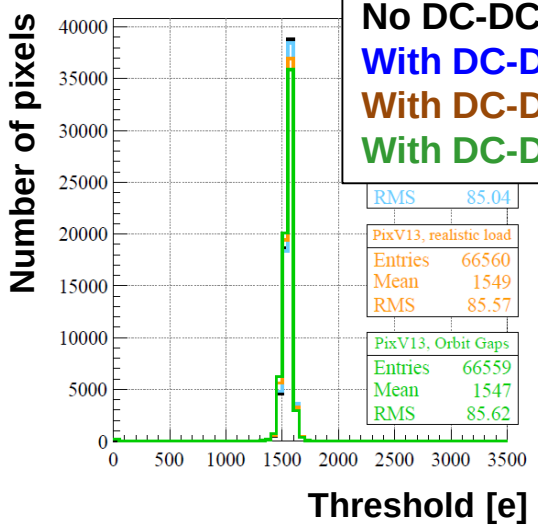




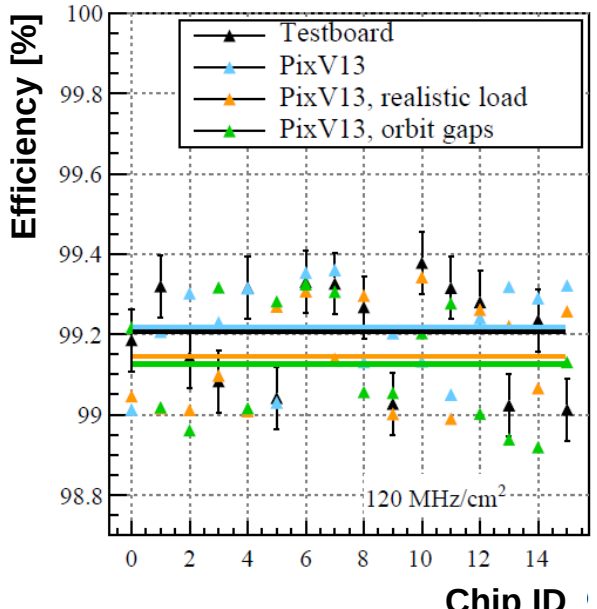
Map of B-field (A.U.)
~ 1mm above coil







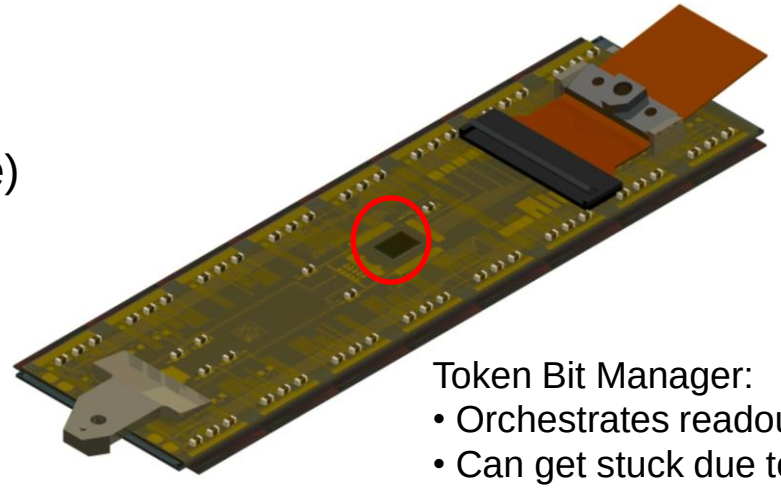
No DC-DC, reference
With DC-DC
With DC-DC, realistic load
With DC-DC, fast load changes



Hit efficiency with X-rays (120 MHz/cm²)

Failures

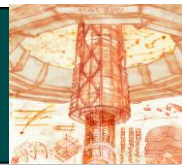
- Detector operation started in ~April 2017
- DC-DC converters worked very well! But then ...
- 5th of October: 5 DC-DC converters in FPIX died (no output voltage)
- First reaction: total disbelief, must be operational error
- 7th of October: first failure in BPIX
- Most failures after disabling/enabling cycles
- Until the end of the run, 5% of DC-DC converters had failed



Token Bit Manager:
- Orchestrates readout of 16 chips
- Can get stuck due to SEU → needs power cycling
- Done via dis/enabling DC-DCs

Impressively fast escalation:
- 10th of October: call by tracker coordinator, task force formed
- 12th of October: problem presented to all of CMS by (deputy) spokesperson
- 13th of October: been contacted by CMS technical coordinator and CMS electronics coordinator
- Around 15th of October: first discussions about pixel extraction
- 2nd of November: meeting with directorate to request to start YETS one week earlier
- At that point basically the complete HEP community knew of and cared about our problems ...

Theories (Selection)



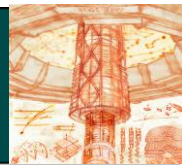
- **Something happened or changed on October 5th or shortly before**
- **Fuses blown**
- **Enabling or disabling is intrinsically risky**
- **Voltage spikes from the power supply (perhaps caused by disabling)**
- **Aging of capacitors**
- **Soldering problems related to thermal cycles**
- **Radiation issue**
- **Intrinsic problem of the ASIC**
- Threshold for enabling changes with irradiation, in DC-DC converter or CCU
- Problem due to fast load changes
- Module currents too high, problems related to configuring
- Communication with CCU does not work reliably
- Grounding issues (shift of control ground wrt LV ground)
- Too high or negative polarity signals at Vin, enable, Vout
- Problem related to ROC reset, done at 70Hz & 100Hz
- HV related (e.g. sparks)
- Chip getting too hot
- Backpowering
- Related to batches, or bad treatment during testing
- **Radiation damage behaving differently because of the presence of the magnetic field**
- **8b4e bunch structure, or parasitic collisions at high z**
- **Lorentz force on inductor when current is flowing through it, inducor moves and makes short with shield**
- **Plastic core in inductor crumbles due to irradiation and makes short**
- **Encapsulant of wires in package not cured**
- **Wire bonds in the ASIC package broken**

Color code:
Obvious ideas
Correct ideas (but only in combination)
Reasonable ideas
Exotic ideas

Strategy

- **Reproduction of problem in the lab: not successfull**
  - Several setups, at CERN and Aachen, even magnetic field tests repeated
- **Measurements in situ, e.g. via Detector Control System**
  - Dedicated debugging tests, sacrificing parts of the DC-DC converters
- **Measurements at power supplies during access**
  - IV characteristics of DC-DC converters, oscilloscope measurements ...
- **Production of new set of DC-DC converters**
  - Identical chip, higher-rated fuse
- **Extraction of pixel detector in shutdown**
  - Debugging, measurement of IV curve of all DC-DC converters (27% bad), exchange of all DC-DC converters
- **Longterm and irradiation tests, mainly from chip designers → in May 2018 problem reproduced & understood**
- **Change of operational procedures in 2018**
  - V_{in} lowered to 9V, enabling abandoned (instead PSs switched off) → no DC-DC converter lost!!

The Course



- **Problem reproduced by chip designers in irradiation tests in May 2018, with dis/enable cycles performed, then X-ray tests**
  - Radiation-induced leakage current in an unprotected transistor (HV NMOS) in FEAST2
  - Current is amplified by a current-mirror by factor ~500
  - Current flows to ground when converter is enabled
  - Current has no path when converter is disabled → charge up of a capacitor → large voltage transients of up to input voltage on a sensitive chip node specified to 3.3V → death or high-current state
  - Details are here: https://project-dcdc.web.cern.ch/project-dcdc/public/Reports.html and in F. Faccio's seminar talk: https://indico.cern.ch/event/788031/

- **Only relevant when TID is above 500krad**
- **New ASICs: FEAST2.2 (available) and FEAST2.3 (in summer 2019)**
  - Internal resistor in parallel to capacitor allows drain of current
- **CMS will exchange all DC-DC converters again in LS2**

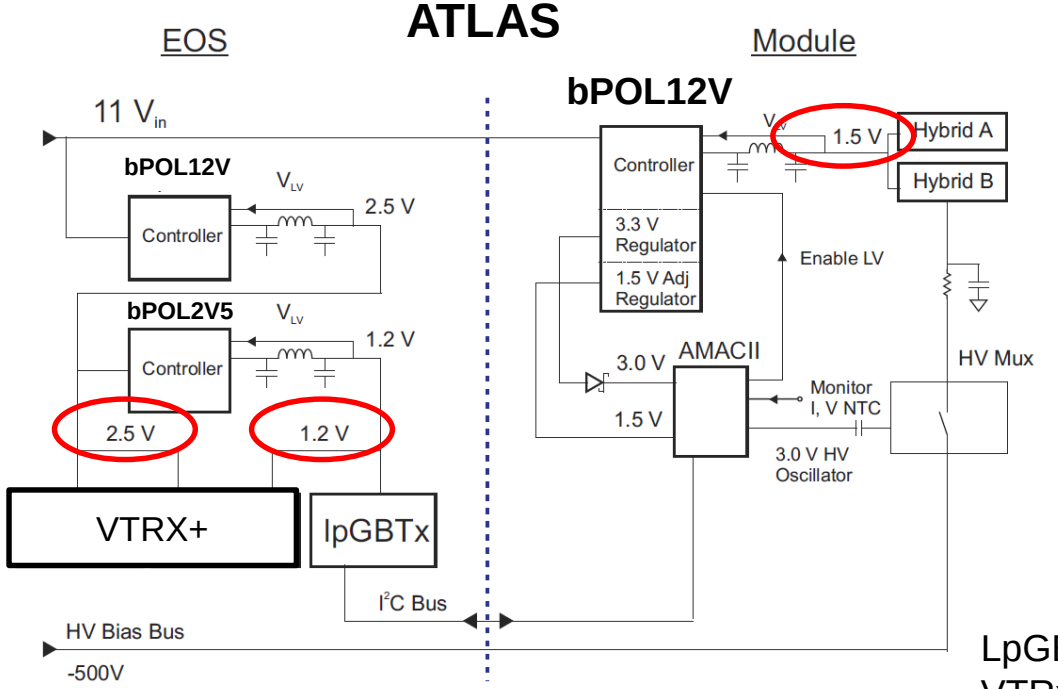
- **We were very lucky – problem would have hit us badly in Phase-2!!**

Phase-2 Strip Trackers: ATLAS & CMS

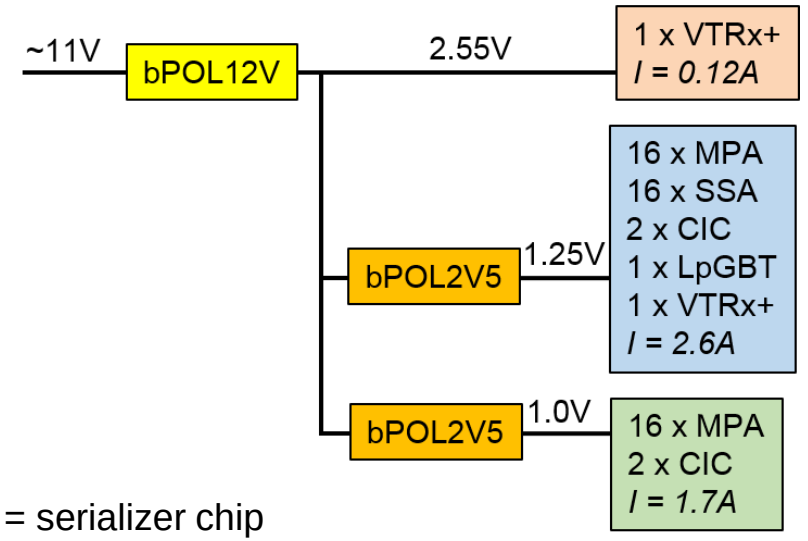
Low Voltage Powering Schemes

	ATLAS	CMS
Supply voltages	1.5V for ROCs 2.5V for VTRx+ 1.2V for LpGBT, VTRx+, ...	1.25V (2S, PS) and 1.0V (PS) for ROCs 2.5V for VTRx+ 1.25V for LpGBT, VTRx
FE power per module	2.9 – 8.5W	5.4W (2S) and 7.8W (PS)
Number of modules	17 888	13 296
Total front-end power	70kW (with TID effects)	85kW

ATLAS



CMS



LpGBT = Low-power GBT = serializer chip
VTRx+ = versatile transceiver = opto-electrical converter

bPOL12V and bPOL2V5

	Name	Type	Vin max	Technology	Radiation specs	Package
Stage1	FEAST2	DCDC buck	12V	350nm CMOS with High Voltage extension at 80V	150Mrad 5e14 n/cm² SEE "immune"	QFN32
	bPOL12V	DCDC buck	10-12V (TBD)	350nm CMOS with High Voltage extension at 25V	150Mrad 2e15 n/cm² SEE "immune"	QFN32
Stage2	bPOL2V5	DCDC buck	2.5V	130nm CMOS		Naked chip with balls for bump bonding
	rPOL2V5	DCDC resonant	2.5V	130nm CMOS		Naked chip with balls for bump bonding
Linear	linPOL12V	Linear regulator	12V	350nm CMOS with High Voltage extension at 25V		DFN8

bPOL12V

- First prototypes made
  - To be fixed: drift of protection features with TID

bPOL2V5

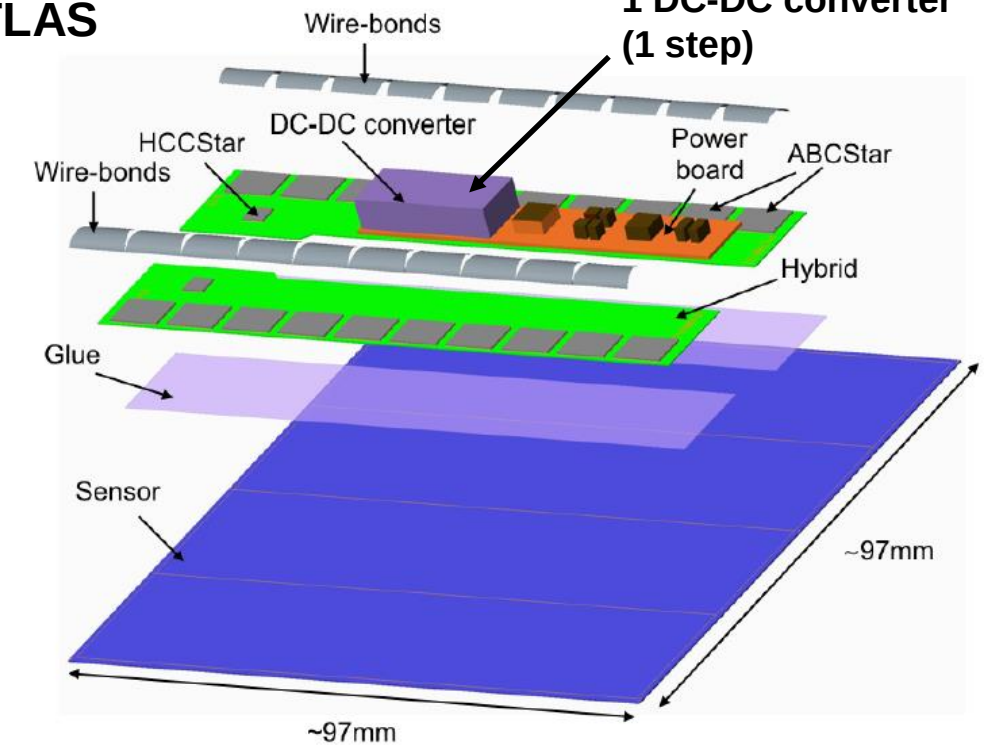
- First prototypes made and 2.5V version available to users
  - Working on a version with 3.3V rated transistors → more margin (but radiation hardness to be tested)

Pre-production chips in Q3 2019

Powering Implementation on Module Level

ATLAS

1 DC-DC converter (1 step)



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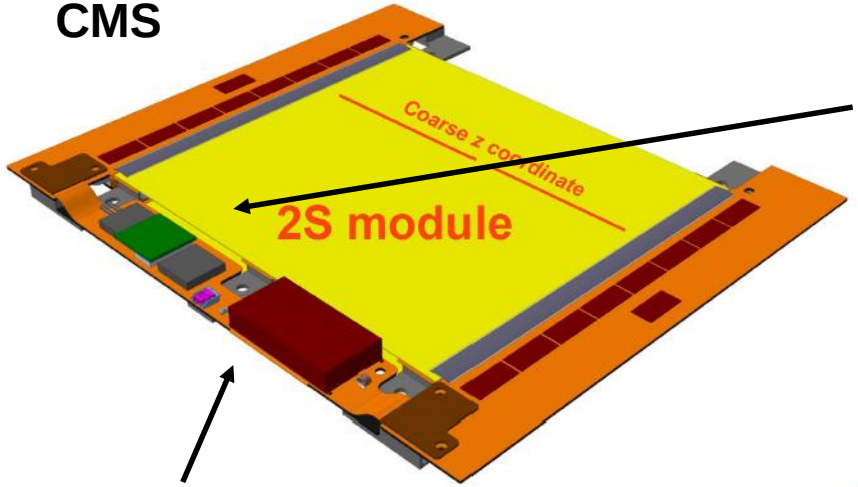
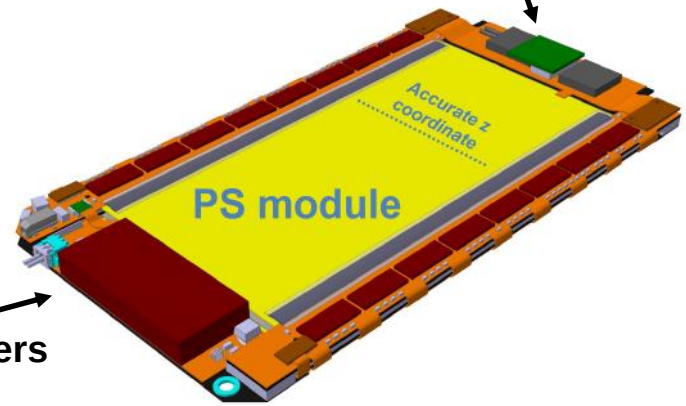


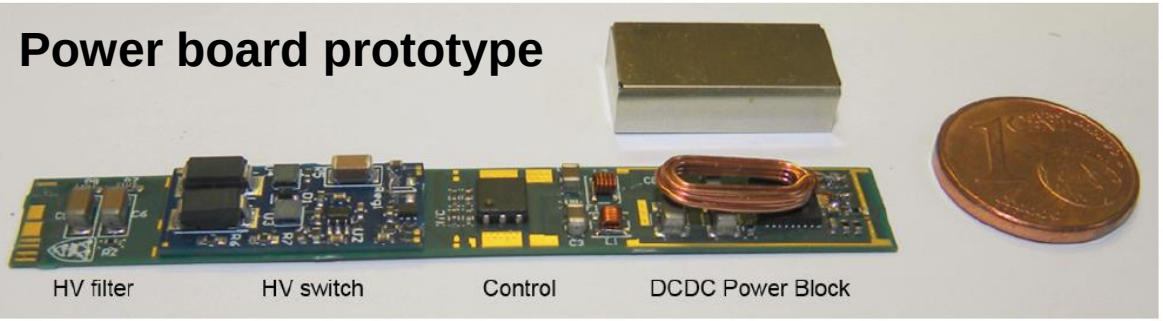
On each module:
1 x LpGBT
1 x VTRx+

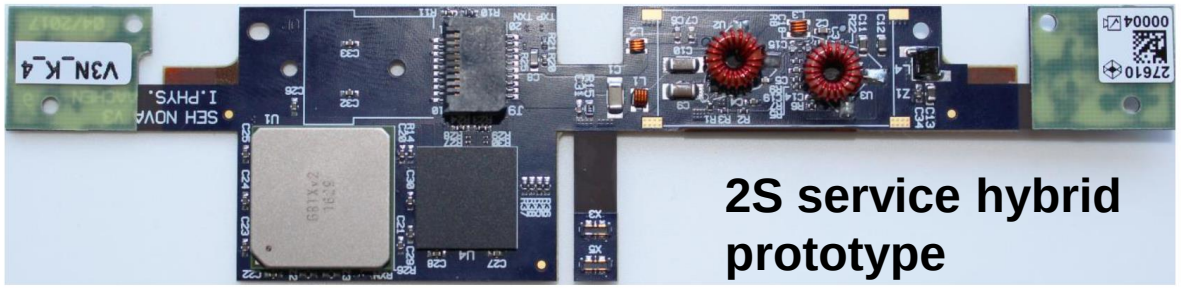
2 DC-DC converters (2 steps)



3 DC-DC converters (2 steps)

Power board prototype

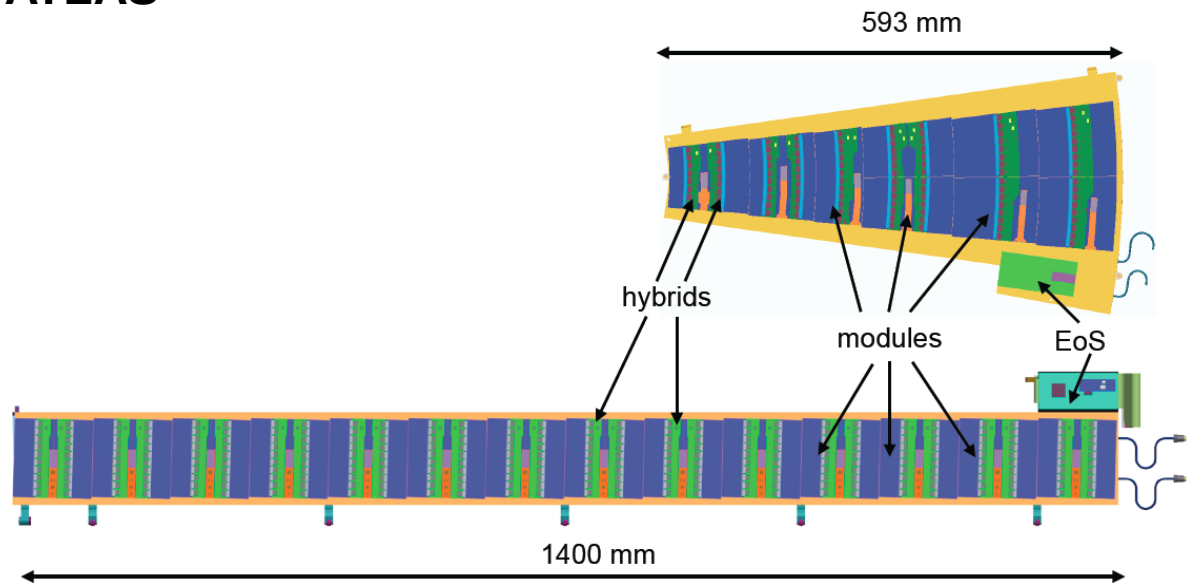




2S service hybrid prototype

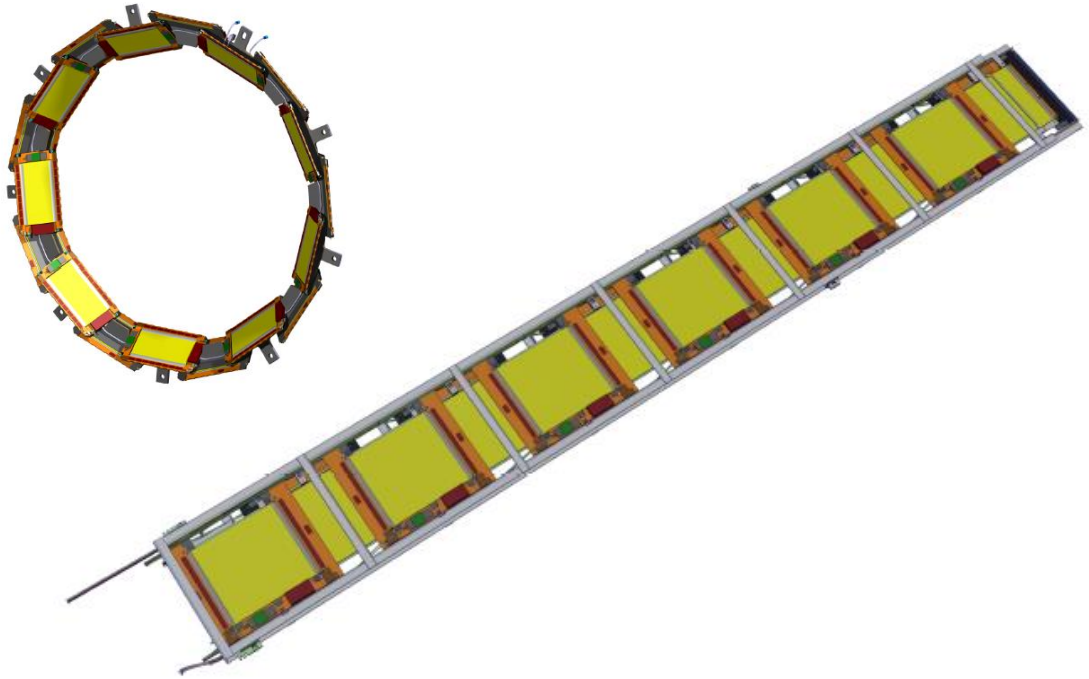
Powering Implementation on Substructure Level

ATLAS



- Two End-of-Substructure cards per stave/petal
- Each carries up to 2 LpGBT + 1 VTRx+
- 2 DC-DC converters on “master“ card (2 steps; 2.5V, 1.2V)
- Power & data channeled through EoS card
- Power and data distributed via copper bus-tapes, co-cured to mechanics, wire-bonded to modules + EoS card
- One power connector + up to 6 fibres per stave/petal

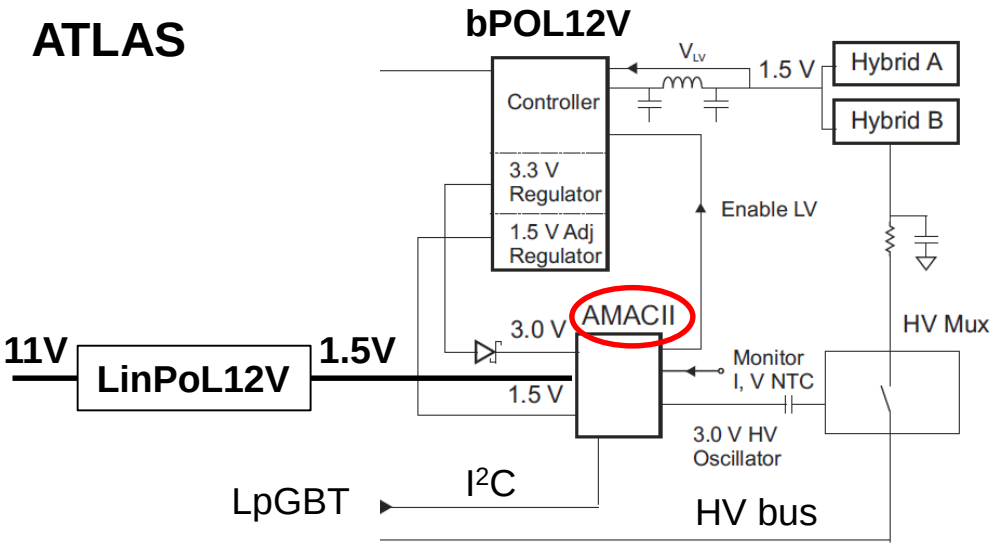
CMS



- No end-of-substructure cards at all!
- Each module carries its own LpGBT + VTRx+
- No single point of failure
- Each module connects to back-end via 3 wires (GND, LV, HV) and 2 optical fibres

Monitoring and Control of DC-DC Converters

ATLAS



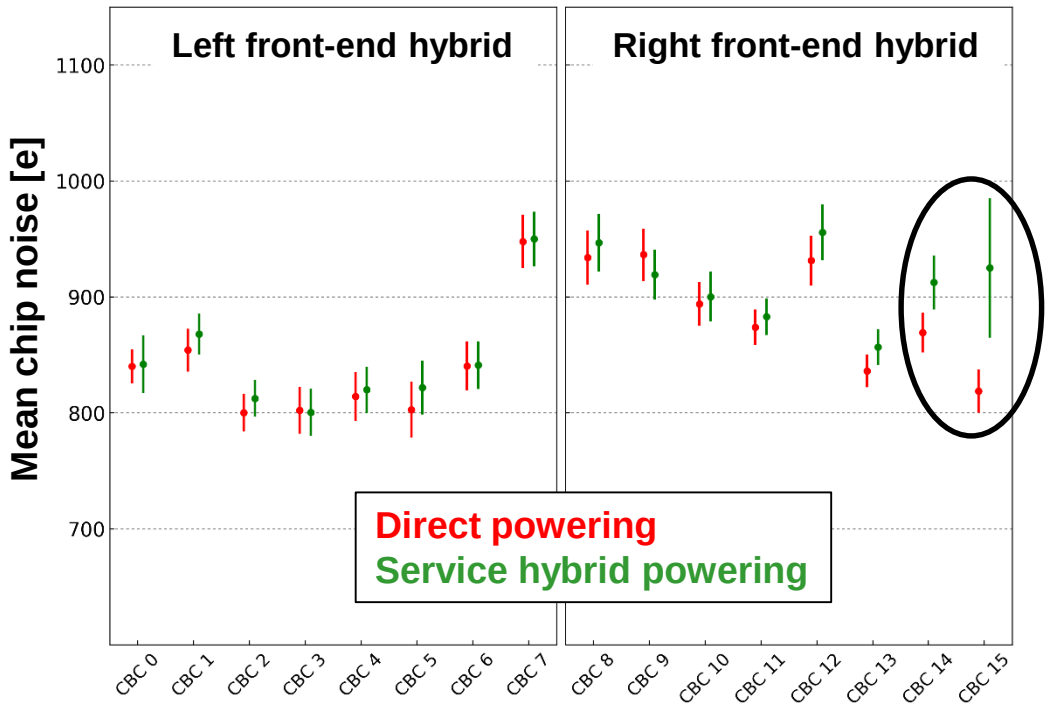
- **Via AMAC chip on power board**
- **Powered up from linear regulator chip, then from DC-DC**
- **Monitoring:**
  - Input & output voltages and currents
  - DC-DC converter‘s temperature
  - Power good signal
- **Controls:**
  - Performs start-up sequence: enables DC-DC converters, when conditions are fine (T), then the other chips
  - Sends warnings, acts as interlock

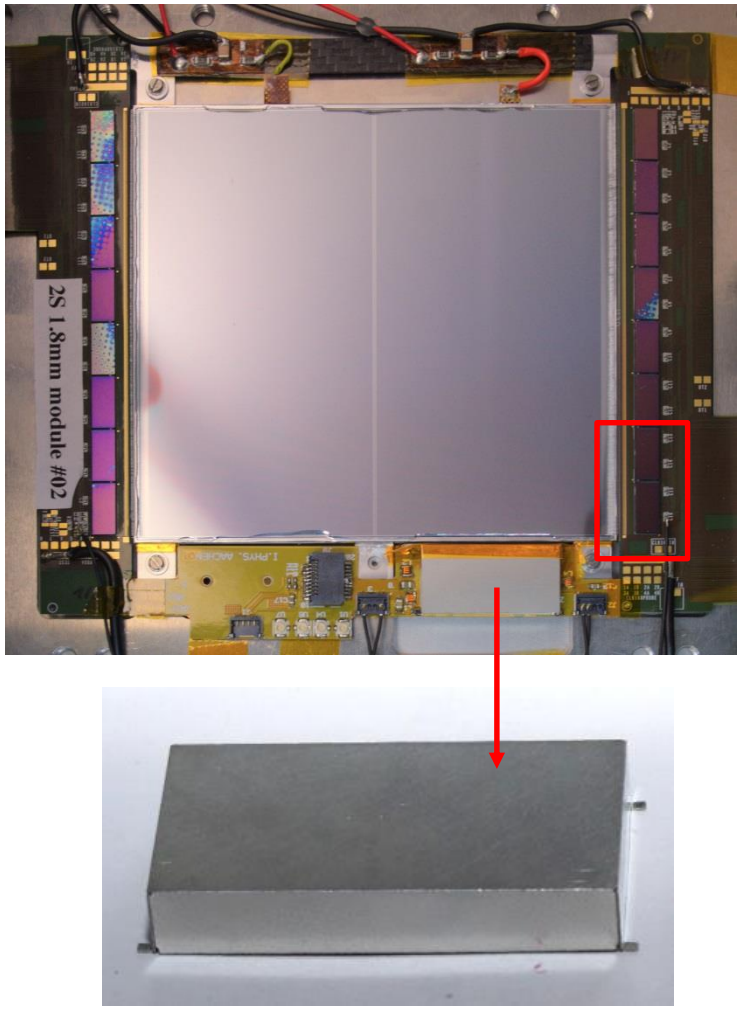
CMS

- **Monitoring via slow control circuit in LpGBT :**
  - Input voltage
  - Output voltages
  - Power good signals (combined signal for PS)
- **Controls:**
  - None – enabling feature not used, as LpGBT powered from DC-DCs and additional wires to be avoided

CMS Prototyping and System Tests

- Several 2S service hybrid prototypes made, all still with FEAST2 and commercial DC-DC converter in 2nd stage
- 2S module prototype powered via DC-DC converters or by direct powering
  - Readout not via service hybrid
- Noise in specs (< 1000e) for all chips
- However, noise slightly increased in two CBCs closest to SEH
- Problem seems related to insufficient ground connection of shield, to be studied





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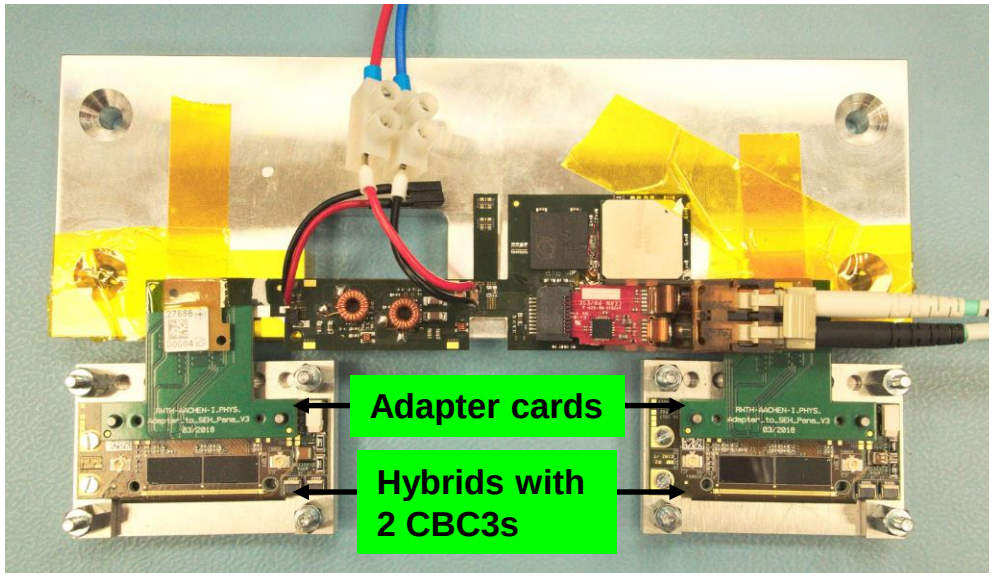
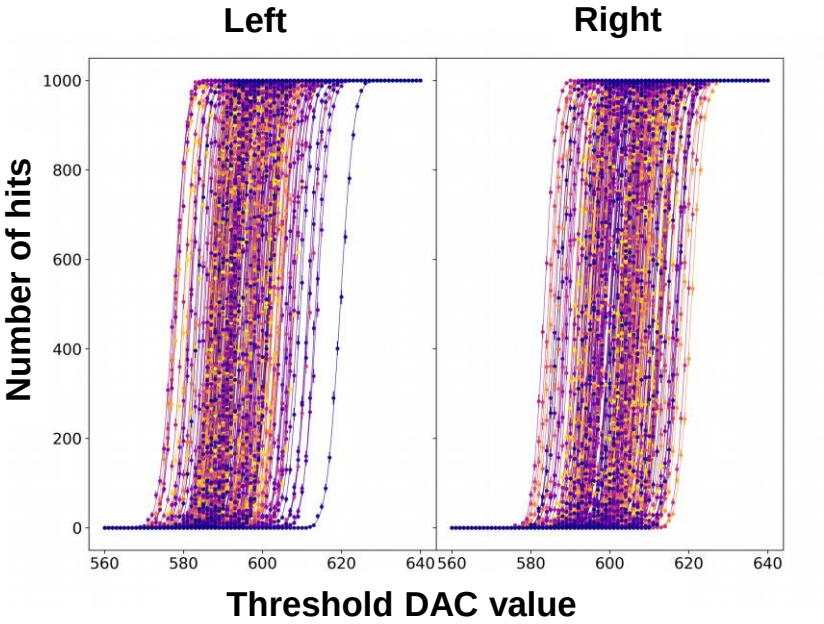
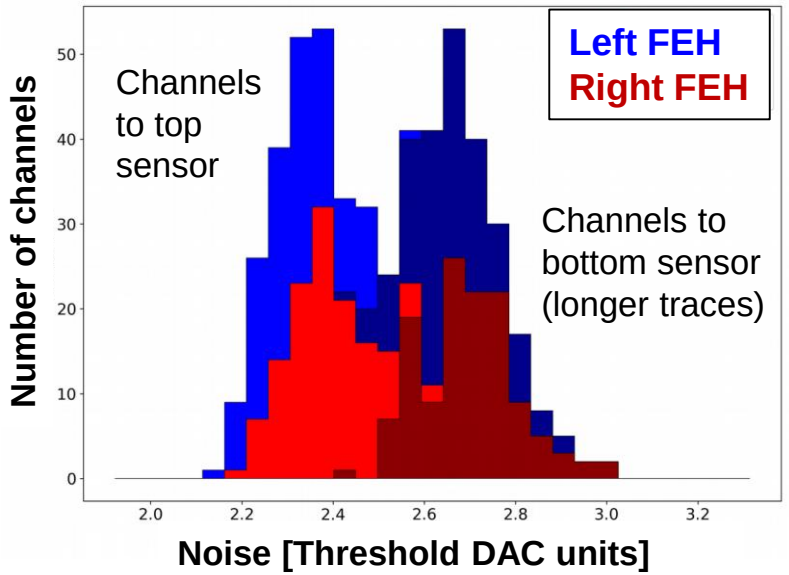
CMS Prototyping and System Tests

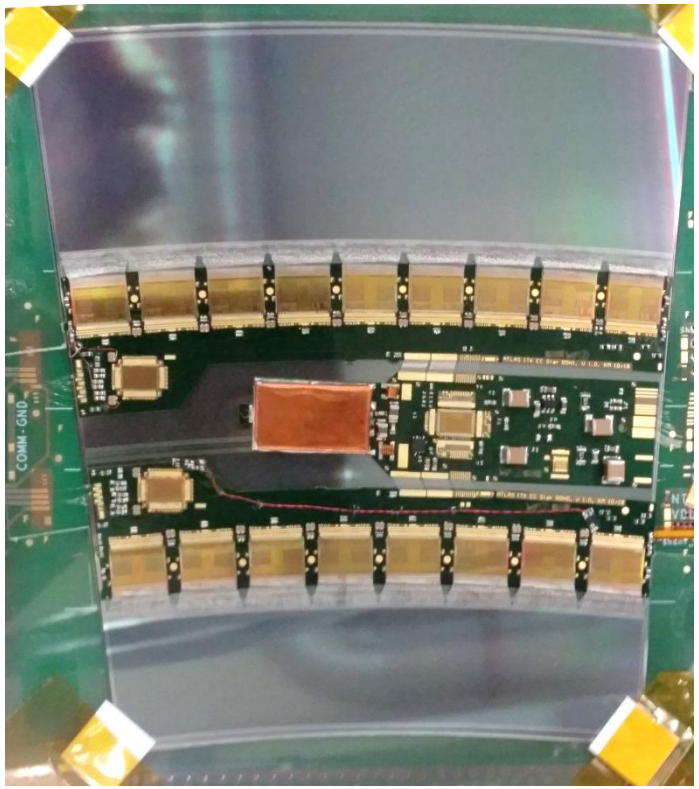
- Most advanced test so far: hybrids with 2 CBC3 readout chips powered and read out via service hybrid
- Readout of data of 1 CBC per side at 320Mb/s via GBTx and VTRx
- GBTx and VTRx also powered via DC-DC converters
- Noise is compatible with direct electrical readout via standard test board
- Tests with full modules this year





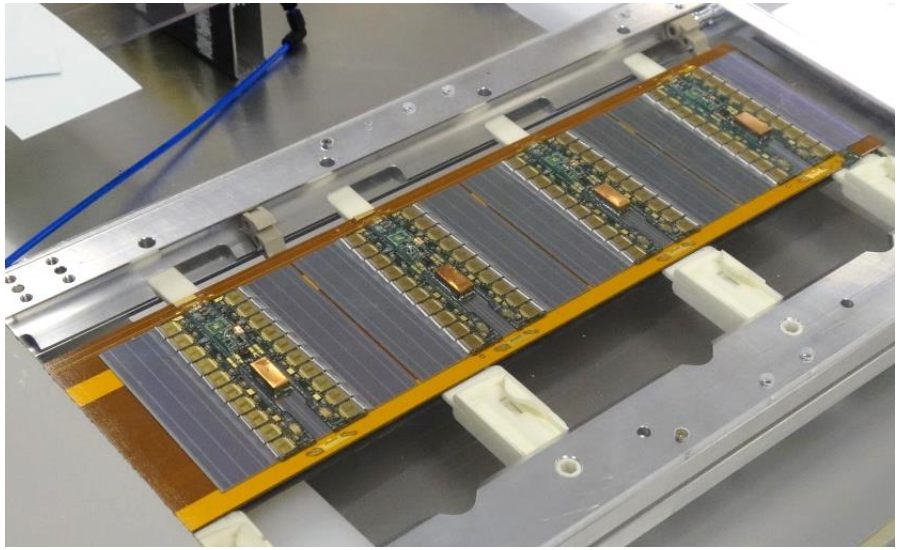


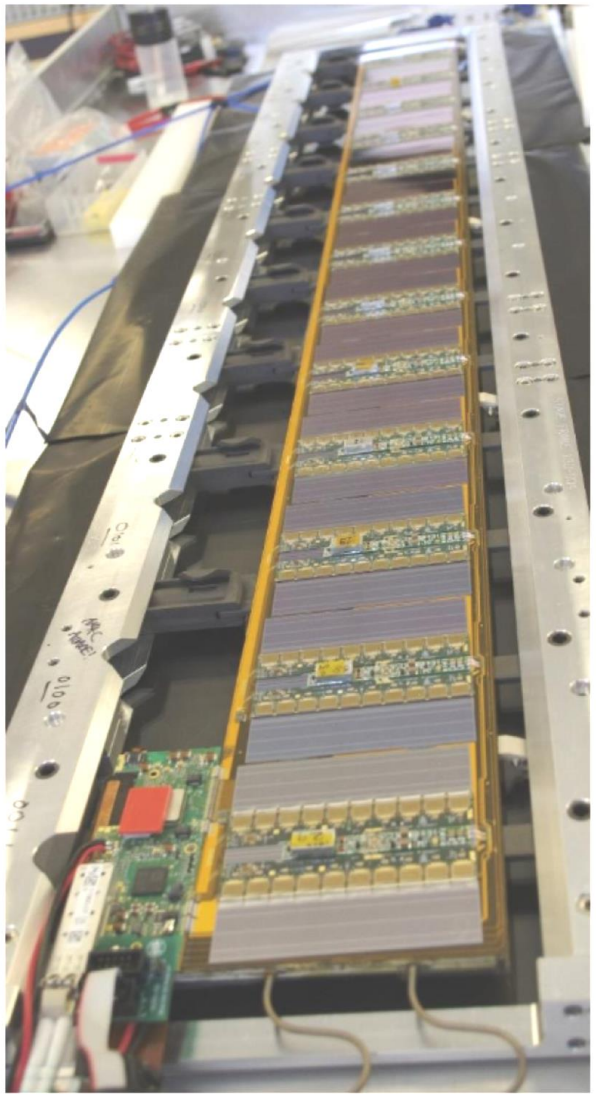
ATLAS Prototyping and System Tests



Freiburg University

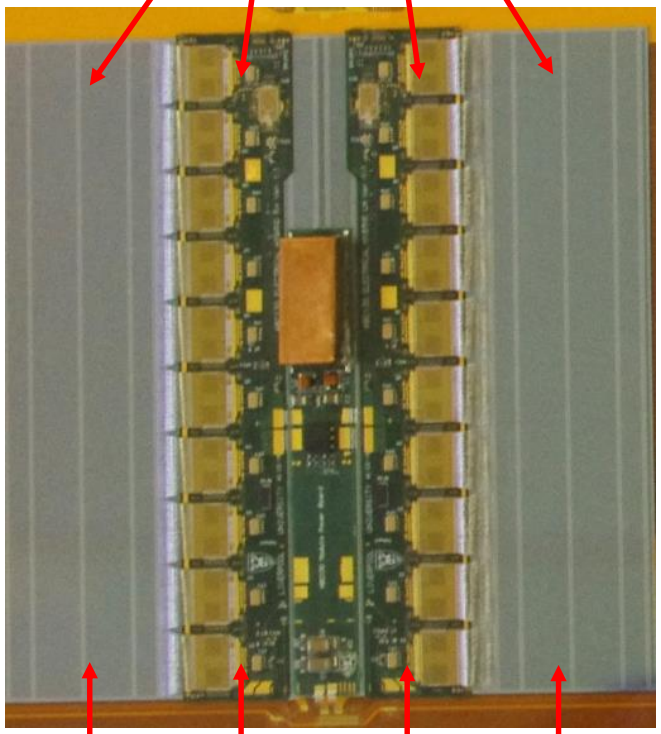
- Barrel short strip modules and endcap Ring 0 modules equipped with power boards
- Several power board variants (barrel + 6 geometries in endcap)
- Still FEAST2 used in prototypes





ATLAS Prototyping and System Tests

Short strip module: 4 rows of strips

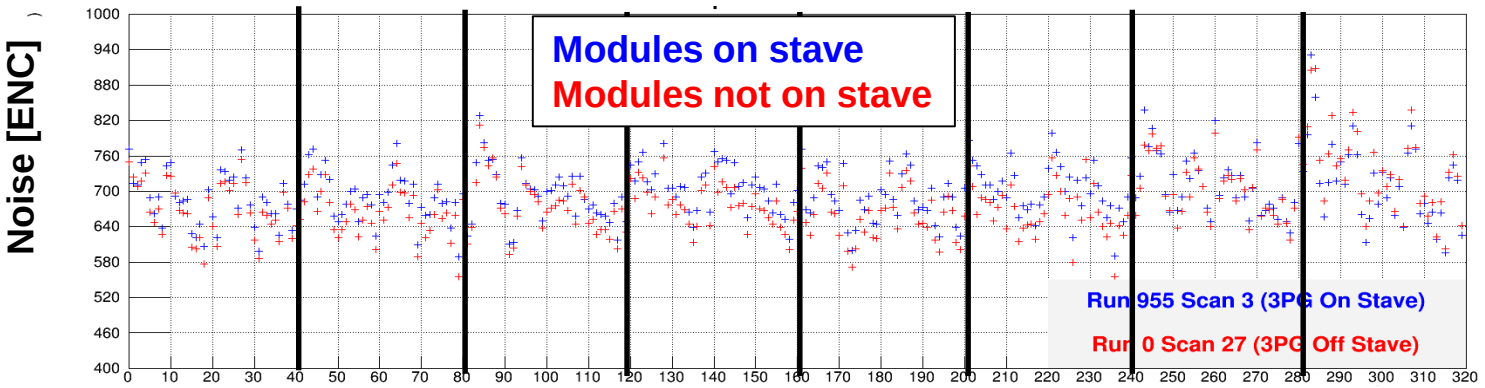


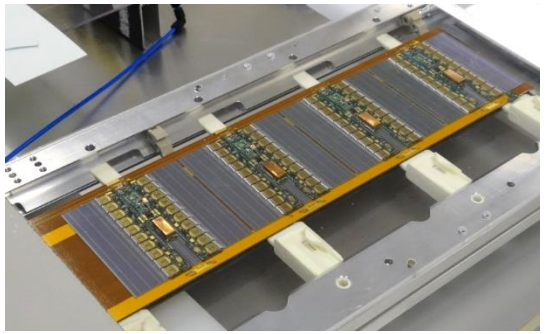
Average noise of 8 modules

676e 721e 706e 665e

- In general, noise slightly (~5%) increased on strip rows below hybrids
- Attributed to increased capacitance due to adjacent gound planes

Noise of 8 modules on stave, each with 10 ABC chips, 4 rows of strips

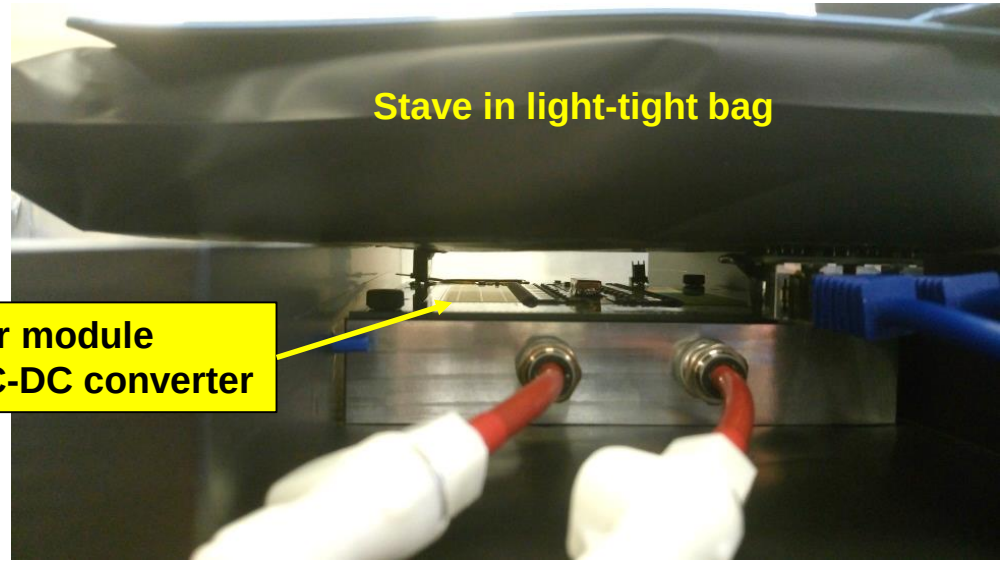




- Noise measurements on a short strip stave prototype
- Module noise on-stave is only ~15e higher than off-stave
- Very uniform, very reproducible

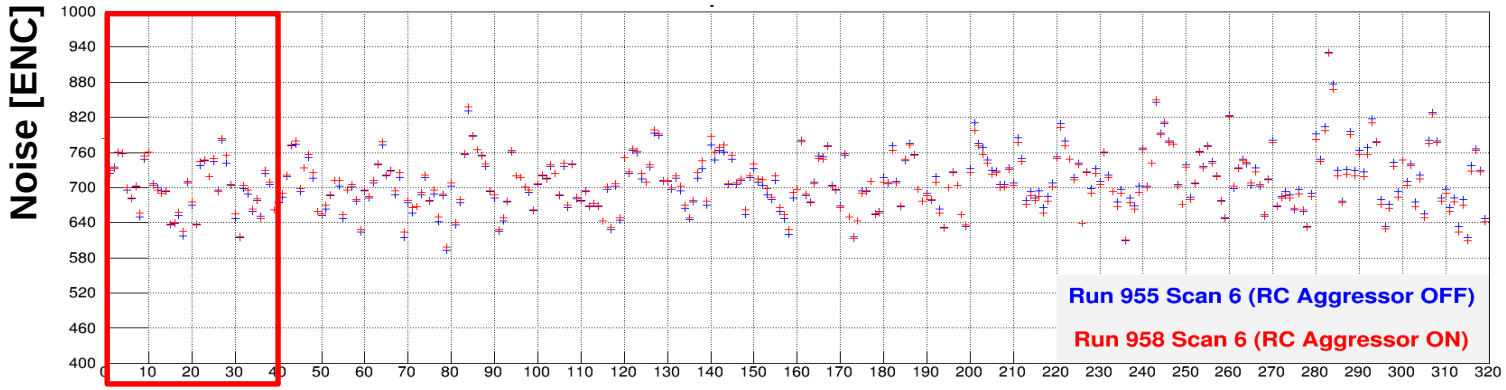
ATLAS Prototyping and System Tests

- "Aggressor study": simulate overlap between staves by placing another module below stave
- Effect on closest stave module insignificant (13e)



Plots taken from talk at TWEPP2017
by Peter Phillips.
Thanks to **Dennis Sperlich** and
Mitch Newcomer for providing information
and for answering questions!

Noise of 8 modules on stave, each with 10 ABC chips, 4 rows of strips



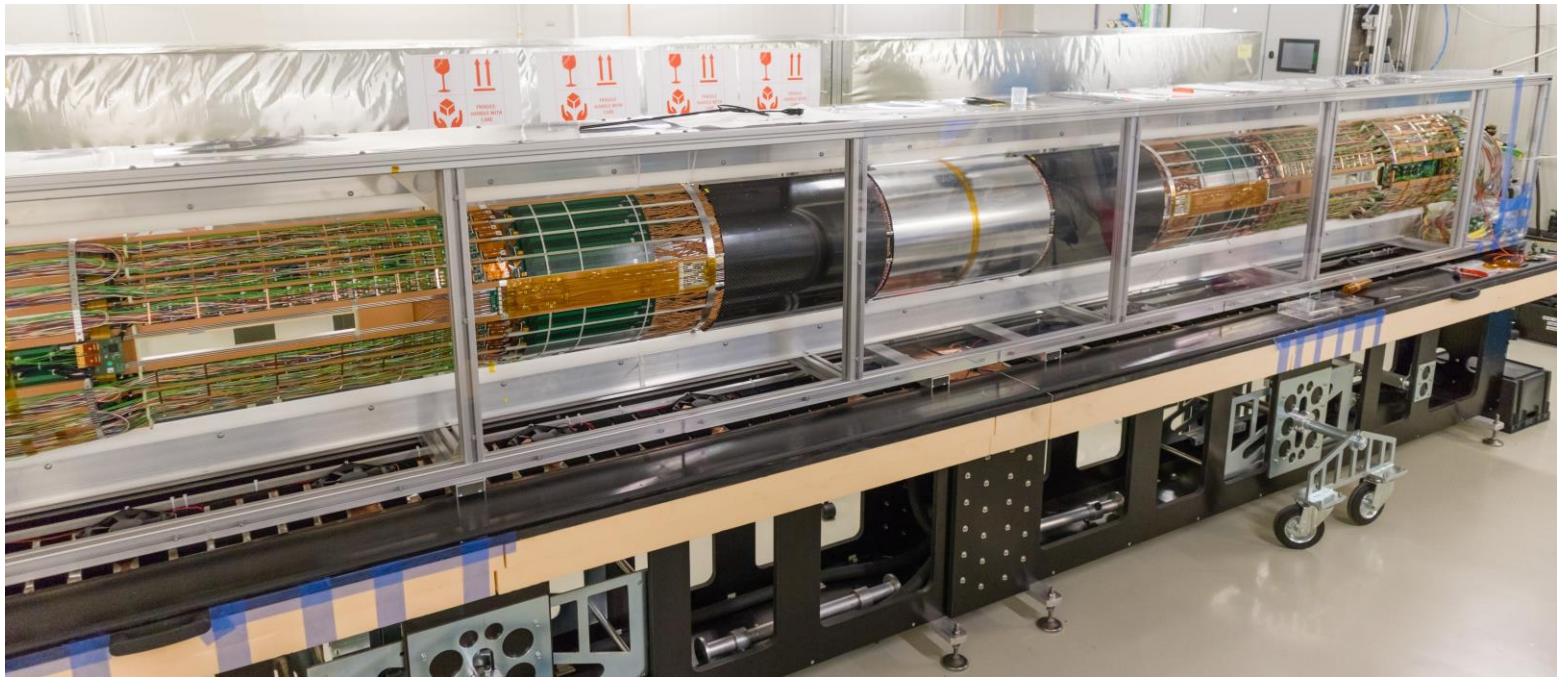
Without aggressor
With aggressor

Conclusions

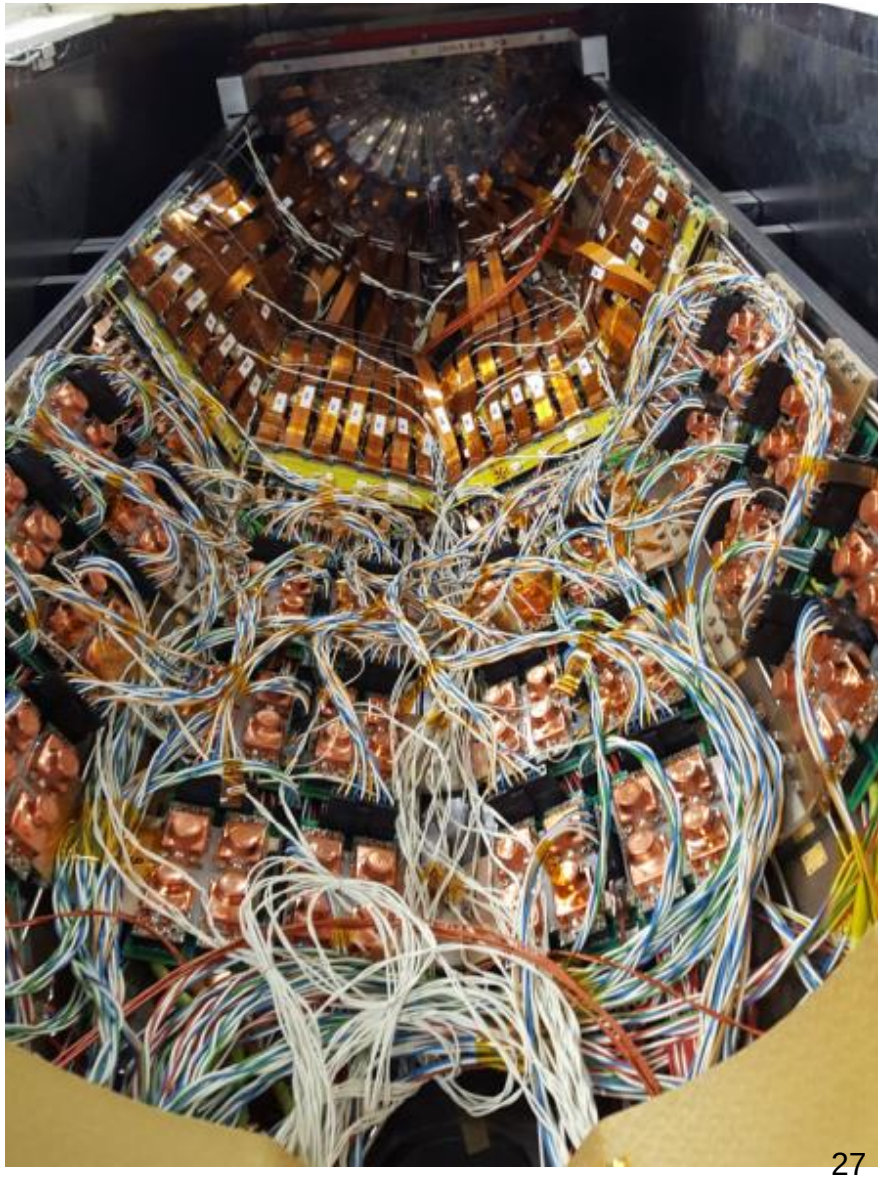
- DC-DC conversion powering is (will be) widely used
- CERN is single supplier of radiation-tolerant DC-DC ASICs
  - Problem with FEAST2 ASIC identified and solved
- DC-DC conversion powering system in CMS Phase-1 pixel detector works very well
- Phase-2 tracker implementations much more complex (in particular, no access possible)
  → still a lot of prototyping and system-testing to be done

Additional Material

How it looks in the Detector



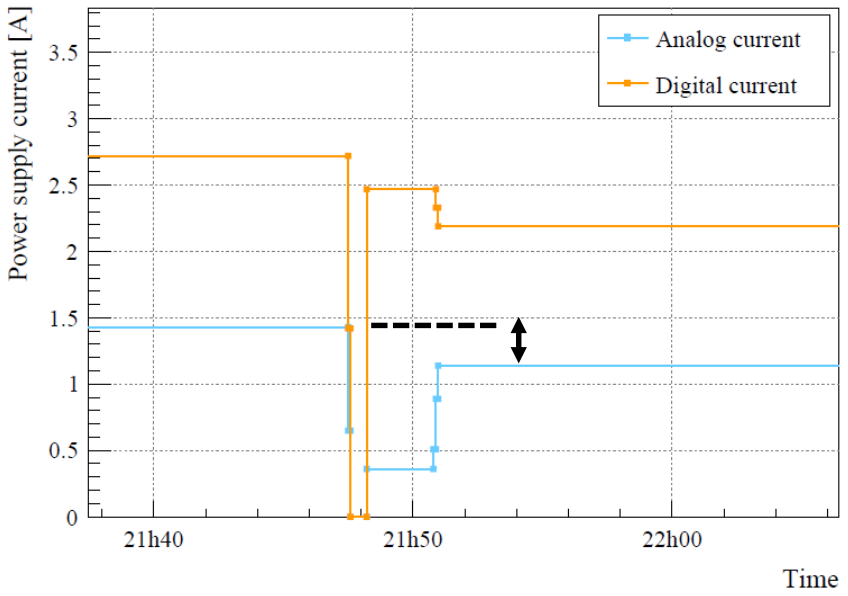
BPIX



FPIX

Failures

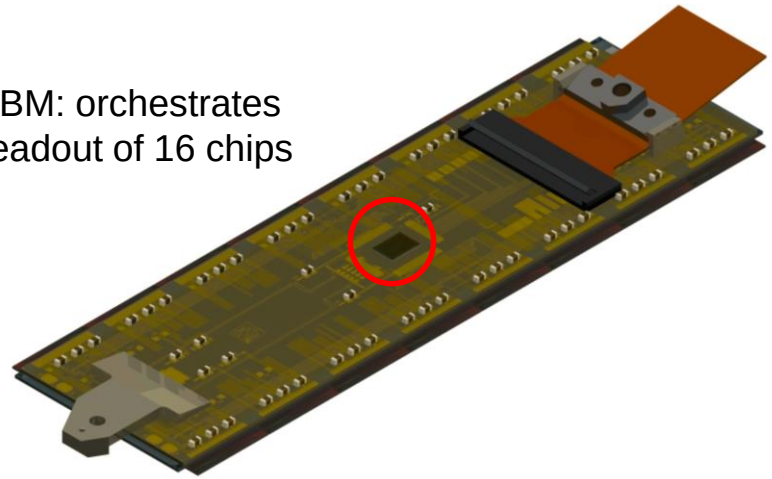
Power supply current in DCS for several pairs of DC-DC converters

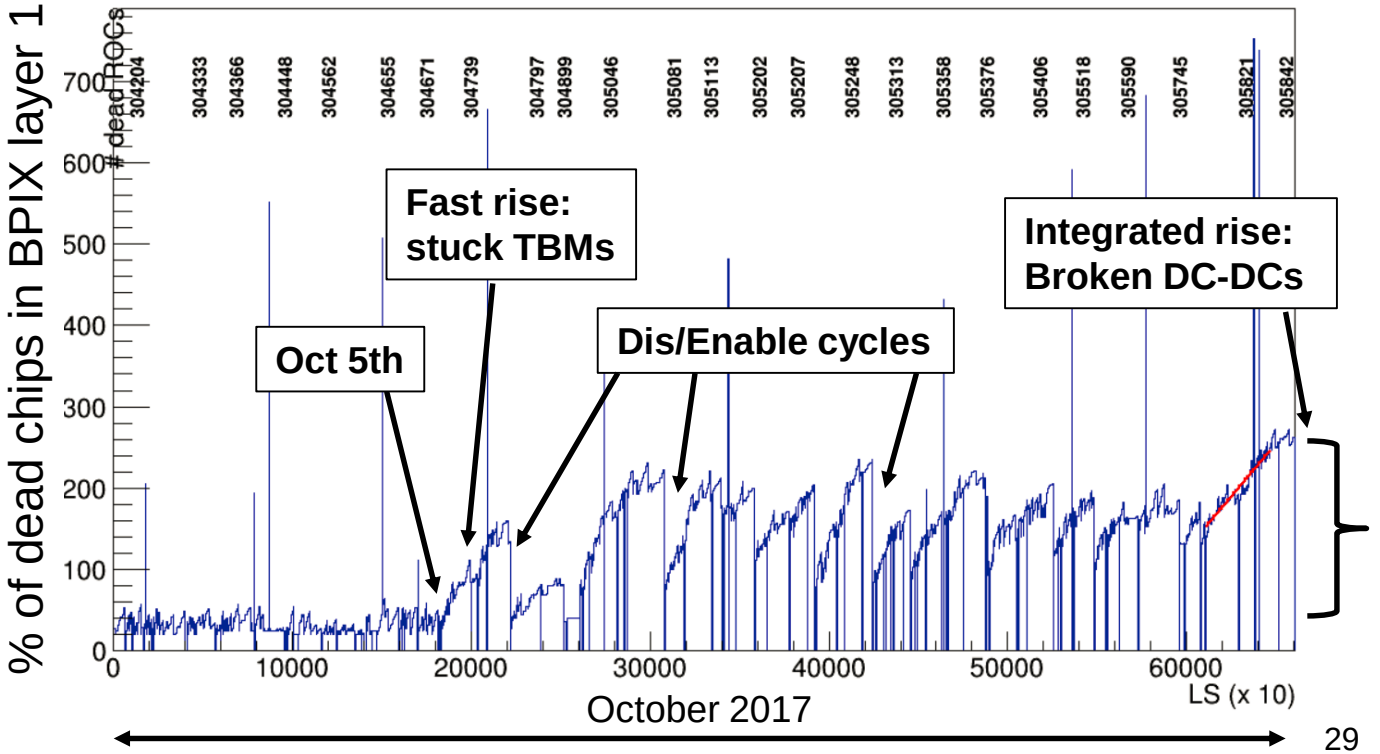


The Dilemma

- Pixel chips (readout chips and Token Bit Manager) suffer from SEUs
- Most can be recovered by resets / reprogramming
- However, TBM can get into a stuck state → needs power cycling
- Dis/enabling of DC-DC converters during fill (ab)used for this
- Layer 1 needed to be power-cycled every 1-2 fills, to keep number of inactive channels < 10%
  - Other layers & disks ~ once per week

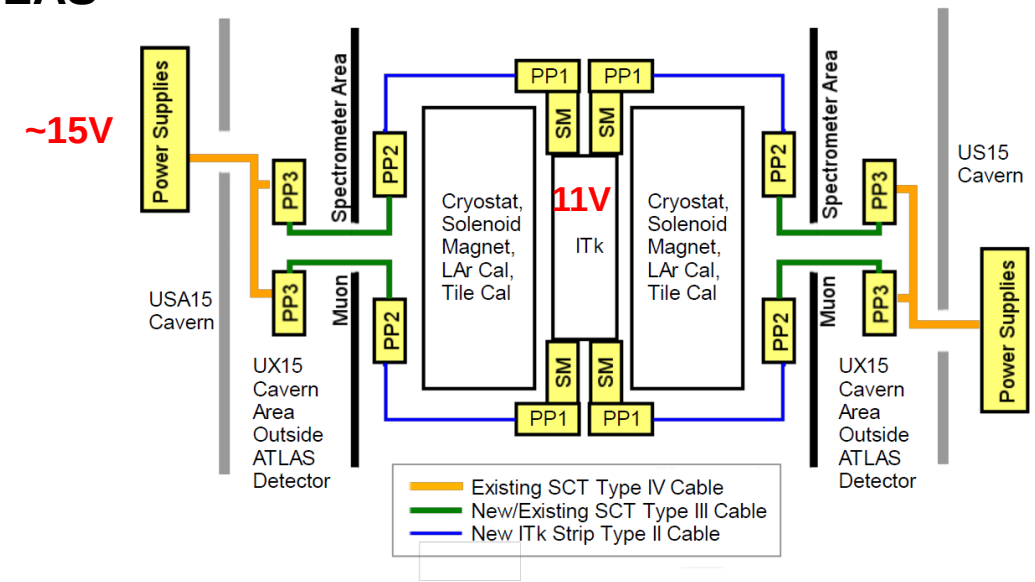
TBM: orchestrates readout of 16 chips





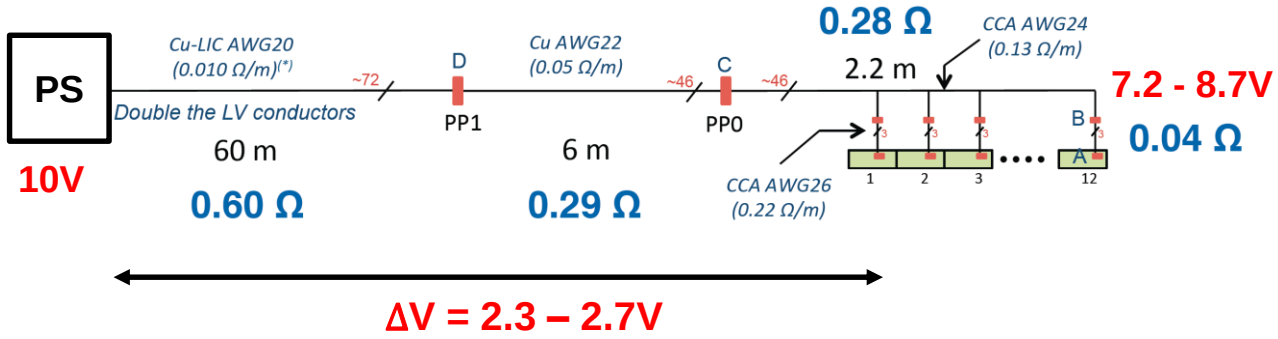
Back-end Implementation

ATLAS



- One stave / 1 side of a petal connected to 1 PS
- Voltage drops of up to 4V
- DC-DC input voltage limit (14V) can be exceeded if no load
  1) Sensing in combination with a voltage limiter in PP2
  2) Additional, magnetic-field & rad-tolerant DC-DC converters that receive 48V, and sense V at FE
     a) in PP3 – may be commercial, with shielding
     b) in PP2 – need air-core, plus cooling

CMS



- O(12) modules connected to 1 PS
- PSs are in the cavern
- Voltage drops of up to 3V
- Do no want extra wires → no sensing!
- Simply accept that DC-DC input voltage is < 10V

- Common price enquiry for power supplies ongoing, organized by CERN