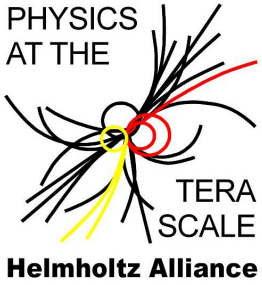

12th Terascale Detector Workshop, 12.-15.03.2019
TU Dresden

FPGAs for Trigger & Data Processing in ATLAS

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Overview

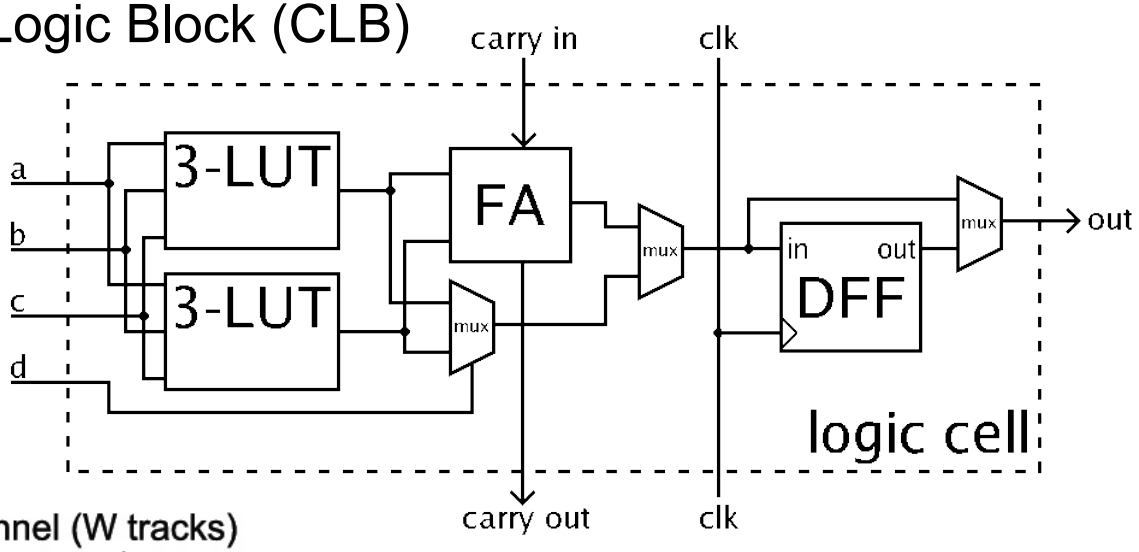
- Short Introduction to FPGAs
- The ATLAS Experiment & its trigger/readout scheme
- FPGA usage in ATLAS:
  - Trigger decision finding (FTK, L1Calo)
  - Trigger distribution (LTI)
  - FELIX readout system
  - RCE readout system
- Summary

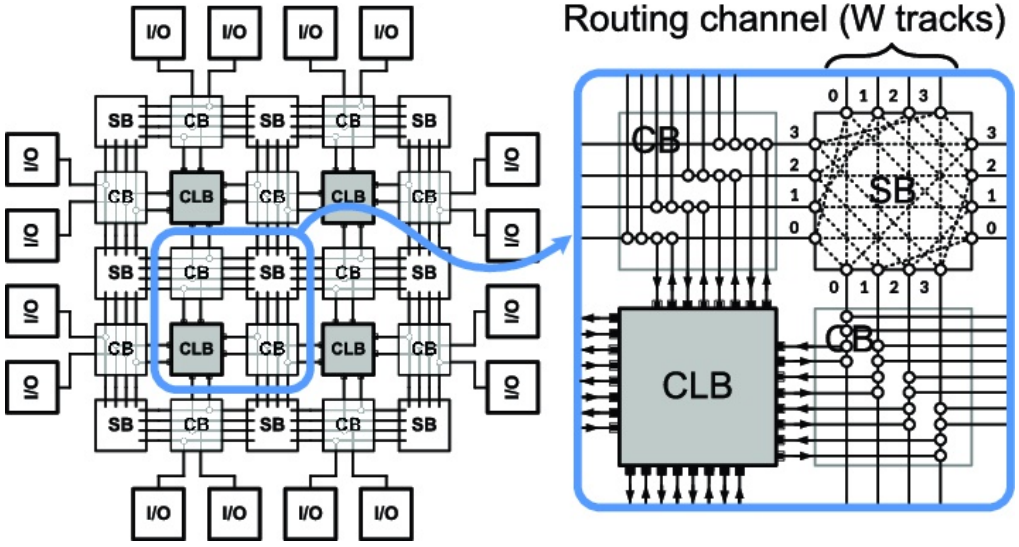
Disclaimer:
This talk is far from being a complete overview of FPGA usage in ATLAS. There will be many more places where FPGAs are used than presented in the following slides.

Introduction

Short Introduction to FPGAs

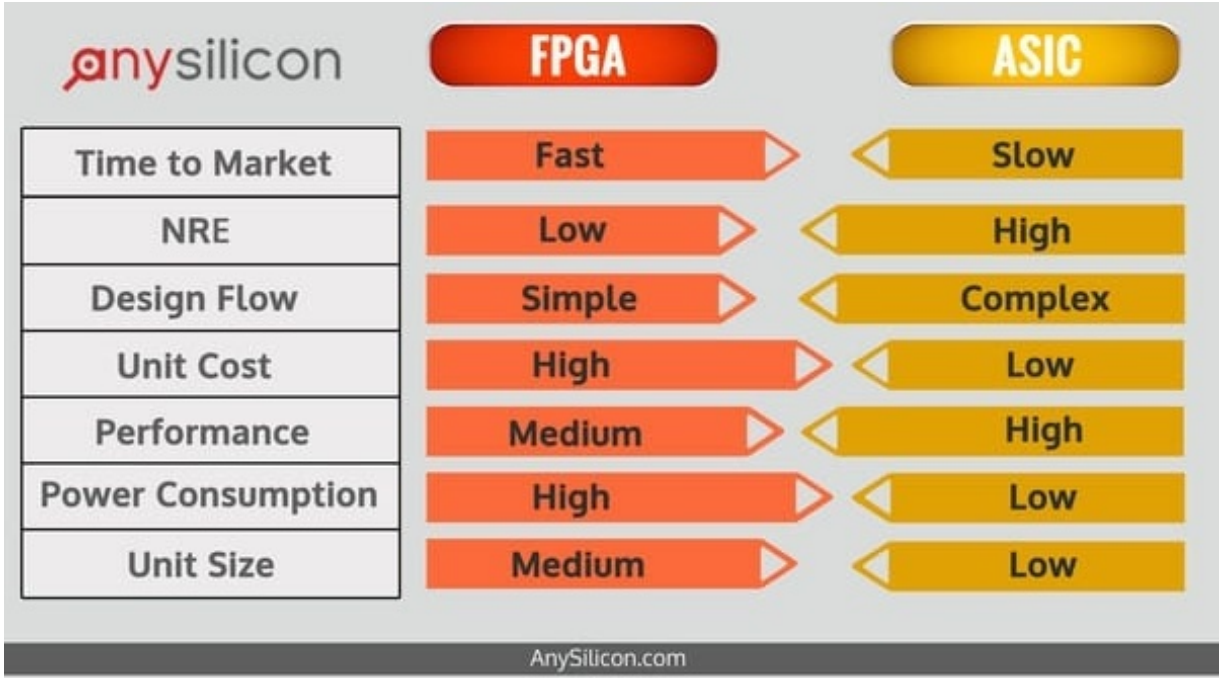
- FPGA: **F**ield **P**rogrammable **G**ate **A**rray
- Central part: Configurable Logic Block (CLB)
  - LUTs for logic
  - Flipflops for storage
- Interconnect:
  - Configurable switching matrix between CLBs





- additional FPGA resources:
  - memory (block RAM)
  - I/O cells
  - high-speed serial transceivers (multi-gigabit)
  - clocking system (PLLs)

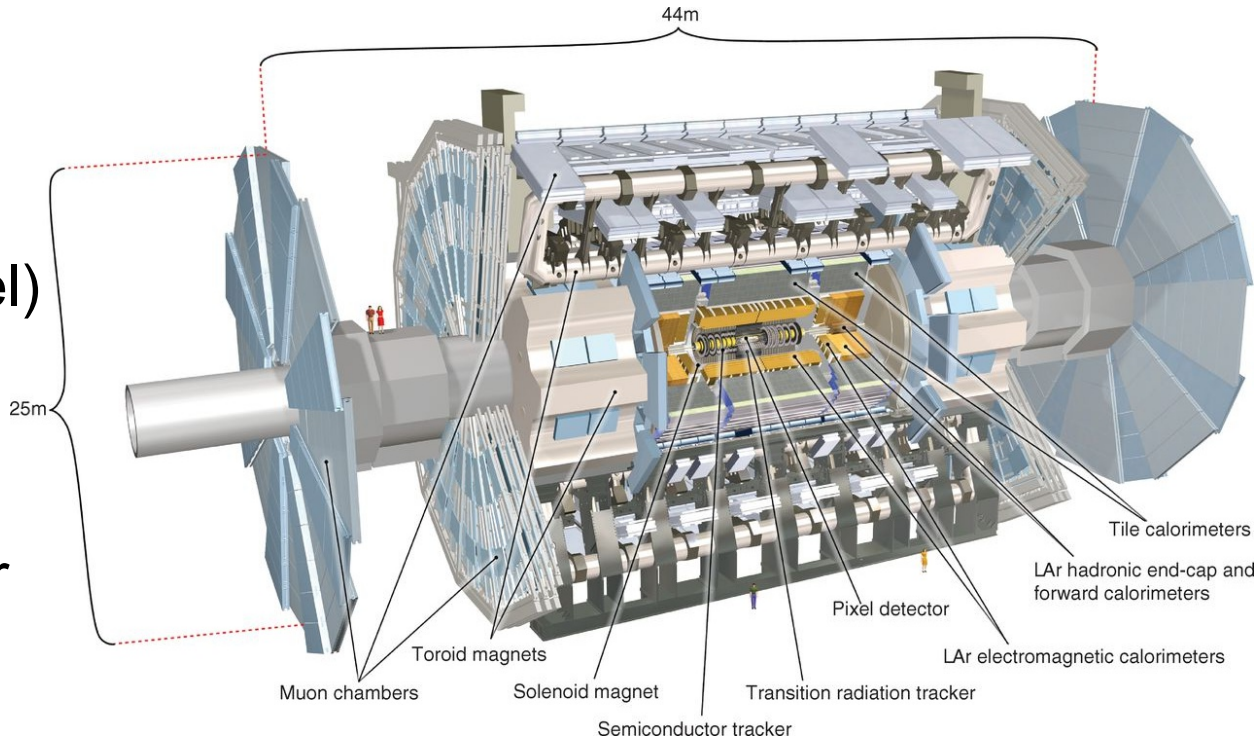
FPGAs vs. (digital) ASIC



- FPGAs are flexible and the logic can be upgraded.
- Additional differences for HEP applications:
  - FPGAs are usually NOT radiation hard (see next talk), ASICs can be built radiation hard
  - FPGAs are good in digital circuits, while ASICs can be integrated with digital and analog circuits together

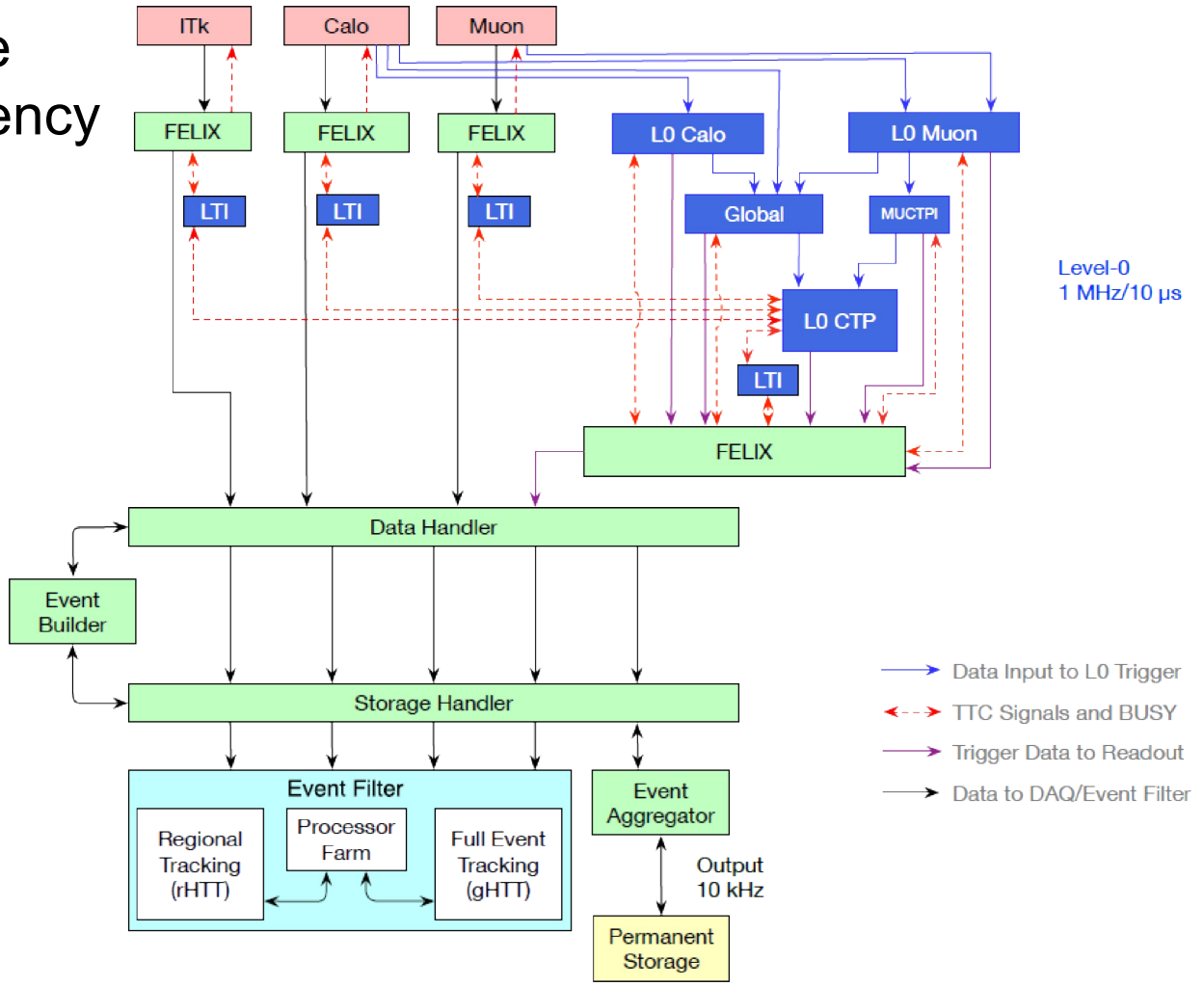
The ATLAS Experiment

- ATLAS is one of the four experiments at the LHC.
- General-purpose particle detector:
  - Tracking detector
  - Calorimeters
  - Muon system
- Phase-I upgrade:
  - Muon system (New Small Wheel)
  - Calorimeters (LAr)
- Phase-II upgrade:
  - new Inner Tracker (ITk)
  - new trigger system



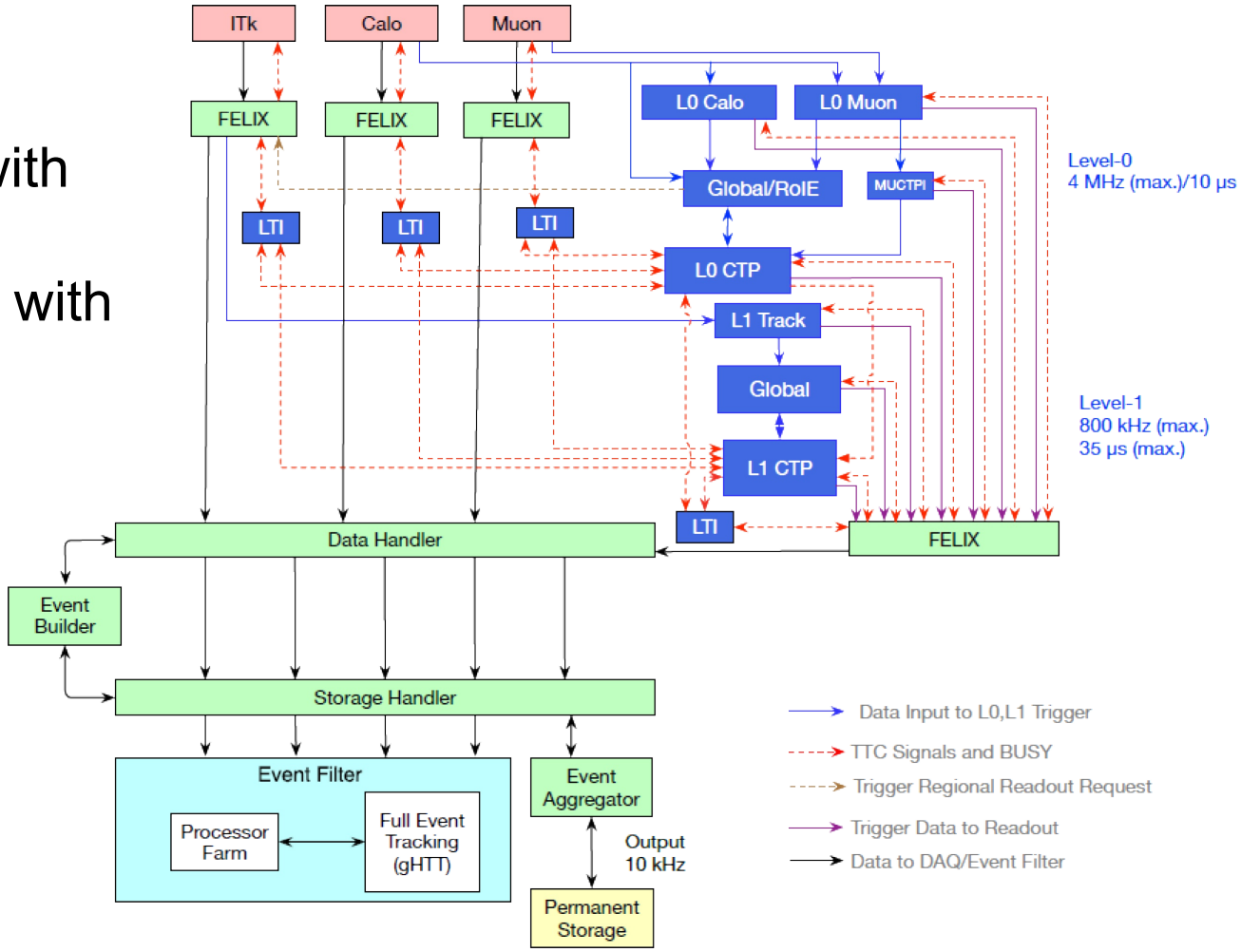
The ATLAS Trigger & Readout Chain (Phase-II)

- Single level system:
  - 1 MHz trigger rate
  - 10 µs allowed latency
- Main inputs for trigger decision:
  - Calorimeters
  - Muon system
- FELIX:
  - First stage readout system
  - Converter from front-end data to commercial Ethernet



The ATLAS Trigger & Readout Chain (Phase-II)

- Also 2-level trigger system may be implemented:
  - L0 rate 4 MHz with 10 µs latency
  - L1 rate 800 kHz with 35 µs latency
- Major difference:
  - Region of interest readout
  - Hardware track trigger as input to L1 trigger decision



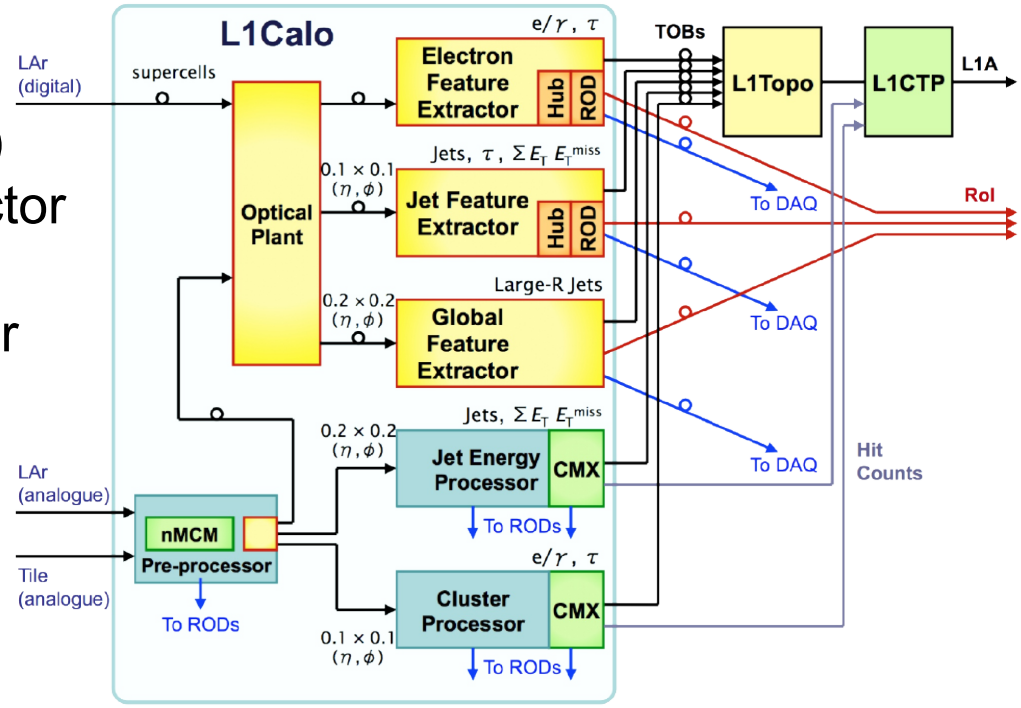
FPGAs in the ATLAS trigger systems

FPGAs in the trigger system

- FPGAs in the trigger system are used in three large areas:
  - Trigger decision finding in the data from calorimeters and muon systems.
  - Hardware track trigger systems (Fast TracKer, FTK)
  - Trigger distribution from Central Trigger (CTP) through Local Trigger interfaces (LTI) to the sub-detectors.
- Main reasons why FPGAs are used:
  - A digital circuit can be designed to have a very **fixed latency**, which is defined by the clock period and propagation times.
  - Trigger distribution system uses a **custom protocol** best suited to the needs of the ATLAS detector.
  - Trigger decision: **High number of events** (40 mio. events/sec.) have to be processed to come to a trigger decision.

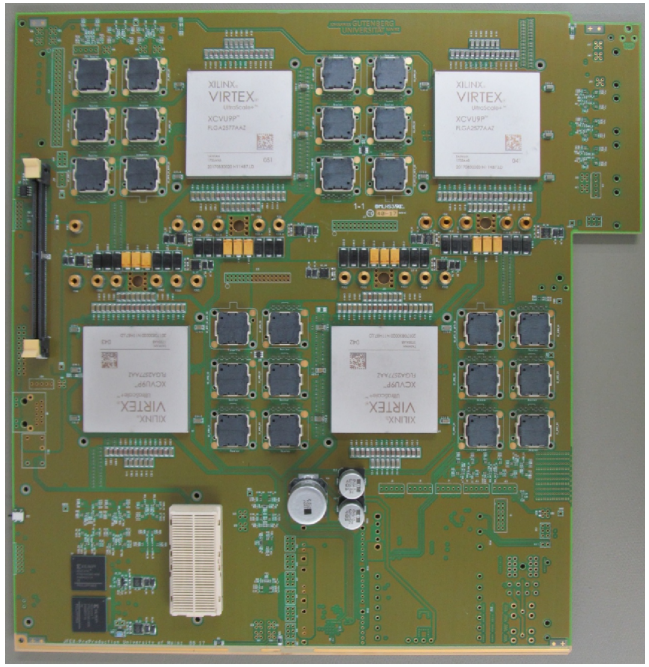
L1Calo trigger upgrades for Phase-I: Overview

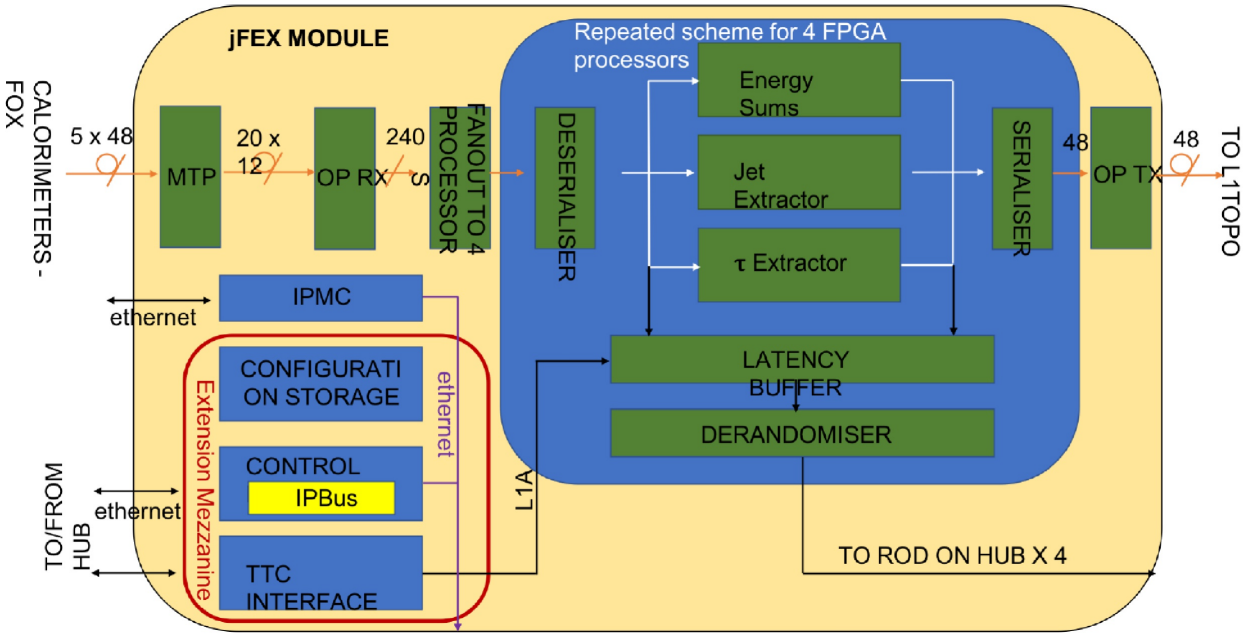
- ATLAS needs a fast trigger system to filter specific event signatures.
- Calorimeter system is one of the main inputs to the ATLAS trigger logic.
  - Upgrade to the Phase-I system for Run3 (2021-2023)
  - eFEX: electron feature extractor
  - **jFEX**: jet feature extractor
  - gFEX: global feature extractor
  - **L1Topo**: topological trigger
- FPGAs are used for processing a high band-width data stream in a small amount of time (decision after **max. 2,5 µs**)



L1Calo trigger upgrades for Phase-I: jFEX

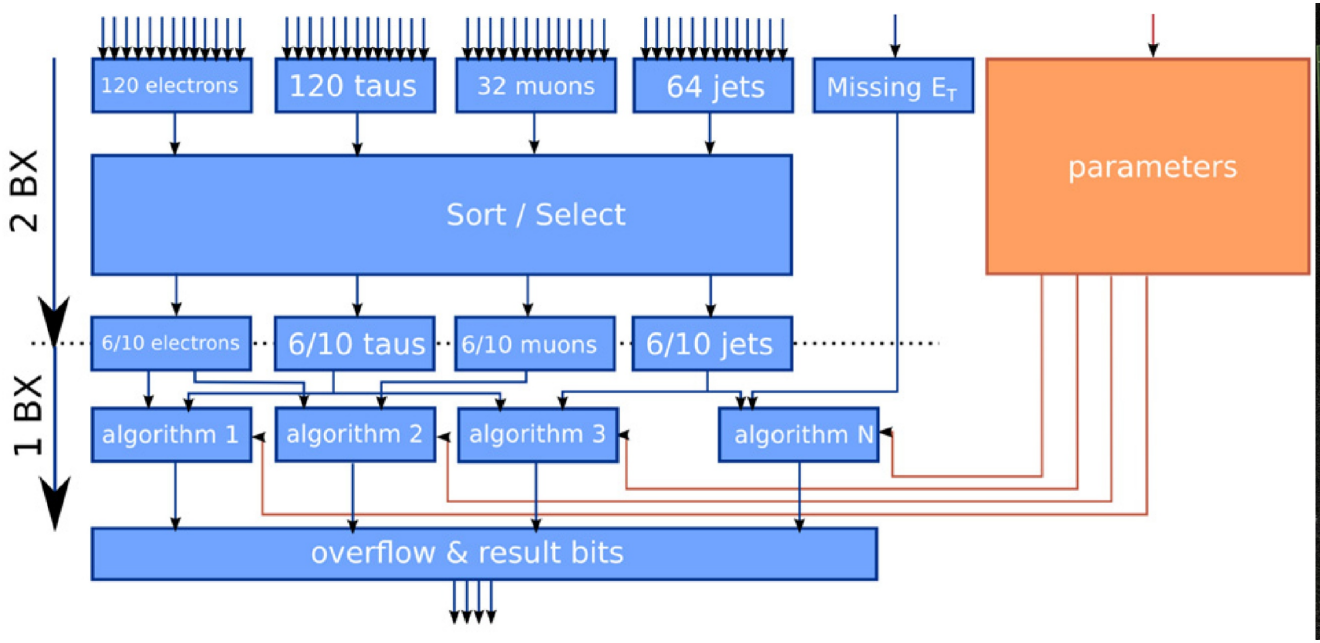
- Jet feature extractor (jFEX) is used to identify jet and tau candidates and calculates traverse energy sum + missing traverse energy (⇨ **important inputs to trigger system!**)
  - 4x Virtex Ultrascale+ VU9P per ATCA board
  - Input bandwidth: **3 Tb/s** with allowed latency: **400 ns**

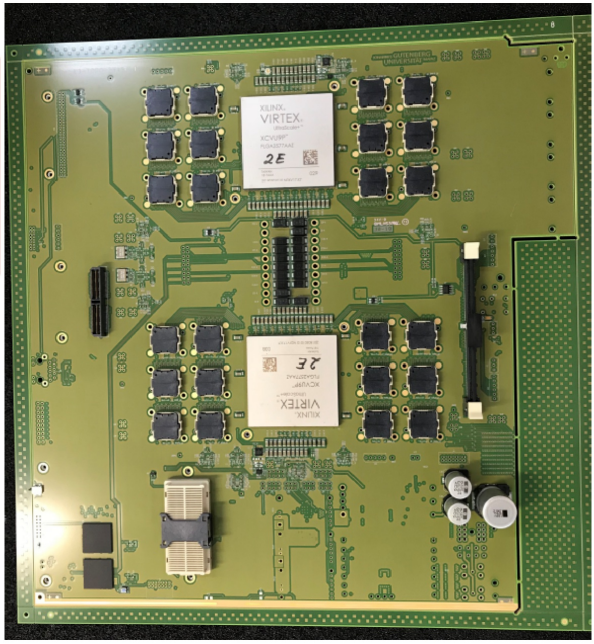




L1Calo trigger upgrades for Phase-I: L1Topo

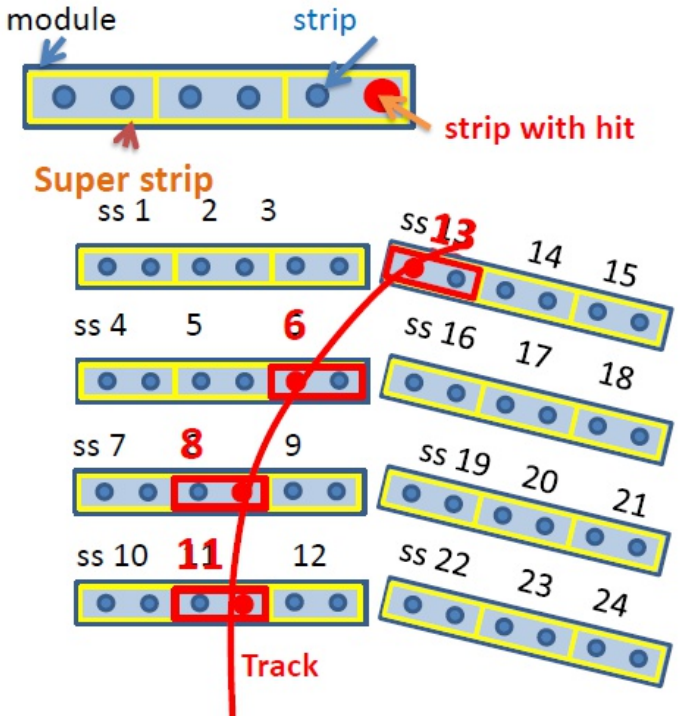
- Topological trigger system combines trigger objects from the feature extractors and provides input to the central trigger system.
- FPGA based system with 2x Xilinx Virtex Ultrascale+ VU9P
- Input bandwidth: **80x 6.4 Gb/s** with max. latency of **150 ns**
- Processing time: **75 ns**

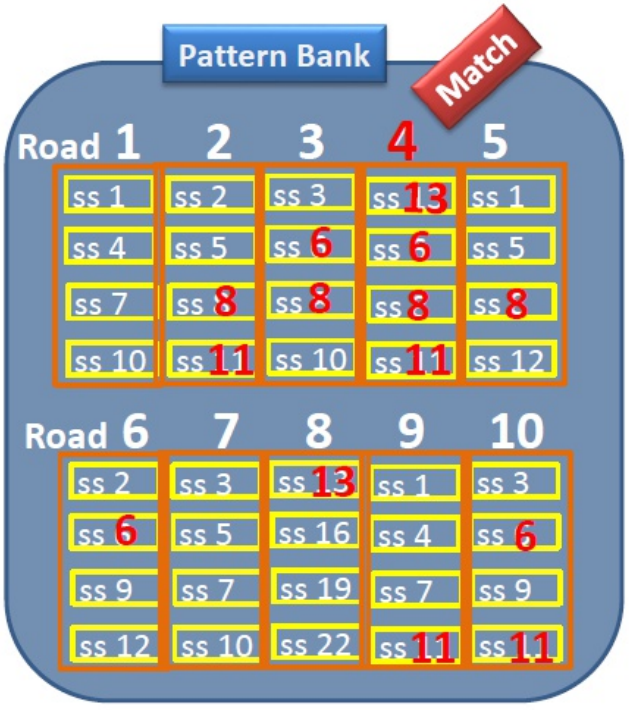




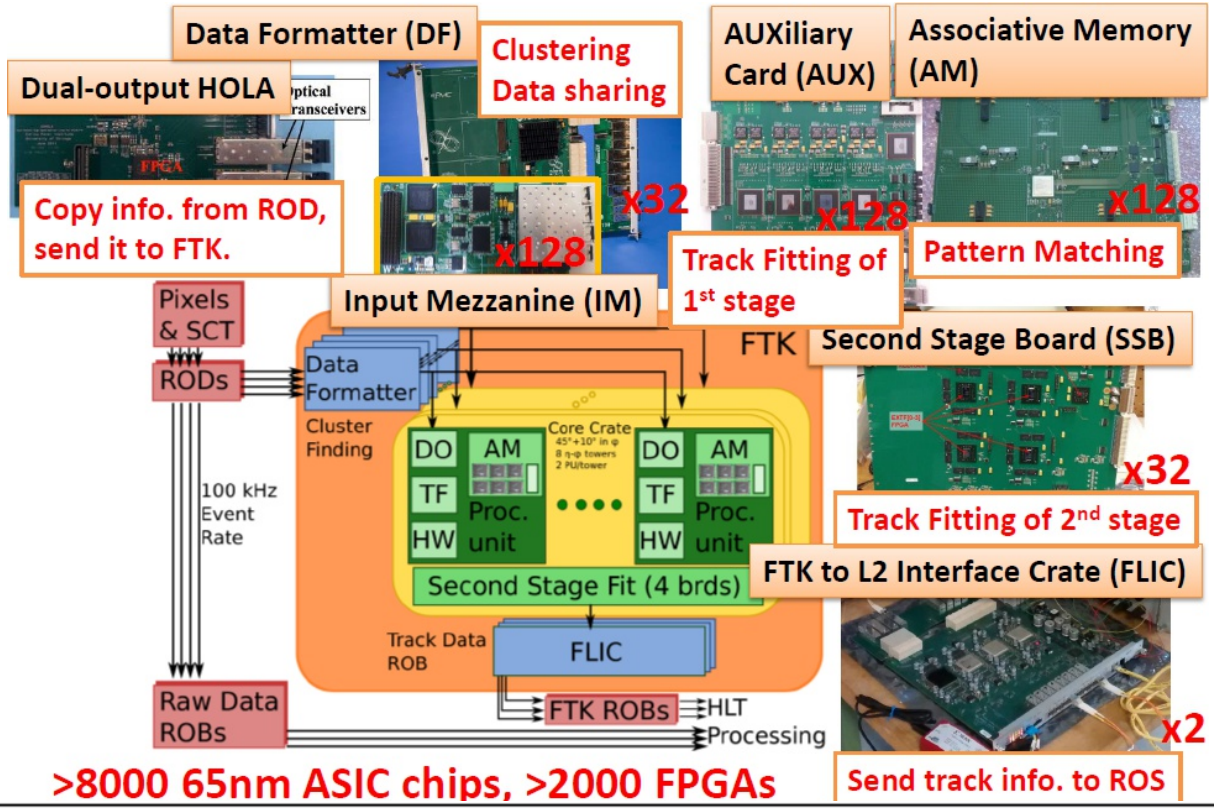
ATLAS Fast TracKer (FTK)

- The Fast TracKer (FTK) is to be forseen to be an additional input to the ATLAS trigger system after Phase-I.
- Goal: Offload the track finding from HLT computers to hardware.
- Algorithm: Compare hits with precalculated patterns.





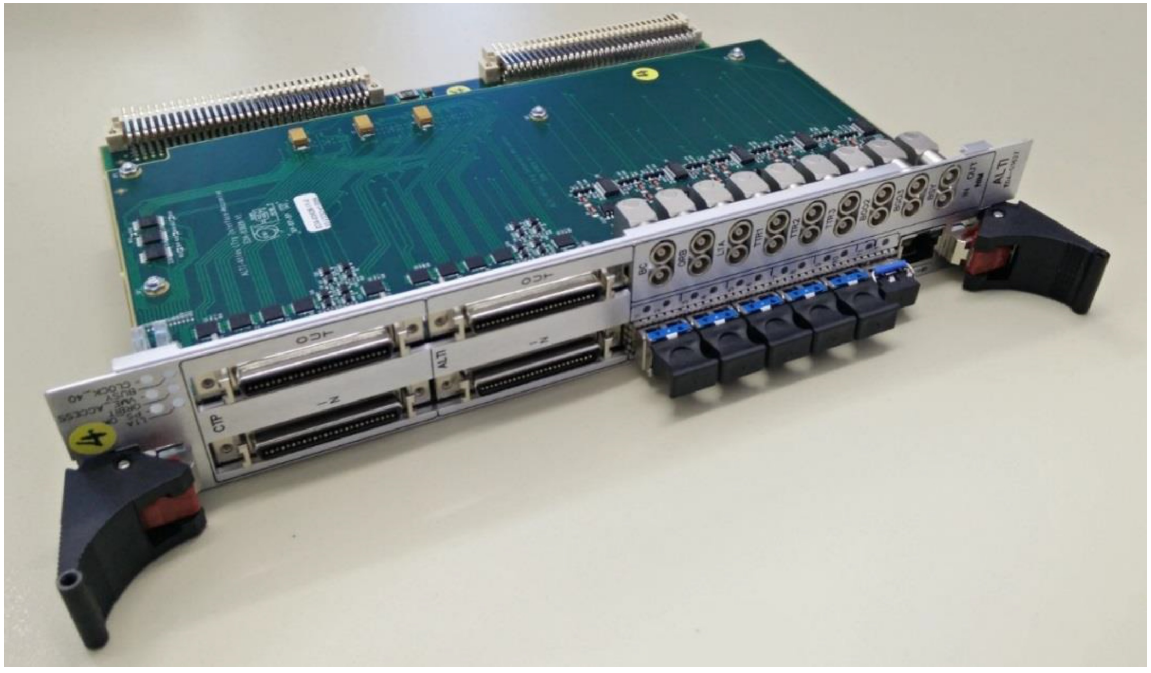
ATLAS FTK System Overview



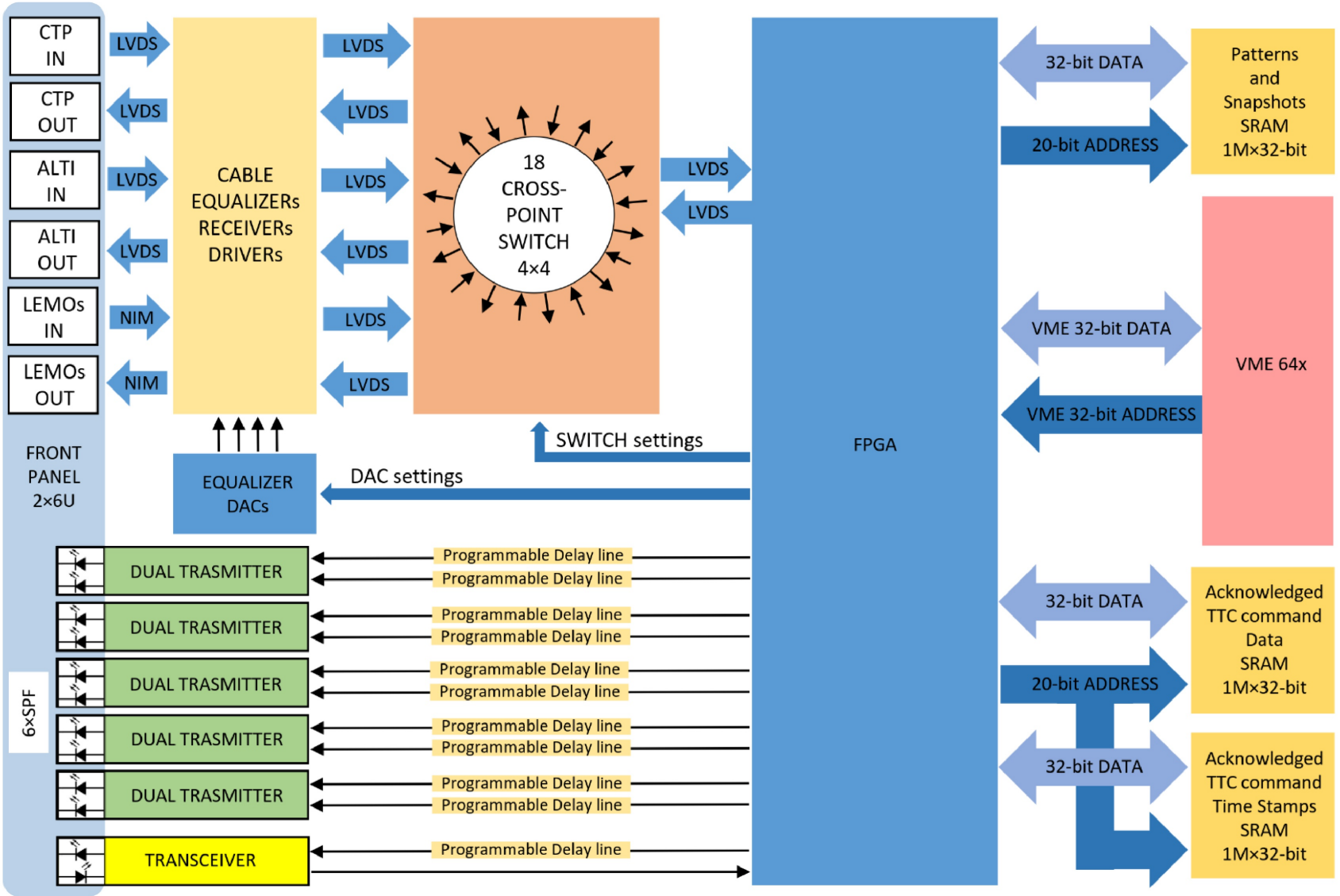
Board Name	Units	Crates/Shelves	FPGA	Connectivity
IM	128	4x 14U ATCA	2x Xilinx Artix-7 or 2x Sparatan-6	4 SPF+
DF	32		1x Xilinx Virtex-7	160 (288) QSFP to AUX and SSB
AUX	64 (128)	6x 9U VME	6x Intel/Altera Arria V	2x QSFP from DF, 1x SFP to SSB
AMB	64 (128)		2x Xilinx Artix-7 + 2x Xilinx Spartan-6	16 AM06 x 4 LAMBs
SSB	32	8x 9U VME	5x Xilinx Kintex-7	QSFP from DF, SFP from AUX, and SFP to FLIC
FLIC	2	1x 6U ATCA	4x Xilinx Virtex-6	SFP from SSB, and SFP to HLT

Local Trigger Distribution (Phase-I): ALTI Overview

- TTC system based on a couple of VME boards for every sub-detector.
  - Receiving and forwarding the trigger signals from central trigger.
  - Generating local triggers for testing.
  - No new production for Phase-I systems, therefore not available.
- Replacement: ATLAS Local Trigger Interface (ALTI)
  - FPGA-based solution (Xilinx Artix-7 200T)
  - VME interface for compatibility
  - Jitter cleaners
  - Optical inputs and outputs to sub-detector systems
  - Electrical interface to CTP

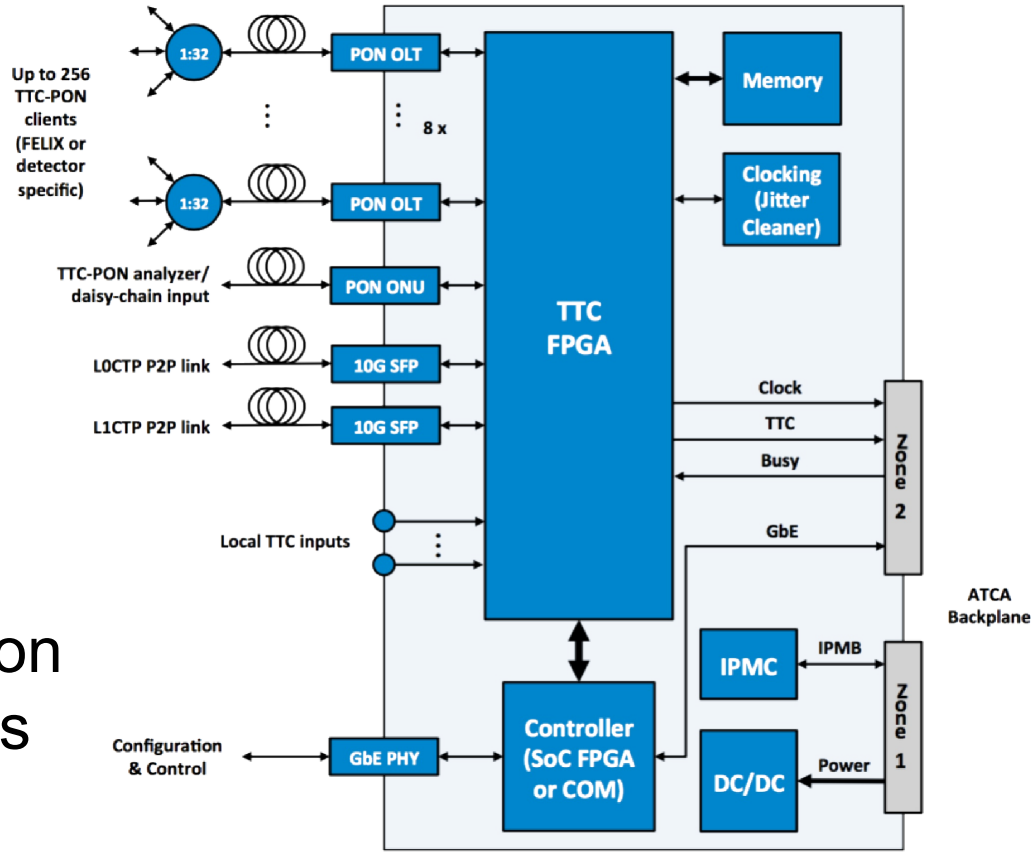


Local Trigger Distribution (Phase-I): ALTI block diagram



Local Trigger Distribution (Phase-II): LTI

- ATLAS TTC network will change to TTC-PON for Phase-II:
  - TTC bandwidth will increase from 80 Mbit/s to 10 Gb/s.
  - Passive optical network, similar to FTTH
- Main features:
  - Modern ATCA blade
  - 10 Gb/s P2P link to central trigger system
  - Can serve up to 8x32 = 256 detector systems in PON mode
  - Standalone running also supported
- Currently in the specification phase. Design process has not yet started.



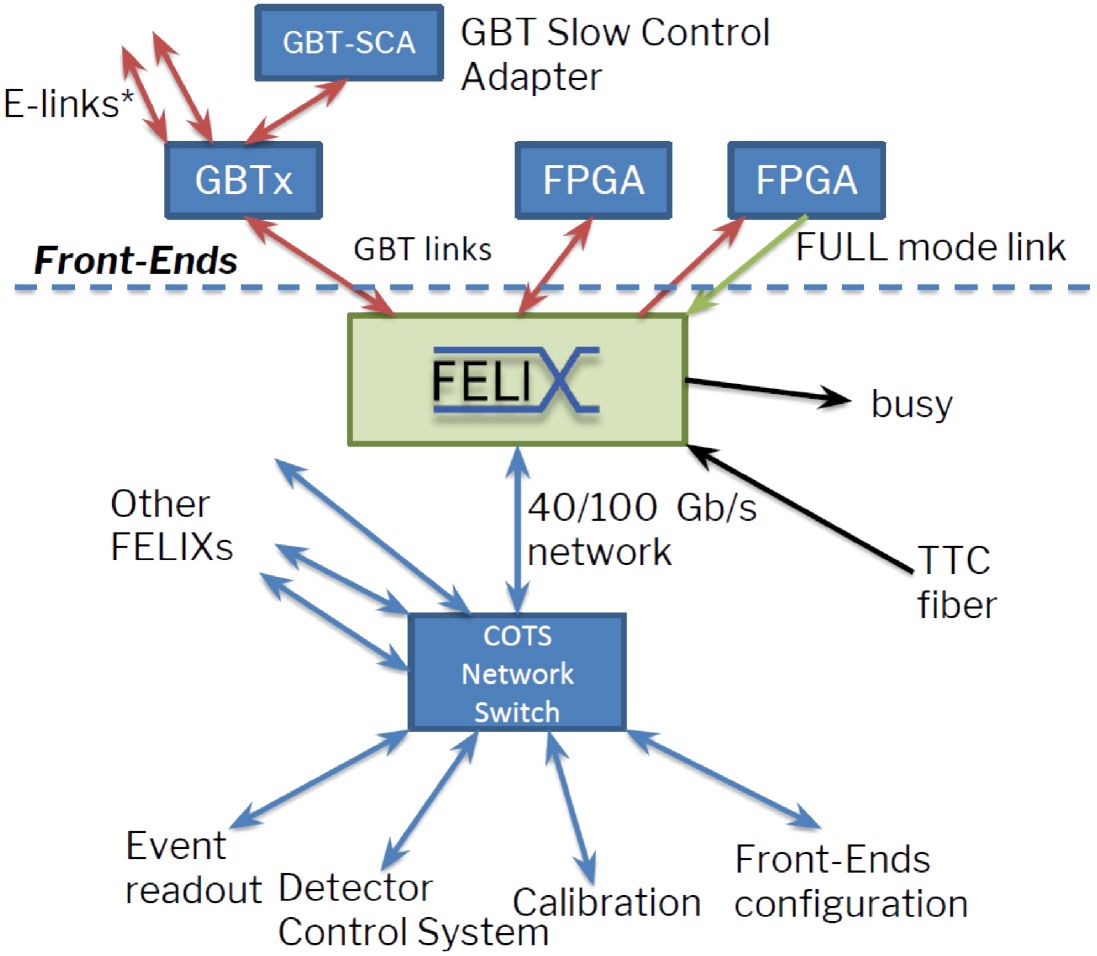
FPGAs in the ATLAS readout

FPGAs in readout systems

- Readout system usually have FPGAs to cope with detector-specific protocols, which also may run at very high datarates.
  - Until Phase-I: Every sub-detector uses his own FPGA development (Readout Driver, ROD)
  - Starting with Phase-I: Trend in ATLAS to harmonize FPGA usage in readout systems by using single FPGA board development for whole ATLAS.
  - Front-End data is sent through network.
  - ROD functionality will move into software.
- Reasons for this policy:
  - **Maintainability** (short-term + long-term)
  - **Commercial network hardware** can be used.
  - Focus on **software development**.

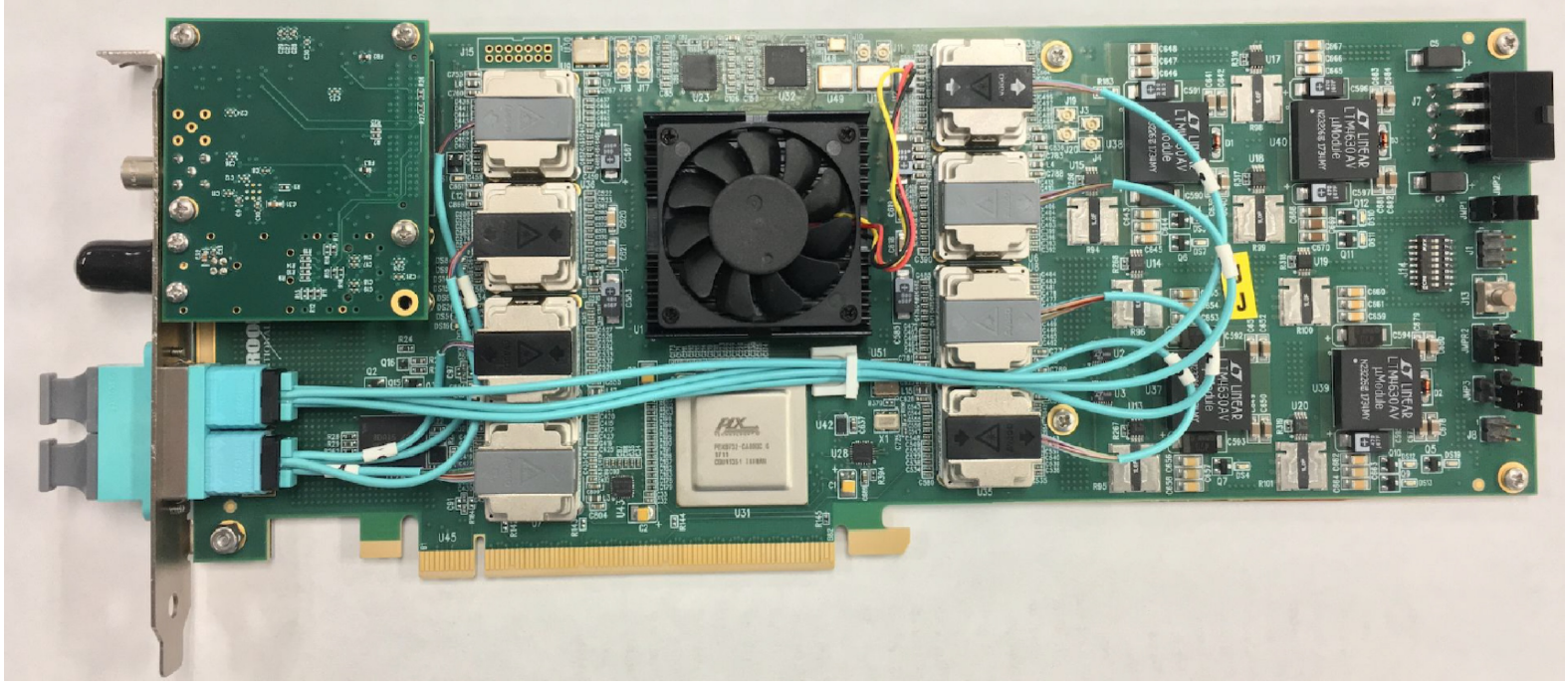
The FELIX Concept

- RODs will be replaced by ATLAS-wide FPGA card + PC with corresponding software package.
- Conversion between front-end links and 40/100G Ethernet.
- GBT mode to work with detector links (with CERN's GBTx chipset)
- FULL mode for inter-FPGA connections



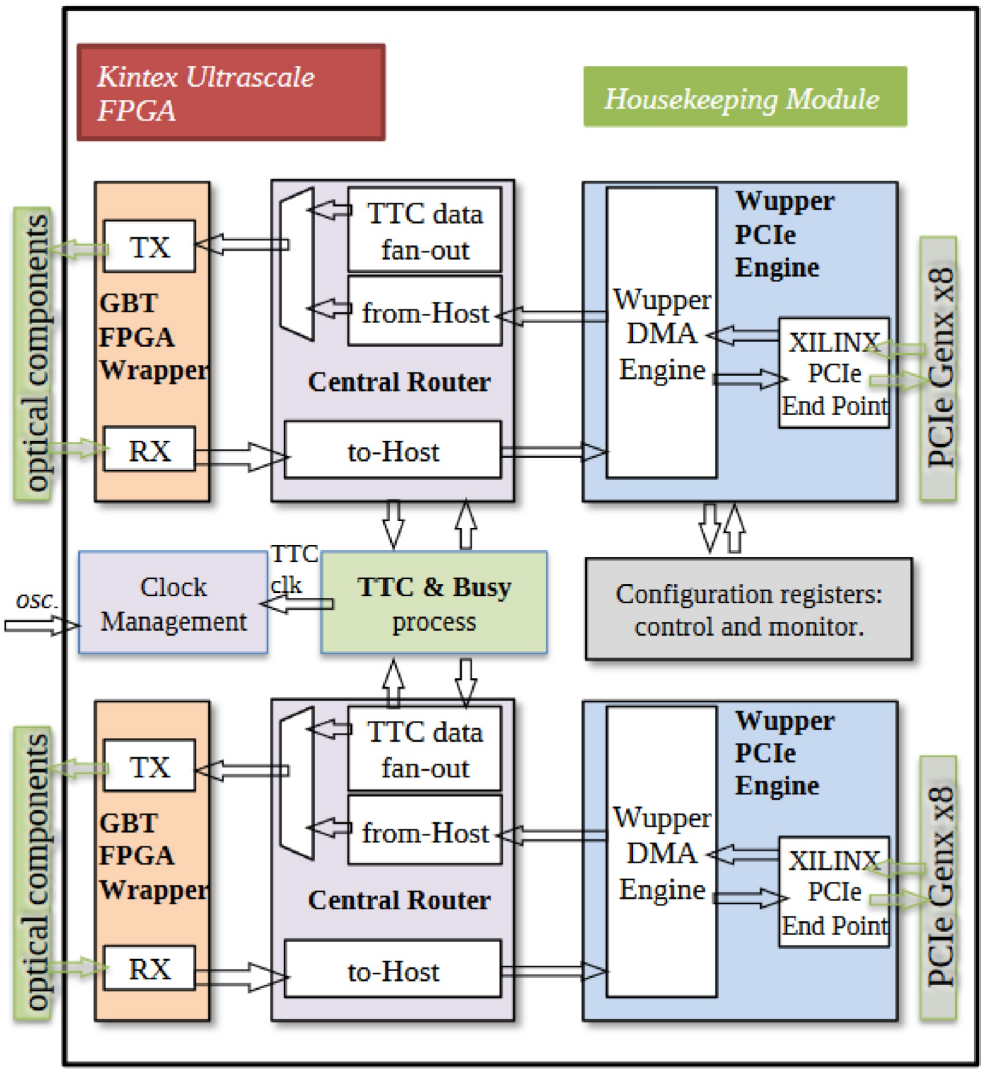
The FELIX Phase-I FPGA board

- PCI Express form-factor card (1 slot full-height, full-length)
- FPGA: Kintex Ultrascale KU115
- PCIe switch: 2x8 lanes into 1x16 lanes PCIe
- TTC mezzanine for interfacing to trigger system. Can be replaced by TTC-PON mezzanine.
- up to 48 optical inputs/outputs to the detector



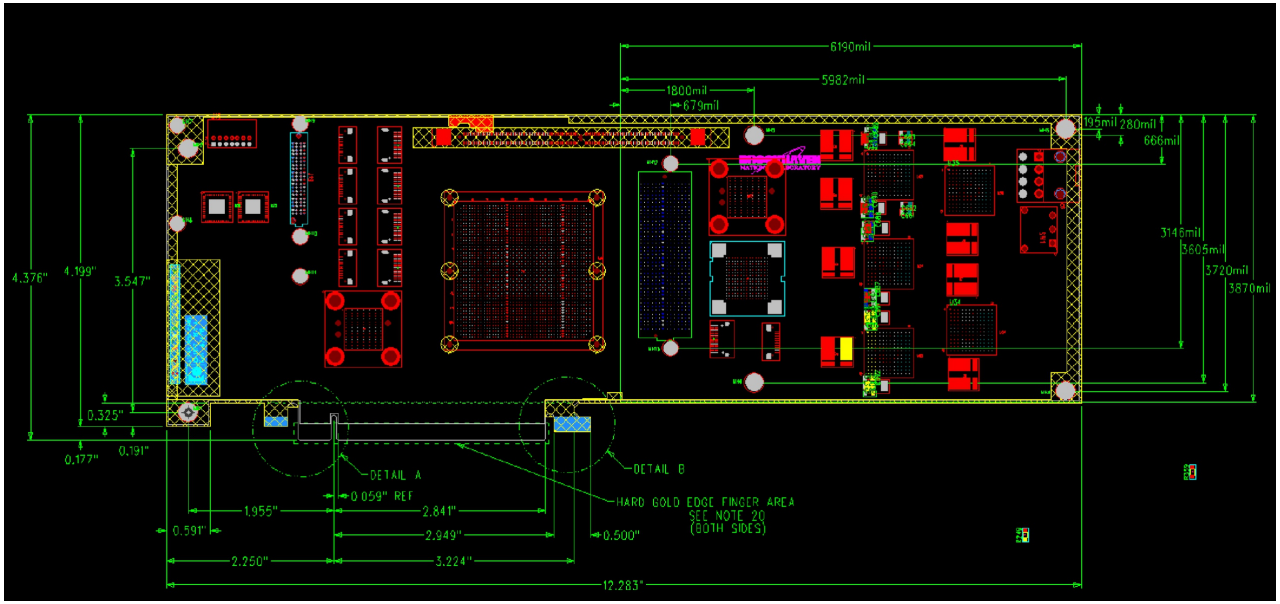
The FELIX Phase-I FPGA firmware

- Two identical blocks with seperate PCIe endpoints:
  - smaller logic blocks for multiplexing
- Main blocks:
  - GBT wrapper
  - Central Router
  - Wupper PCIe engine
  - TTC interface
- Central Router contains the core functionality of FELIX:
  - Decoding/Decompressing of datastreams from the detector (8b10b,HDLC)
  - Encoding data + TTC signals to the detector



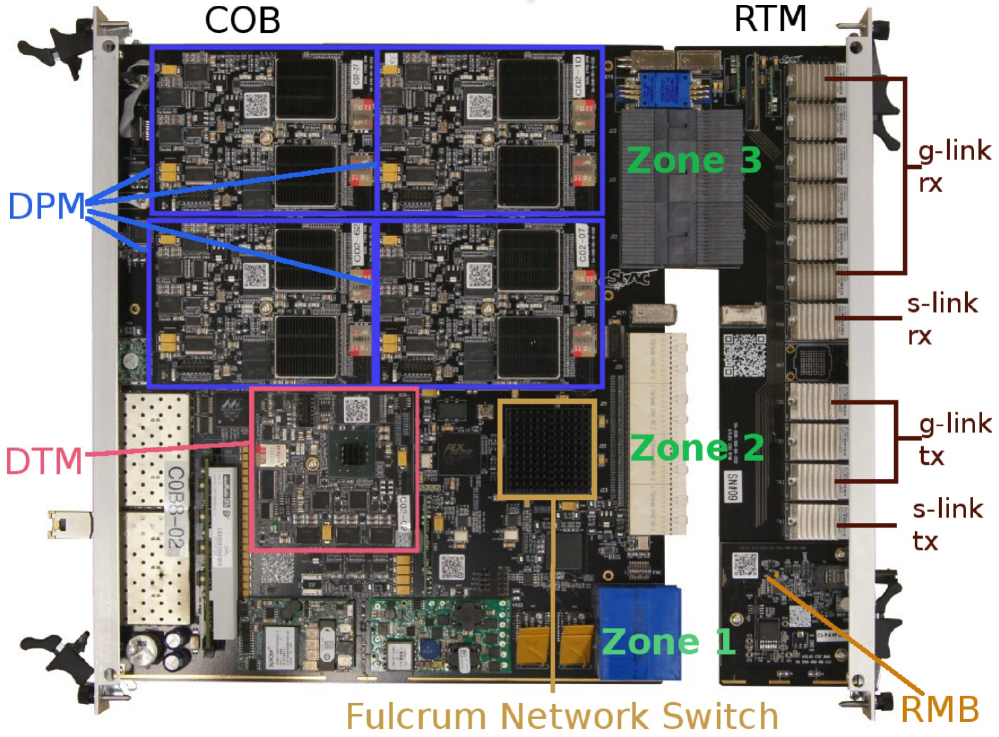
Outlook on FELIX for Phase-II

- After the Phase-II upgrade all subdetectors will use FELIX as readout system.
- Most demanding: new all-silicon Inner Tracker (ITk)
  - 7000-10000 uplink fibres with 10 Gb/s each (i.e. 200-250 FELIX cards)
  - Total bandwidth: **70-100 Tb/s**
- Phase-II prototyping has just started:
  - New board design with Xilinx Virtex VU9P:
  - Support for PCIe Gen3, 16 lanes
- New HBM US+ and Versal FPGAs have support for PCIe 4.0, but not yet general available



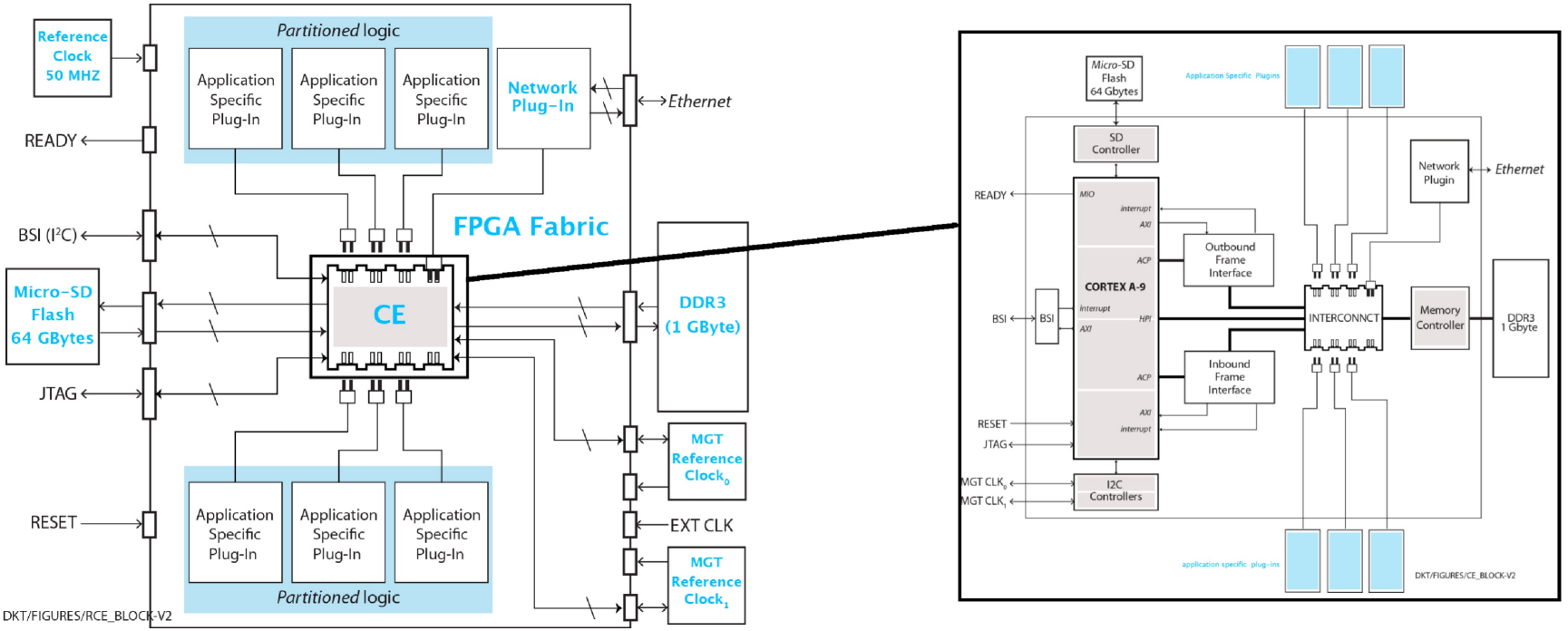
Reconfigurable Cluster Element (RCE) readout

- Is used in some small detectors:
  - muon cathode strip chambers (CSC)
  - ATLAS forward proton detector (AFP)
  - Insertable b-Layer (IBL): only during commissioning
  - Inner Tracker (ITk): demonstrator readout
- ATCA system
  - Cluster on board (COB) with Rear-Transistion-Module (RTM)
  - RCE-mezzanines with SoC FPGA
  - 10G Ethernet switch
- FPGAs:
  - DPM: Zynq Z7045
  - DTM: Zynq Z7030



RCE Firmware

- Firmware split into 2 parts:
  - application independent part: Zynq subsystem
  - application dependent part: user code
- Interconnect: AXI/AXI-stream



Summary

- FPGAs are widely used in ATLAS.
- Off-Detector systems are highly customized electronics and handle non-standard protocols.
- Trigger systems and detector readout systems have different requirements on FPGA:
  - Trigger: Deterministic low processing time
  - Readout: High throughput
- FPGAs meet these requirements and are much cheaper at the required quantities and more flexible than ASICs.
- FPGAs cannot replace ASICs inside the detector due to energy consumption and radiation hardness.
- ATLAS mainly uses Xilinx FPGAs.

Thank You for Your attention!