FPGAs for ps Timing

Why Time measurements, Why to use FPGAs, FPGAs as TDC in running experiments

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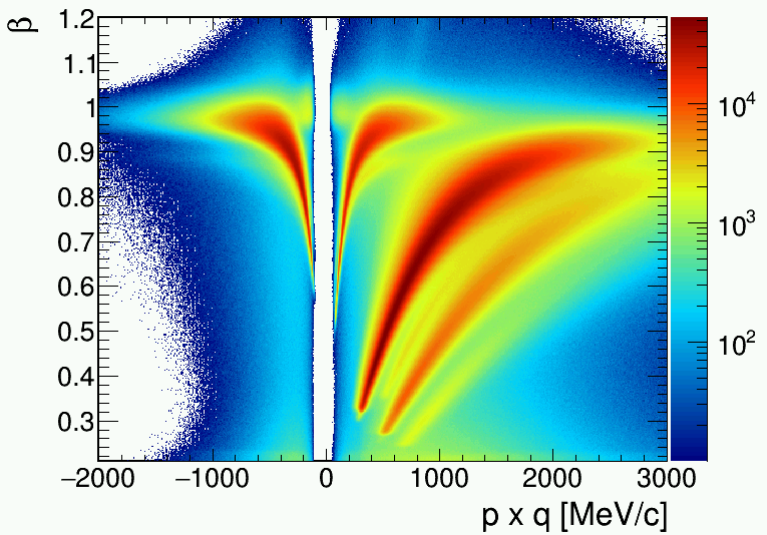
Outline

Time Measurements in Particle Physics: Why?

Time of Flight (ToF) applications for particle identification



"Live" plot of the currently running HADES measurement campaign @GSI.

Other "trivial" applications of time measurements

- Arrivial time to separate events (free running data acquisition)
- Pile-up (>1 reaction in integration time of detectors) rejection

Conclusion: Time measurements are used in every experiment.

Time Measurements: How?

How to obtain the time measurement

- Oscilloscope (ADC) gives the best representation of the original signal and best possiblilties for offline processing and correction
- ADCs draw a lot of power, are expensive and additional massive data processing necessary $\rightarrow$ heat, price, space
- possible to use efficiently if time interval is short (selective trigger)

Typical photomultiplier signals on oscilloscope

Time Measurements with TDC

- If the number of channels increase and a very good time precision is needed
  - Signal discrimination (threshold) and time difference measurement is a feasible and effective option
- Amplitude measurement: direct Time over Threshold (ToT)
  - not linear and limited dynamic range
- Time measurement can also be used for precise charge measurement

Consequence: Use time measurement for all detectors in the system

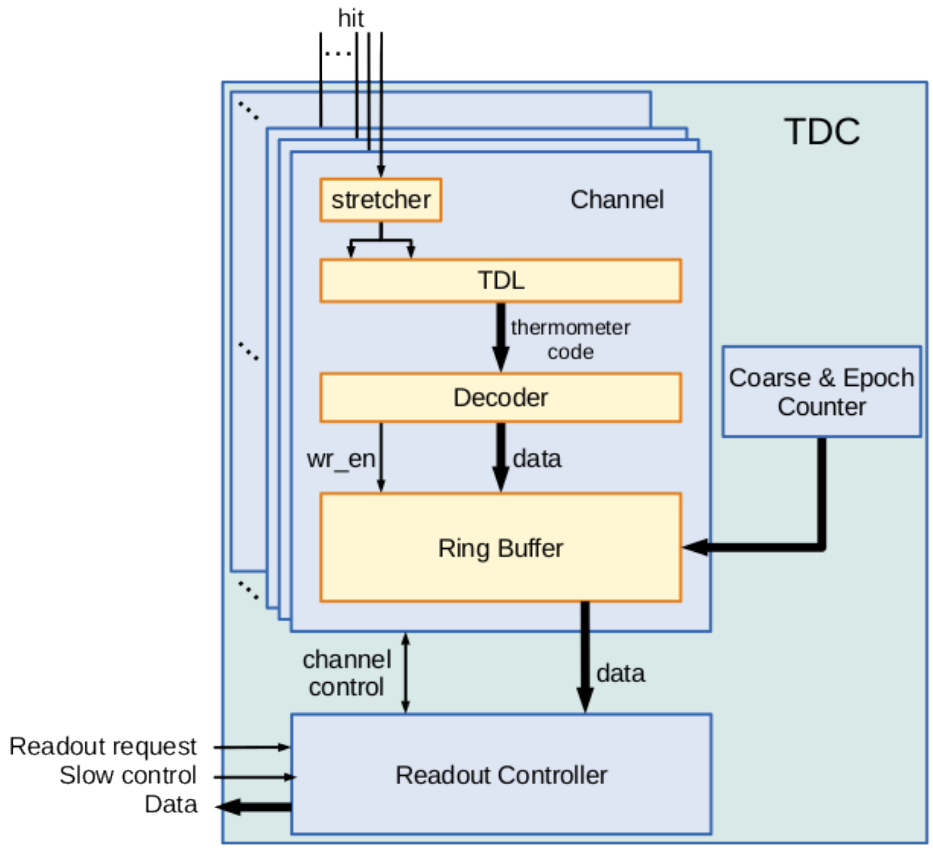
- Many different methods of "direct" time measurement are possible
- A very flexible, precise, low power, small and cheap Time to Digital (TDC) converter is needed

Motivation for building TDCs with an FPGA

- To be independent from not easy to acquire ASICs from the community.
  - should be easily available, industrial quality in design, package and documentation
  - vendor independent (not really easy!)
  - based on FPGAs (TDC, DAQ, FEE-Discriminator) and other parts with a second source
  - We "misuse" digital FPGAs in the asynchronous and analoge domain
    - an FPGA is more than a digital device $\rightarrow$ go deep in FPGA architecture
    - use intrinsic delays for time measurements, pulse stretching and signal delays
    - use LVDS-input buffers for signal discrimination
- To be flexible in functionality
  - Add and change functionality nobody thought of when the TDC was build

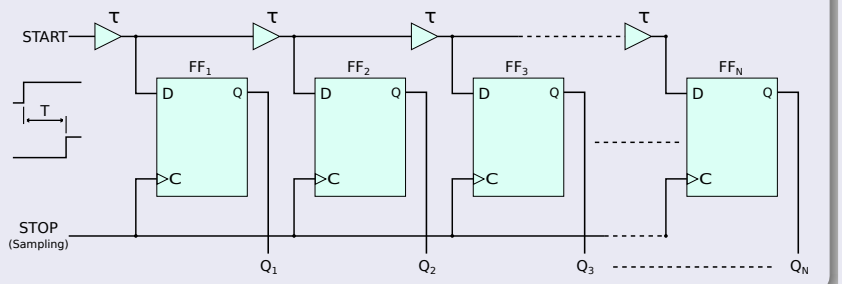
Basic Operation of an FPGA-TDC

- Coarse & Epoch counters for long measurement range
- Tapped Delay Line for fine time interpolator
- Stretcher for measuring the traling edge in the same channel
- Decoder: thermocode $\rightarrow$ binary
- Ring buffer for the latest hit signals

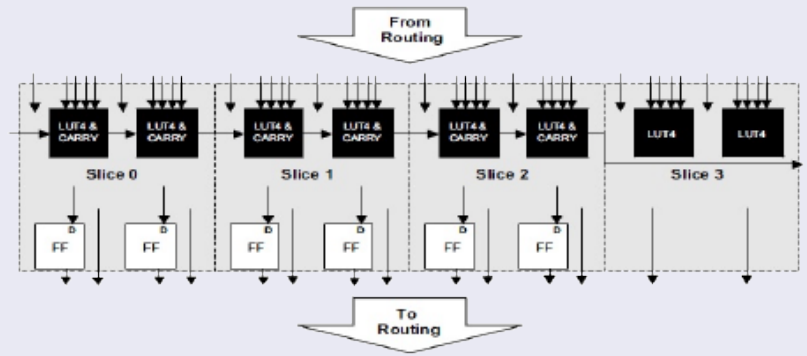


Fine Time Interpolation

Tapped Delay Line



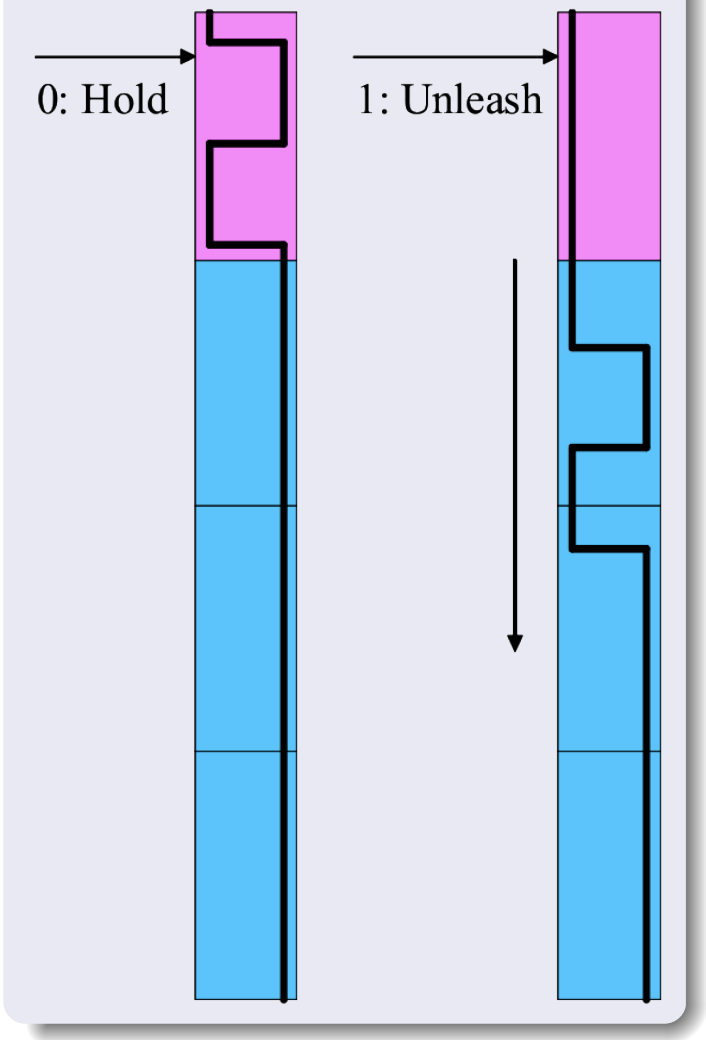
Internal FPGA Structure



- Propagation of the start signal is sampled with the stop signal
- Suits well with the FPGA architecture
- Carry chain for delay line $\rightarrow$ small bin width
- Clock signal as common stop signal $\rightarrow$ minimal skew
- Coarse & Epoch counters $\rightarrow$ $\sim$45 minutes measurement range

FPGA-TDC: Further improvements

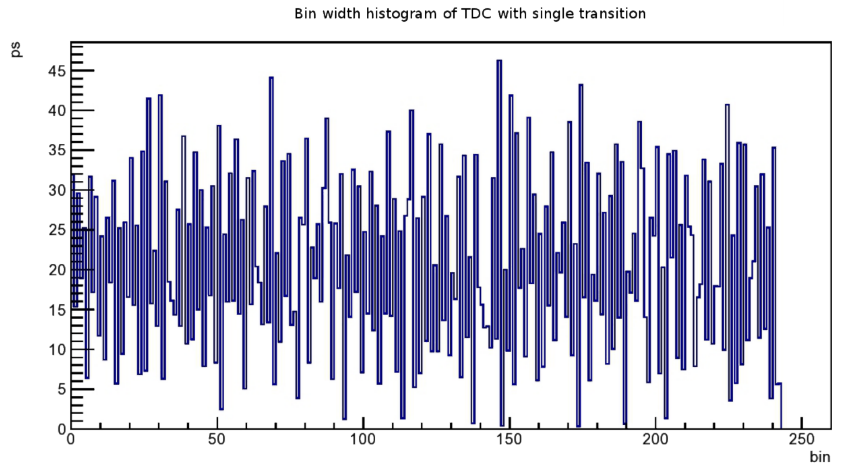
Wave Union Launcher

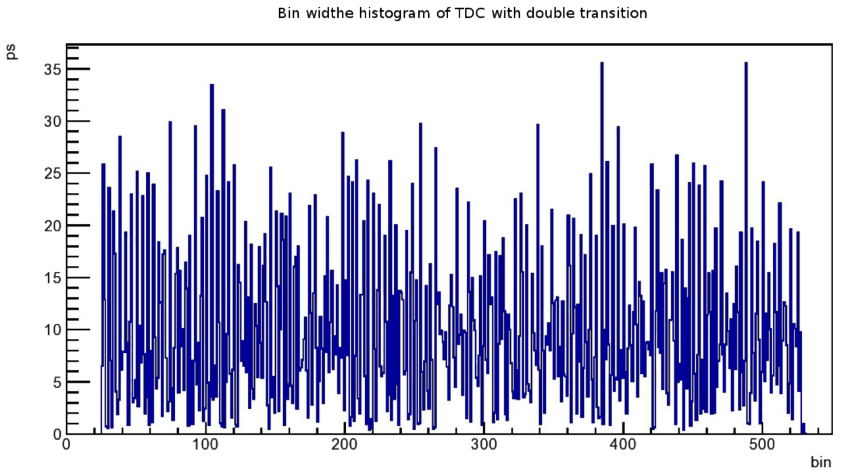


- Non-uniform intrinsic delays → Ultra wide bins
- the precision of the TDC is reduced
- Wave Union Launcher [Jinyuan Wu]:
  - send many transitions to the delay line, when a hit signal arrives, thereby increase the number of measurements on the delay line and even out ultra wide bins (UWB)

FPGA-TDCs: Bin Width (DNL)

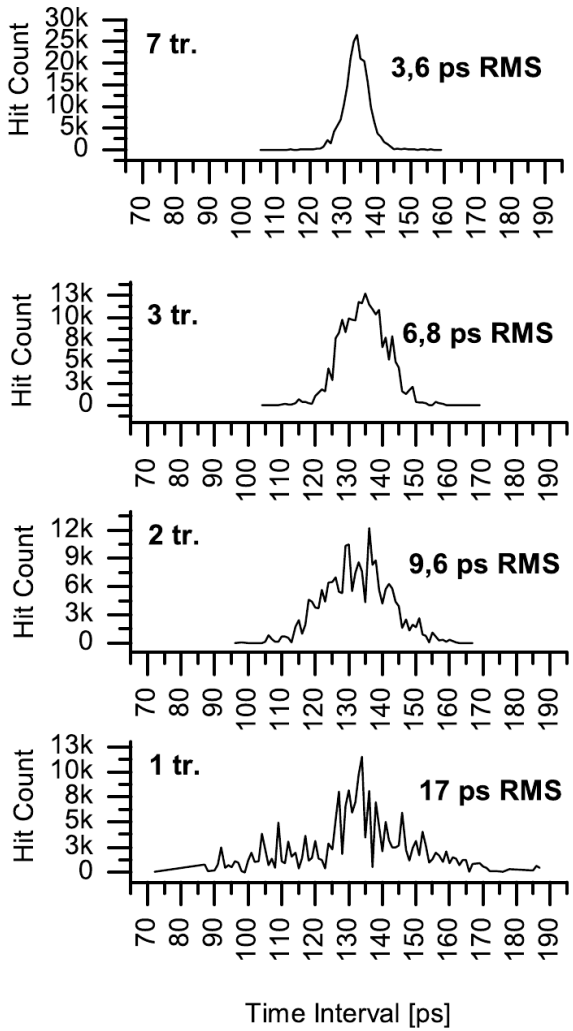
- Non-linearities caused by non-uniform intrinsic delays
- UWBs increase non-linearities
- WUL averages the locations of the transition on the delay line, thus dividing the UWBs
- Max bw: 45ps $\rightarrow$ 35ps
- Avg bw: 20ps $\rightarrow$ 10ps
- Calibration of the TDC further decreases the non-linearity





Features of FPGA TDCs

- FPGA TDCs can be very precise time measurement devices
- trade-off between time precision and used resources
- FPGA TDCs are flexible
  - implemented features can be easily changed (trigger, windows, scalers, etc.)
  - new ideas pop up quite often



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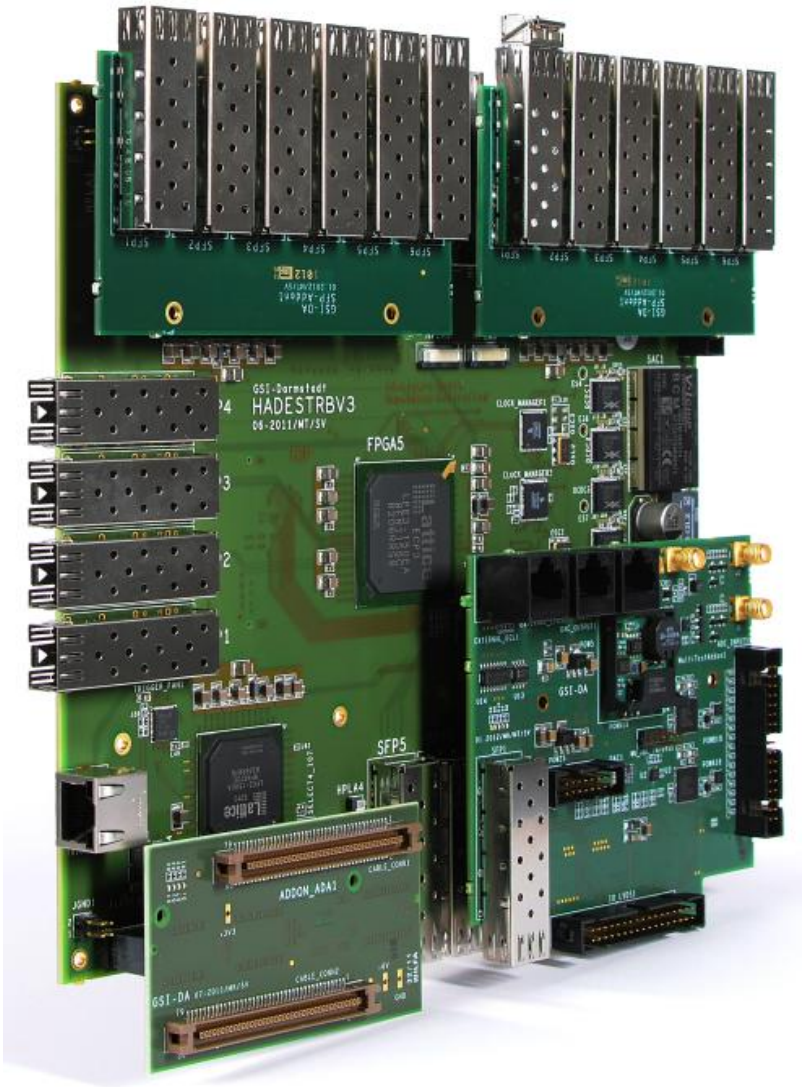
TRB Platform: Features

- Versatile and meanwhile technically mature platform for TDC measurements and digital readout
- consists of FPGA-firmware, DAQ- and (online-)calibration-software and hardware
- most important ingredient: the TRB team (a collaboration) behind all of it for (necessary) support [`http://trb.gsi.de`]
- many channels (256 single edge) on one board and as cheap as possible
- leading edge time precision: 8-12ps RMS
- hitrates <50MHz (burst)
- DAQ: 140MBytes/s via two 1GbE links

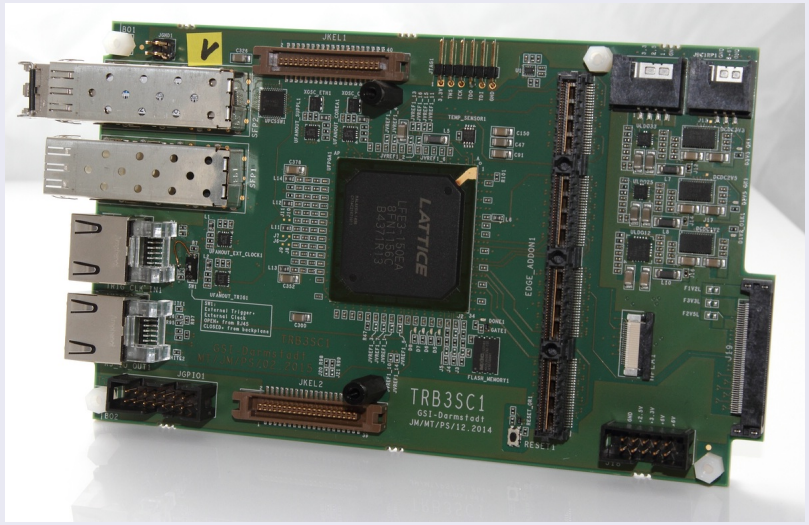
TRB Platform: TRB3 module



- 4 times high speed 208-pin connector for various AddONs
- Addons available:
  - 6/8 port Hubs
  - NIM/ECL-Input
  - standard 100mil pins
  - Padiwa-Adapter
  - etc. [http://trb.gsi.de]

TRB Platform: Some Hardware II

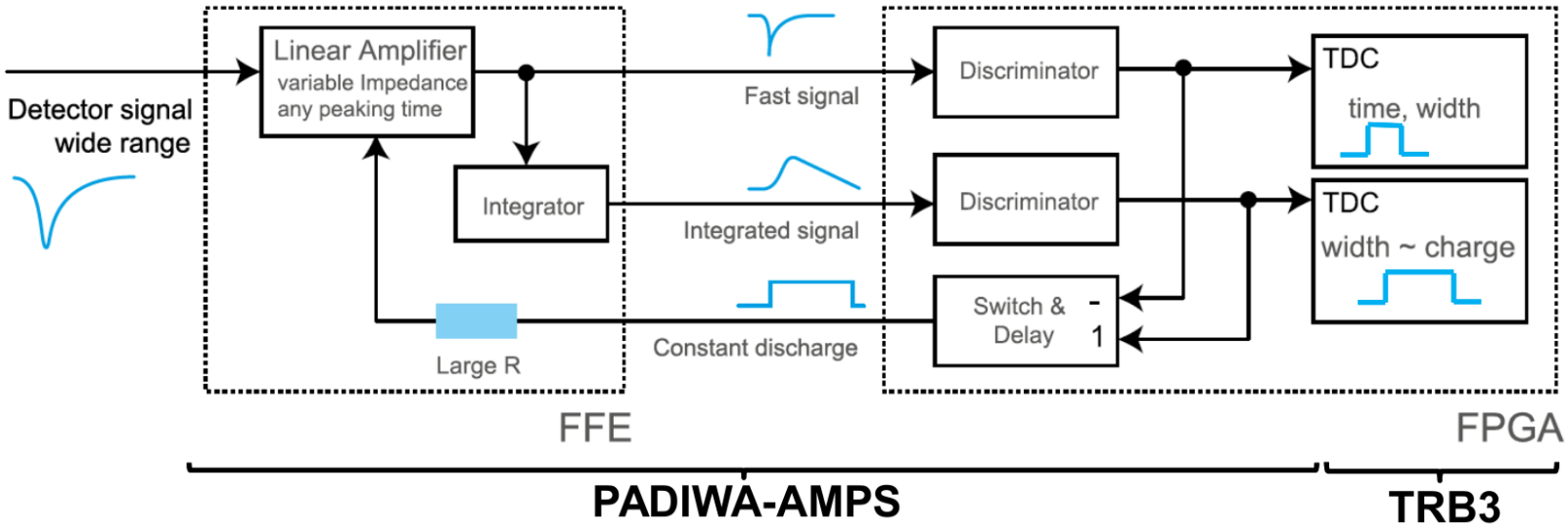
TRBsc



TRB3sc Crate

- 1/4 of TRB3 on a single card
- fits in 19" standard crate system with FPGA-connectivity in backplane
- better DC/DC converters for higher time precision
- higher DAQ speed

FPGA-TDC: Charge Measurement



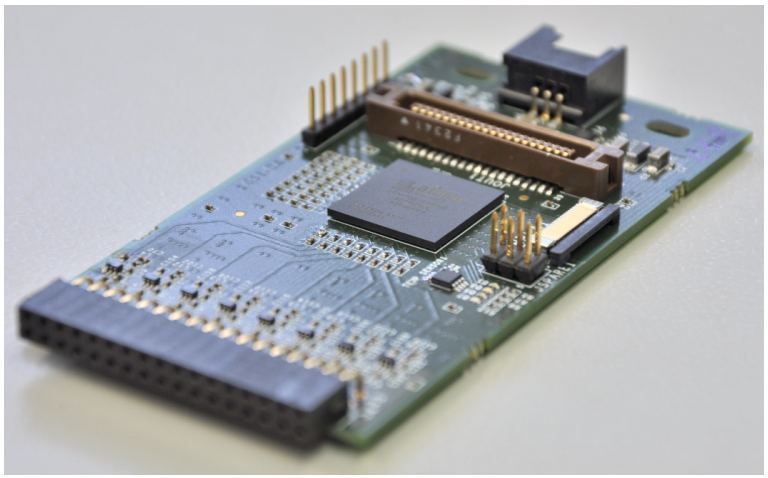
Modified Wilkinson ADC:

- "Come-and-Kiss"-principe: Commercial of the shelf and keep it small and simple.
- Input signal is integrated with a capacitor
- Capacitor is discharged using a constant current source triggered by the input signal
- Measured charge precision: 0.22%

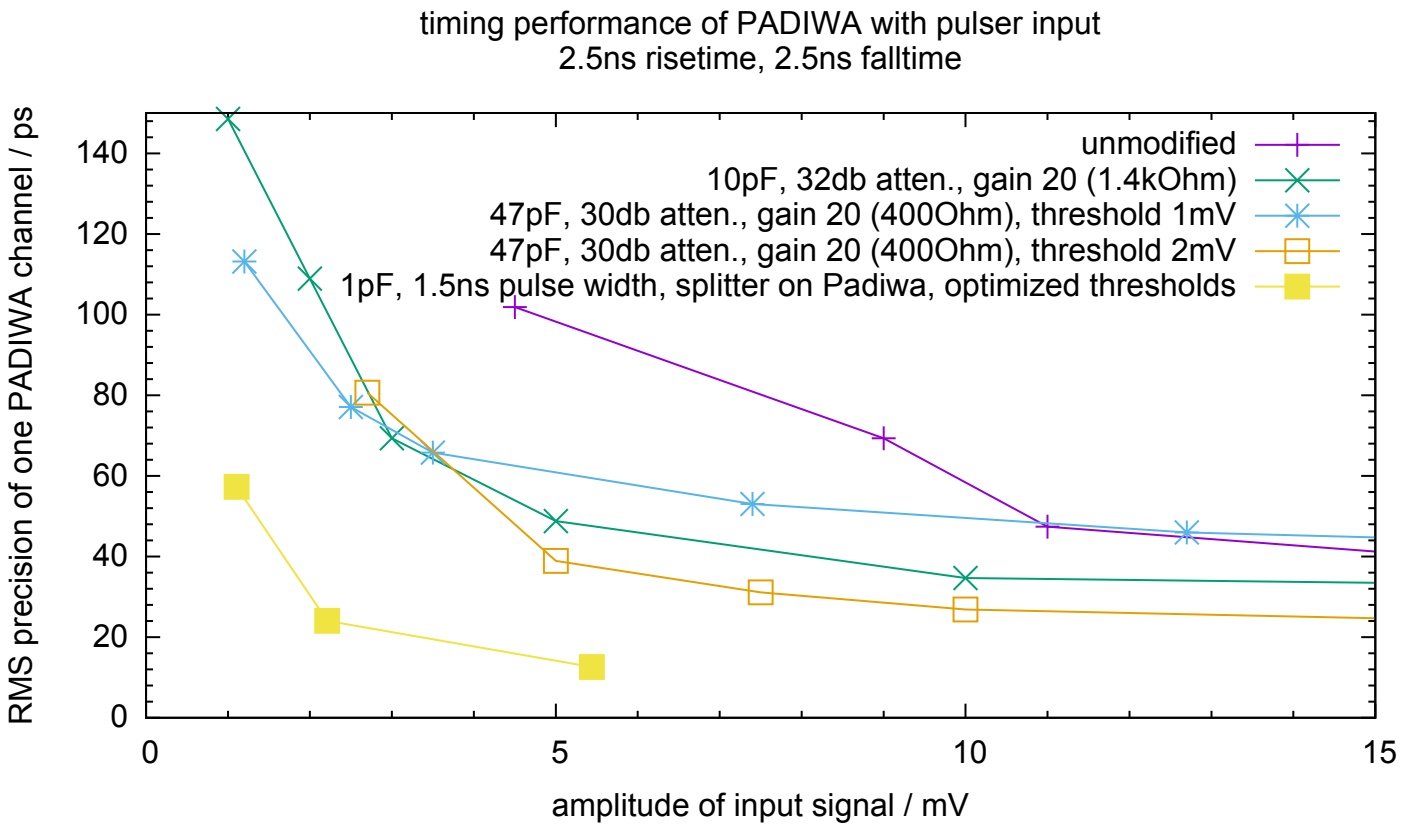
Experiences and Limits

What did we learn?

- TRB DAQ-Systems work very well and stable also for "larger" systems
- FPGA-TDC working horse of the whole DAQ/FEE-system
- Padiwa-FEE works for many users very well
- but. . . .



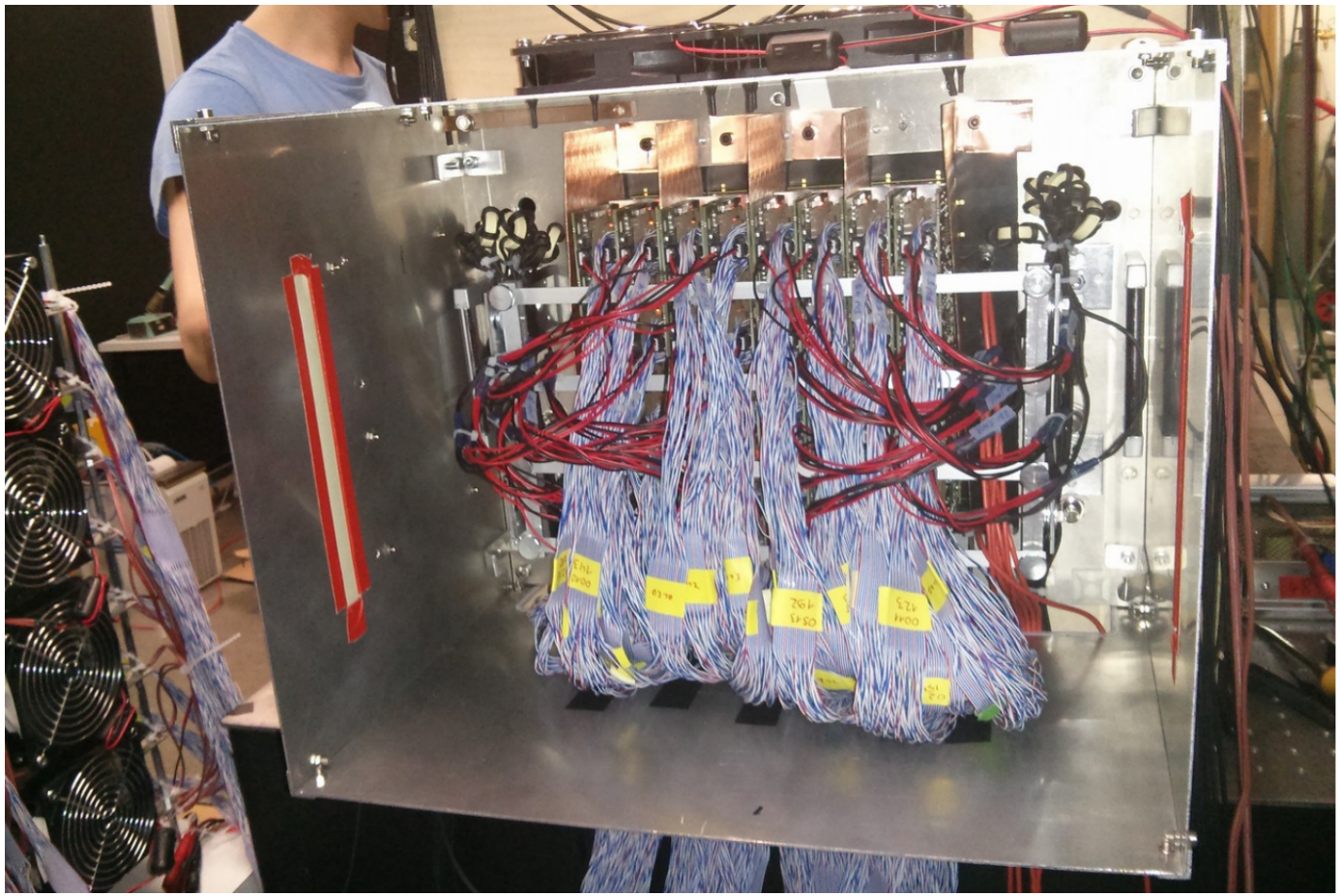
Padiwa Timing Results



- timing measurements in the lab are very good
- "trivial": signal to noise determines timing precision

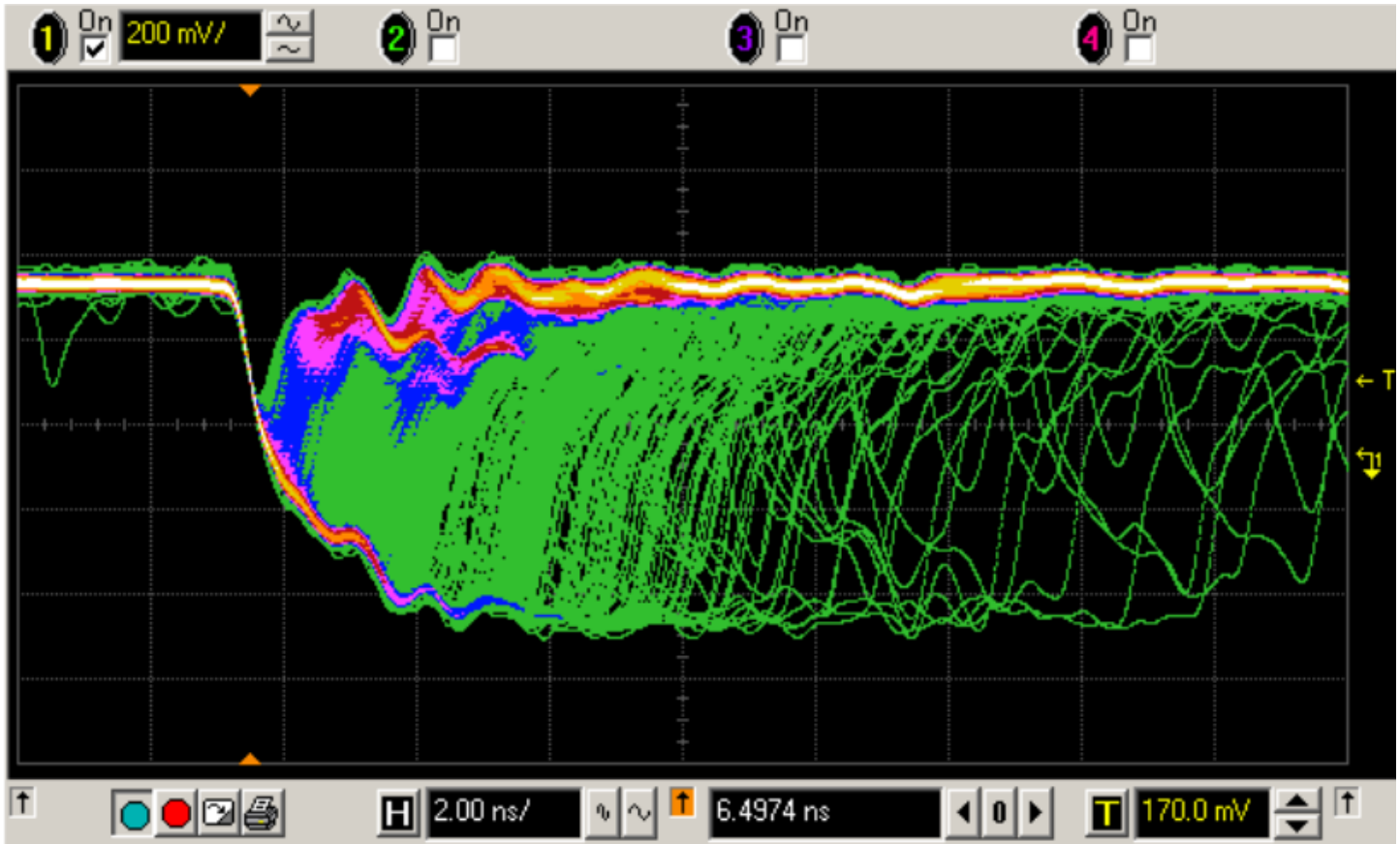
Feature and Problem at the same Time

- The TRB platform is a stable and flexible
- Flexibility has a (high) price
  - Cables everywhere! (Fine for ~1k channels.)



Effects of Cables

- Mechanically this becomes a problem (densities)
  - Barrel-DIRC-beam-time clearly showed that this is more than a inconvenience
- Long cables damp the signal away

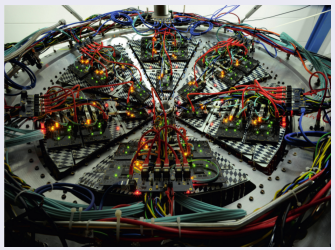


Solution

- Rethink mechanics/cables/connectors
- Improve on noise to the input of the FEE
- Improve on noise immunity of FEE
- Work together in a larger team!
- Some pressure!

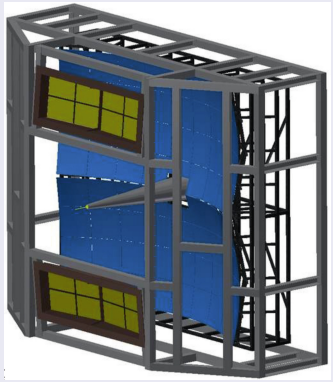
Team for a total of 100k channels

HADES-RICH



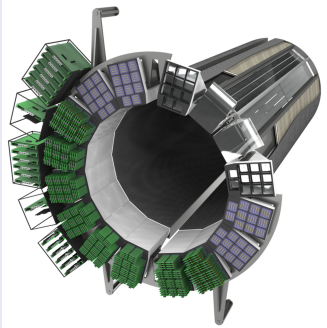
- 28k channels MA-PMT
- existing detector
- beamtime in 2018/2019

CBM-RICH



- 55k channels MA-PMT
- to be finished in 2020

PANDA-Barrel-DIRC



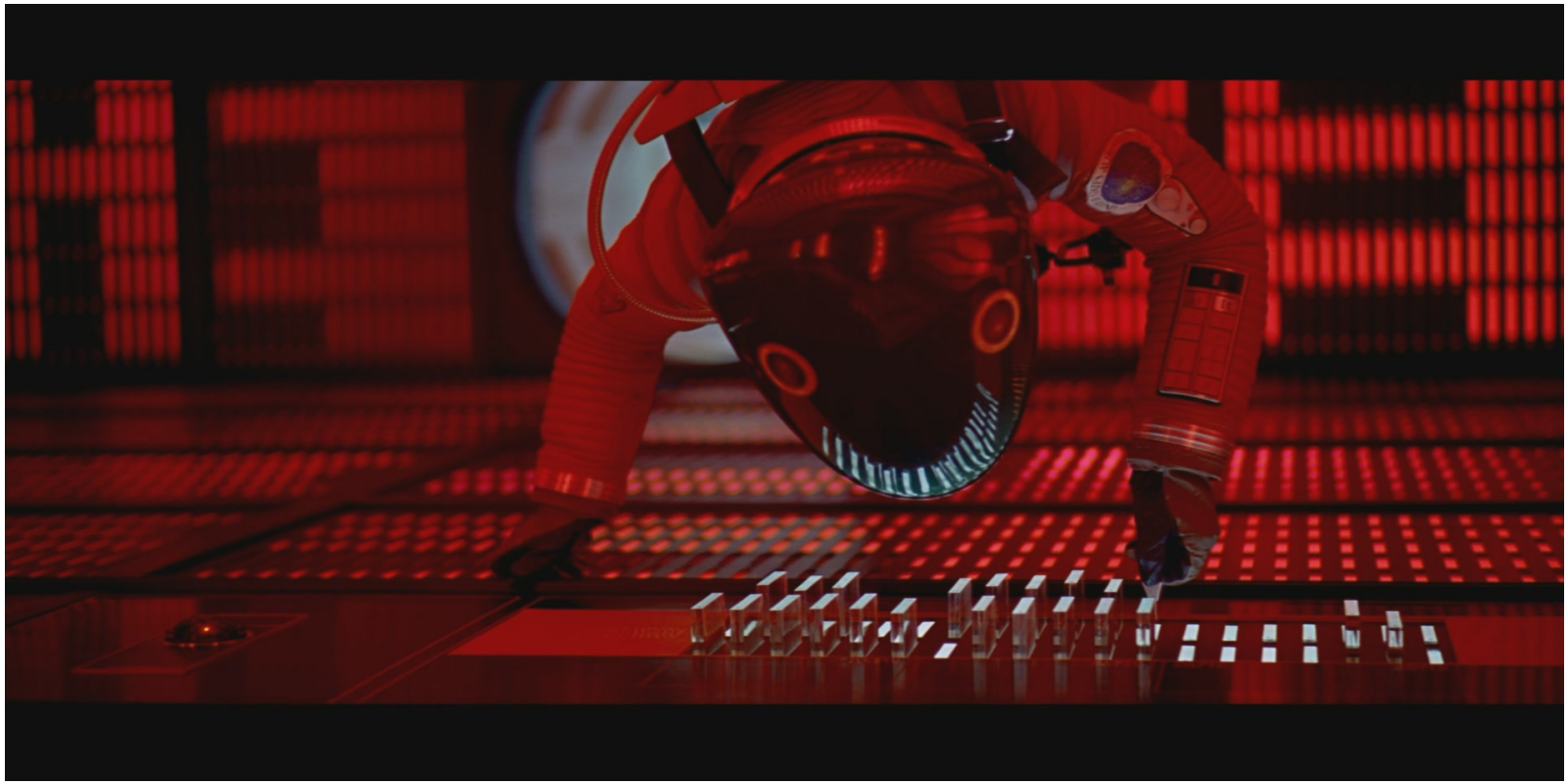
- 11k channels MCP-PMT
- smaller signals

TRB Collaboration

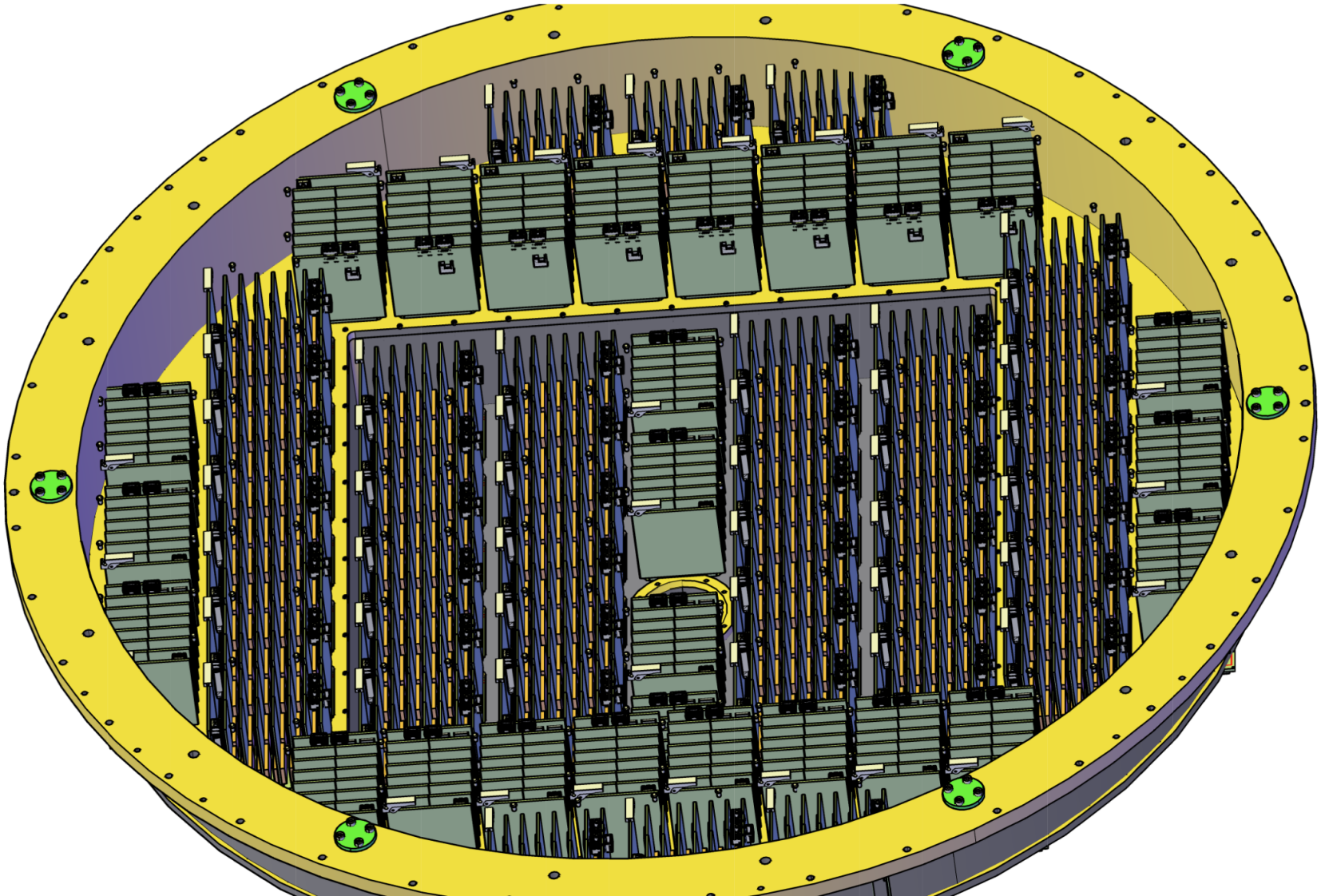
Team of ∼8 developpers (hard and software)

HAL9000: Inspiration

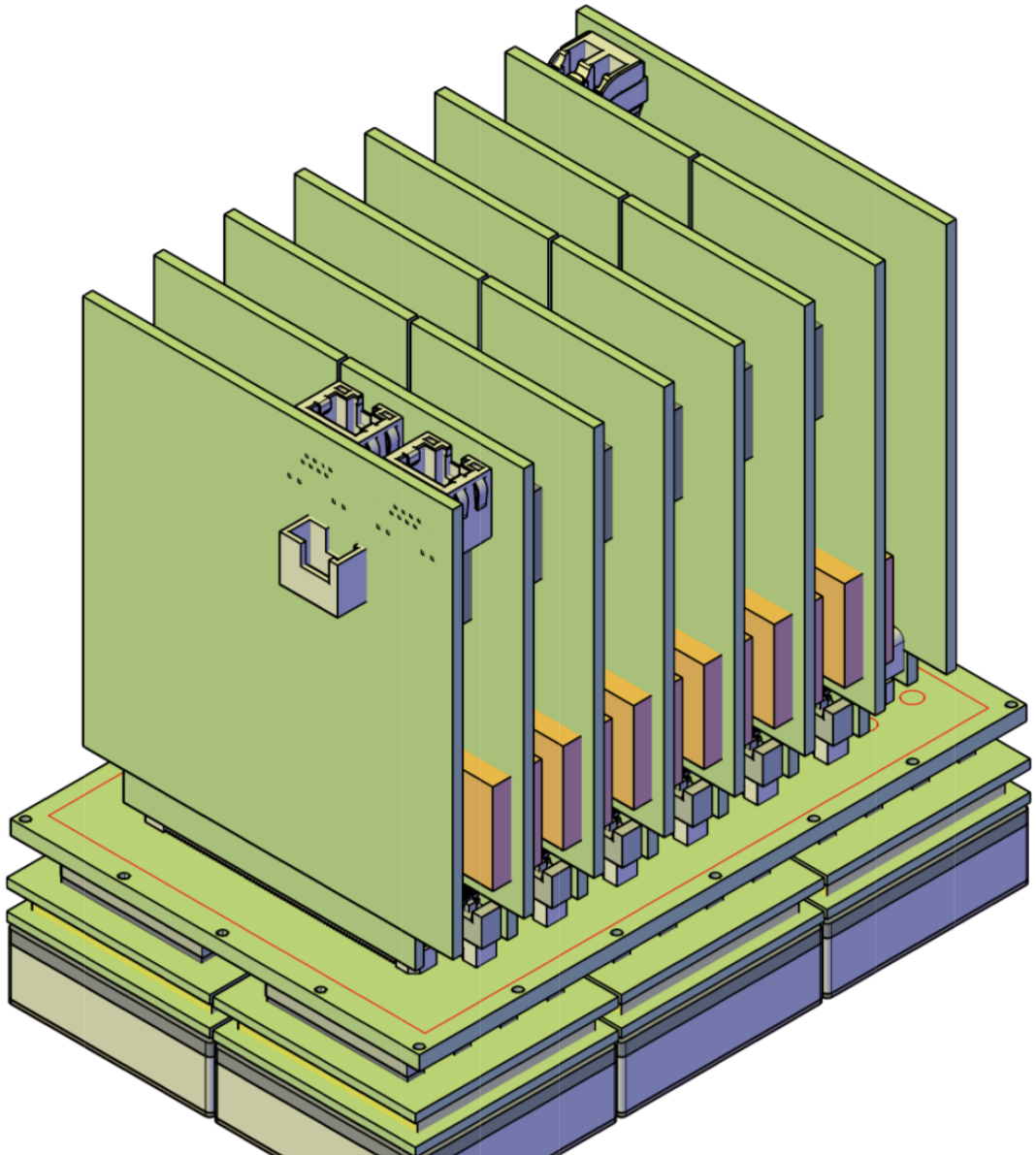
- Stanley Kubrick solved this problem in 1968 :-)



Backplane Granularity and Dimensions: Long and Tedious Optimization



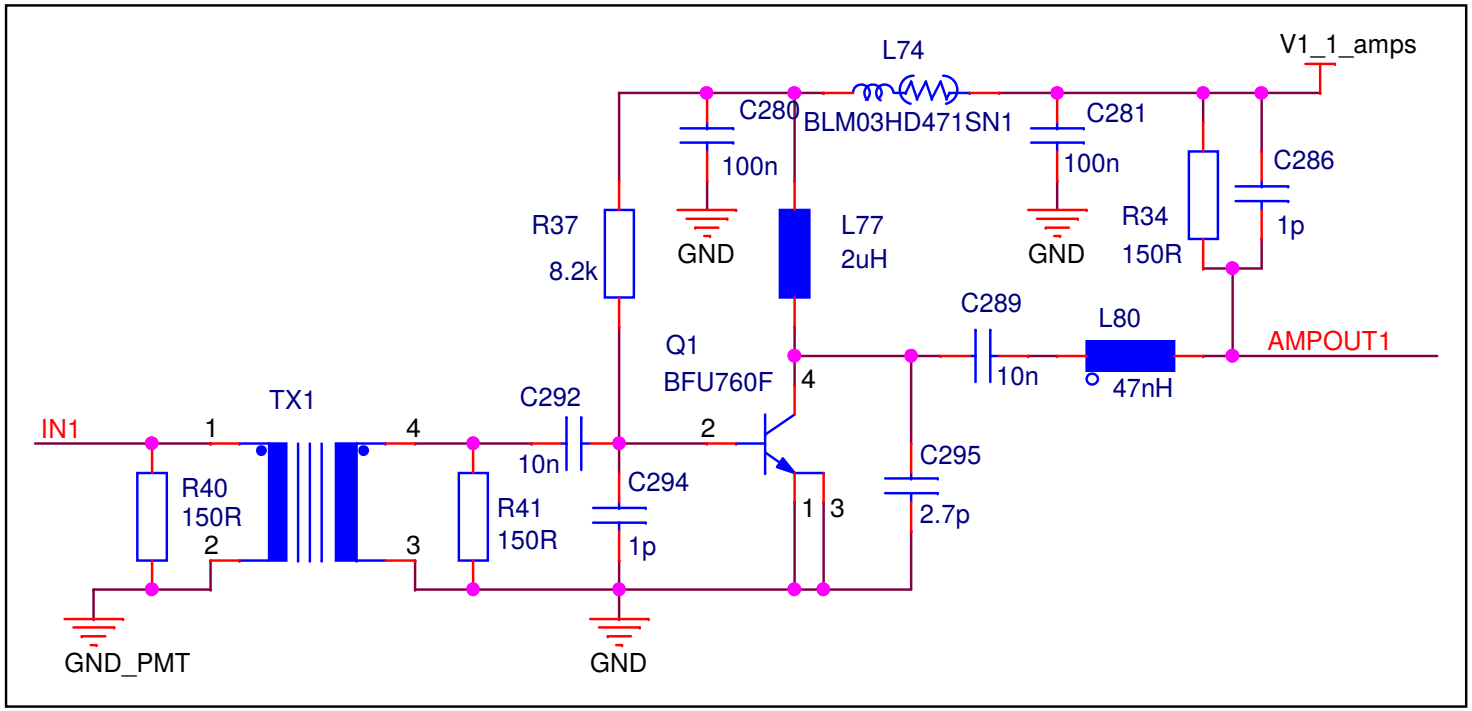
DiRICH concept



DiRICH Requirements and Design Consequences

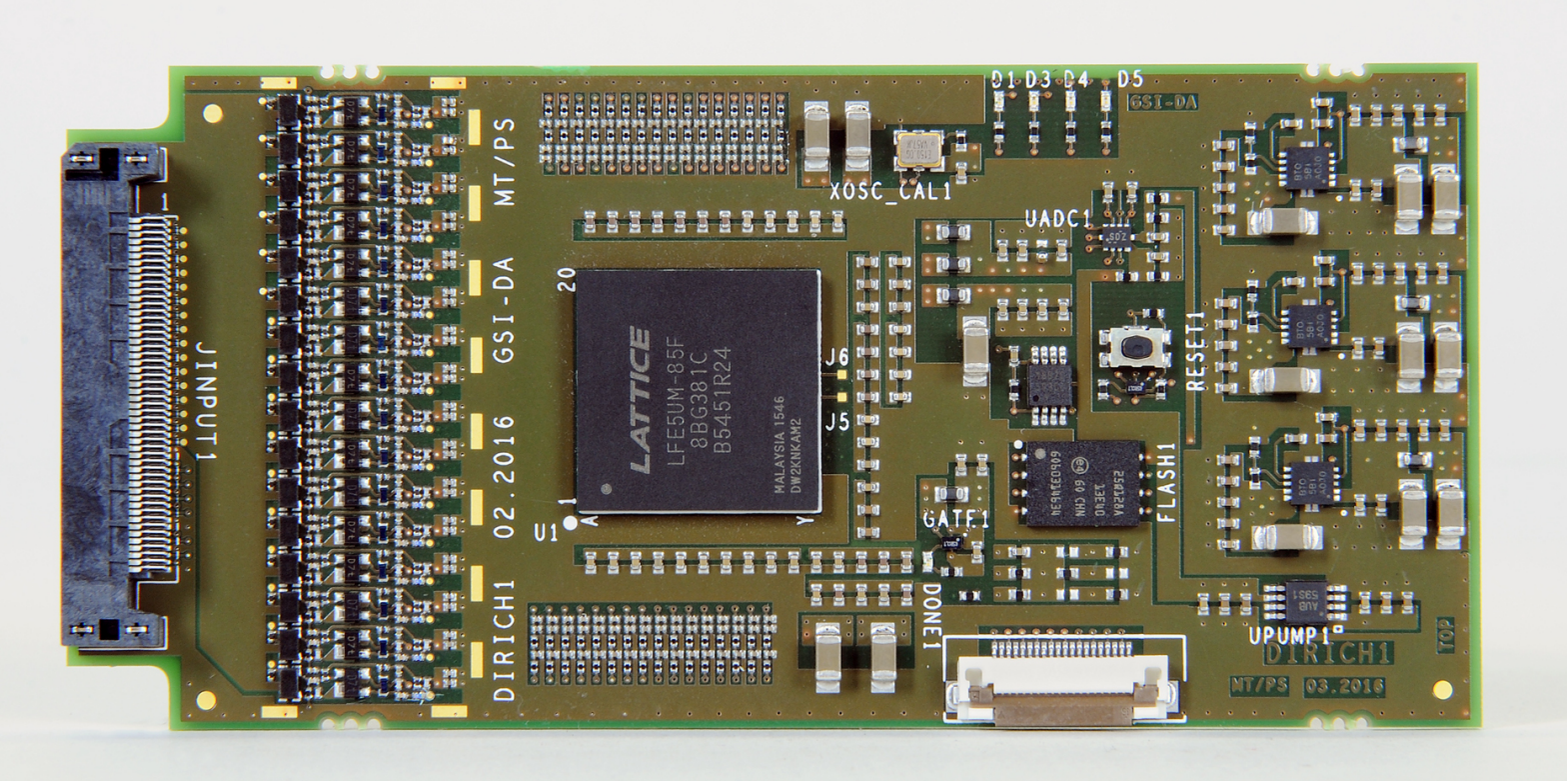
- FEE module for 32 channels
- Amplification, Discrimination, TDC + DAQ
- "no" cables
- analog input signals and digital output signals (serial transmission) over the same connector
- low power consumption
- only possible with newest FPGAs (price/performance) and very high pin-count connectors
- galvanically isolate PMT from FEE with transformers
  - reduces issues with HV-power-supply GND connection

DiRICH: Amplifier Schematics



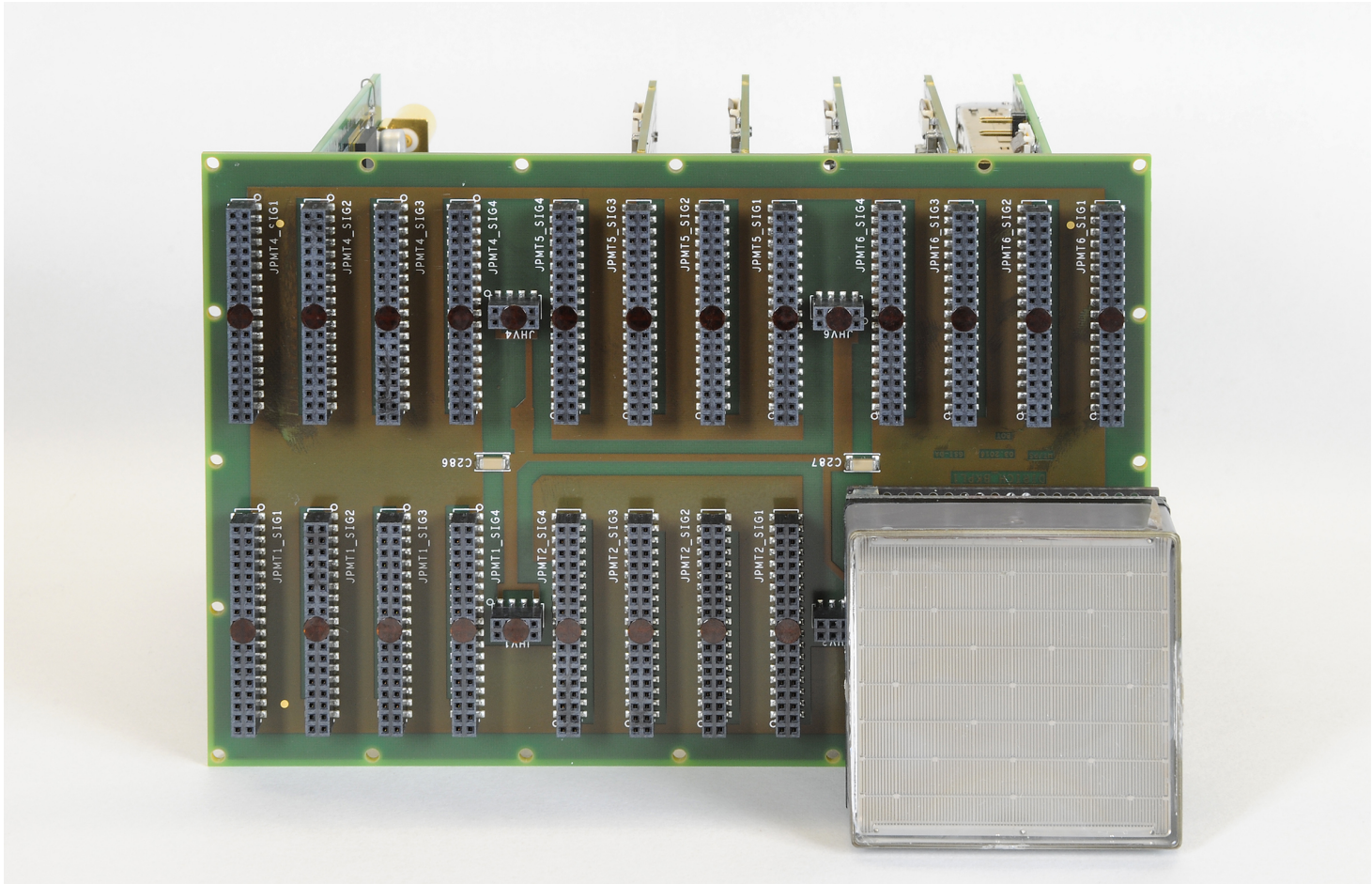
- BFU760F: fast transistor (40 GHz transition freq.)
- low power consumption: 12mW
- high gain: $\sim$30
- simple (no specific higher order shaping)

DiRICH: Put to Reality



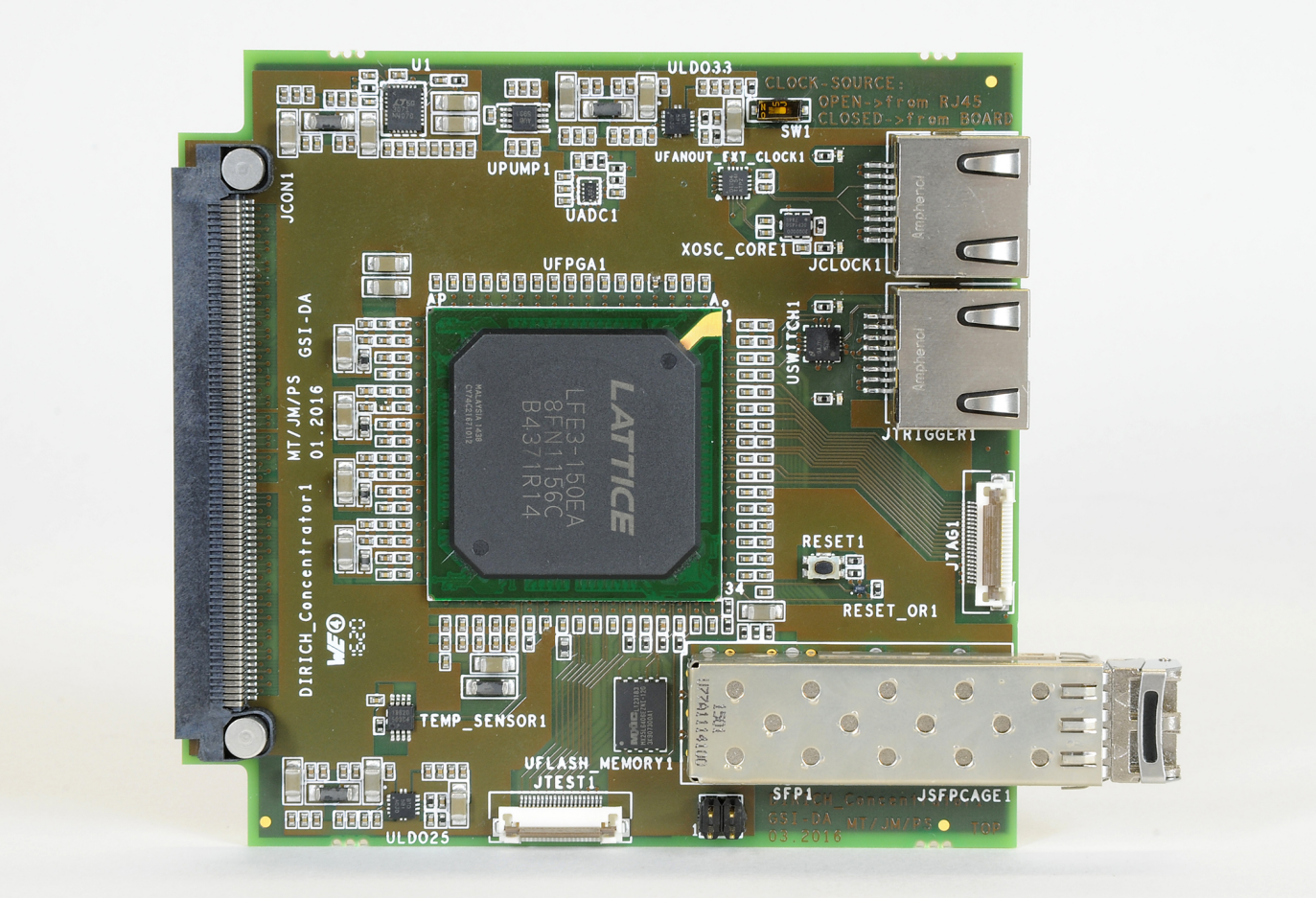
- 47mm x 100mm area, 300μm x 600μm components, 0201
- transformer, gain 30 amps, 16bit-DAC, discriminator, high precision TDC, DAQ + TrbNet (2Gbit/s SERDES), slow-control and voltage-regulation

DiRICH: Backplane



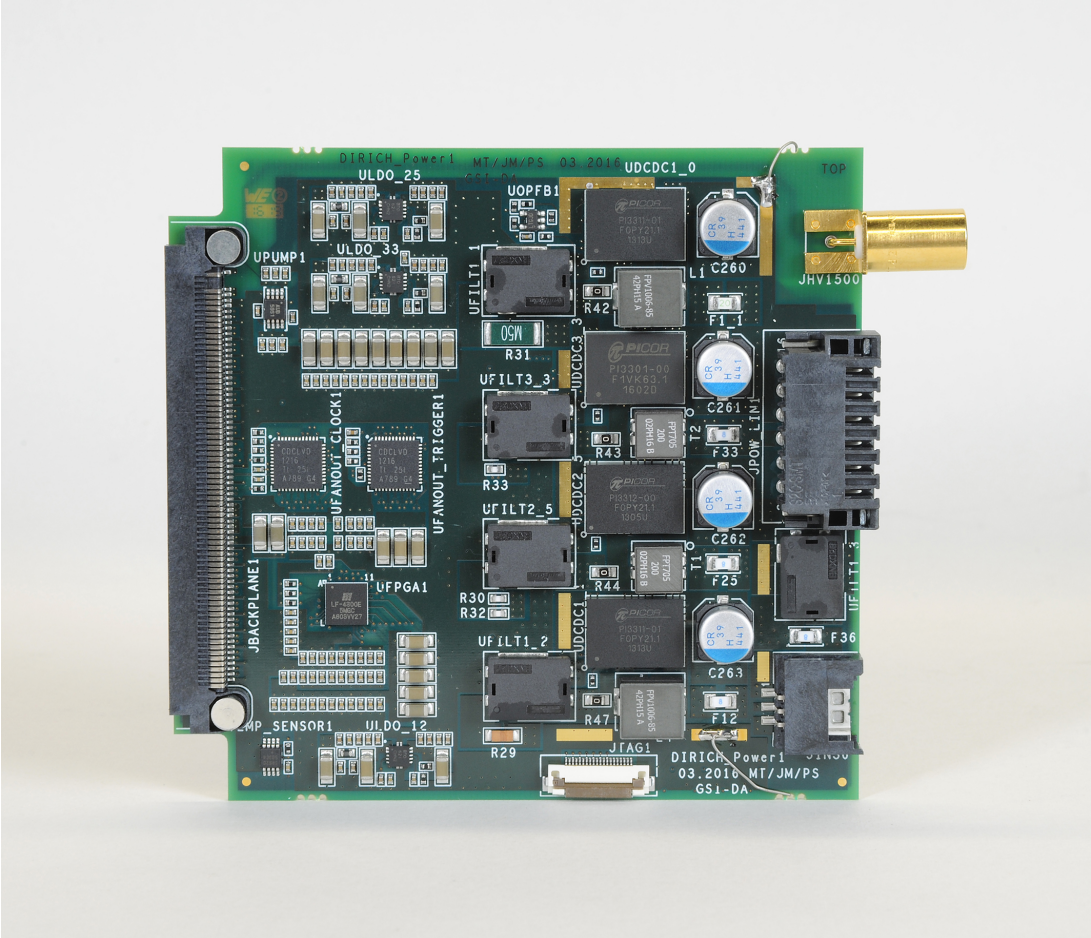
- Backplane with 12 DiRICH, 6 MA-PMTs (384 channels)
- real challenge in layout, 14 layers with stacked microvias.

DiRICH: Concentrator



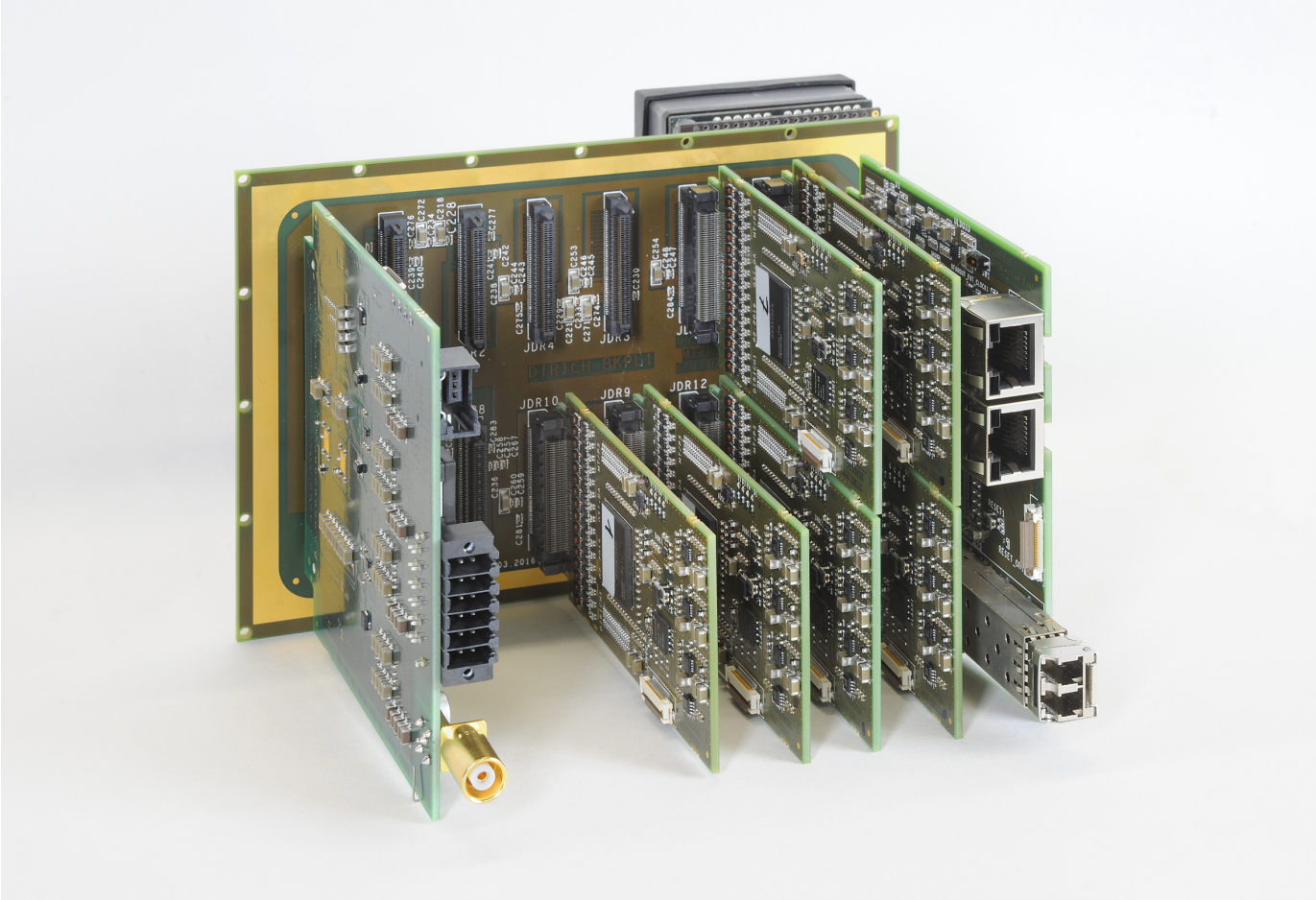
- Concentrator module: aggregates 12 TrbNet links to 1 TrbNet link

DiRICH: Power



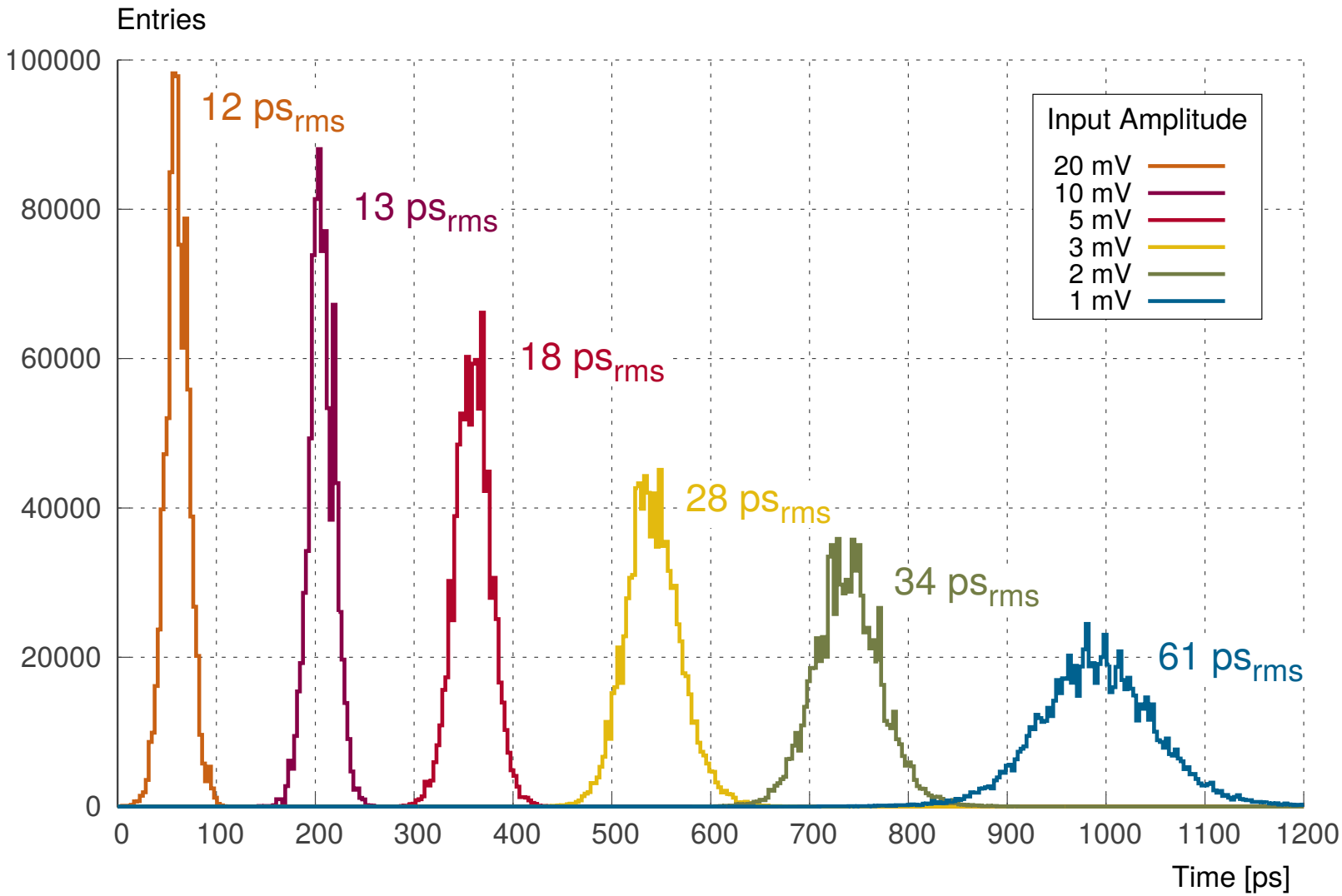
- Power module (both, DC/DC and Linear) + HV + Clock + Trigger-Distribution

DiRICH: System

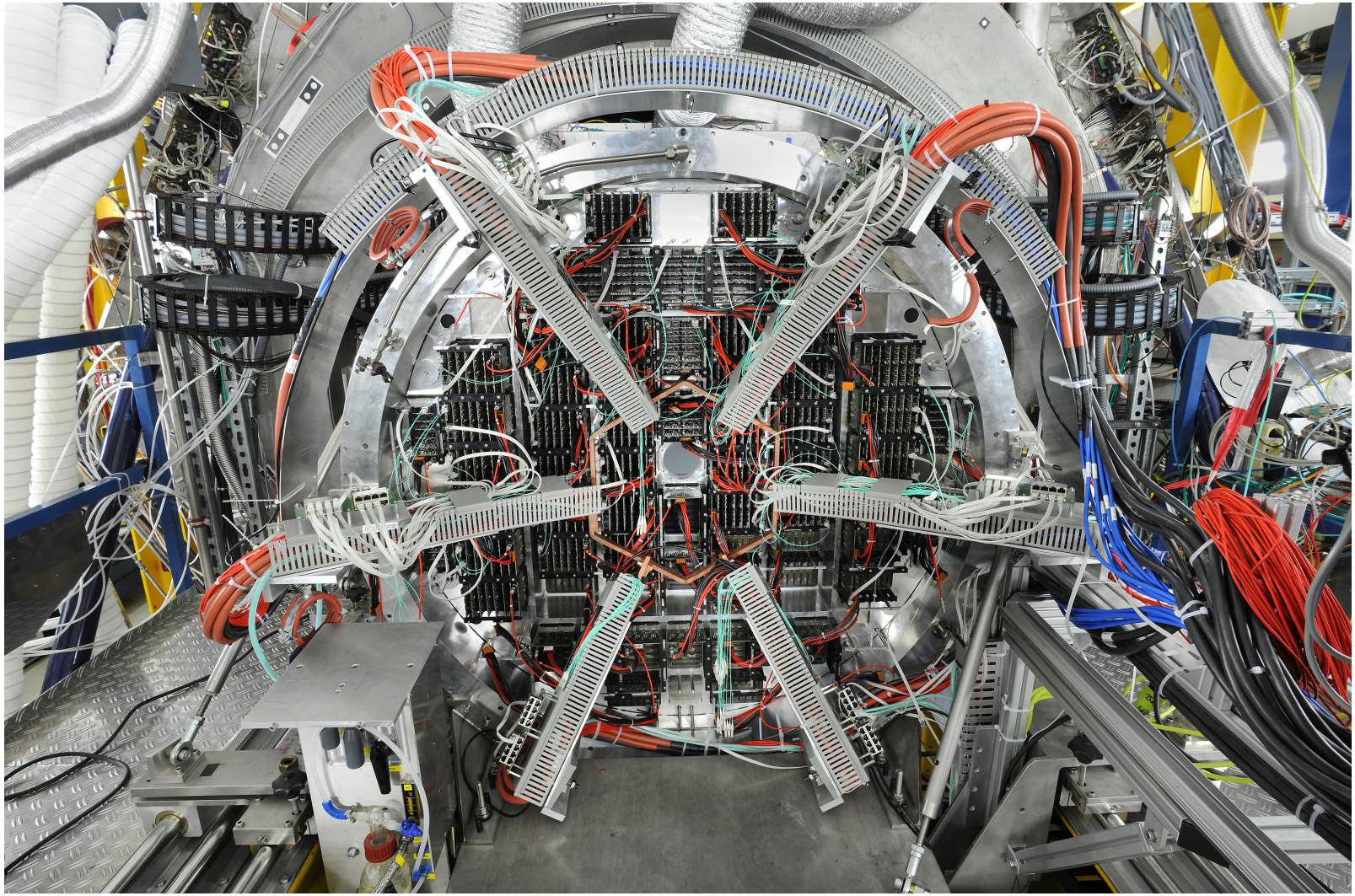


- All DiRICH photos by Gabi Otto @GSI
- All fits in :-) How does it perform ?

Timing Performance in the Lab



HADES RICH Detector



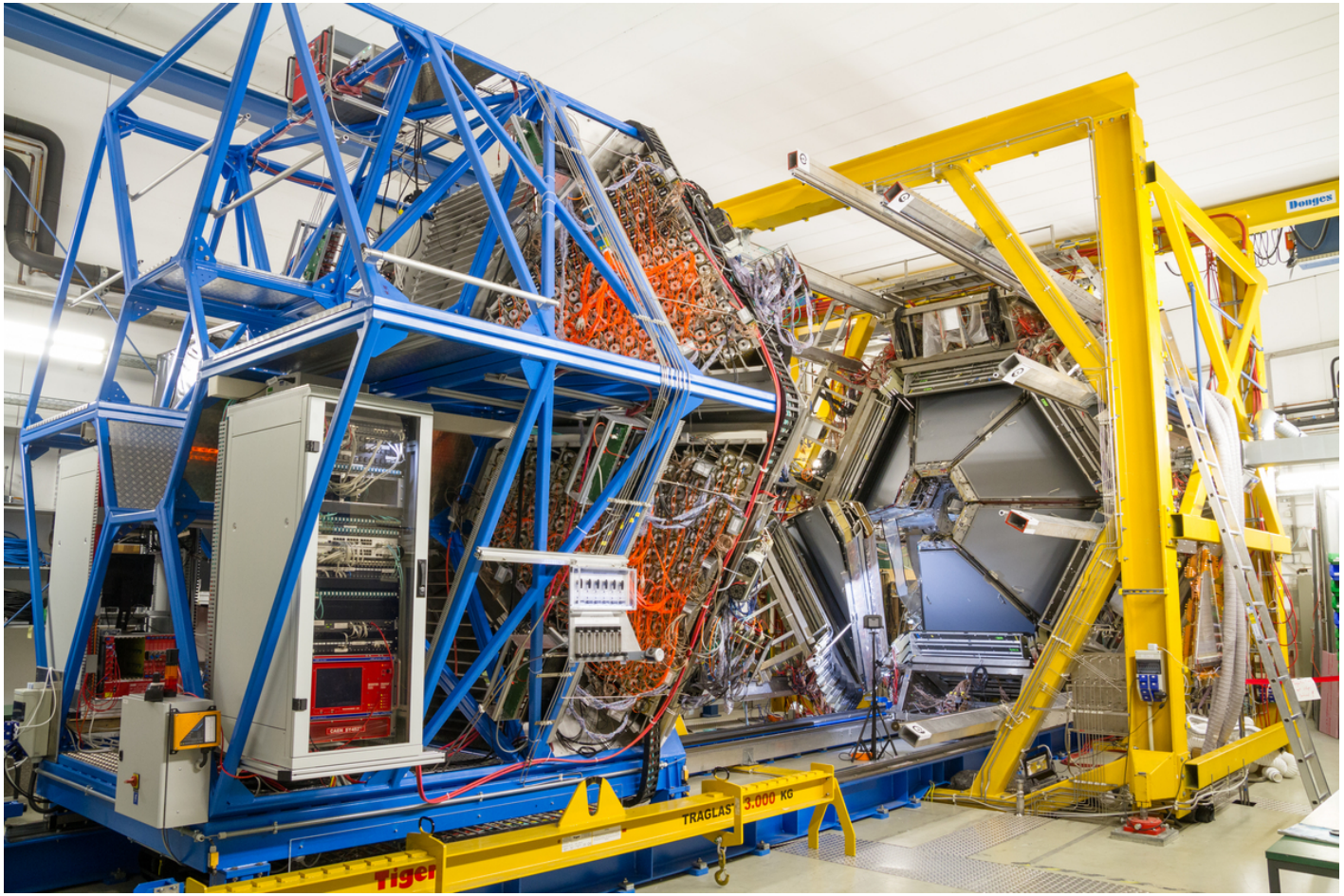
Live view of running experiment:

http://web-docs.gsi.de/~webhades/onlineMon/mar19/hades-online.html

Summary

- The TRB (with its associated FPGA-TDC + DAQ) is a mature platform (hardware and software) useful for many applications
  - Collaboration takes care of constant development and maintenance
- based on the "come-and-kiss" principle
  - no hard to acquire ASICs used
  - due to modern commercial components (small, less power) now closer to the ASIC domain
- limitations for larger systems
  - cable-hell and noise
- larger application specific systems: need to optimize
  - hard and software is "easy" to adapt to special applications
- MA-PMT and MCP-PMT applications are quite common and we can share the achievements and effort

Summary II



- The HADES detector uses only TDCs for analog to digital conversion. Including the Electromagnetic Calorimeter.

Thank you for your attention!