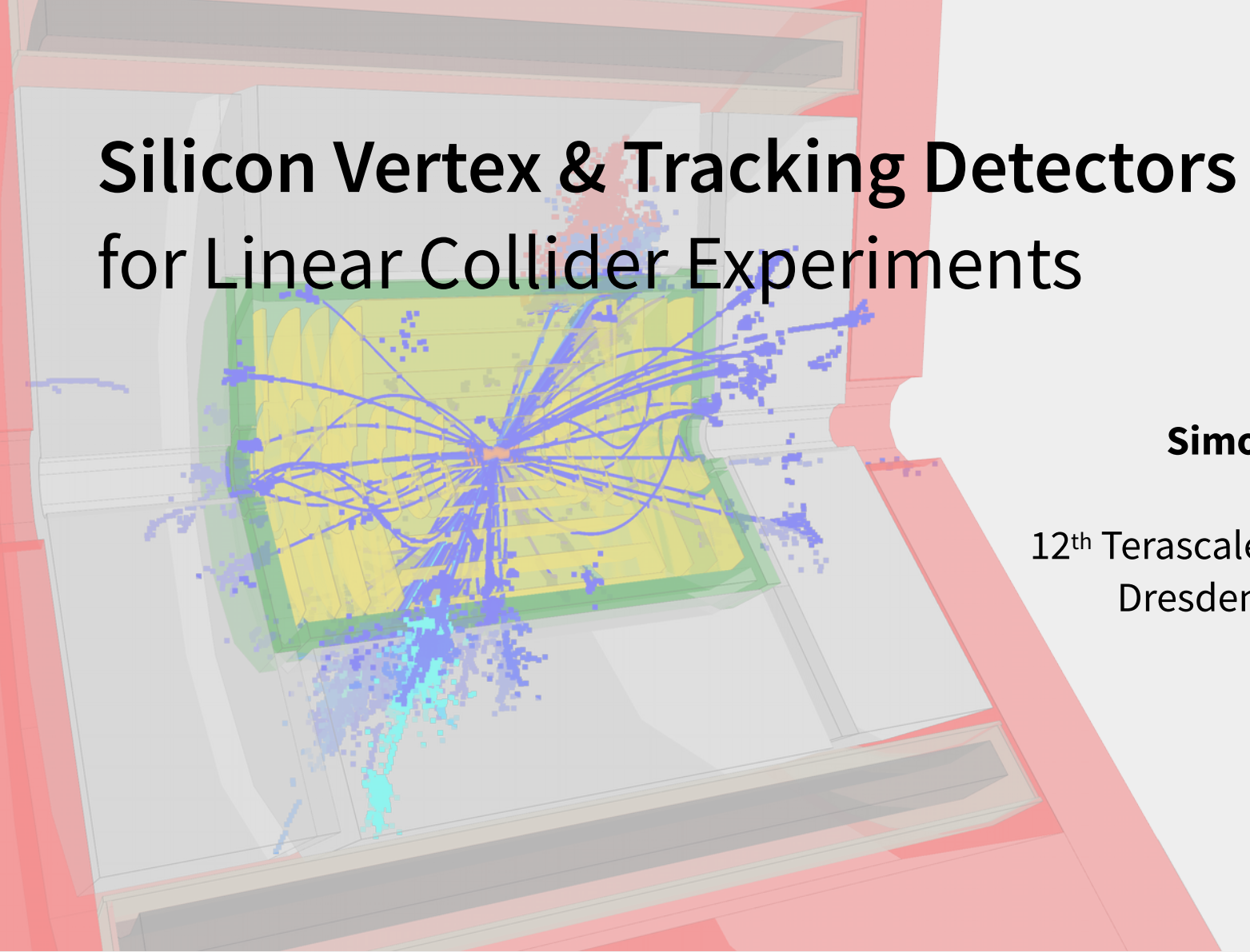
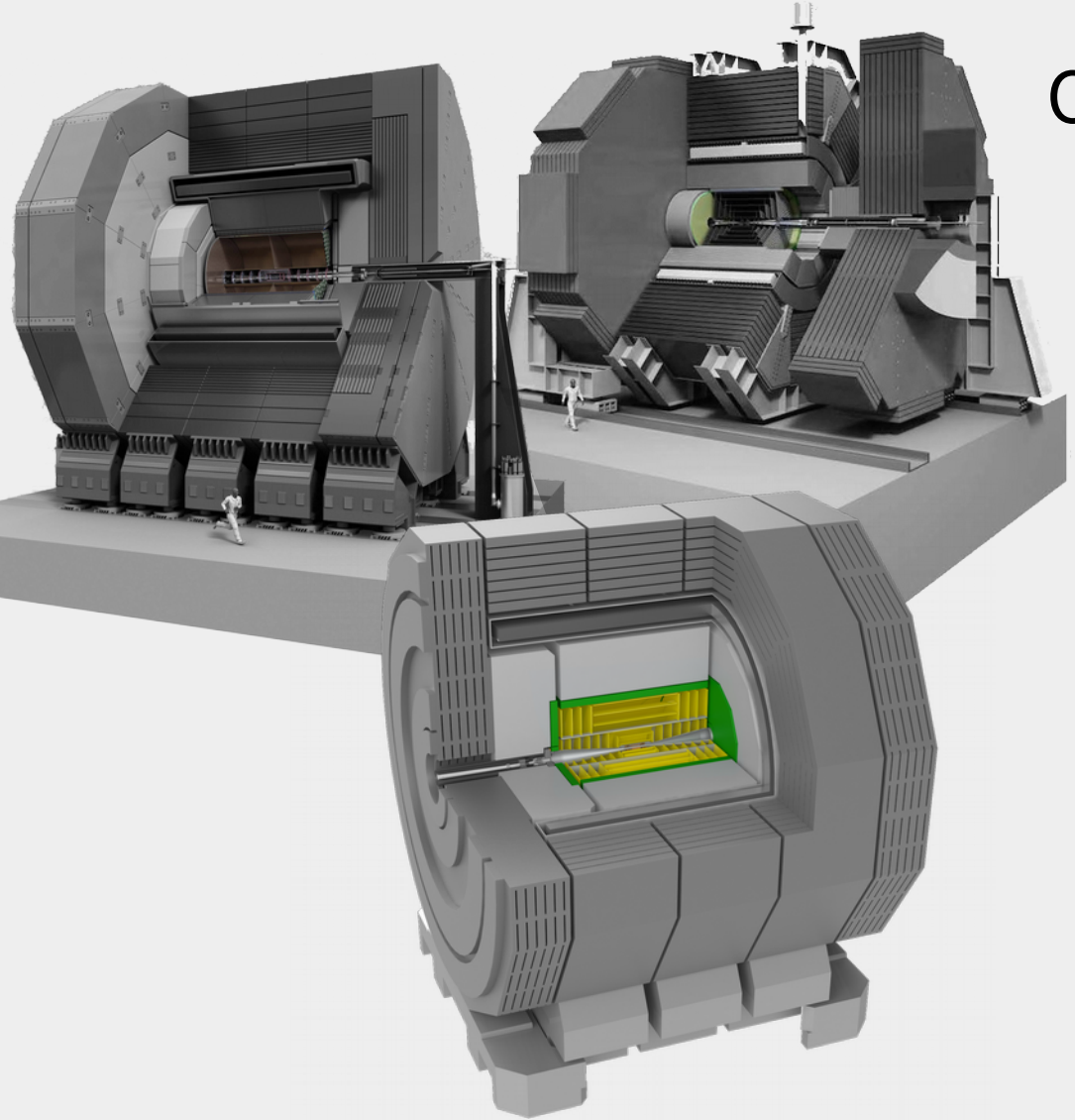
http://clicdp.cern.ch



Silicon Vertex & Tracking Detectors
for Linear Collider Experiments

Simon Spannagel, CERN

12th Terascale Detector Workshop
Dresden, 12 – 15 March 2019



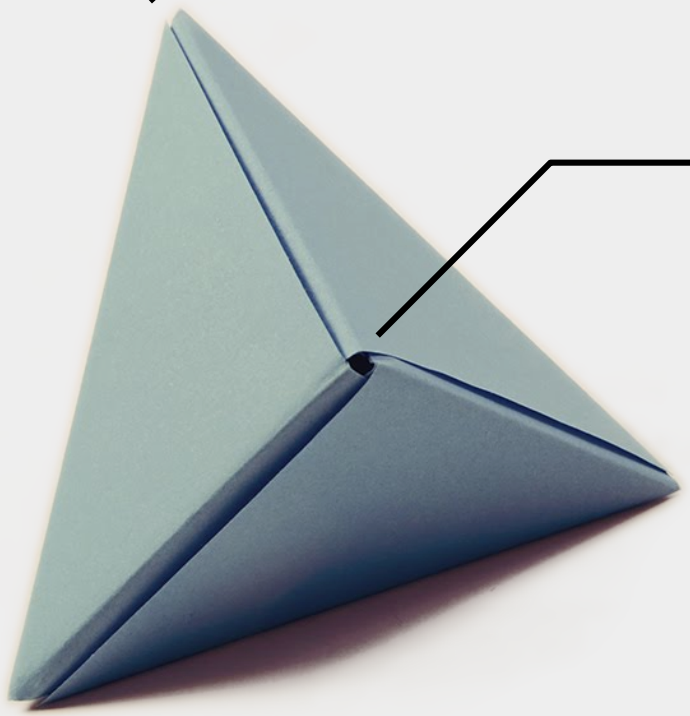
Outline

- Challenges & Requirements
- Tracking Detector Concepts
- Silicon Technologies
- Mechanics & Cooling
- R&D Tools

Challenges for Silicon Detectors

Material Budget

Radiation Hardness



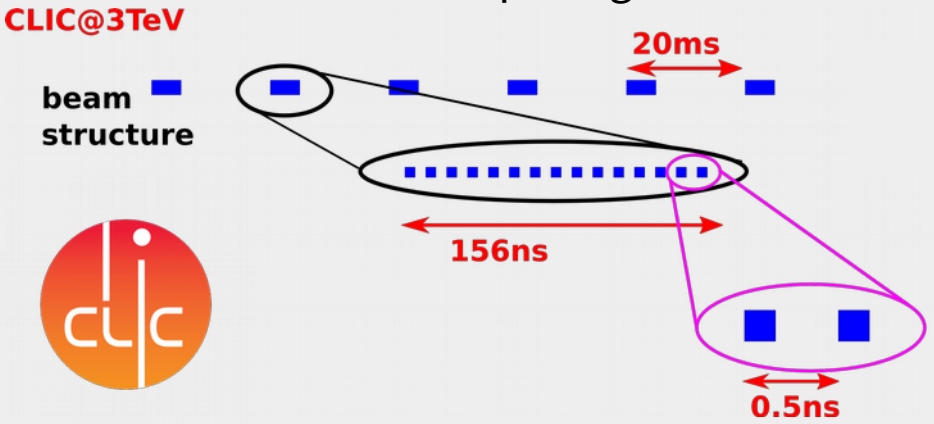
Readout Speed &
Power Consumption

Resolution &
Granularity

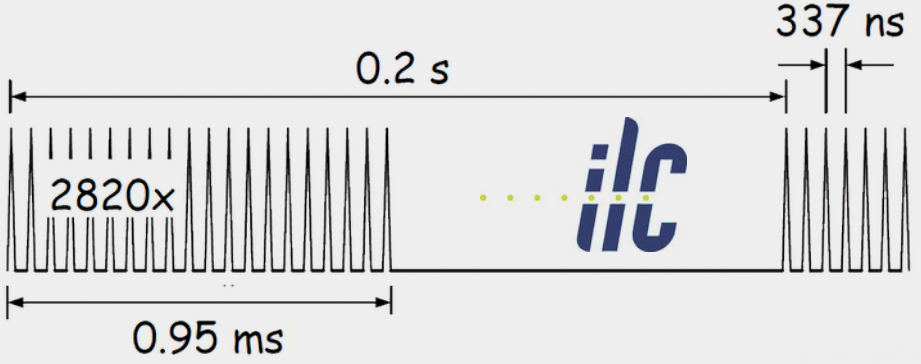
Beam Structure

- Linear colliders operate in bunch trains
  - Low duty cycle: trigger-less, frame-based readout architecture
  - Possibility for power pulsing:
    switch detector components off between trains to reduce heat dissipation

CLIC: 312 bunches **(156 ns)**, 50 Hz rep. rate
0.5 ns bunch spacing

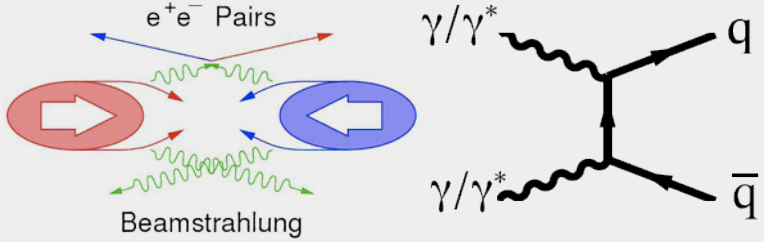


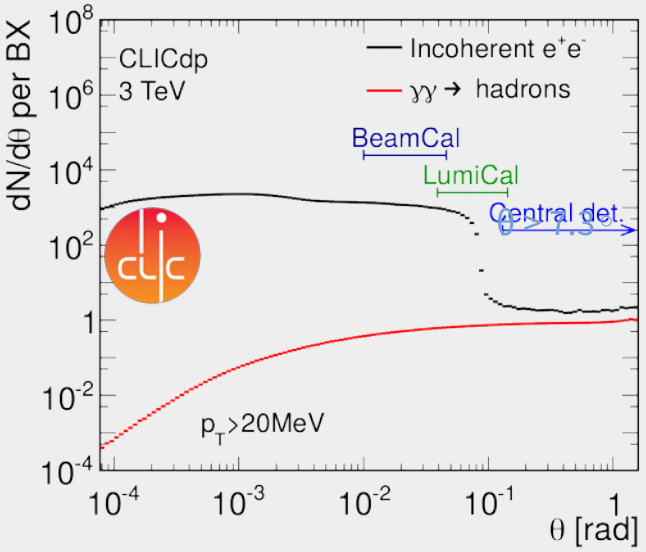
ILC: 2820 bunches **(~1 ms)**, 5 Hz repetition rate
337 ns bunch spacing



Beam-induced Backgrounds

- High luminosity achieved by small beams
  - CLIC (3 TeV): **40 nm** (x) x **1 nm** (y)
  - ILC (500 GeV): **500 nm** (x) x **5 nm** (y)
  - Resulting high e-field leads to beam-beam interactions
- Generates background particles, reduces √s

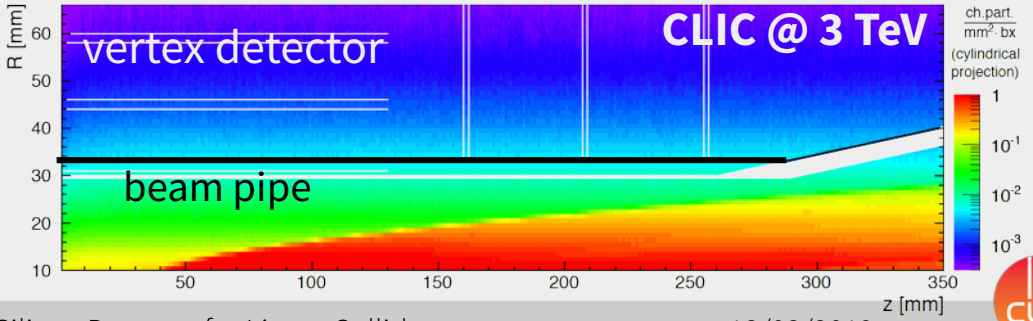




Fluence at first vertex layer **< 10^{11} n_{eq} / cm^2**

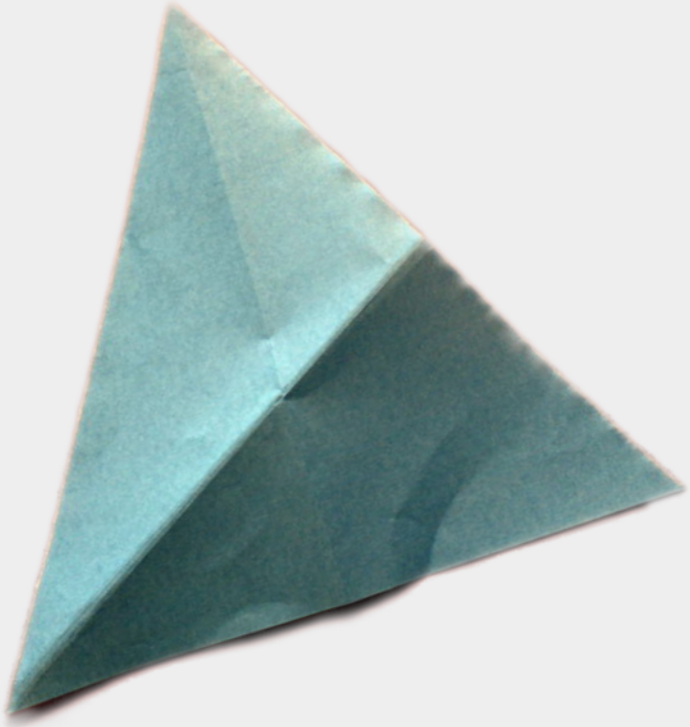
Main backgrounds in detector acceptance:

- **Incoherent e + e − pairs:** high occupancies → granularity
- **γγ → hadrons:** impact on granularity, layout, physics



Challenges for Silicon Detectors *at Linear Colliders*

Material Budget

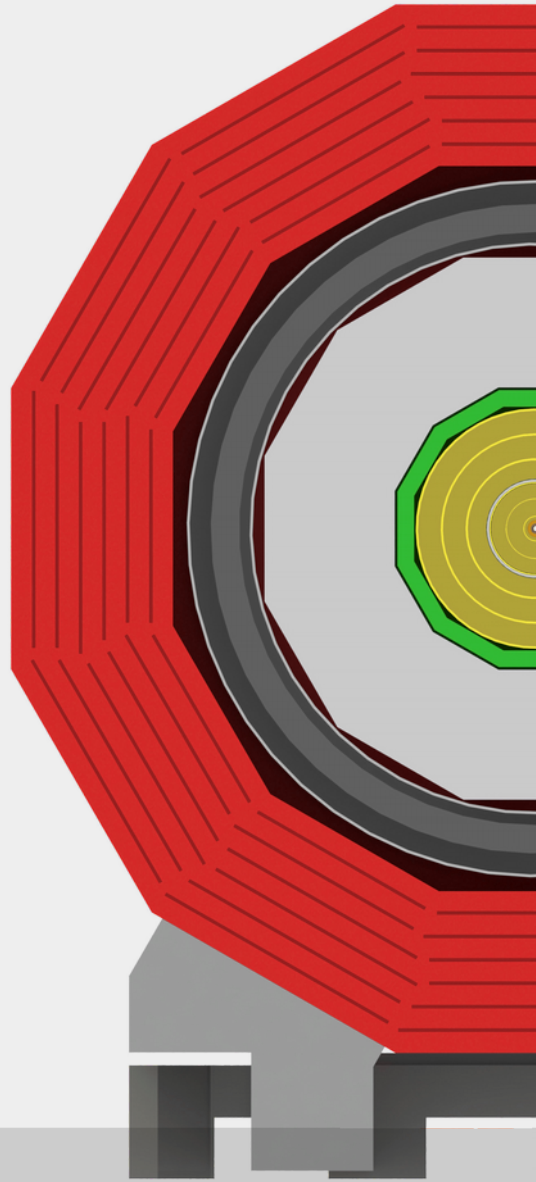


Radiation Hardness

Readout Speed &
Power Consumption

Resolution &
Granularity

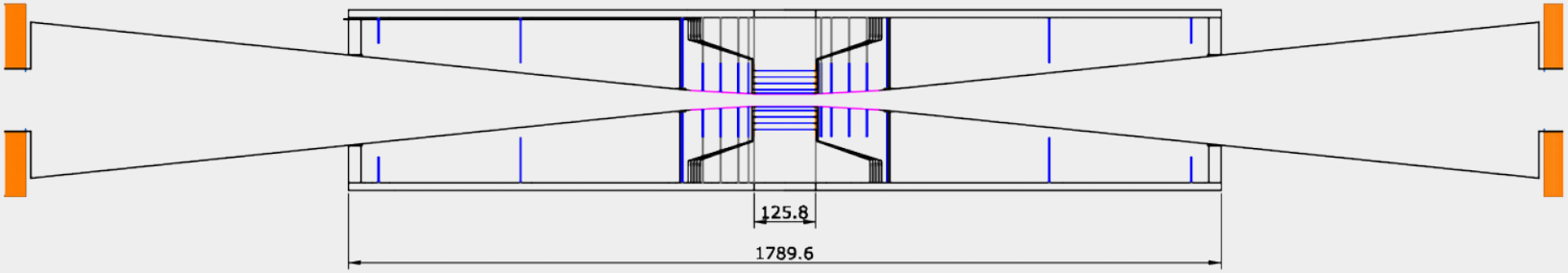
Vertex & Tracking Detector Concepts
for Experiments at ILC and CLIC



Requirements – Comparison

	Linear Collider	(HL-) LHC (ATLAS/CMS)
Radiation Tolerance	• **< 10^{11} n_{eq} / cm^2** (vertex)	• O(10^{16} n_{eq} / cm^2) (vertex)
Material Budget (barrel)	• **1 – 2% X_0** (vertex) **10 – 15% X_0** (tracker)	• 10 – 15% X_0 (vertex) 30 – 40% X_0 (tracker)
Single-point Resolution	• **≤ 3 µm – 7 µm**	• 5 µm – 30 µm
Time Resolution	• **5 ns (CLIC)** / 0.3 µs (ILC)	• 25 ns (1 BC)
Tracking Acceptance	• $\|\eta\| \approx 2.7$	• $\|\eta\| \approx 4$
Min. Granularity	• **≤ 25 µm x 25 µm**	• 50 µm x 50 µm
Active Area	• ~1 m^2 / ~200 m^2	• ~1 m^2 / ~200 m^2

SiD Vertex Detector



Requirements

- **Low mass**
  < 0.3% X_0 per layer
- **Low power consumption**
  13 mW/cm^{-2}
- **High single-point resolution**
  σ_{SP} ~ 5 µm
- **1-bunch time stamping** ~ 0.3 µs

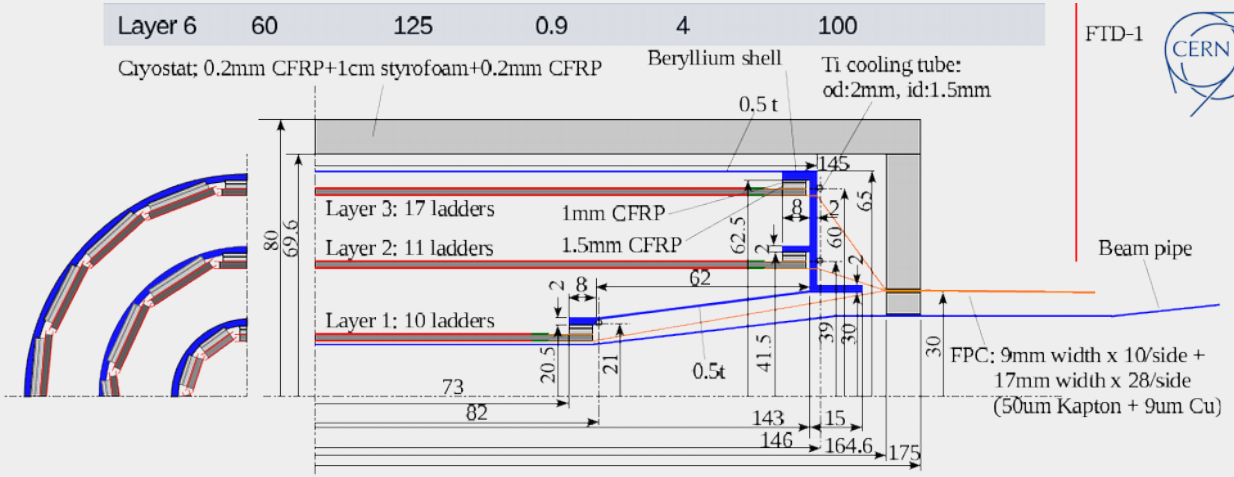
Current design:

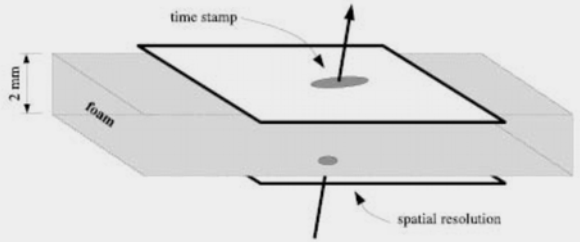
- "Short barrel" approach:
  - 5 barrel layers,
  - 4 disks at short distance
  - 3 disks at longer distance
- Pixels pitch: 20 x 20 µm^2
- CMOS based detectors with timestamps

ILD Vertex Detector

Requirements

- **Low mass**
  0.3% X_0 per double-layer
- **Low power consumption**
  to minimize material budget
- **High single-point resolution**
  σ_{SP} ~ 3 µm
- **Readout time** ~ 50 µs – 100 µs

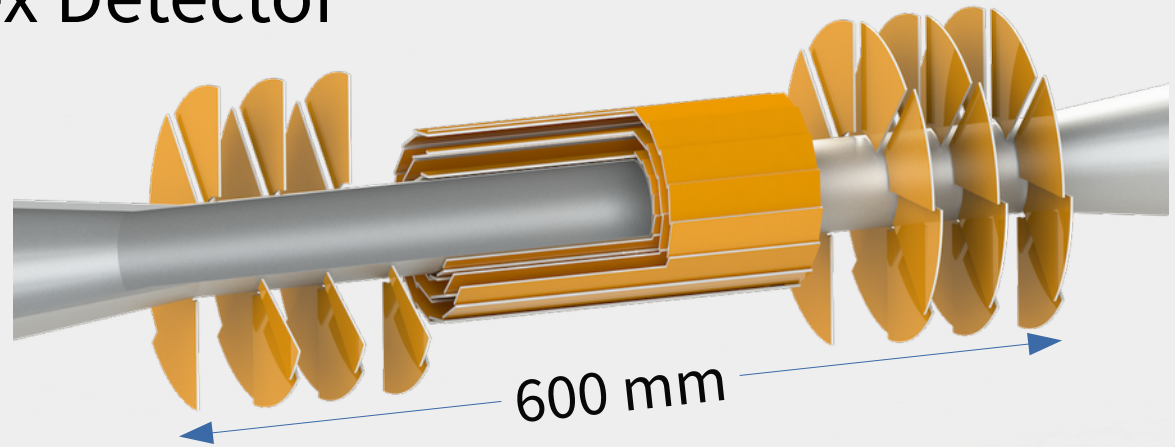




Current design:

- "Long Barrel": 3 double sided ladders
- Layers 1 & 2: focus on resolution
  - Small pixels: 17 x 17 / 33 µm²
- Layer 3-6: focus on low power consumption
  - Large pixels: 25 / 35 x 35 µm²
- FTD: 7 forward disk for extended coverage
- Technologies: MIMOSA / DEPFET / FPCCD / SOI

CLICdet Vertex Detector



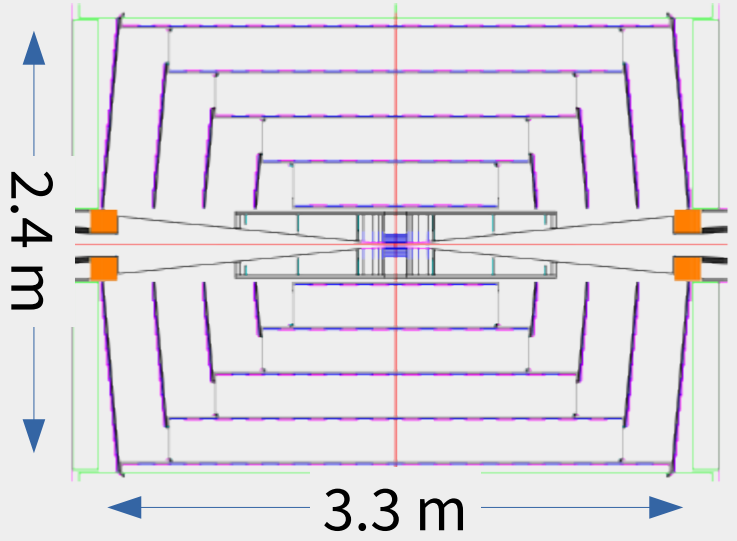
Requirements

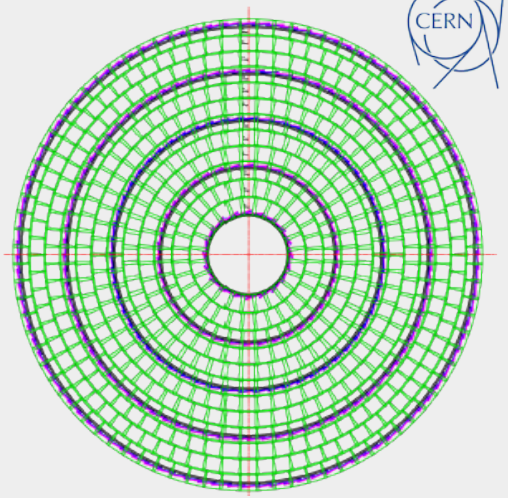
- **Low mass**
  0.2% X_0 per double-layer
- **Low power consumption**
  50 mW/cm^{-2}
- **High single-point resolution**
  σ_{SP} ~ 3 µm
- **Precise time stamping** ~ 5 ns

Current design:

- Hybrid pixel detectors in double layers
- 50+50 µm sensor+ASIC, 25 µm pitch
- Surface area of ~ 0.84 m^2
- Three barrel layers, 2x three spiral disks

SiD Tracking Detector





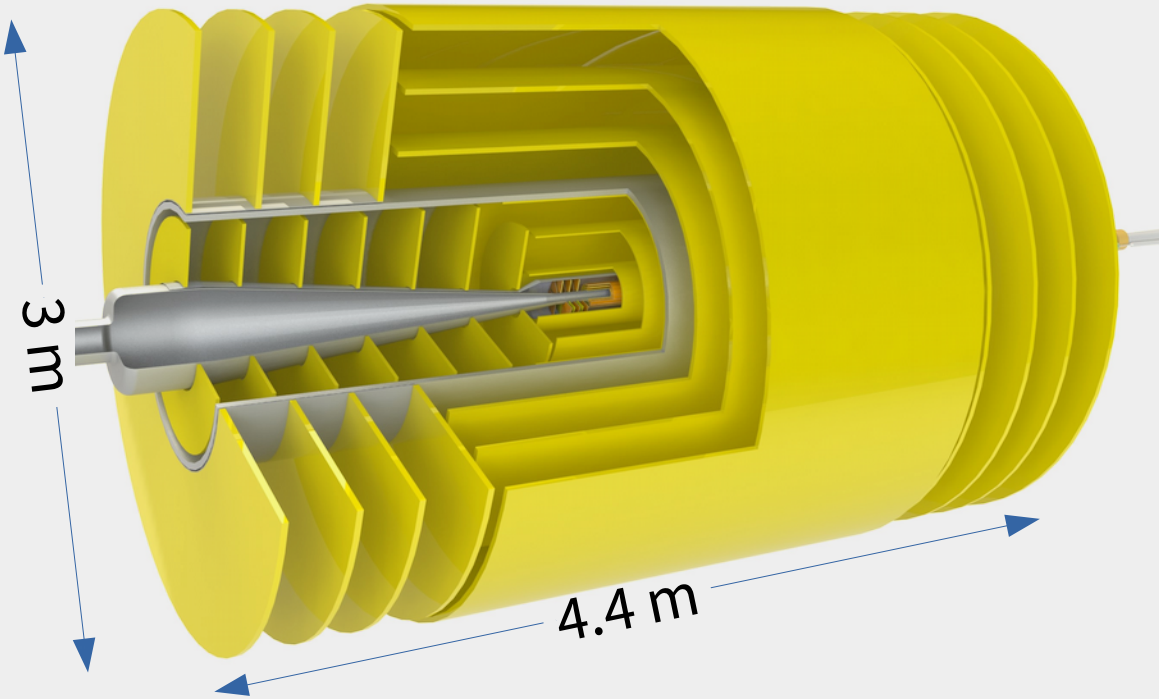
Requirements

- **Low mass**
  < 20% X_0 in the active region
- **High single-point resolution**
  σ_{SP} ~ 10 µm
- **Good momentum resolution**
  σ_{pT}/p_T ~ 2 – 5 × 10^{-5} GeV^{-1}
- **1-bunch time resolution** ~ 300 ns

Current design:

- Single-sided micro-strips, 25 µm pitch, alternate strip readout: KPiX ASIC
- Bump-bonded directly to the module
- 5 barrel layers / 4 disks, gas-cooled

CLICdet Tracking Detector



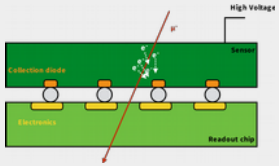
Requirements

- **Low mass, high rigidity**
  1 – 2% X_0 per layer
- **Good single-point resolution**
  $\sigma_{SP} \sim 7$ µm
- **Good momentum resolution**
  $\sigma_{pT}/p_T \sim 2 \times 10^{-5}$ GeV^{-1}
- **High granularity**
  few % occupancy from backgrounds

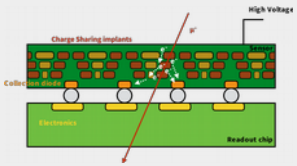
Current design:

- Monolithic detector with (elongated) pixels
- 200 µm sensor, including electronics
- Surface area of approx. 140 m^2
- Leakless water cooling

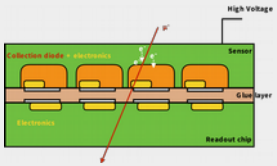
Silicon Technologies
for Vertex & Tracking Detectors



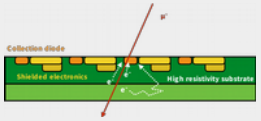
Hybrid



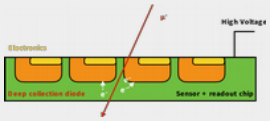
ELAD



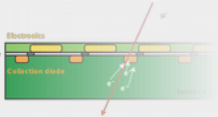
Capacitive



HR-CMOS



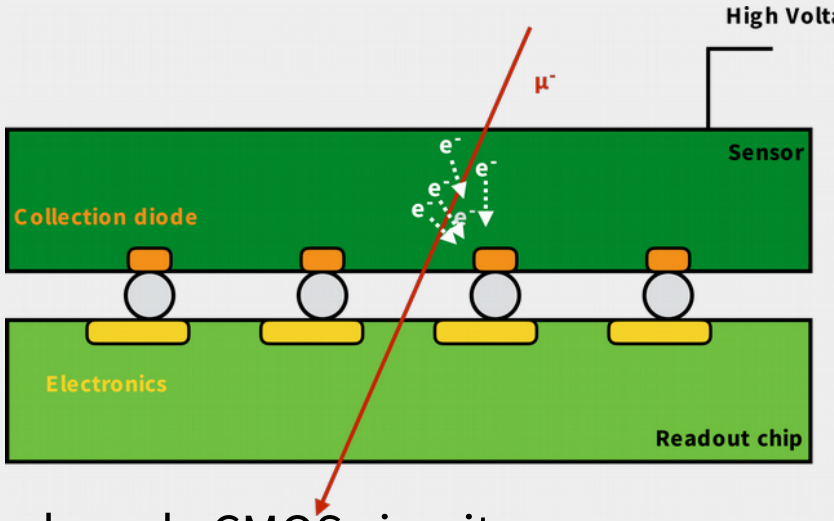
HV-CMOS



SOI

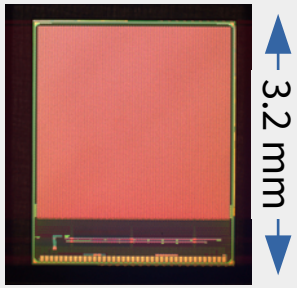
• • •

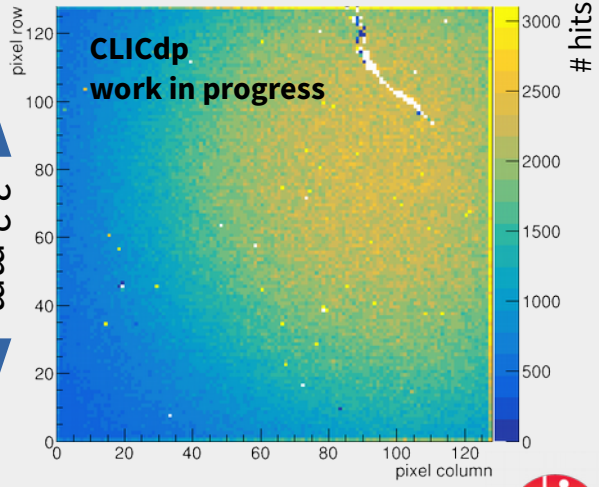
Hybrid Pixel Detectors



- Traditional design of HEP silicon pixel detectors with independent parts:
  - Sensor (high-resistivity silicon & pn-junction)
  - CMOS chip, interconnect: solder bumps
- Allows extensive functionality on-pixel using mixed-mode CMOS circuits

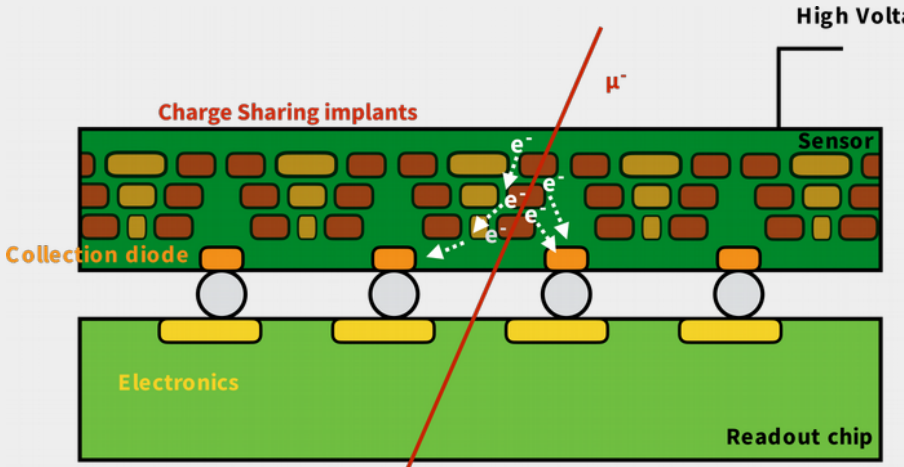
- **CLICpix2 Prototype**, per-pixel charge & arrival time
  - 65nm CMOS, 25 x 25 μm² pitch, power pulsing
  - Successfully tested in lab & test beam
  - Challenge: bump bonding with 25μm pitch
  - Challenge: achieve 3 μm resolution with 50 μm sensors

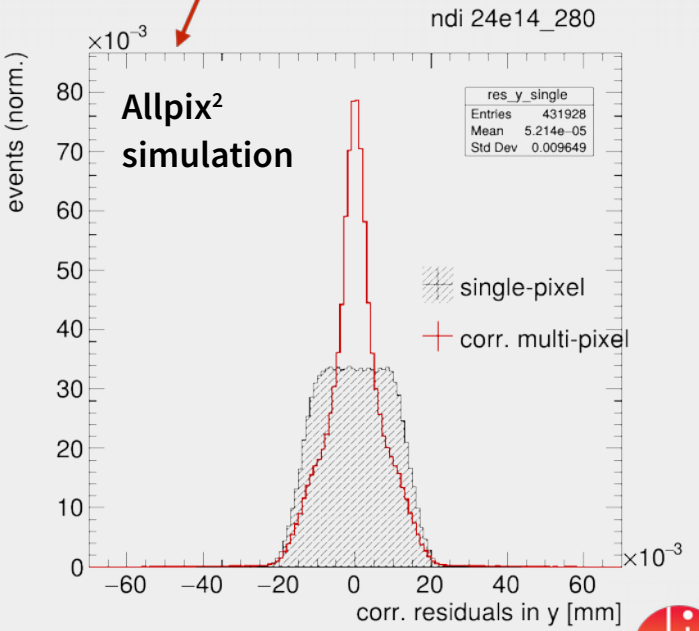




Enhanced Lateral Drift Detectors

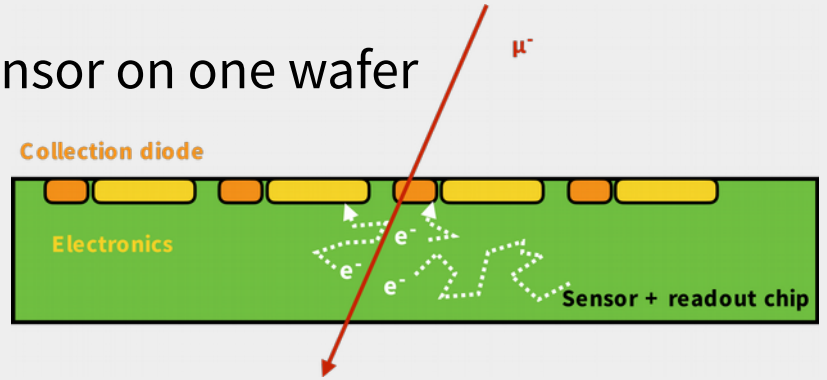
- Position resolution in **thin sensors** limited to pitch / √12 (almost no charge sharing)
- New concept: **enhance charge sharing**
  Enhanced LAteral Drift sensors (ELAD)
  - Close to theoretical optimum: linear charge sharing
- Deep implants to alter field, improve resolution
  - Lateral spread of charges during drift, cluster size ~2
- Challenges:
  - Complex production process, adds cost
  - Have to avoid low-field regions (recombination)
- Simulations: implantation process, sensor performance

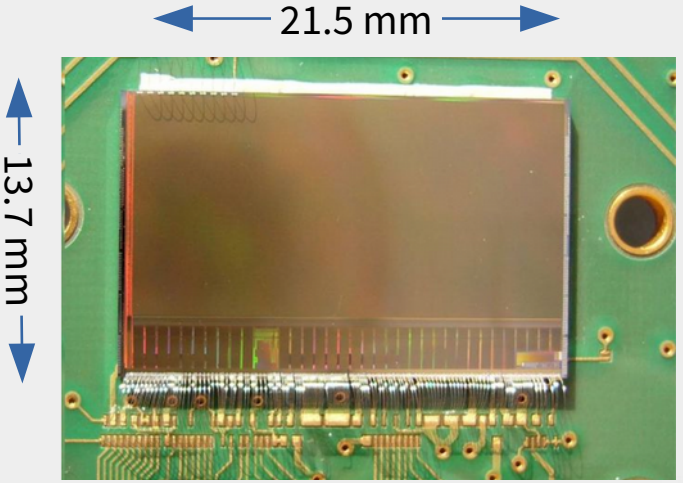




Monolithic Active Pixel Sensors

- Fully integrated Si detector - electronics & sensor on one wafer
  - Low material budget, no bump-bonding
- MIMOSA26 – ILC vertex detector studies
  - 18.4 µm x 18.4 µm pitch, binary readout
  - Well known from beam telescopes...





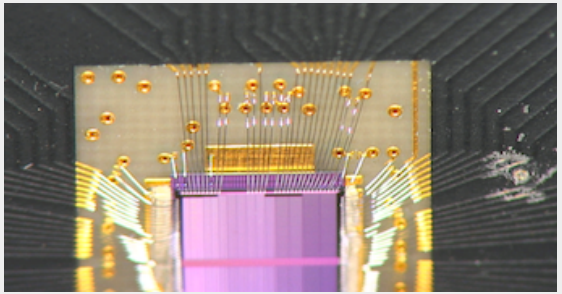
Monolithic High-Resistivity CMOS Sensors

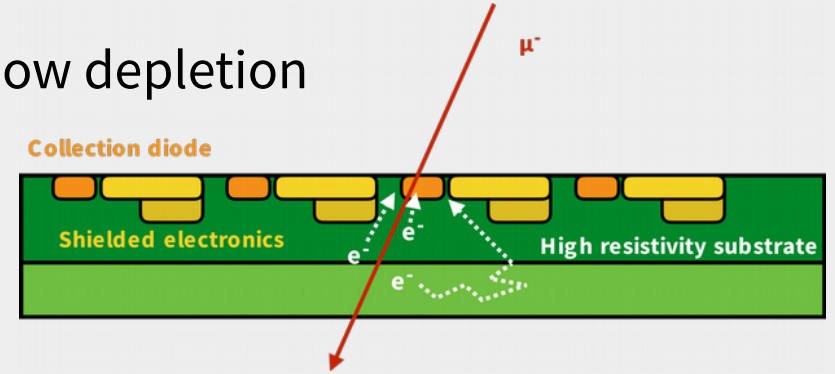
- Introduce high-resistivity epitaxial layer to allow depletion
- Electronics outside charge-collection well
  - Small collection diode, small capacitance
  - Challenge: effect of p-wells on charge collection / electric field
- Analog performance: **ALICE Investigator** chip
  - Good spatial & time resolution at very low threshold at 28 x 28 µm² pitch:

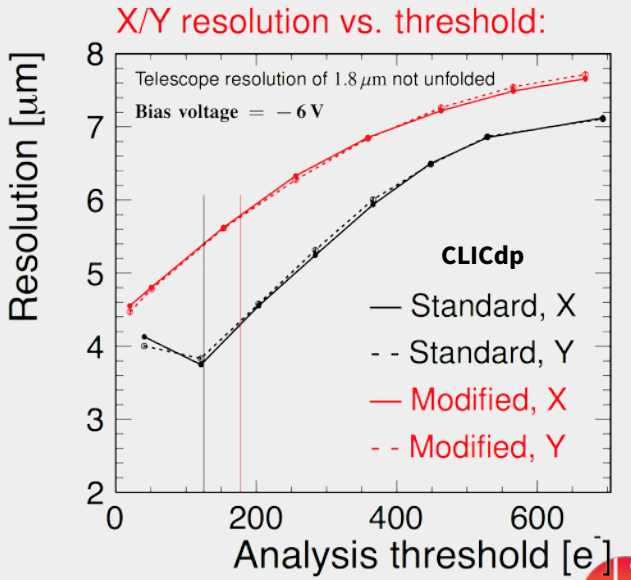
    Efficiency > 99.3%

    Time resolution $\sigma_t < 5$ ns

    Spatial resolution σ_{SP} ~4 µm



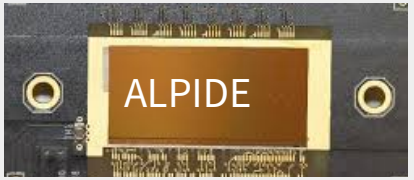




ALPIDE, MIMOSIS, PSIRA, CLICTD

Many fully-integrated sensors in this **180nm** technology:

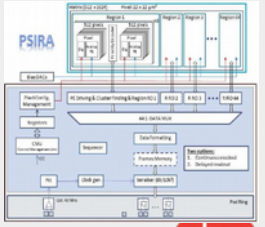
- **ALPIDE**: Sensor for the ALICE ITS upgrade **production**
  - First large-area MAPS detector @ LHC, 29 µm x 27 µm pitch



- **MIMOSIS**: Sensor for CBM @ FAIR **prototypes**
  - 30 µm x 27 µm pitch, data-driven readout, ~ 10^8 hits / cm^2 / s

- **CLICTD**: Sensor for CLIC Tracking Detector **submitted to foundry**
  - 300 µm x 30 µm pixels with 8-bit ToA and 5-bit ToT, few ns time resolution
  - Analog domain divided in 8 sub-pixels for prompt charge collection

- **PSIRA**: Sensor concept for ILD Vertex detector **design phase**
  - Evolution of MIMOSIS design: better resolution, faster readout



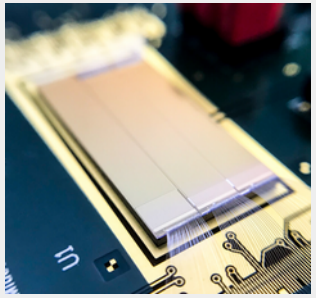
Monolithic High-Voltage CMOS Sensors

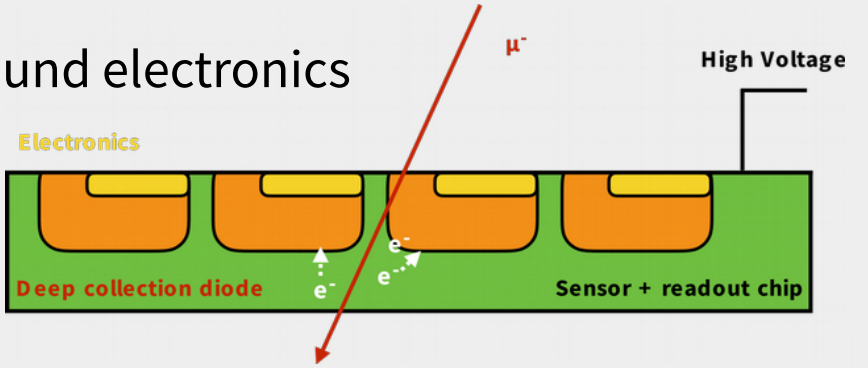
- Shield electronics via deep collection diode around electronics
  - Allows high bias voltage to be applied:
    Fast & large signal, large depletion volume
- Challenge: large collection diode leads to
  - large input capacitance
  - increased power consumption
- Prototype: **ATLASpix** (MuPix8 on same reticle)
  - **180nm**, 130µm x 40µm pixel pitch

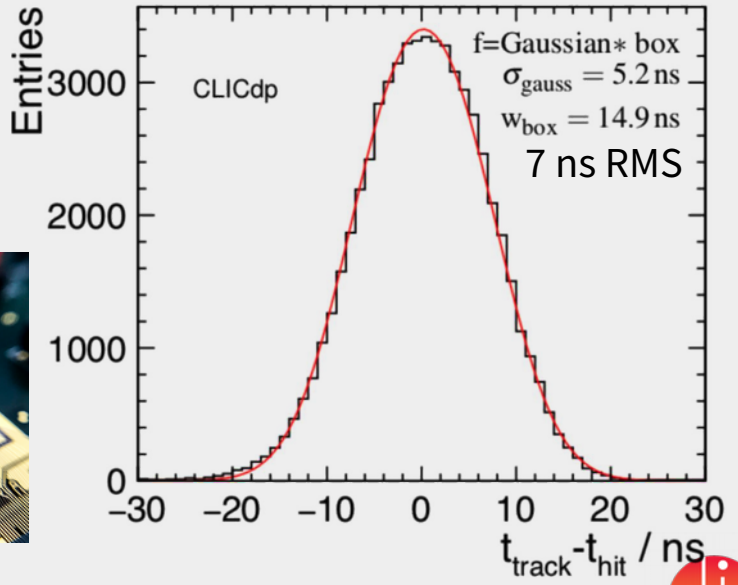
    Efficiency > 99.7%

    Time resolution σ_t ~7 ns (RMS)

    Spatial resolution σ_{SP} ~13 µm

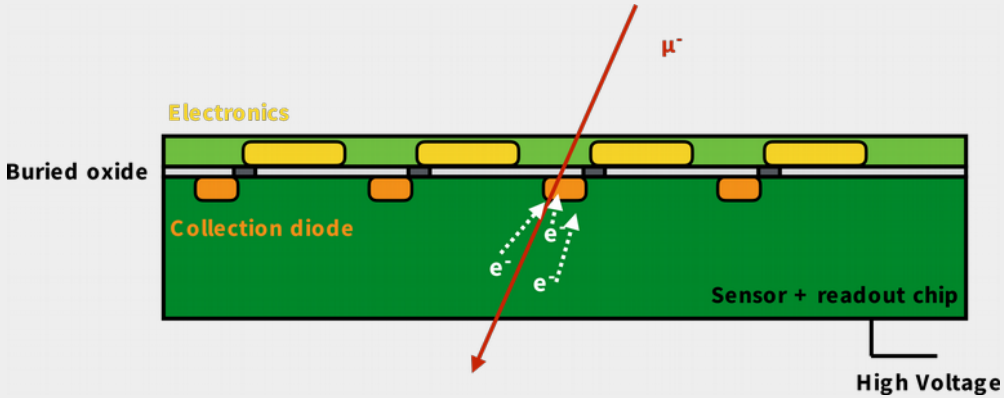


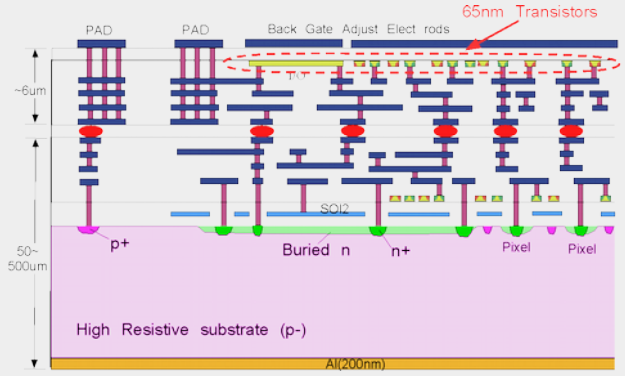


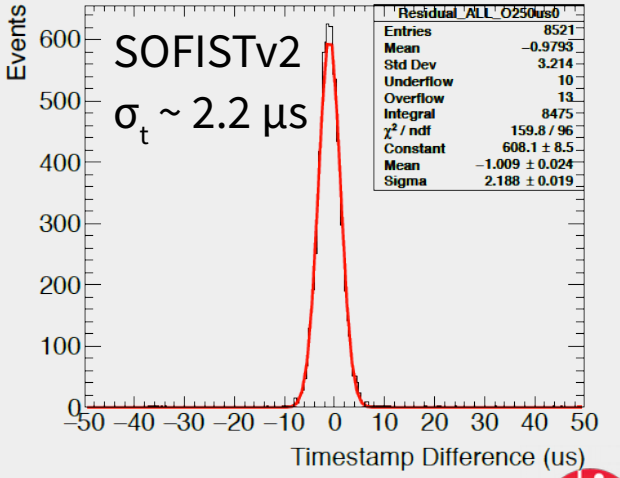


Monolithic Silicon-on-Insulator Sensors

- Monolithic sensor on single wafer with high-resistivity substrate
- Separate sensor/electronics by insulation oxide layer, connect by vias
- Prototypes in Lapis 0.2 µm process
  - **Cracow SOI chip**, ~30 µm x 30 µm pitch, single- & double-SOI, different r/o schemes
  - **CLIPS**: design for vertex
  - **SOFIST prototype**, 20 µm x 20 µm pitch, 3D stacking technology

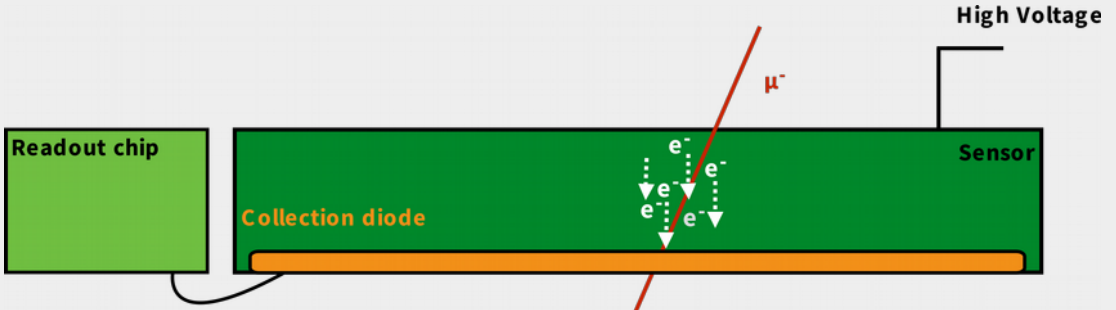


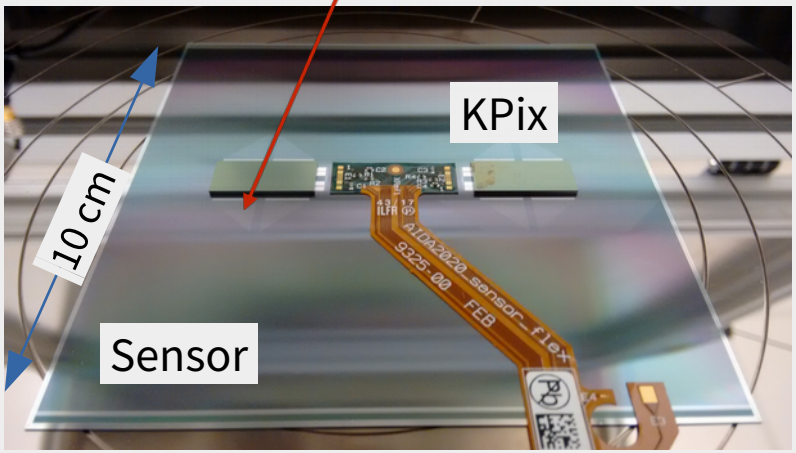


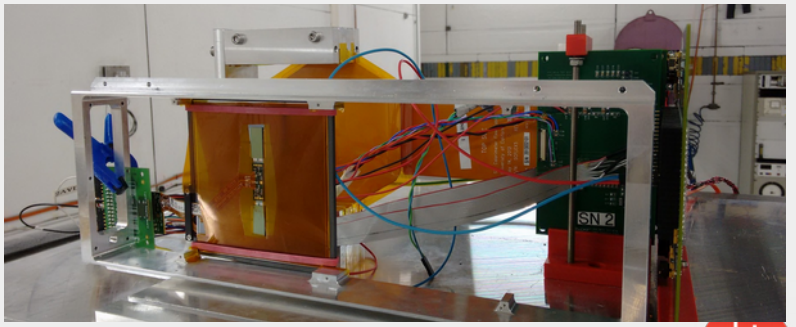


Silicon Strip Detectors

- Implants AC-coupled, separate FE
- SiD Strip Tracker module prototypes
  - Hybrid-less silicon strip sensor, integrated pitch adapter and digital readout
  - Strip pitch of 25 µm, every 2nd strip read out, ~7 µm tracking resolution
  - Sensor: 10 cm x 10 cm, thickness 320 µm
  - ASIC (KPix) bump bonded to sensor surface
- First sensor fully assembled 2018
- First application:
  LYCORIS – Large Area Telescope at DESY Test Beam

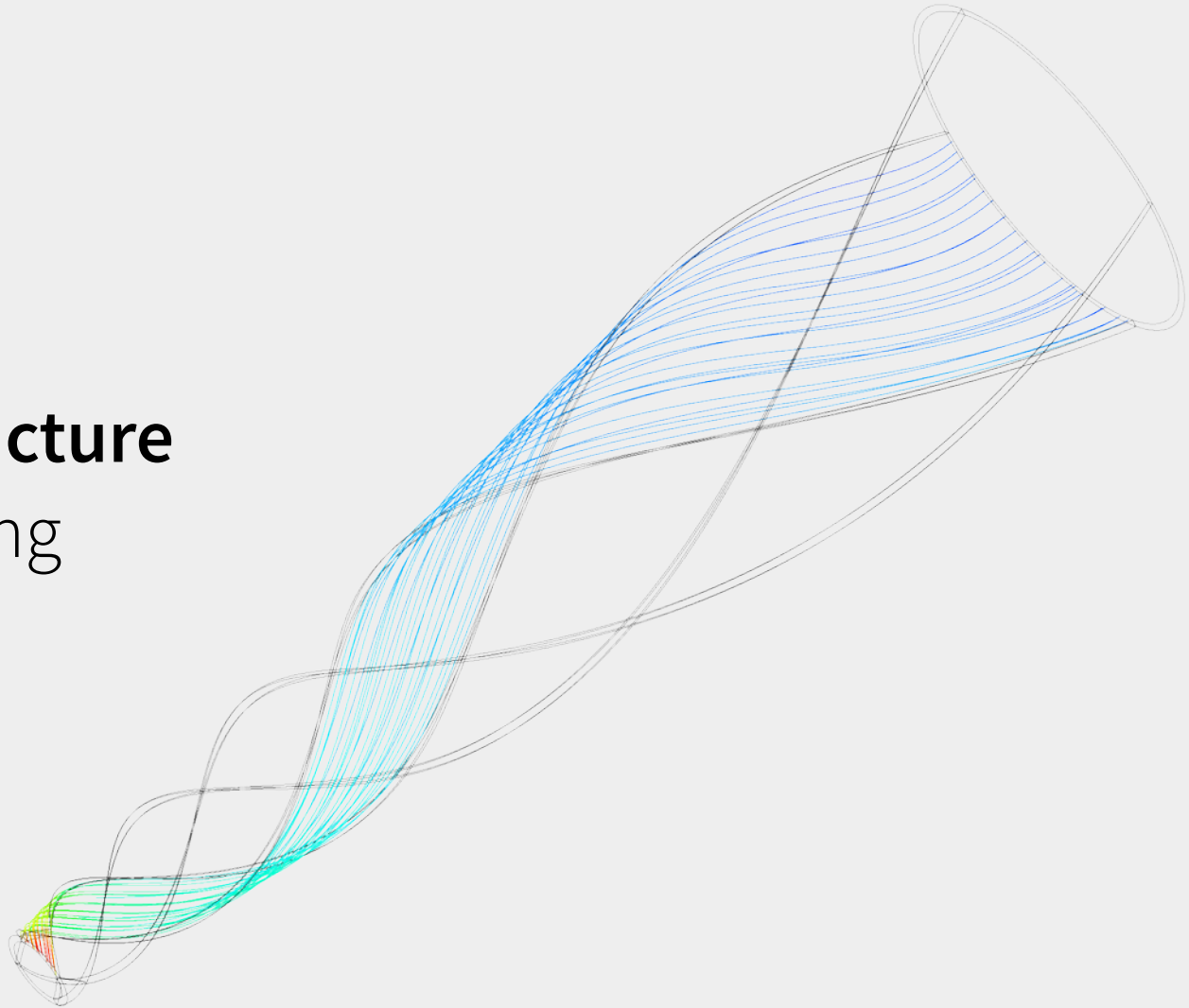






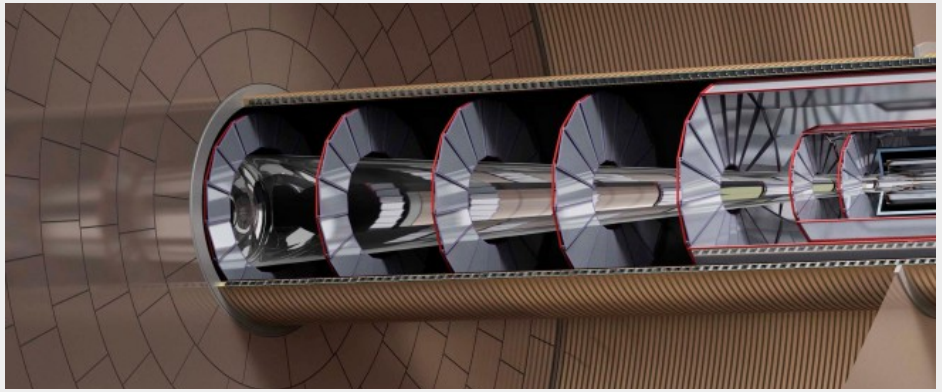
Detector Infrastructure

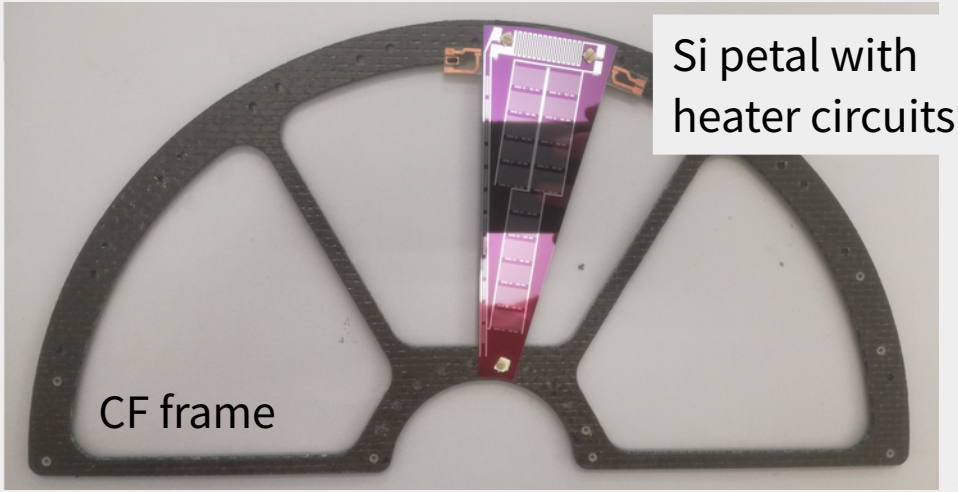
Mechanics & Cooling



ILD: Forward Tracking Disks Mockups

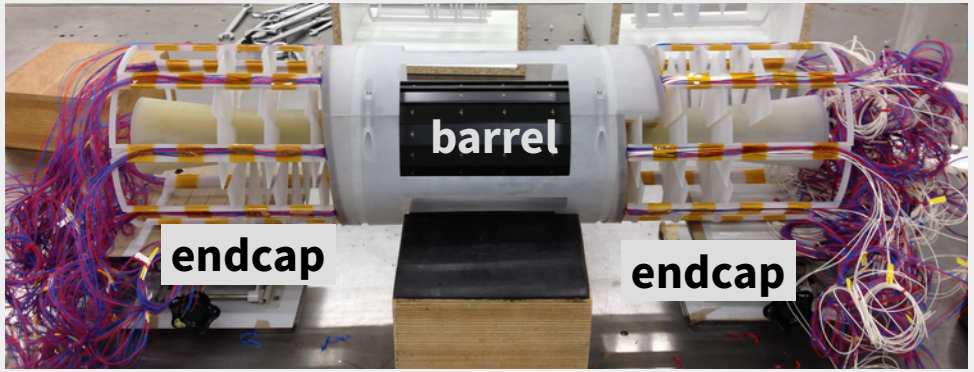
- 7 disks of Si detectors for forward region not covered by TPC
  - < 0.7% X_0 per disk
- Thermo-mechanical mockups
  - Silicon technology yet undecided
  - Gain experience with CF+Si structures
- Characterization:
  - CF disk planarity
  - Vibrations from forced airflow cooling
  - Heat dissipation

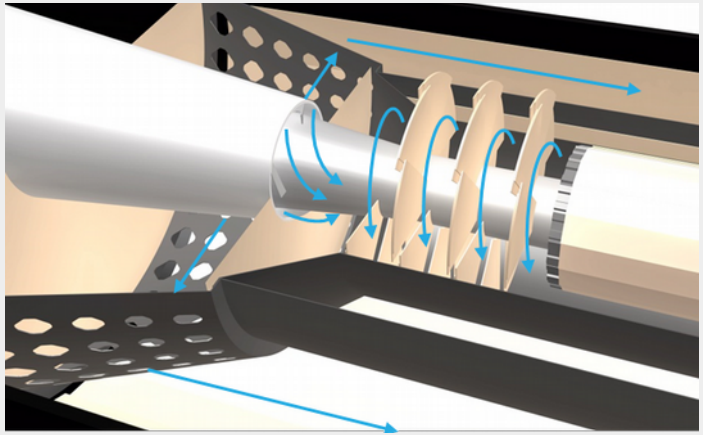


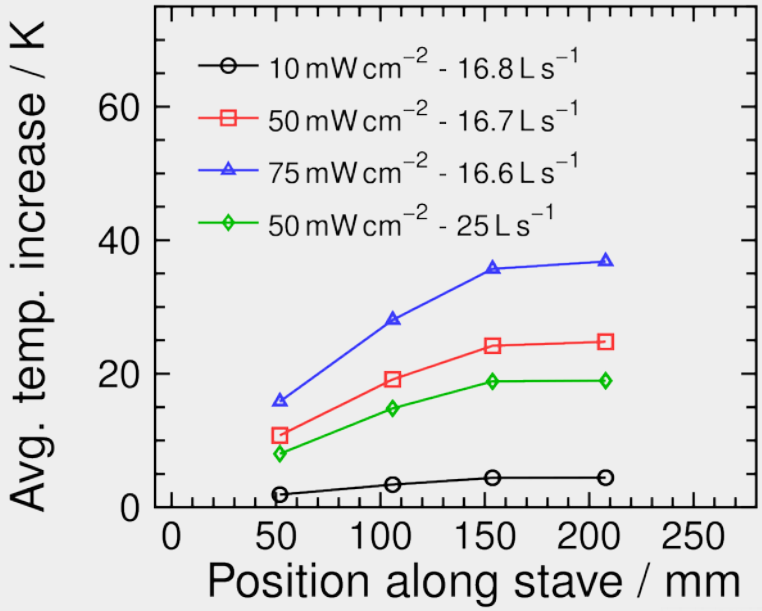


CLICdet: Vertex Air Cooling

- Vertex detector cooled with forced air flow for minimum material
- Spiral vertex disks direct air flow
  - Simulations of velocity, temperature, vibrations
  - Verification with 1:1 thermo-mechanical mockup

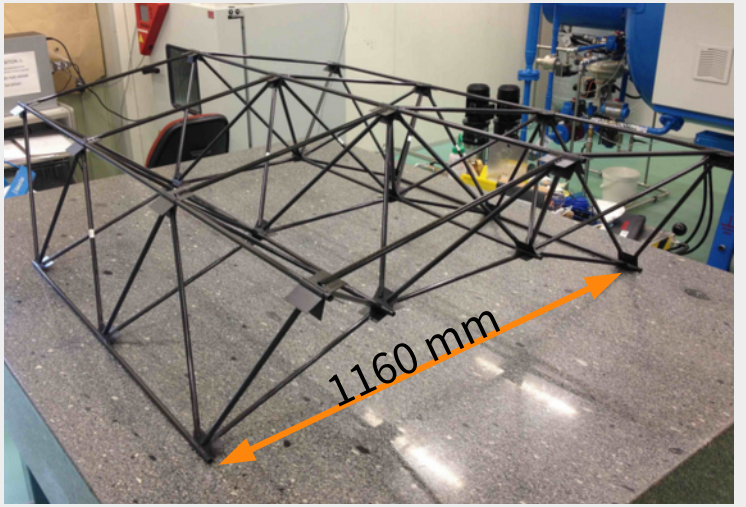


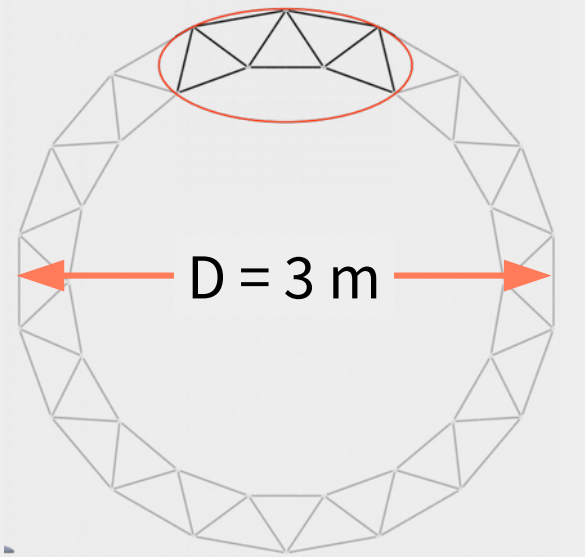




CLICdet: Lightweight Support for Tracking Detector

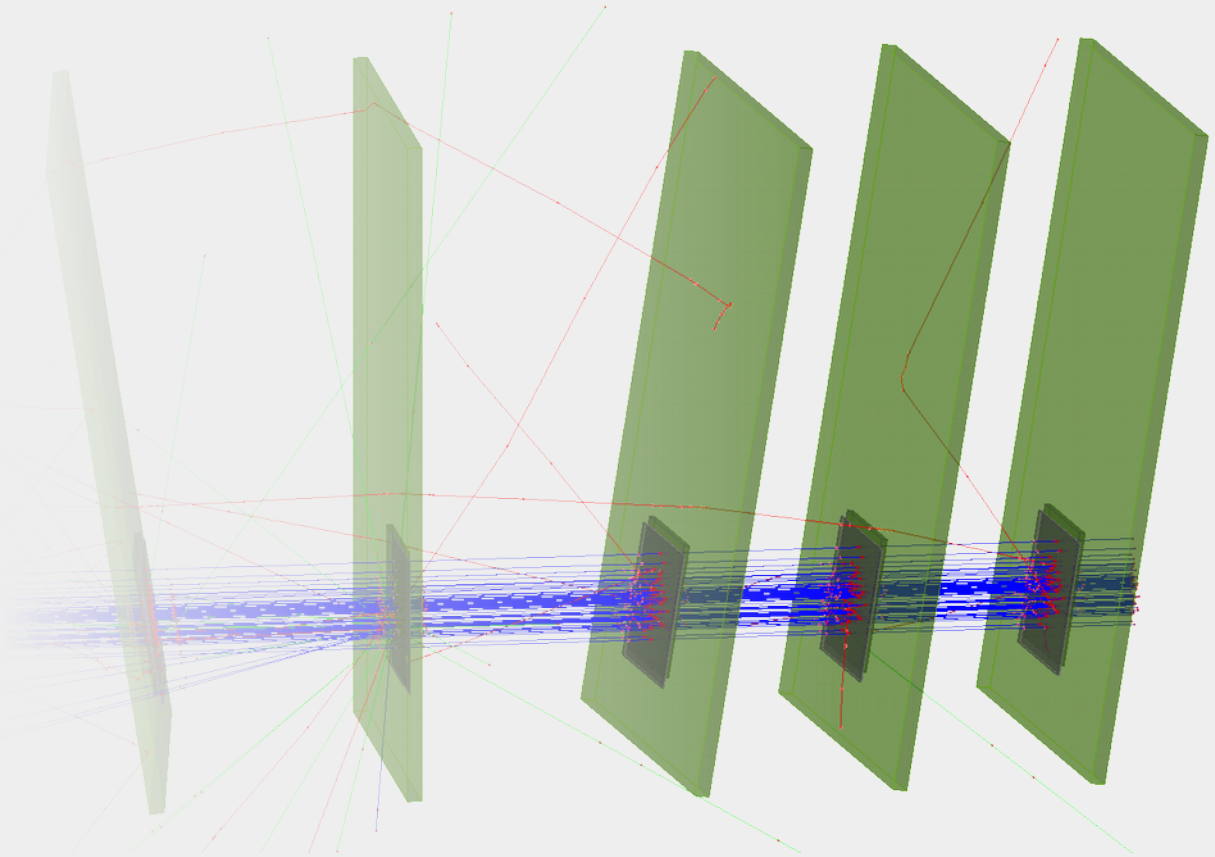
- Proof-of-concept for light tracking detector mechanics
  - Confirm stability and material budget assumptions
  - Off-the-shelf carbon fiber tubes
  - Custom nodes developed and fabricated





- Profiting from recent LHC developments: ALICE ITS upgrade's outer stave
- Stiffness achieved with low mass structure
- Total weight of the prototype: 926 g

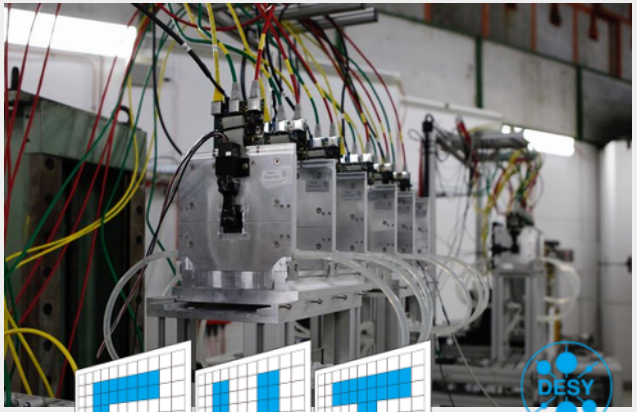
Tools

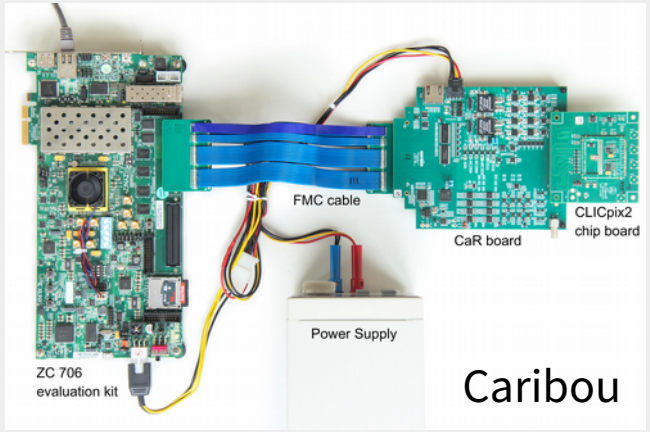


Tools for the Community

Linear Collider Silicon detector R&D has helped to create many widely used tools…

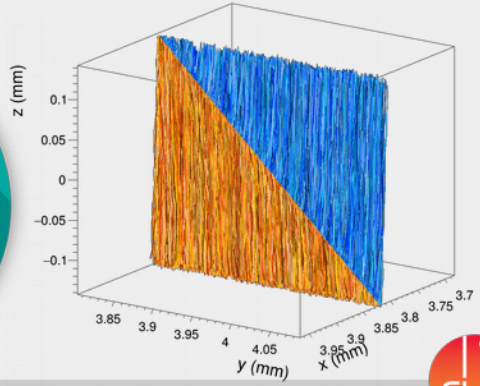
- Beam telescopes
- Readout systems
- Reconstruction software
- Simulation software





Corryvreckan

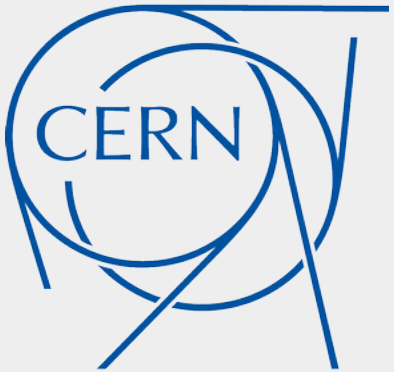
ap² allpix squared



In a nutshell…

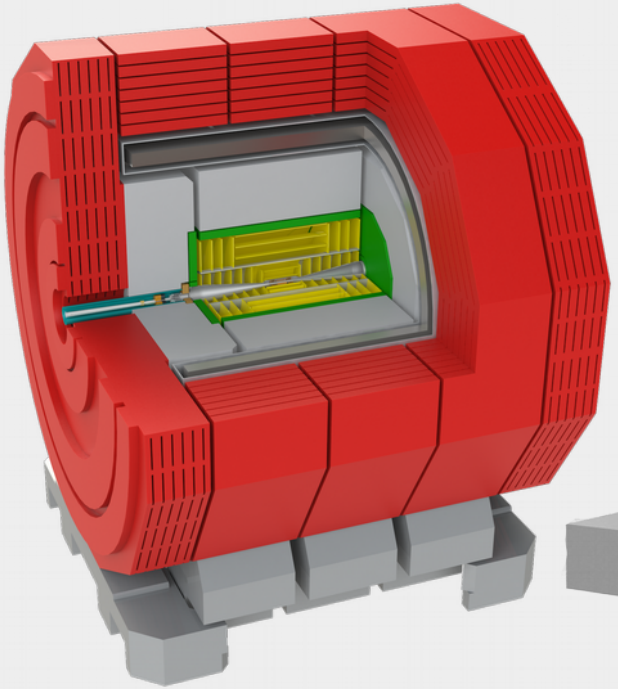
Summary

- Unique challenges for silicon detectors at linear colliders
  - Ultra-lightweight detector systems
  - High resolution sensors (spatial & temporal)
- Many design goals for LC detectors achieved –
  but yet need to be united in a single detector system
- R&D profits from developments for LHC detectors and vice versa
- Many prototypes based on commerical CMOS imaging technology
- Trend to “pixels everywhere”
- Great possibility to explore new technologies

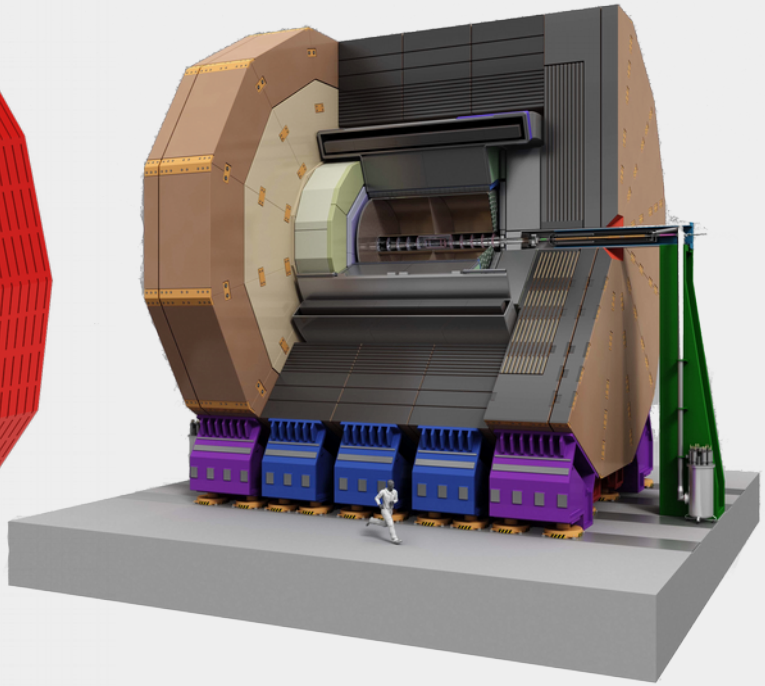

CERN

Three LC Detector Models

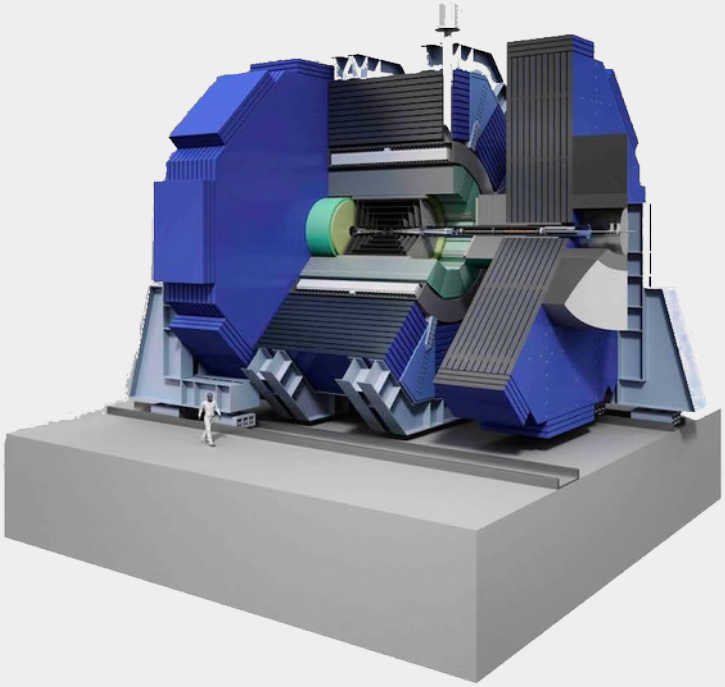
CLICdet



ILD

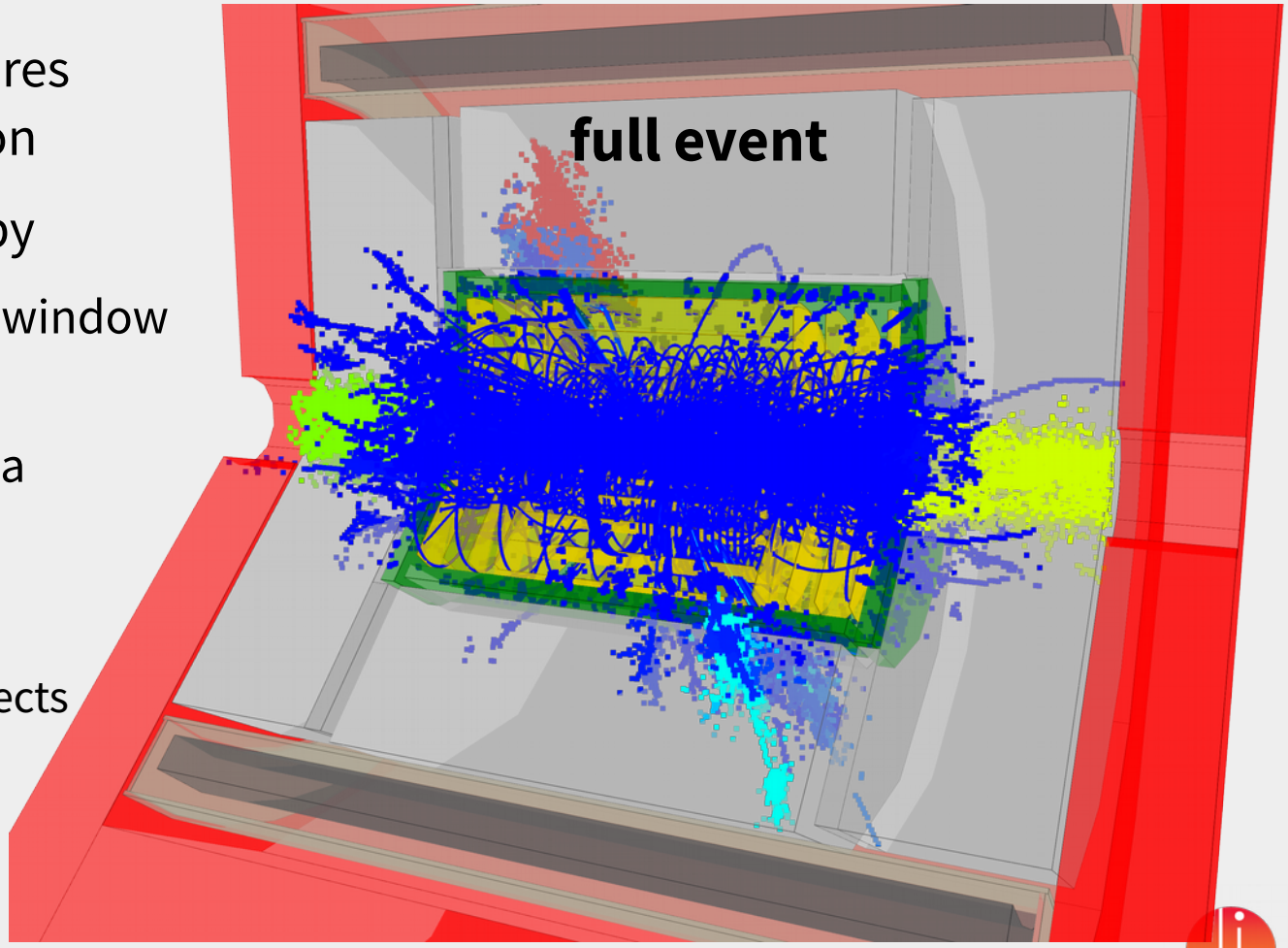


SiD



CLIC: Background suppression @ **3 TeV**

- Short bunch spacing requires precise hit time information
- Background suppression by
  - Defining reconstruction window around physics event
  - Suppress background via
    - Timing requirements
    - Particle type and p_T
    - Retaining high-p_T objects
- Example: full-hadronic $t\bar{t}$ event



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