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TERASCALE WORKSHOP 2019

SERIAL POWERING IN PIXEL DETECTORS

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OUTLINE

- why serial powering?
- key ingredients for a serially powered silicon pixel detector
- challenges in serial powering

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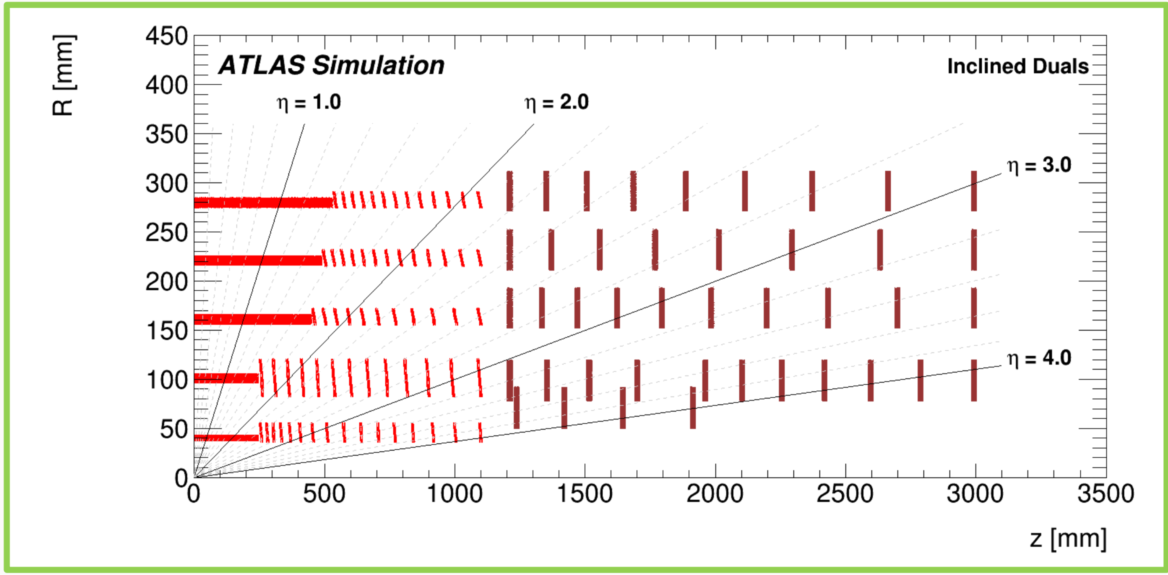
- key ingredients for a serially powered silicon pixel detector
- challenges in serial powering

I will mostly use the planned upgrade of the ATLAS Pixel Detector as an example – most of what will be shown applies to the CMS upgrade in a very similar way

ATLAS INNER TRACKER PIXEL DETECTOR

- 5 barrel layers:
  - flat section up to z = 500mm
  - inclined section up to z = 1200mm
  - endcap rings up to z = 3000mmm
- coverage of tracks with |η| < 4
- about 10.000 hybrid pixel modules
  → about 40.000 FE chips

- 50x50 μm^2 or 25x100 μm^2 pixels
- 2 innermost layers will be replaceable after collecting 2000 fb^{-1}



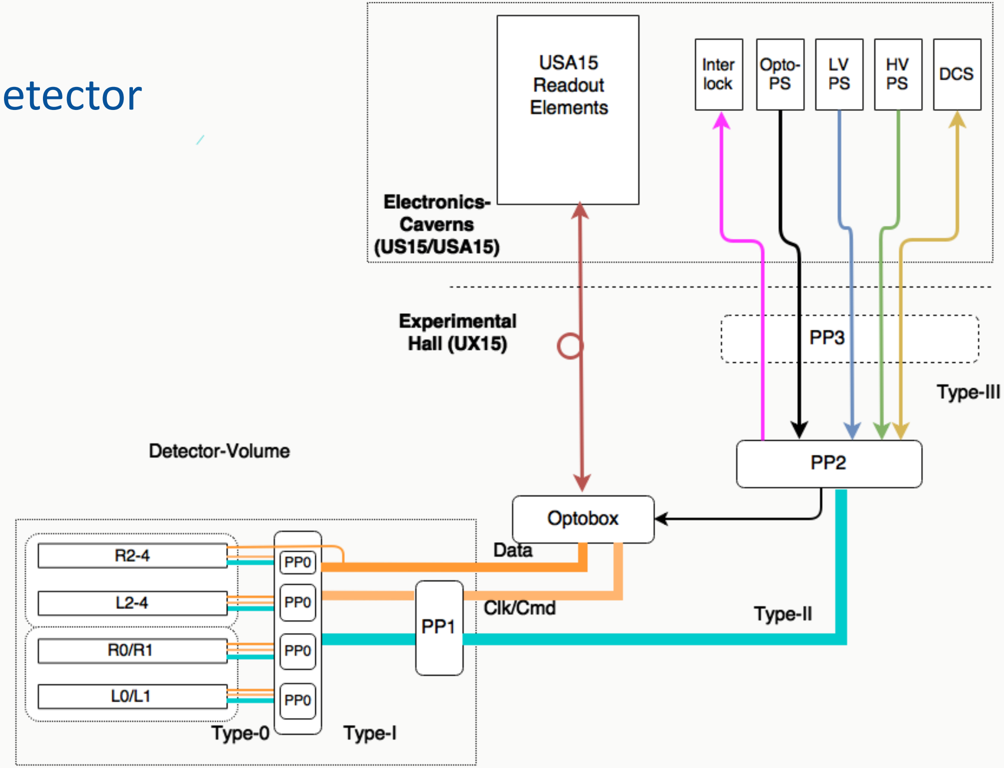
Candidate Layout for the ATLAS Pixel Upgrade

- general reference: CERN-LHCC-2017-21; ATLAS-TDR-030

SERVICES OVERVIEW

- services overview of the ATLAS ITk Pixel Detector
  - off-detector services
    - power supplies, readout electronics
    - Type-3 cables, about 60m-80m long
    - Type-2 cables, about 12m long
  - on-detector services
    - Type-1 cables, about 6m long
    - Type-0 services, about 1m long

→ typical current path for a power line:
about 200m



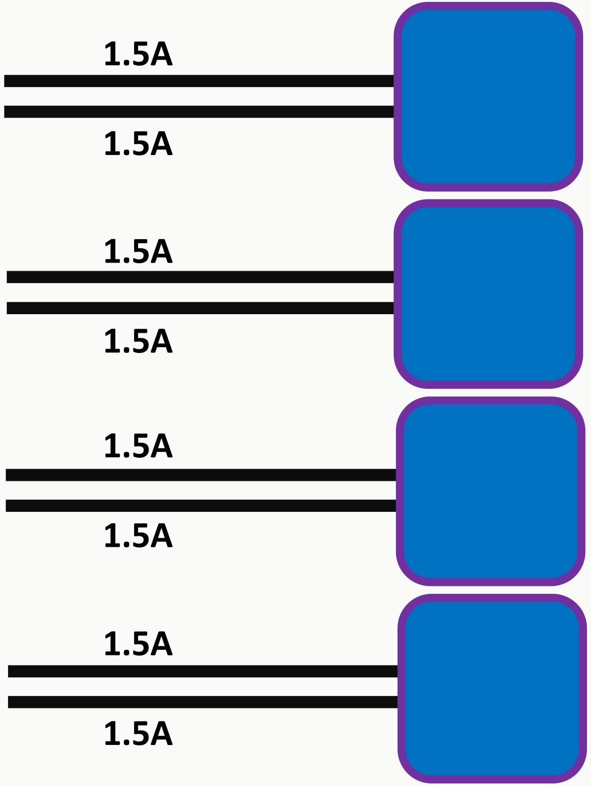
PARALLEL POWERING?

- Front-End Chips for the ATLAS and CMS upgrade:
  - pixel matrix with about 150.000 pixels
    - each pixel consumes between ~6uA and ~10uA
  - about 200mA required to run the chip periphery

  → actual per chip current consumption: 1.1A – 1.7A

  → voltage drop across every chip: about 1.5V

  → total power dissipated in FE chips: about 90kW



→ 40.000 FE chips, assuming each draws 1.5A

→ each powered with it's own 200m long cable

→ assuming we have **thick** cables: AWG12, 5.2 mOhms/m

→ total resistance per cable: about 1 Ohm

→ total power dissipation on these cables: **90kW**

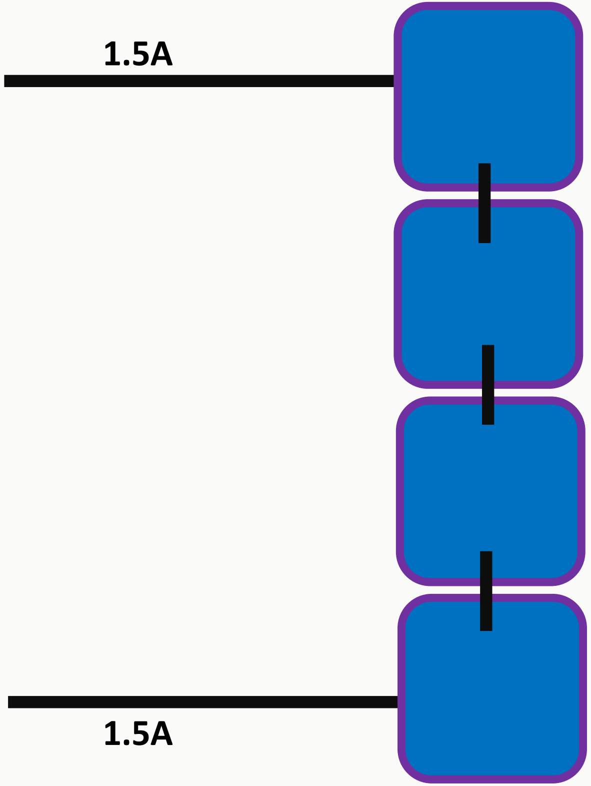
→ total cooling budget: about 180kW – this is **too much**

SERIAL POWERING

- recycle the current on-detector
  - average serial powering modularity: 8 modules

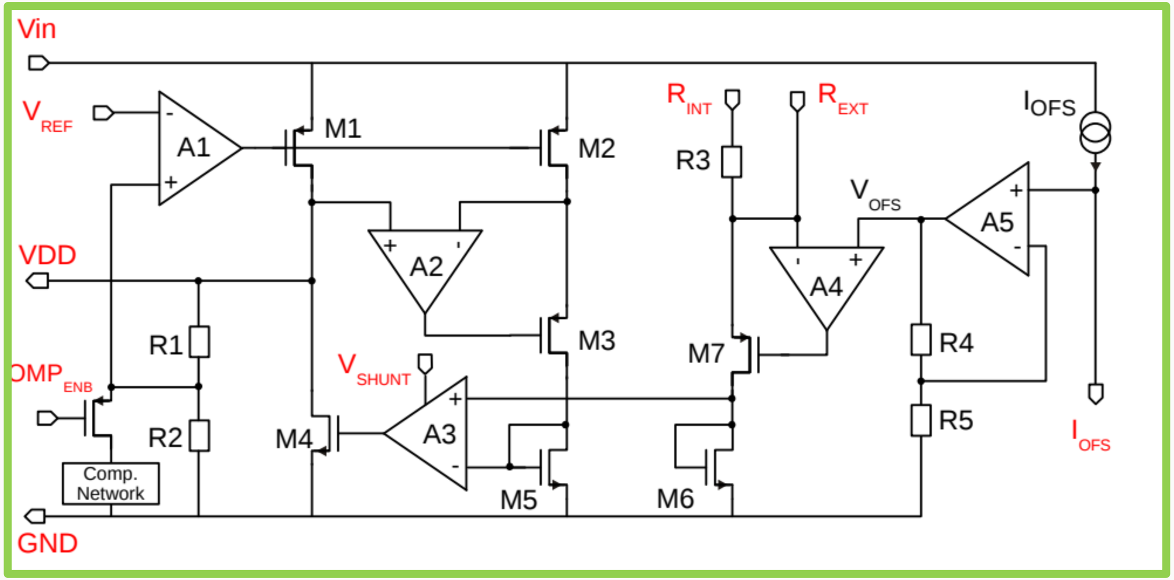
  - assuming single chip modules: losses on cables go down to **11kW**
  - the number of cable we require also goes down by a factor of 8
    → less material in the detector
  - the number of required power supplies goes down by a factor of 8
    → less space required in services caverns

- advantages come at a cost
  - actual current consumption per FE depends on instantaneous hit-rate
    → different instantaneous current consumption for all FE chips in a chain
  - voltage drop from one module to the next
    → need AC coupled data transmission
    → with 3D modules: length of serial powering chain limited!
    → biasing of sensors can get a little tricky
    → . . .



HOW TO POWER A SERIAL POWERING CHAIN

- provide as much current to the full chain at all times as we expect at peak hit-rate
  → constant current source
- each chip requires a local voltage regulator and a shunt to draw any surplus current
  → Shunt-LDO regulator



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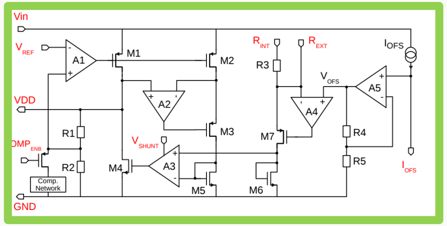

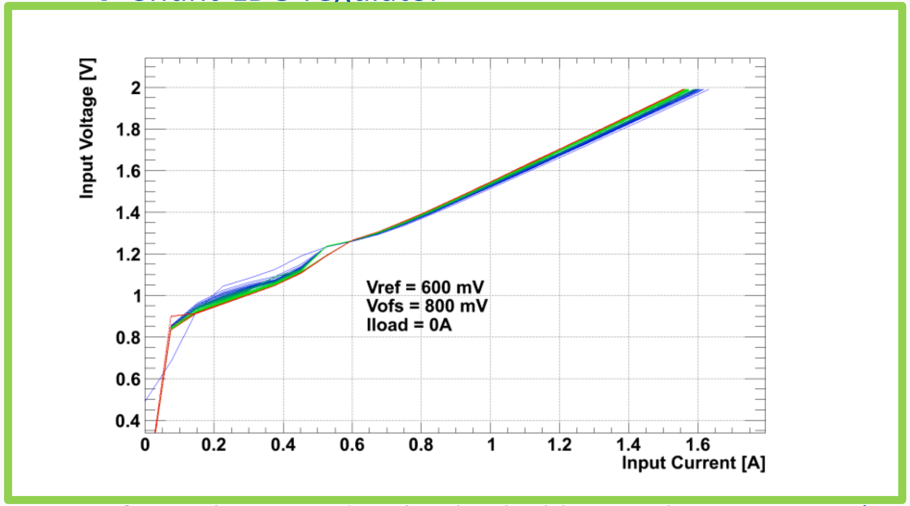

→ Vin = Vofs + R3/k * Iin

from the outside, this looks like a voltage source (Voffset) connected in series to a resistor (R3/k)

→ constant voltage drop at constant current independent of actual chip current consumption

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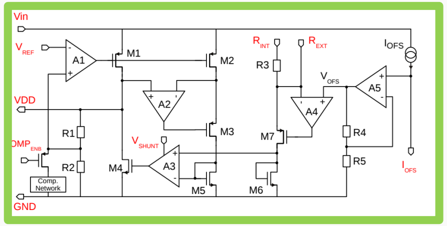

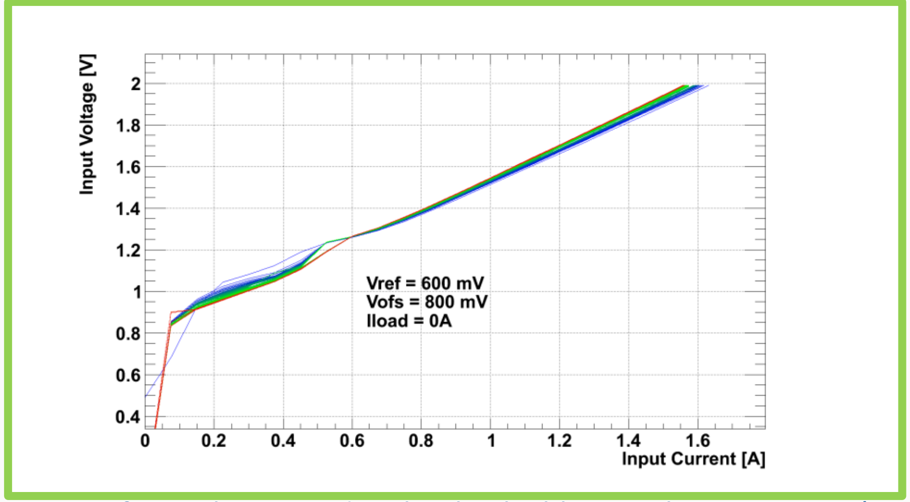

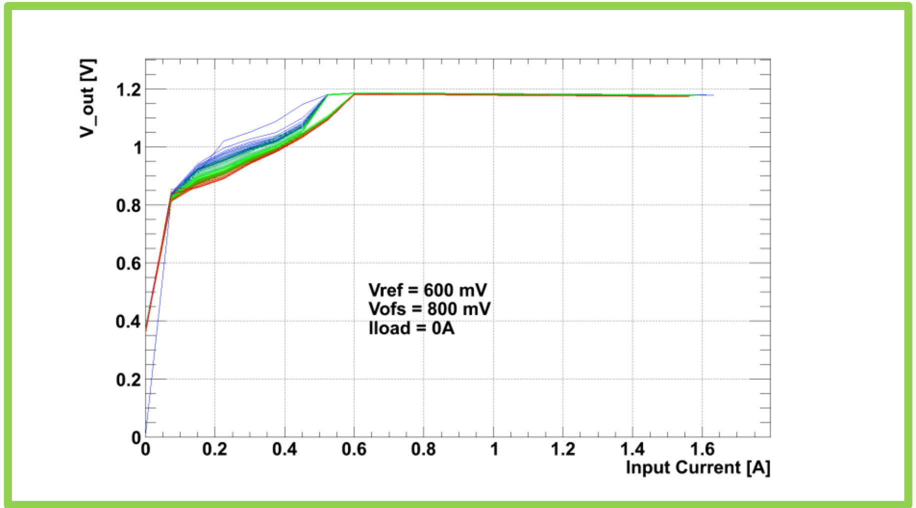

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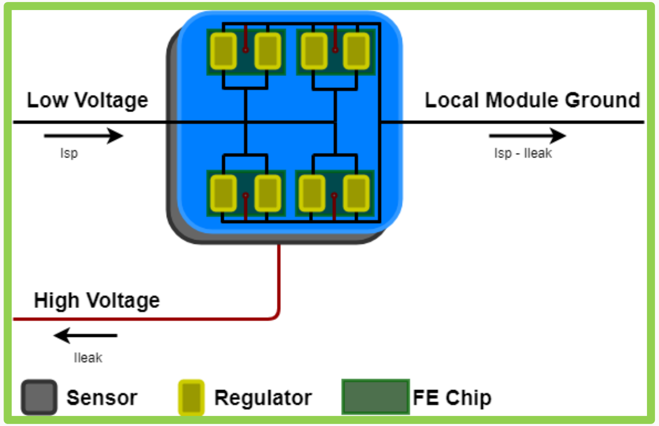
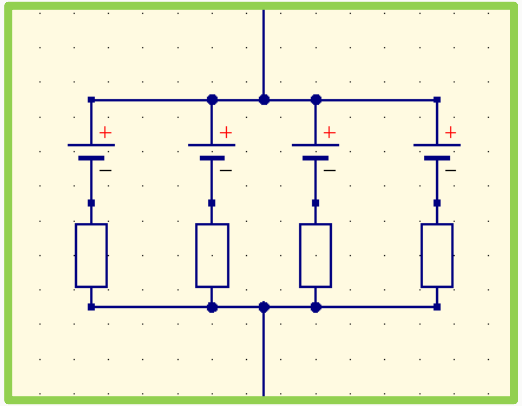
→ constant voltage drop at constant current independent of actual chip current consumption

WHAT IF?

- a chip in the chain becomes high-ohmic?
  - the rest of the chain would be disabled
  - mitigate problem by connecting chips in parallel
    → SLDO regulators need to be able to shunt the extra current
    → total voltage drop over the module must not exceed limits for safe operation
    → thermal management of the module must be able to handle the extra power





everything working fine
→ Input Current: 6A
→ Vofset: 0.9V
→ Reffective: 0.1 Ohms
→ Input Voltage: 1.5V
→ Total Power: 9W

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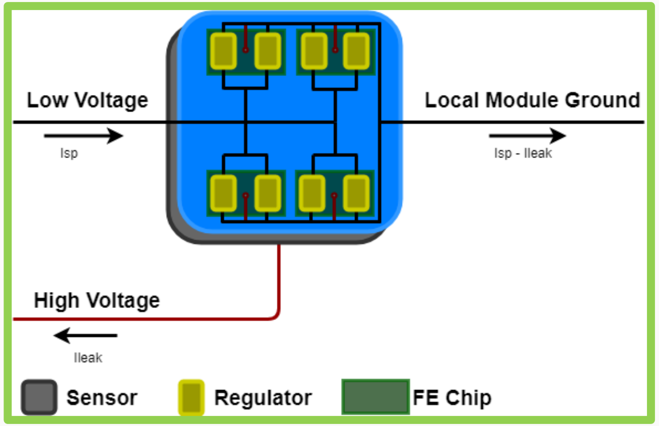

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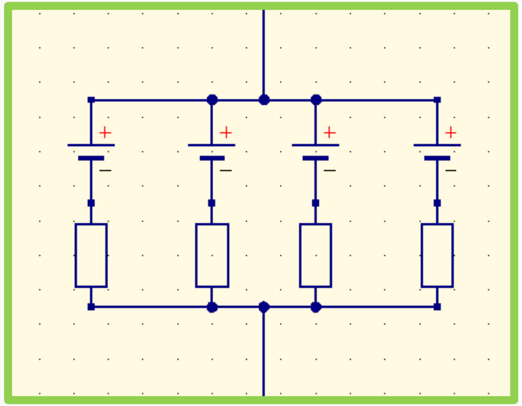

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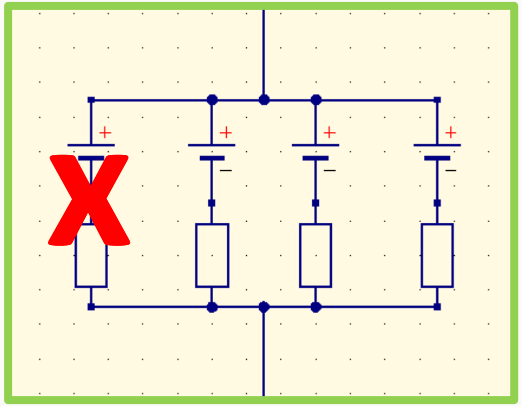
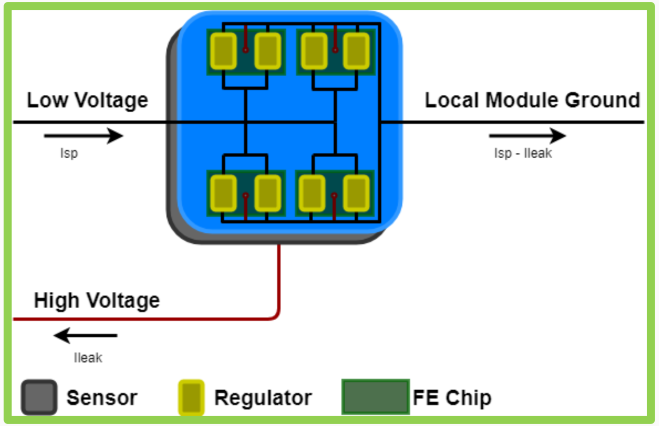


1 FE open
→ Input Current: 6A
→ Vofset: 0.9V
→ Reffective: 0.13 Ohms
→ Input Voltage: 1.7V
→ total Power: 10.2W

WHAT IF?



- a chip in the chain becomes high-ohmic?
  - the rest of the chain would be disabled
  - mitigate problem by connecting chips in parallel
    - → SLDO regulators need to be able to shunt the extra current
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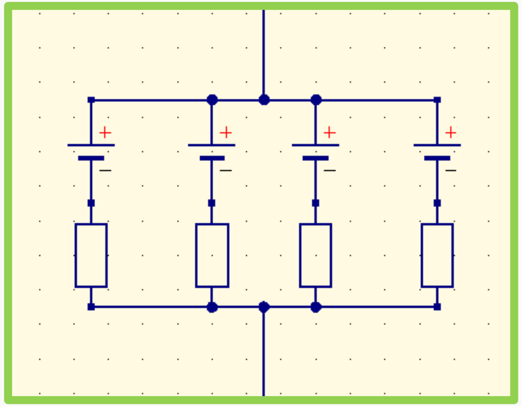
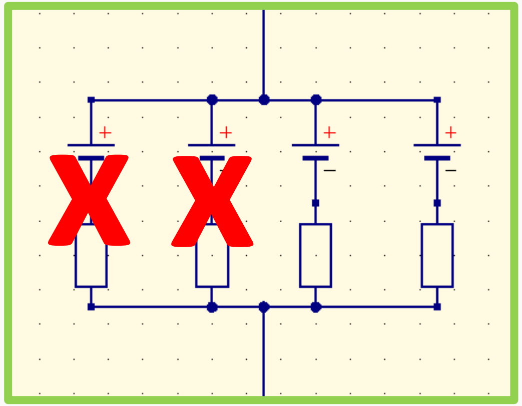


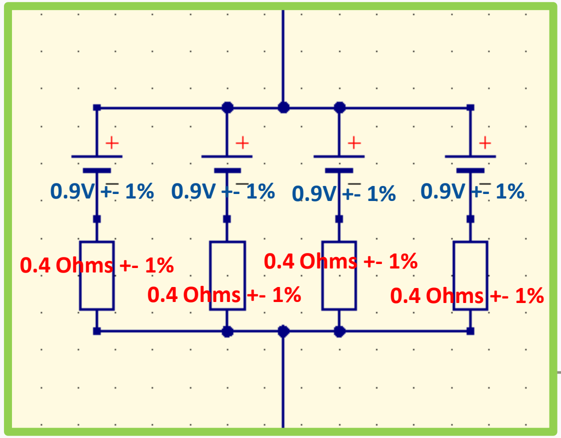
everything working fine
→ Input Current: 6A
→ Vofset: 0.9V
→ Reffective: 0.1 Ohms
→ Input Voltage: 1.5V
→ Total Power: 9W



2 FE open
→ Input Current: 6A
→ Vofset: 0.9V
→ Reffective: 0.2 Ohms
→ Input Voltage: 2.1V
→ total Power: 12.6W

OPERATING CHIP IN PARALLEL AGAIN...

- the FE chips on a module are operated in parallel:
  - → single sensor tile, DC coupled: same ground potential required
  - → current distribution becomes a challenge
    - → voltage drop on all regulators is the same
    - → offset voltage and slope determined by external resistors: small differences O(1%) expected
    - → not every FE gets exactly 25% of the total current
    - → hit-rate can spike significantly: increase load current in single regulators
      - → compensate by supplying more current than nominally required: shunt current overhead
        - → how much?

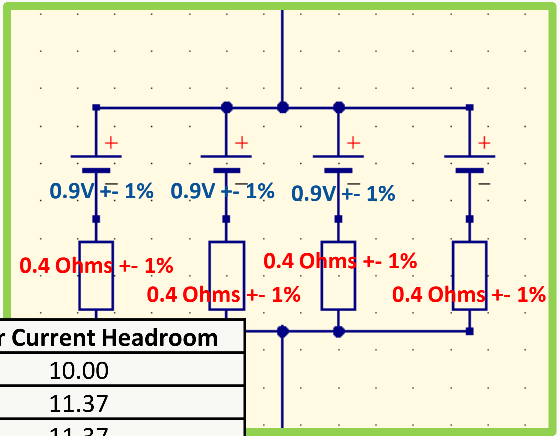


higher offset: lower current through resistor
higher resistor: lower current through resistor

worst case:
→ downwards fluctuation for both offset and slope in all other chips (Chips 1, 2, 3)
→ upwards fluctuation for both offset and slope in one chip (Chip 4)
→ Chip 4 gets significantly smaller current

AN EXAMPLE

- worst case scenario for a quad chip module:
  - 10% shunt current headroom supplied
  - 1% variation in offset and slope: 5% difference in terms of current
  - half of the safety we have



	Slope [Ohms]	Offset resistor [kOhms]	Offset [V]	Serial Current [A]	Voltage Drop [V]	Required Current	Leftover Current Headroom
Module	0.10		0.90	6.00	1.49	5.45	10.00
FE 1	0.39	445.50	0.88	1.52	1.49	1.36	11.37
FE 2	0.39	445.50	0.88	1.52	1.49	1.36	11.37
FE 3	0.39	445.50	0.88	1.52	1.49	1.36	11.37
FE 4	0.41	454.50	0.92	1.44	1.49	1.36	5.90
Target	0.40	450.00		0.05			

required current depends on hit-rate

hit-rate can only be roughly estimated from simulation

variations of up to 10% seen between simulation and measurement in current detector

1% variation in offset and slope in combination with a 10% variation in hit-rate leaves almost no headroom

AN EXAMPLE

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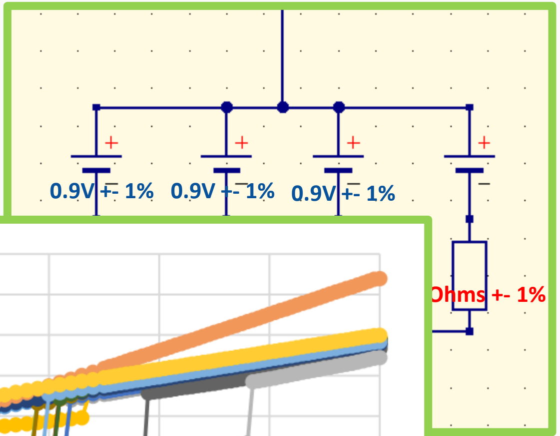

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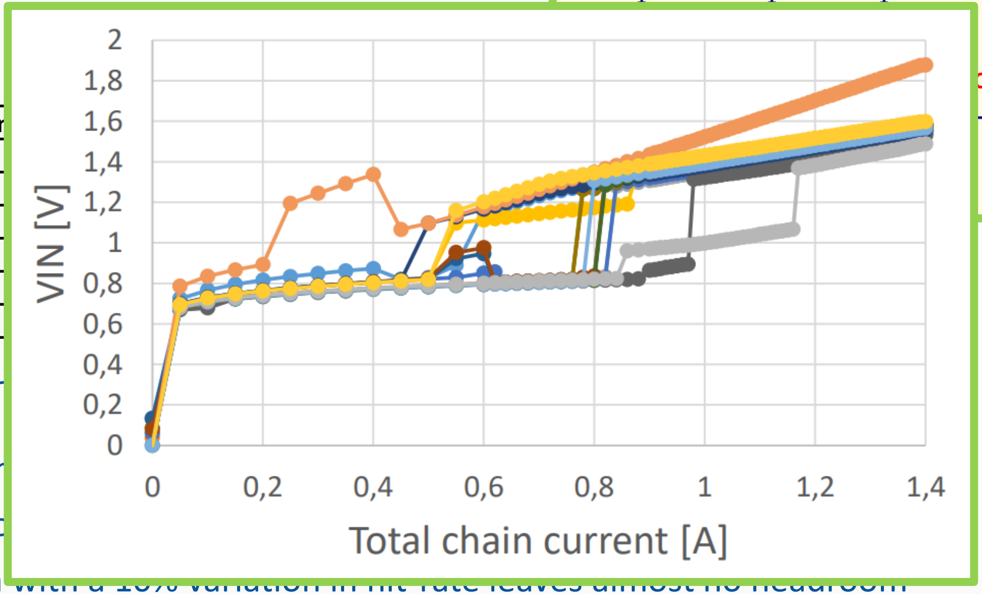

required current depends on hit-rate

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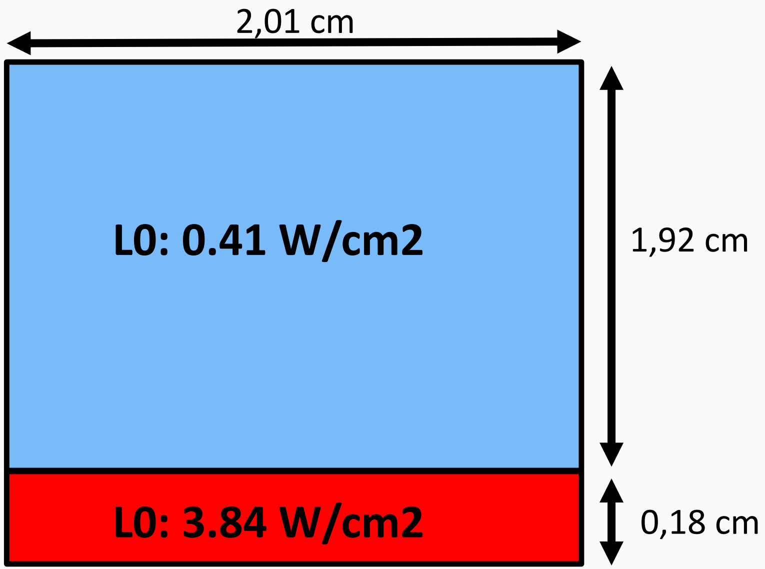
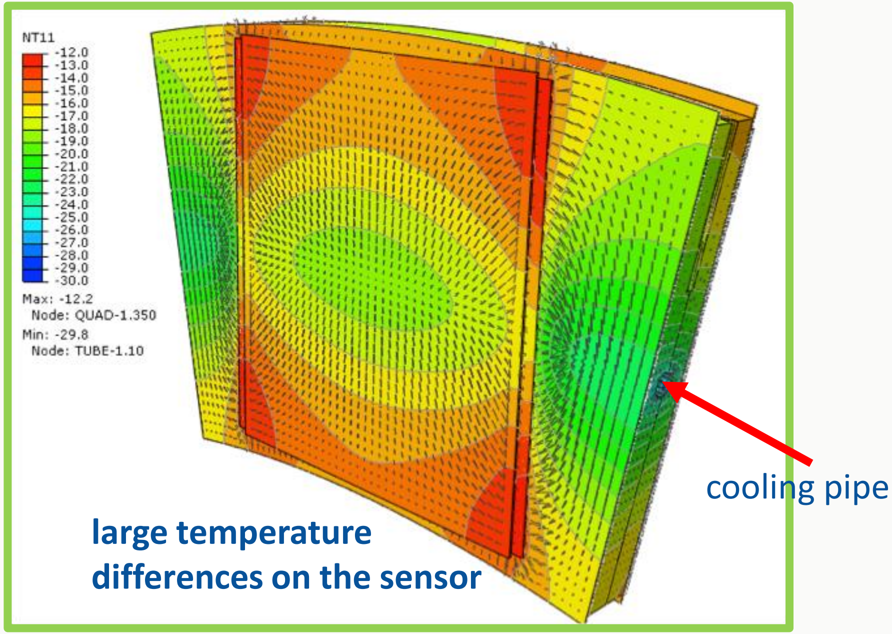
variations of up to 10% seen between simulatic

1% variation in offset and slope in combination

THERMAL CHALLENGES

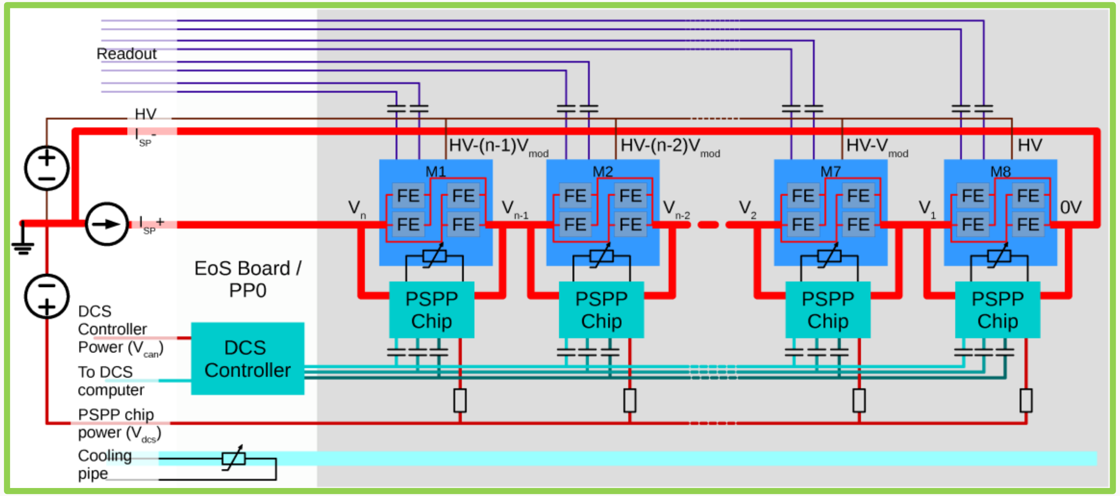
- significant fraction of total module power is dissipated on the chip periphery
  - almost 40% of the total power dissipated in less than 10% of the chip area
  - challenging for the cooling system

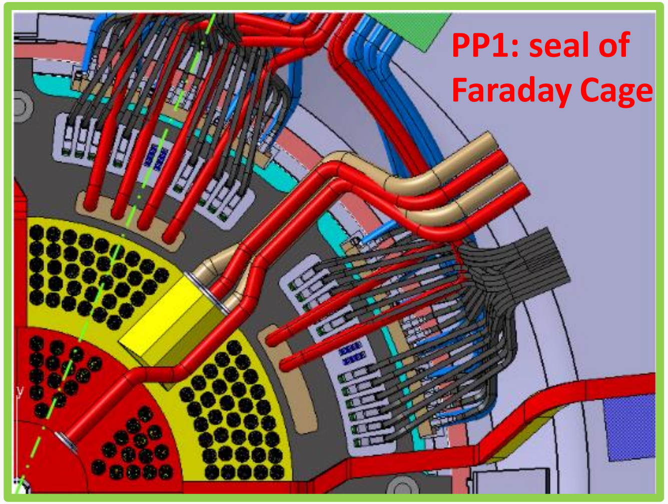




HIGH VOLTAGE DISTRIBUTION ISSUES

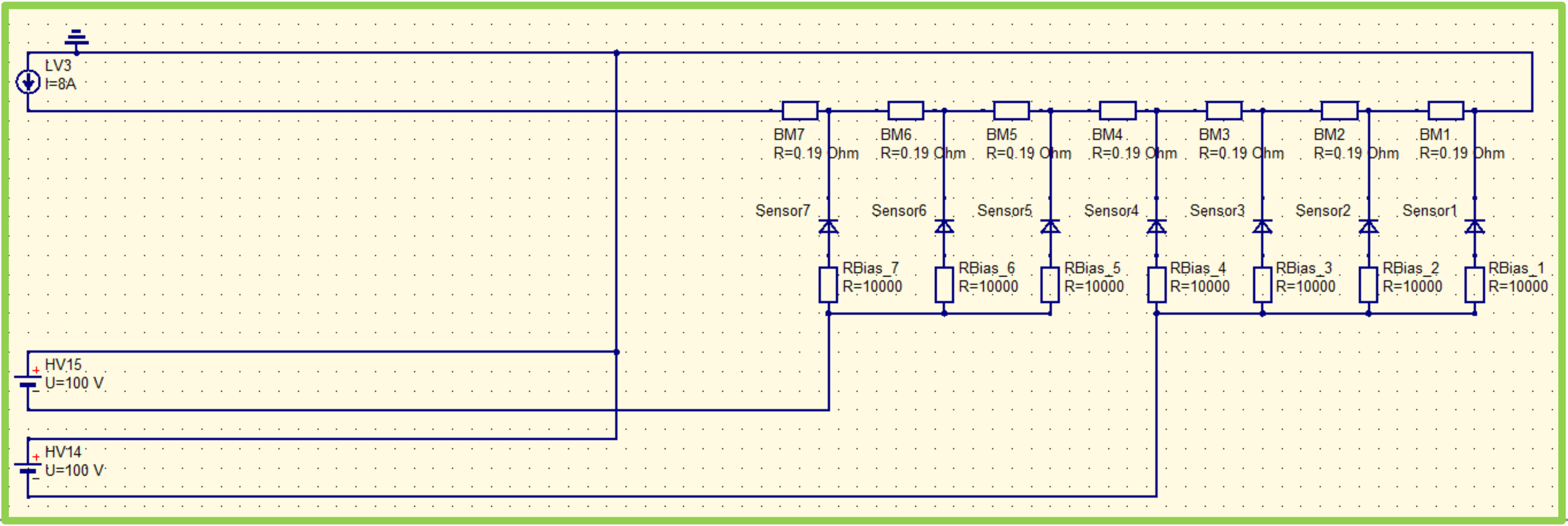
- we can not put enough cables into the detector to provide an individual HV line for each sensor
  - parallel distribution of sensor bias voltage to a subset or all modules in a serial powering chain
  - HV referenced to local module ground different effective bias voltage on every single sensor
  - long chains with 3D sensors not desirable
    → depletion voltage as high as 10 V, breakdown voltage as low as 20V





OTHER SYSTEM ASPECTS

- our grounding and shielding rules require us to tie the return lines of all power supplies to each other in the detector
  - in combination with our current power supplies, this generates a potential problem
    - HV power supplies act as high-ohmic resistors when switched off



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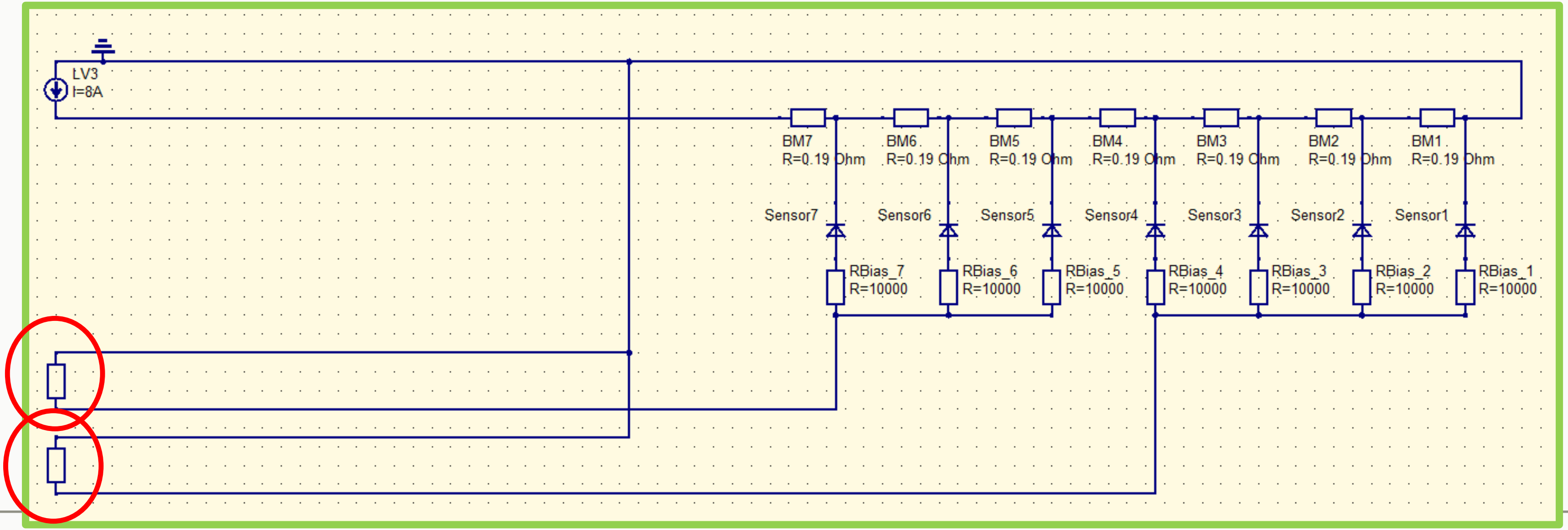

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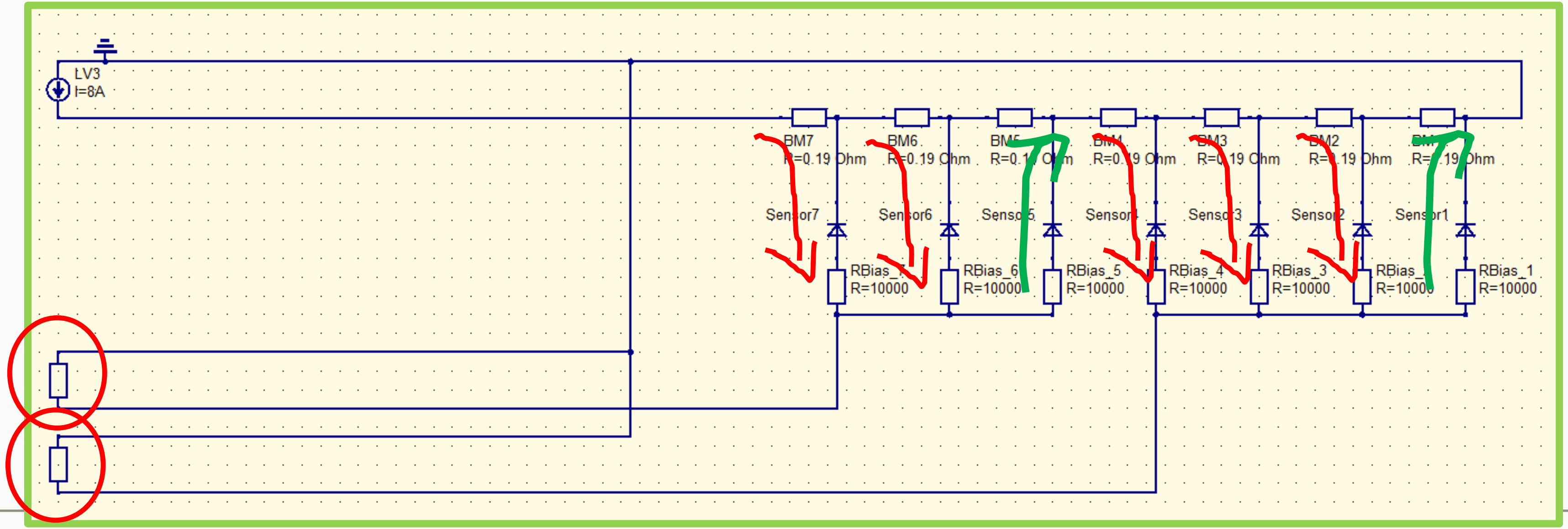
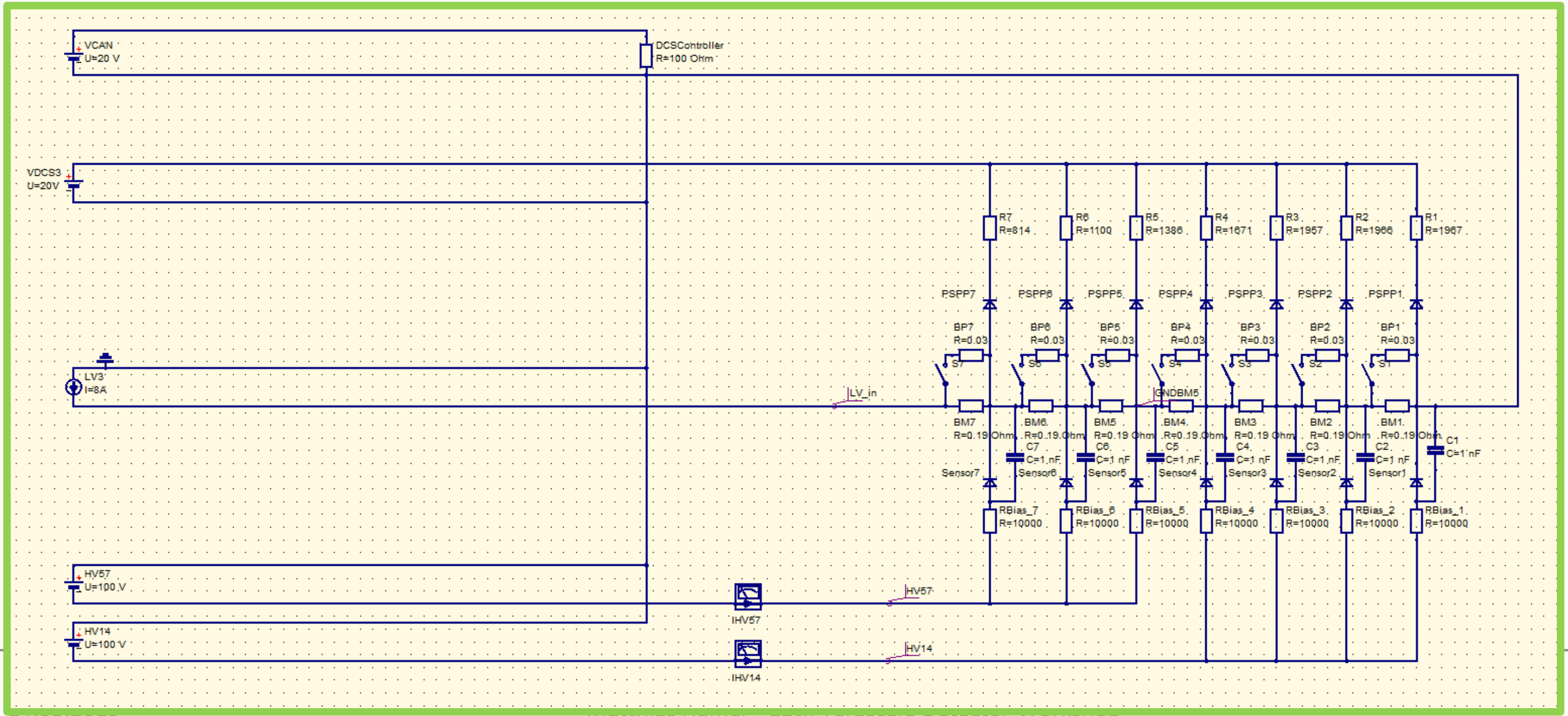
    - LV on → small effective bias on each sensor → return path through modules has lower resistance than HV PSU



OTHER SYSTEM ASPECTS

- a similar effect with the PSPP chips
  - our current LV power supplies are shorted when switched off; VDCS generates a negative voltage drop on FE chips



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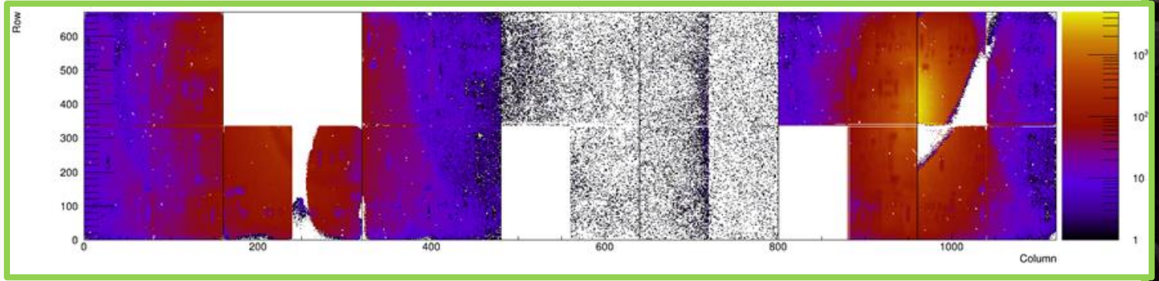
SERIAL POWERING IN ACTION

- several prototypes have been built by now
  - proof of principle at Bonn some time ago
  - prototype with realistic services, power supplies, local supports at CERN
  - long serial powering chain (13 modules) in Liverpool
  - ...



simultaneous source scan with full prototype

OB local support with FE-I4 SP chain and PSPP chips

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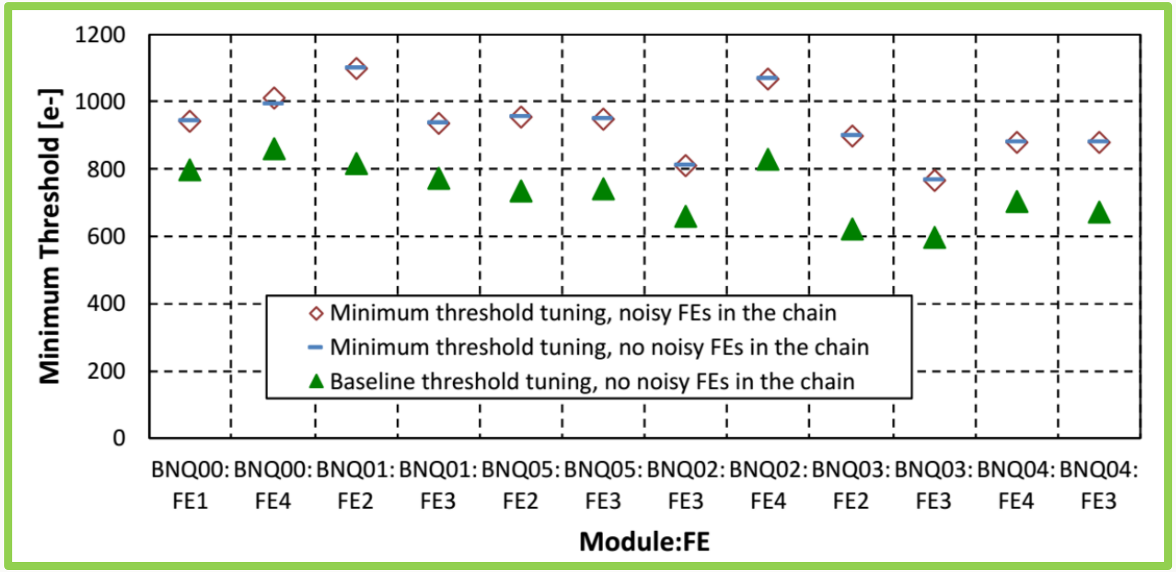
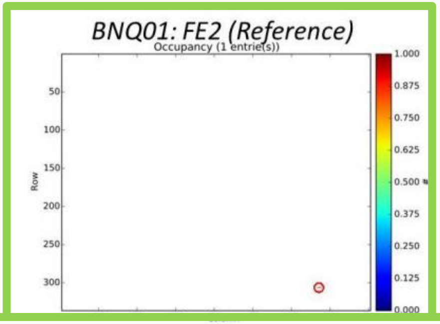
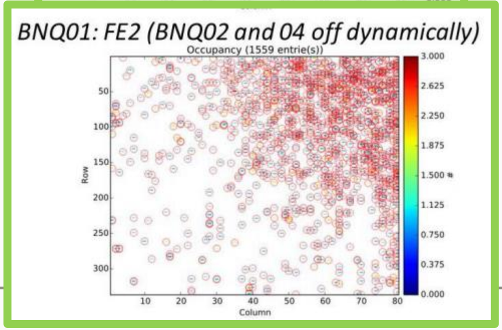
SERIAL POWERING IN ACTION

- effects of transients in the LV line
  - noise pickup
  - with FE-I4 modules, oscillations can be triggered by overloading the SLDO regulator (noisy module)
  - effect on remaining modules was tested: low to no effect

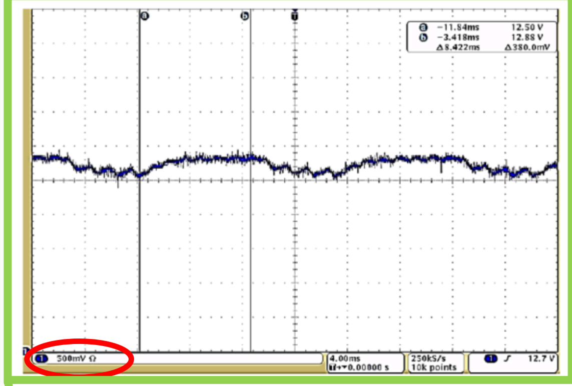


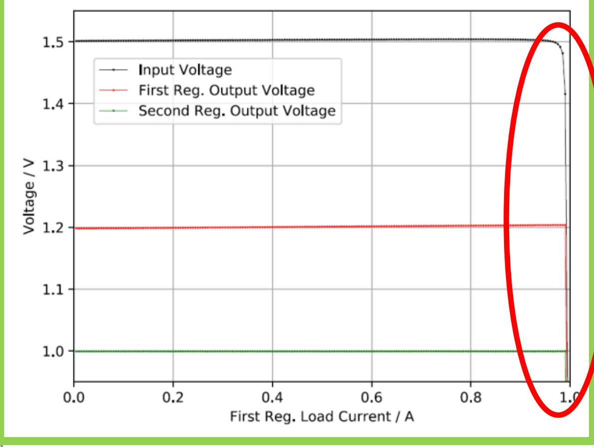


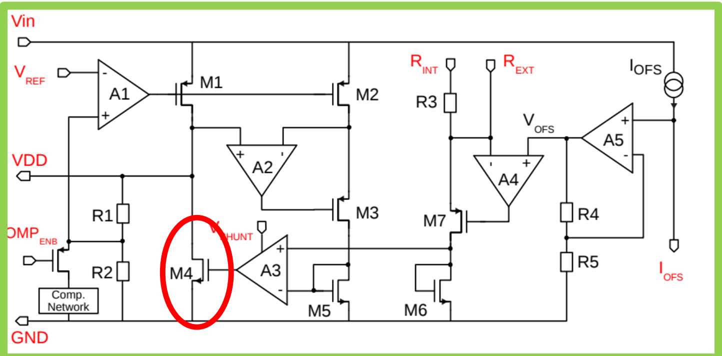


UPGRADES FOR SERIAL POWERING

- protection mechanisms for front-ends required:
  - large transients can be dangerous for modules
- FE chips for ATLAS and CMS upgrades will have two protection mechanisms:
  - overvoltage protection
    → simply voltage clamp (2V) in parallel to regulator
  - under-shunt-current protection
    → shunt current is sensed and output voltage of regulator is lowered if this shunt current is too small







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SUMMARY

- Serial Powering is Standard Solution for the ATLAS and CMS Pixel Detector Upgrades
  - lower losses on powering cables
  - less material in the detector
  - not DC-DC converters in the detector

- Serial Powering comes with several challenges:
  - parallel powering of front-end chips on modules
  - distribution of high voltage to sensors
  - safe operation of chain in case of noisy front-ends
  - thermal management of the modules
  - right choice of power supplies