DHH preparation for Phase3
DHC Firmware Status

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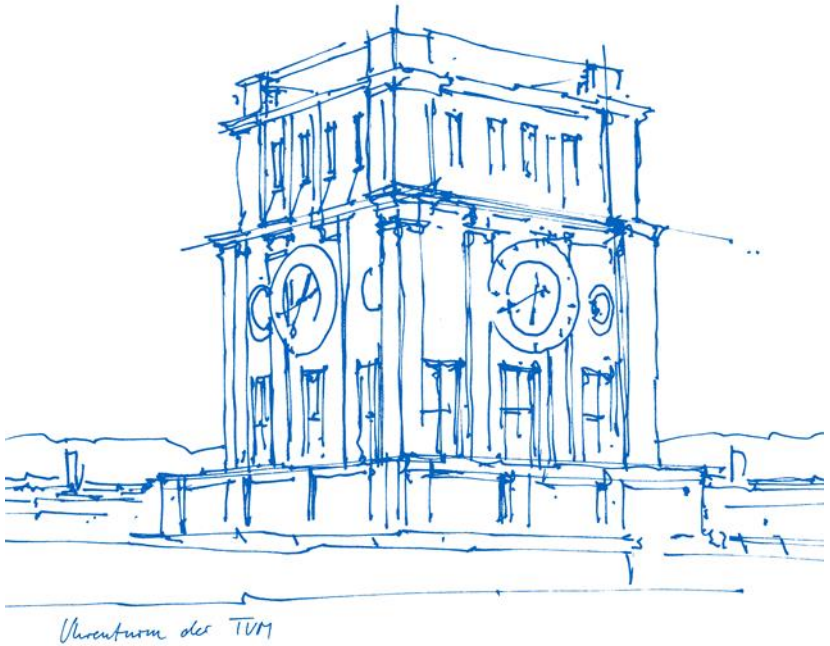


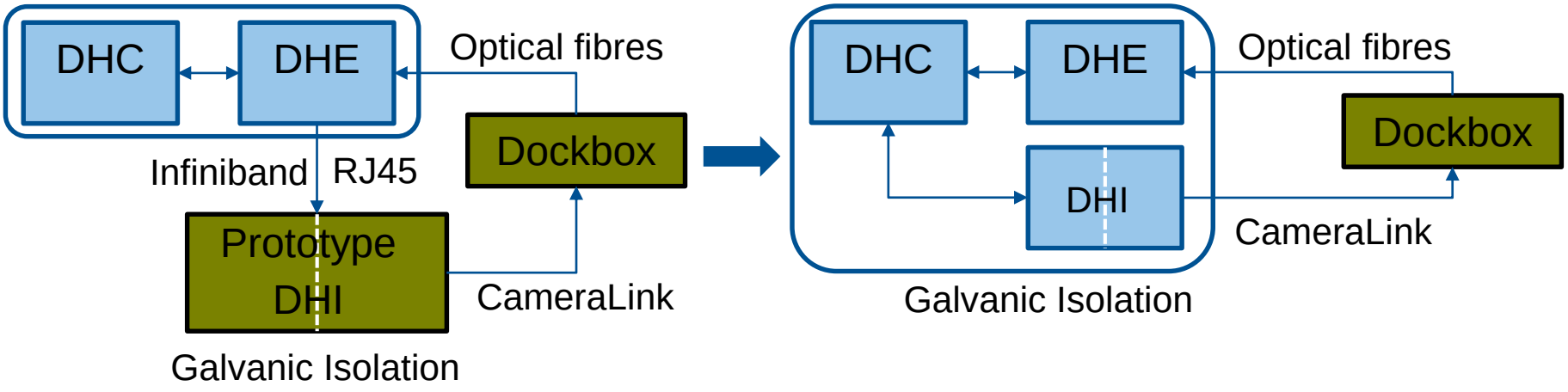
Phase 3 Setup

PXD in phase 3

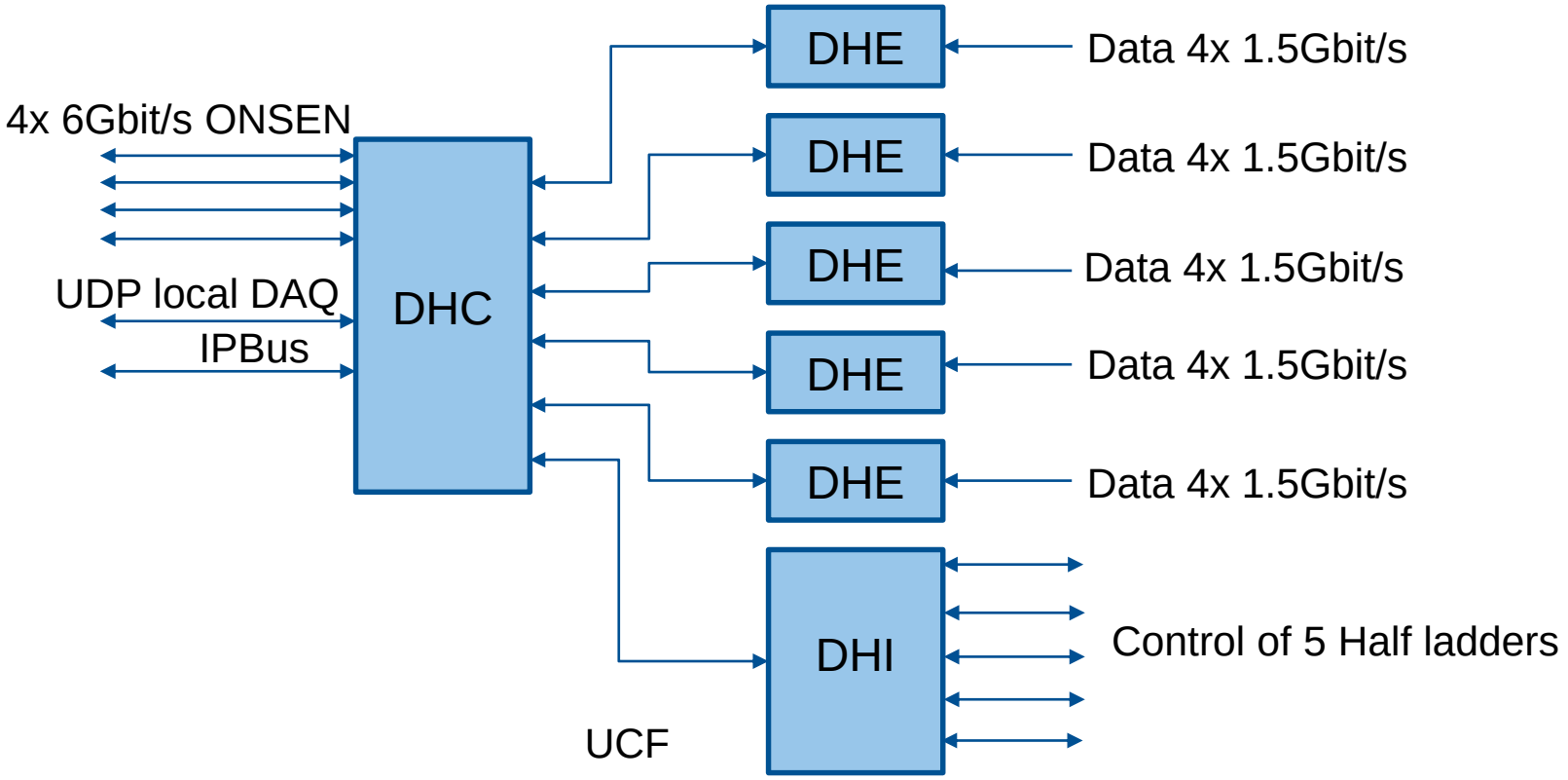
- 8 inner ladders
- 2 outer ladders

  ⇒ 20 half ladders ⇒ 20 DHEs ⇒ 4 DHH systems
- Per DHH: 4 inner and 1 outer module

Difference compared to phase 3: new DHI



DHH system Overview



DHH Installation at KEK

Four full DHH systems installed next to the cleanroom
Running with the full system

One more full DHH system available for DAQ tests

Two more modules shipped but not used and not tested at KEK

Experience during commissioning

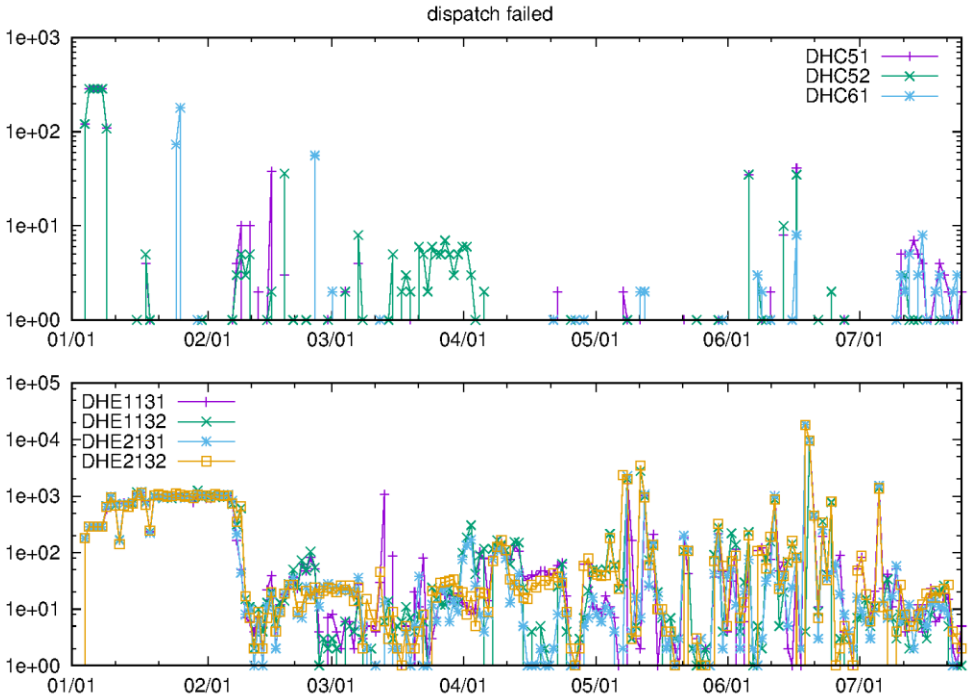
- Initial problems to establish the DHP-DHE connection
  - Caused by dust on the optical interfaces
  - Please take care to cover them carefully during shipment
- Sometimes issues with the DHP-DHE connection
  - Caused by wrong configuration of clocks or DHI registers
  - Hardwire FCK parameters on DHI, flexibility not needed anymore
- Bad optical connection at dockbox PCB

- One JTAG-USB connector broken and replaced by spare RTM

- Issues with DHI clock, fixed (see Igors talk)

Issues with slow control

- Dispatch errors on IPBus:
  - Lost UDP packets
- Does it have any impact?
- Observed already during Phase 2



Issues with slow control

- During commissioning problems configuring the clock-recovery chip
- Only power-cycle of a full carrier recovers
- Maybe observed once during Phase 2

- Problem appeared after running the DAQ test-setup in parallel
- Happens when several clocks are configured in parallel
  ⇒ Issues with the load on pxdioc1?

- DHE IOCs running on shroud (ATOM based, very weak computer)
  ⇒ No problems configuring the clock (Only when configuring more than 10 at once)
- Having the system running for several days => No dispatch errors

```
2018-10-08 15:44:36.665 [info   ] [dhi.p3.4] Dispatch OK again.
2018-10-08 15:55:11.771 [severe ] [dhe.p3.4] Dispatch FAILED by THROWING unknown
2018-10-08 15:55:11.773 [info   ] [dhe.p3.4] Dispatch OK again.
2018-10-08 16:08:08.262 [severe ] [dhi.p3.4] Dispatch FAILED by THROWING unknown
2018-10-08 16:08:08.264 [info   ] [dhi.p3.4] Dispatch OK again.
2018-10-08 16:08:18.063 [severe ] [dhi.p3.4] Dispatch FAILED by THROWING unknown
2018-10-08 16:08:18.064 [info   ] [dhi.p3.4] Dispatch OK again.
2018-10-08 16:10:47.263 [severe ] [dhe.p3.4] Dispatch FAILED by THROWING unknown
2018-10-08 16:10:47.267 [info   ] [dhe.p3.4] Dispatch OK again.
2018-10-08 16:15:22.562 [severe ] [dhe.p3.4] Dispatch FAILED by THROWING unknown
2018-10-08 16:15:22.568 [info   ] [dhe.p3.4] Dispatch OK again.
```

```
2018-09-22 03:39:59.096 [config ] [DHHutils] Clock frequency will be set to 76.23 MHz
2018-09-22 03:39:59.096 [info   ] [I2CDevic] I2C clock prescaler = 0x3f
2018-09-22 03:39:59.098 [info   ] [I2CDevic] I2C Status at initialization = 0x1
2018-09-22 03:39:59.102 [fine   ] [Si5338Dr] Starting Si5338 configuration using initSi5338
2018-09-22 03:40:05.371 [config ] [Si5338Dr] Si5338 Initialized
2018-09-22 05:55:13.937 [config ] [DHHutils] Clock frequency will be set to 76.23 MHz
2018-09-22 05:55:13.937 [info   ] [I2CDevic] I2C clock prescaler = 0x3f
2018-09-22 05:55:13.938 [info   ] [I2CDevic] I2C Status at initialization = 0x1
2018-09-22 05:55:13.942 [fine   ] [Si5338Dr] Starting Si5338 configuration using initSi5338
2018-09-22 05:55:19.772 [config ] [Si5338Dr] Si5338 Initialized
```

DHC status

Link to ONSEN

- Each DHH has 4 optical links to ONSEN
- 3 out of 16 are not stable
- Possible issue: capacitors on DHC and RTM connected serially

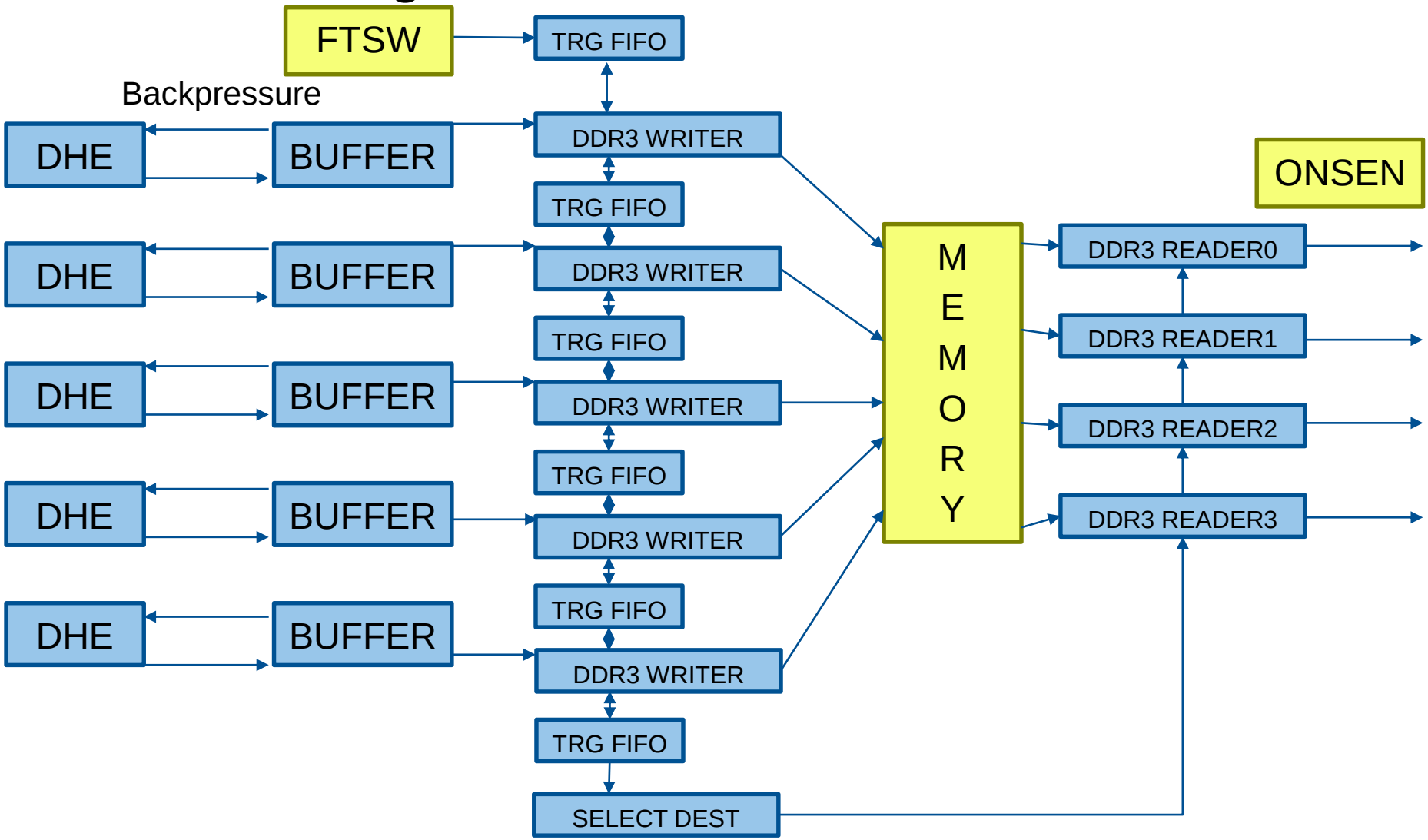
  ⇒ Removal tested in the lab improved the link quality
- Automatic reset procedure implemented

  ⇒ needs to be tested together with ONSEN

- ONSEN links only established during runs
  - Makes debugging more complicated
  - Can we keep them up constantly

- Modifications next week, assistance from ONSEN?

Load balancing



Load balancing

- Introduce backpressure from DHC to DHE
- Introduce BUSY from DHE

- Data written to consecutively into memory for one event
- DHC header only added at the end
- Data to local DAQ only from one output stream

- Development of the code ~60% done
- Still needs time for simulation and testing

Gated mode testing

How to interpret data from FTSW?

Injveto, injkick, injvpos, injvpre, injvlen, injvfull, injvgate

When do these signal come?

Documentation needed

Does standalone FTSW firmware proves that information?