DHH Related Issues and DHE Firmware

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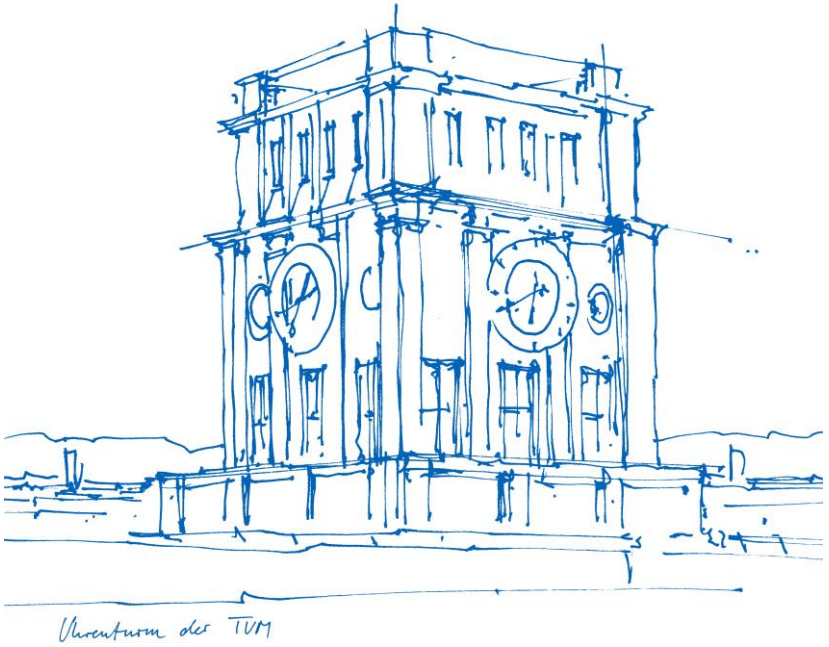
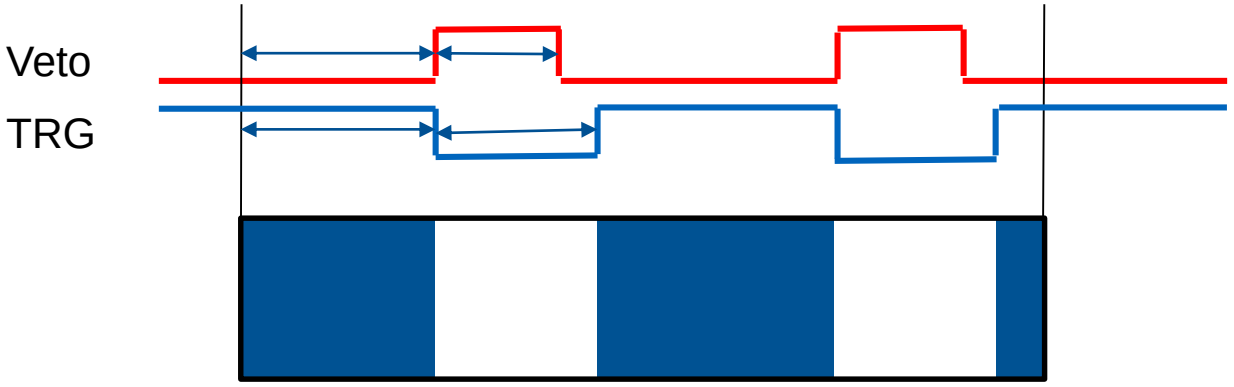


GCK CLOCK Quality in DHI

Firmware for Gated Mode Test

GATED mode test

- Programmable position and length of TRIGGER and GATE(VETO) signals
- Programming parameters:
  - Start of TRIGGER inhibit (8 bits), duration of TRIGGER inhibit (8 bits)
  - Start of GATE(VETO) (8 bits), duration of GATE (8 bits)



Frame length counter, Revo length counter, Veto length counter, TRG length counter

DHE firmware was working fine

DHI firmware was losing synchronization => GCK clock quality ?

Debugging Firmware

Three counters generate REVO cycles

1. GCK clock produced by Silicon Lab chip – main method

   127 MHz(FTSW CLK) * 3 / 5 => 76 MHz => GCK

   REVO = GCK / 1536

2. Xilinx Mixed Mode Clock Manager

   127 MHz * 3 / 5 => GCKref1

   REVOref1 = GCKref1 / 1536

3. Digital Logic

   CLK = 127 MHz / 5 => CLKref2

   REVOref2 = CLKref2 / 512

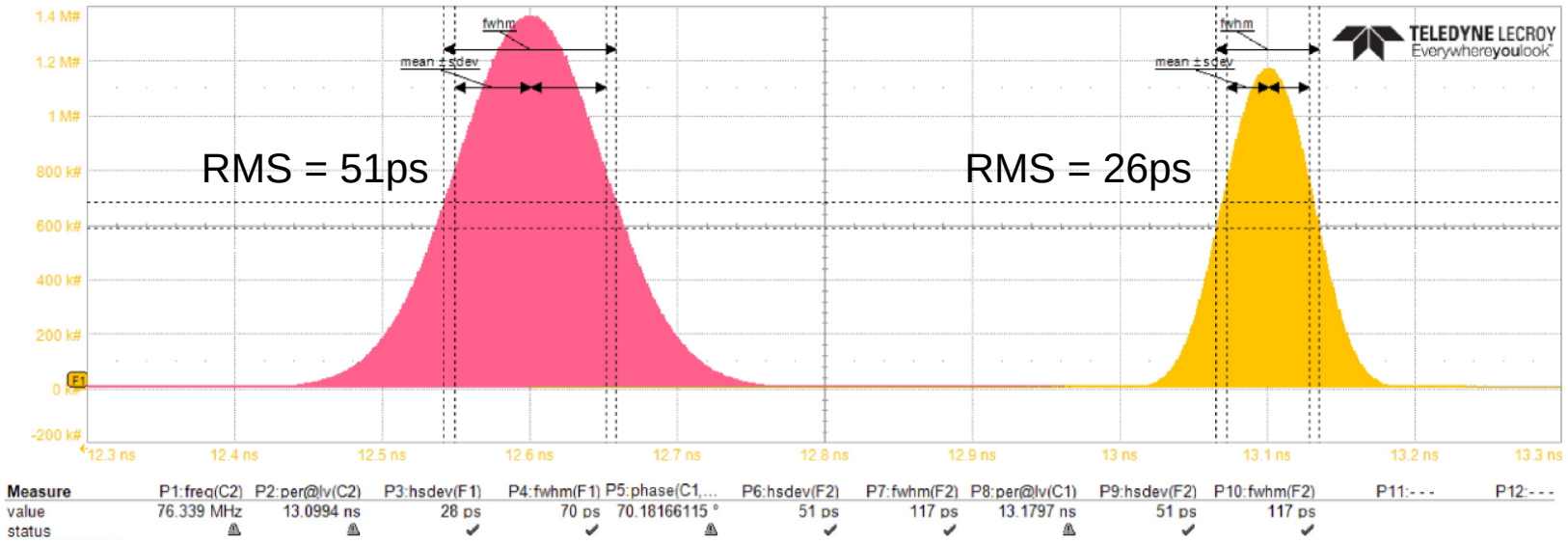
REVO was not working synchronously with REVOref1 and REVOref2

DHI GCK Clock Quality

GCK period jitter

DHI in ATCA shelf

DHI in VME crate



Problem was originated in DCDC converter in DHI

Additional 47uF capacitors at DC-DC inputs reduced jitter to 30 ps

All DHIs at KEK were modified accordingly

Glenair Optical Link's Tests

Test of all 40 links between Dockbox PCB and DHH

- Glenair transmitters are light source
- Light power in MPO connector at DHH

Results :

- 37 links have expected value of 0.2-0.3 mW
- 3 links were below 0.1mW and required replugging of fiber to improve value to above 0.2mW

Quality of optical connection is a point of concern

Glenair offers PULL-PROOF "P" type connector and not PULL-PROOF "N" type.

Glenair comment :

Pool-proof does not provide locking of connector

<u>For final installation quality of optical contacts to be measured!!!</u>

High Speed Link Stability

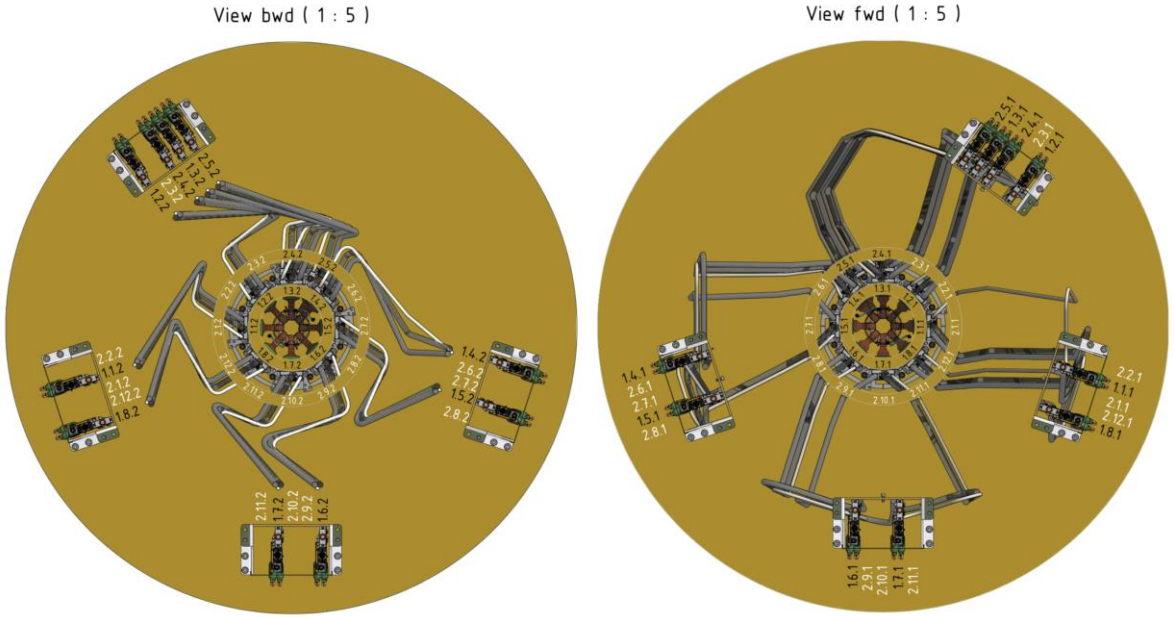
Improving GCK jitter performance in DHI improved stability of high speed links

Links are not stable when only DHPTs are powered.

Powering of full module makes links more stable. Similar effect was observed during phase2 ???

Link stability issue should be investigated further

Wiring of Optical Links for Phase 3



Dock boxes are arranged differently than was anticipated :

Instead of 5xDB PCB/box we have 4xDB PCB/box – 16 fibers, 2xDB PCB/box – 8 fibers

Two type of optical cable x12 and x8.

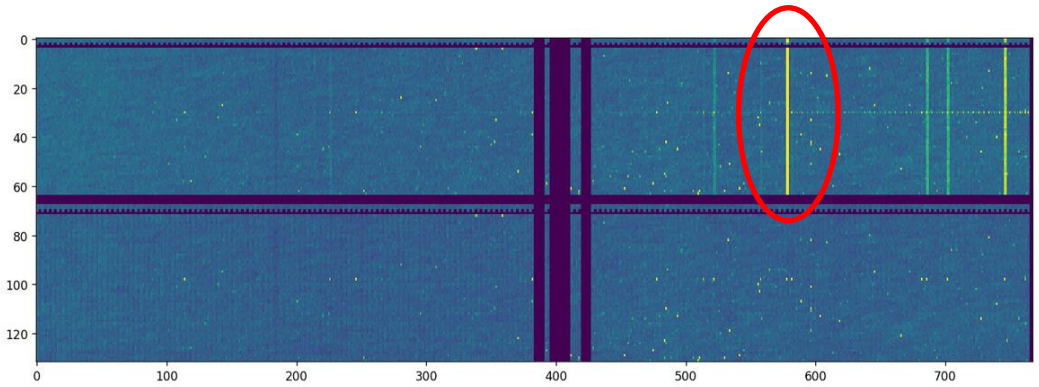
Possible wiring to DHH :

- 5 DHH with 4 DHE in each DHH. One DHH will have FWD and BWD modules
- 4 DHH + Patch cables MPO-LC ⇔ LC-MPO restore original reading scheme

DHE Firmware

DHE Overlapping Trigger Firmware Status

Last firmware version was released on 26.06.18
It was tested during one Lumi run. Readout was stable.
A problem was observed:



Top part shows all hits.
Second half is the same DHPT data but without last hit in frame.

Firmware test to be continued.

DHE Overlapping Trigger Firmware Status

Following tests to be performed :

- fixed hit pattern with different occupancy from 0.5 to 2.5 % occupancy
- random trigger test up to 30 kHz and 1% occupancy

Known limitations:

- 2.5 Gb/s maximum data rate between DHE and DHC
- At 30 kHz trigger rate detector occupancy shall be below 1%
- Exceeding maximum data rate causes data loss

Firmware improvements:

- add DDR3 memory to provide deeper buffer and data skew for data balancing
- Back pressure from DHC
- BUSY signal from DHE to DHC to block FTSW when memory buffer collects N events
- maximum event size will be limited to 25% occupancy

I expect to complete firmware by end of October and test it at DESY in November

Test Stand at DESY

We asked collaboration to install one full DHH at DESY with 5 detector modules attached

Why it's needed?

DESY has an infrastructure : Slow Control, BonnDAQ, PSs, ATCA shelf, cables
PXD schedule at KEK is very busy

- detector commissioning with SVD, cosmic test, reallocation to detector and commissioning again

  => no time or very limited time for read out tests

Tasks to be done at DESY :

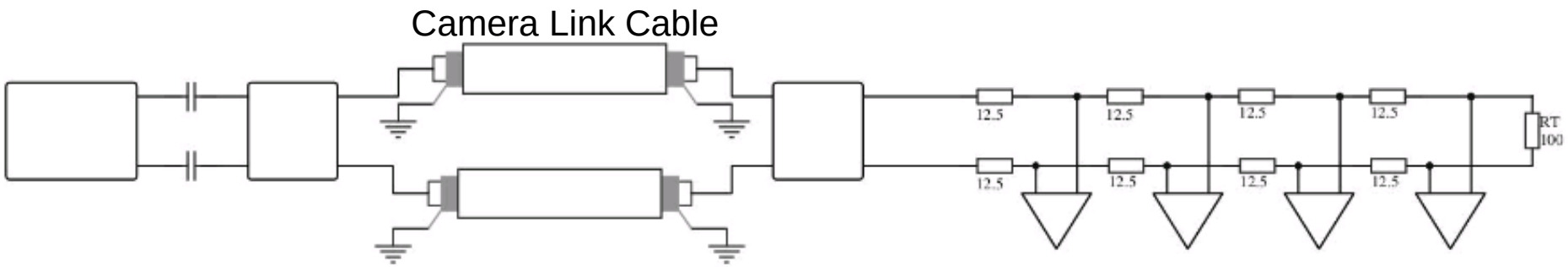
- Test of DHE firmware for 30kHz readout
- Test of DHC firmware for load balancing
- Keep the system in a running state to address any issue discovered at KEK

Plan is to install the stand and make it working this week

GCK Transmission Line

GCK Transmission Line

EMCM module.

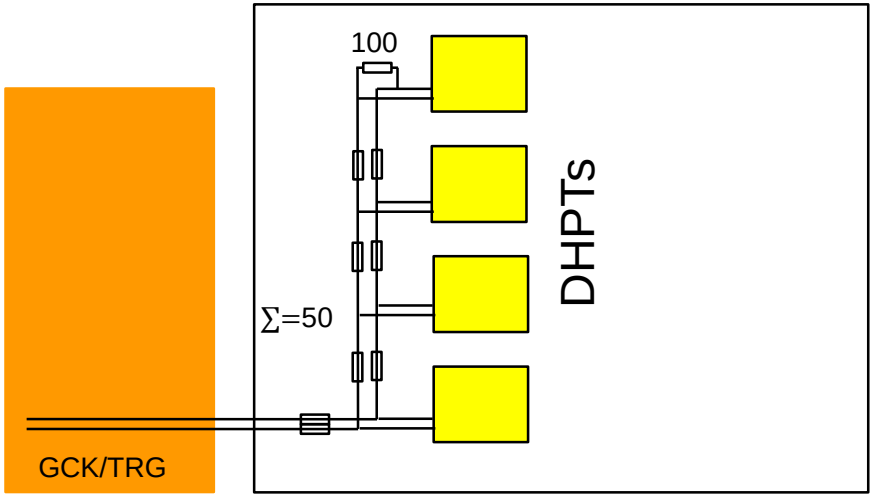


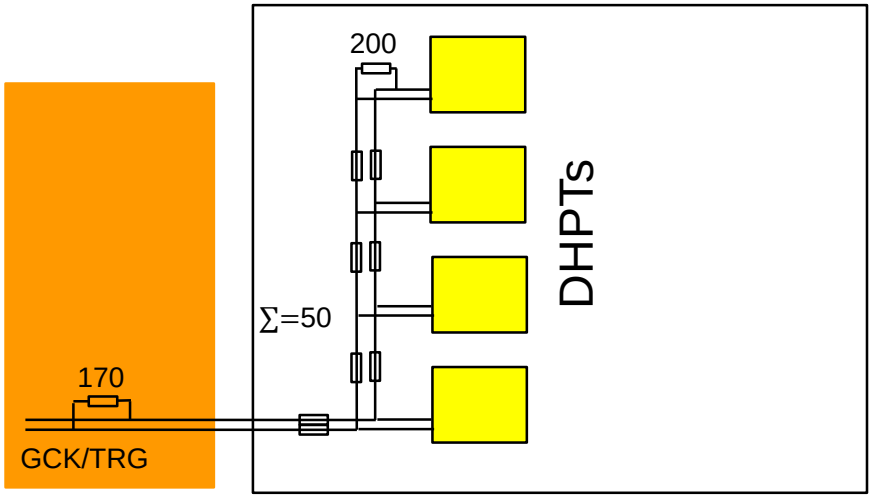
GCK line has additional serial resistance of about 100 Ohm in EMCM
Real detector module is improved but still additional serial resistance is about 50 Ohm

Due to serial impedance of wiring on detector module transmission line is terminated with wrong impedance and cause reflections.

Possible Improvement of GCK and TRG signals' problem

1. Reduce serial resistance of traces for GCK signal on detector module
2. Match line impedance
   - increase termination resistor to 200 Ohm => increase signal swing and reduce effect of serial resistance
   - Add 170 Ohm resistor to match resistance to 100 Ohm of transmission line





THANK YOU