Gated Mode of Half Shells

PXD Workshop

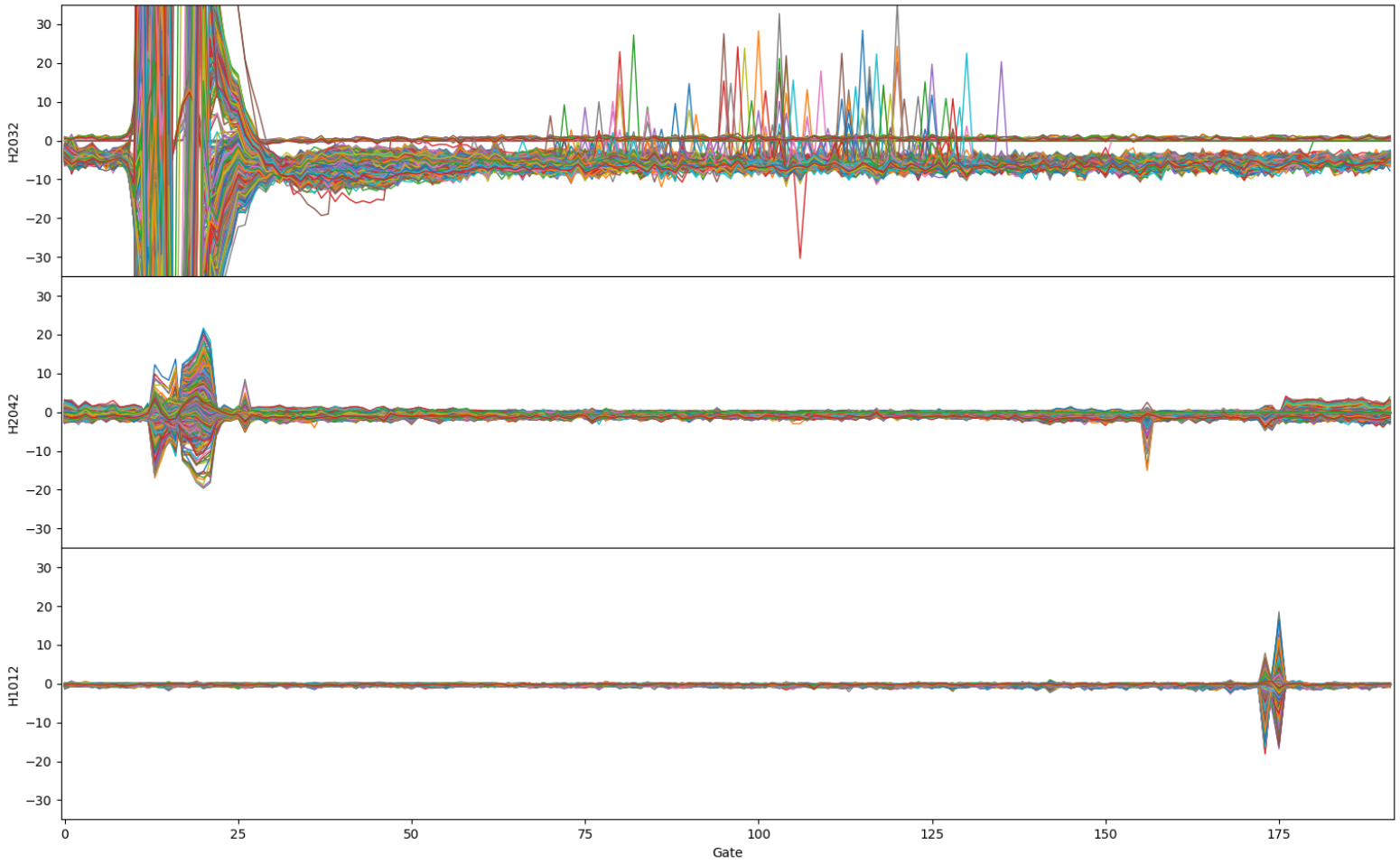
Felix J. Müller on behalf of the DESY PXD Team
Hamburg, 09.10.2018

DESY.

Gated Mode at DESY.

- Performed transition to more realistic GM operation
  - GM triggered by DHI-firmware
  - Automatic upload of GM switcher sequence with DHH-sequence IOC
- Single module tests
  - Checked influence of GM length on currents
- Run GM on 9 modules simultaneously on HS 1
- Ped estals for all 9 modules
- zs-data with and w/o threshold for 1 DHH card
  - Asynchronous trigger between DHH causes random crosstalk interference

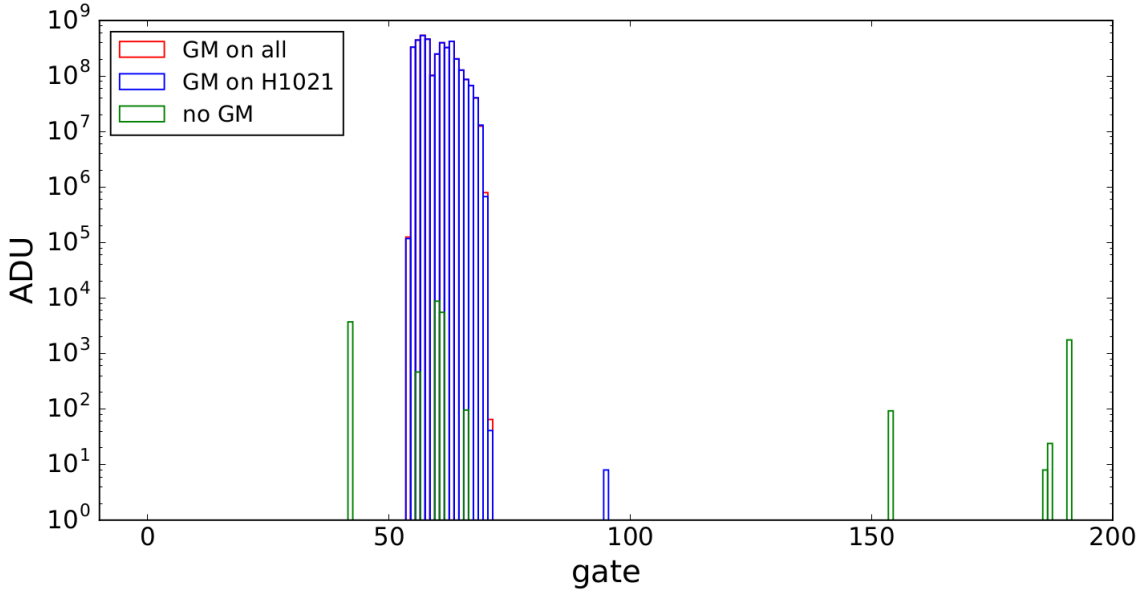
Crosstalk.

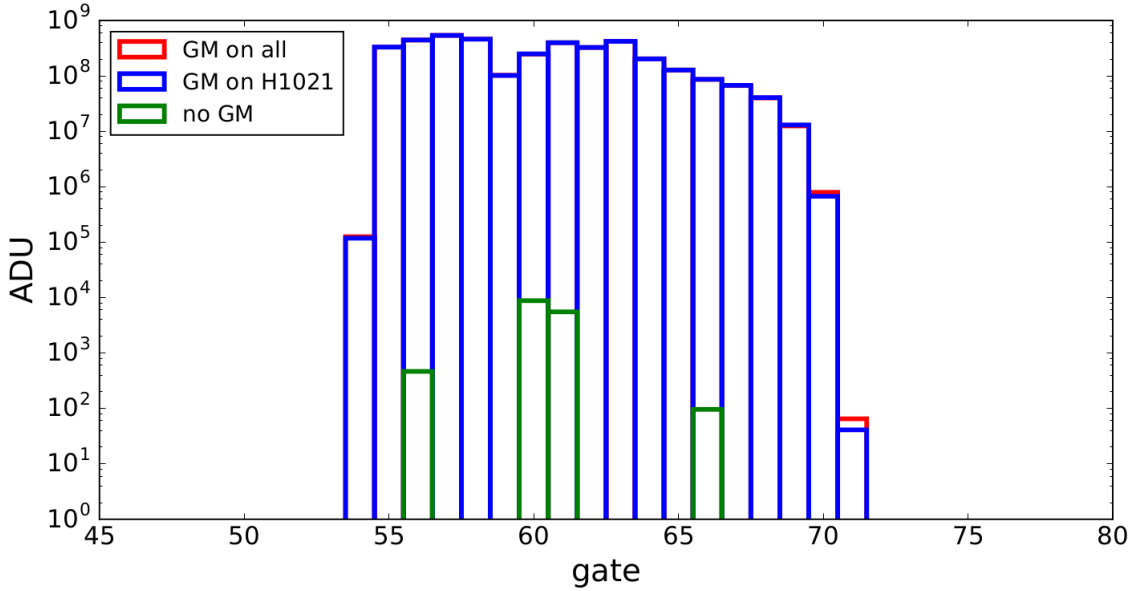

H2032
H2042
H1012
30
20
10
0
−10
−20
−30
0
25
50
75
100
125
150
175
Gate

Crosstalk.

- GM on one module influences the pedestals on other modules
  - First observed at KEK
  - Only observed within one DHH
- All modules are in GM at the same time → no problem?
  - Longer pedestal oscillations?
- zs-data with GM on H1021 only and all modules on the DHH
- Small increase at gate 71 due to crosstalk
  - 5000 frames and less than 100 hits

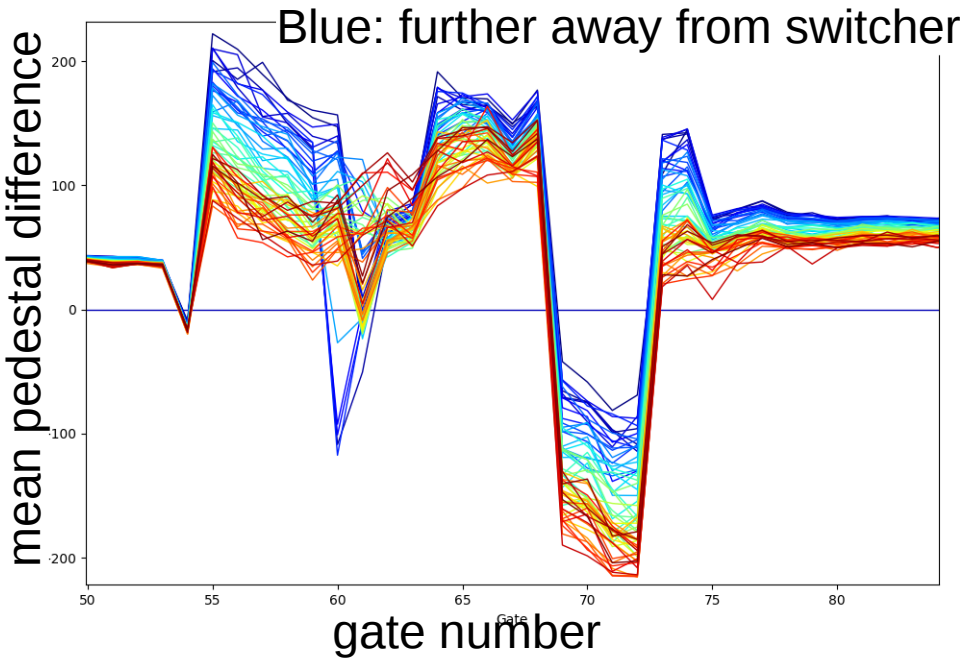
    → No real difference for data taking

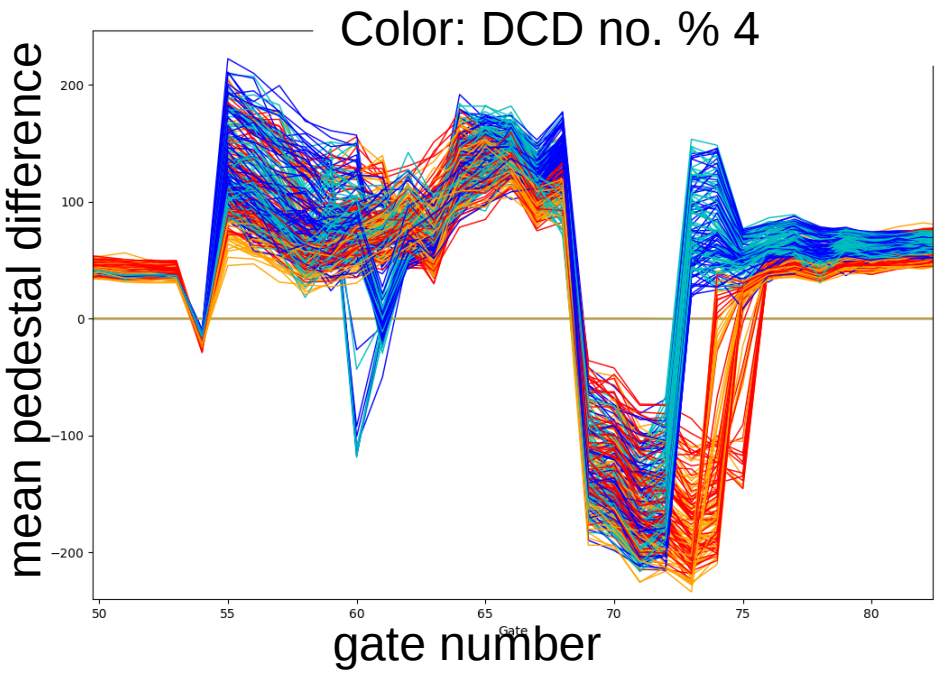


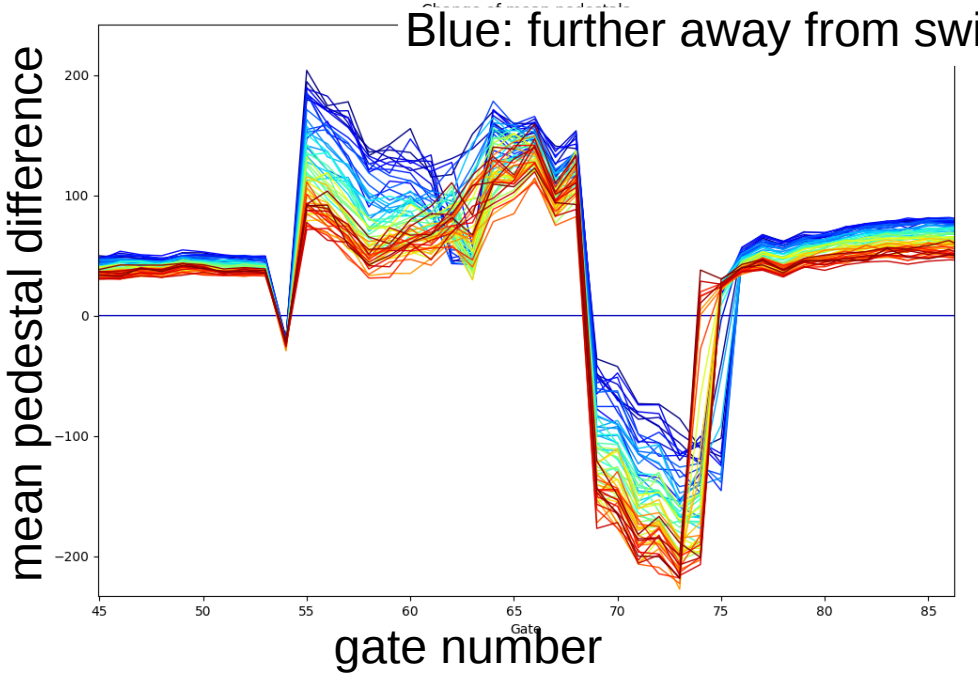


Pedestal Fluctuations.

- Two type of systematic behaviors
  - Earlier and consistent transition but overshoot
  - Later and more fluctuating transition but no overshoot

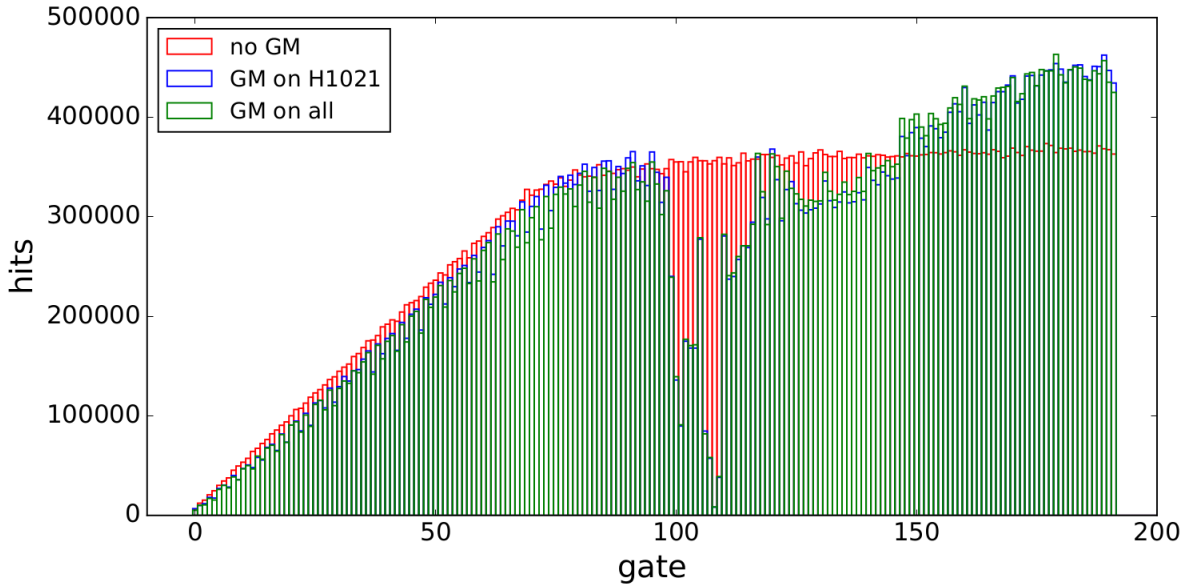


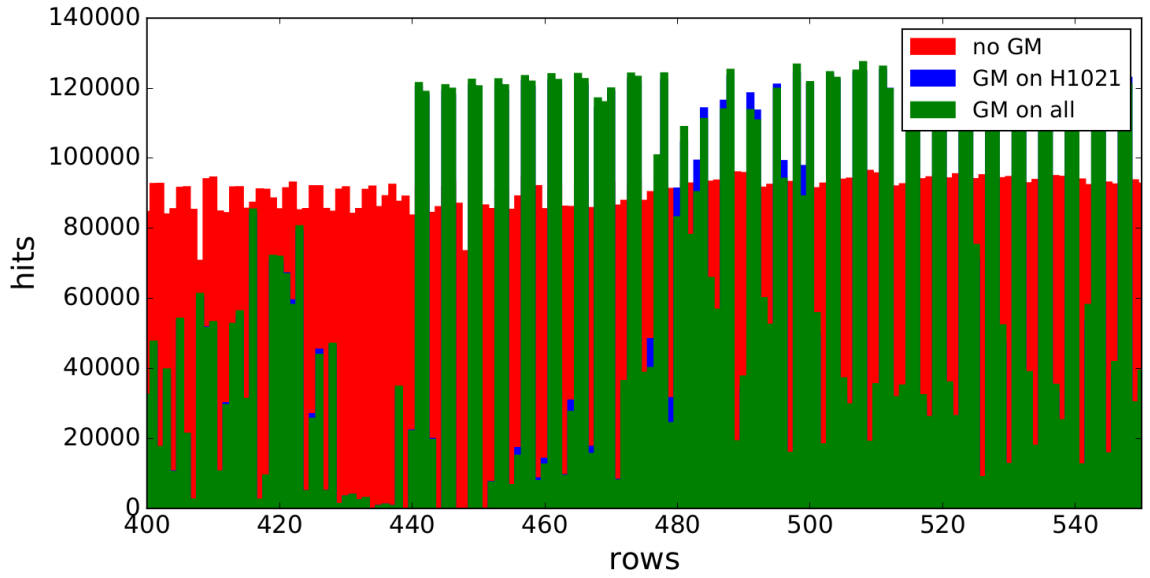




Pedestal Fluctuations.

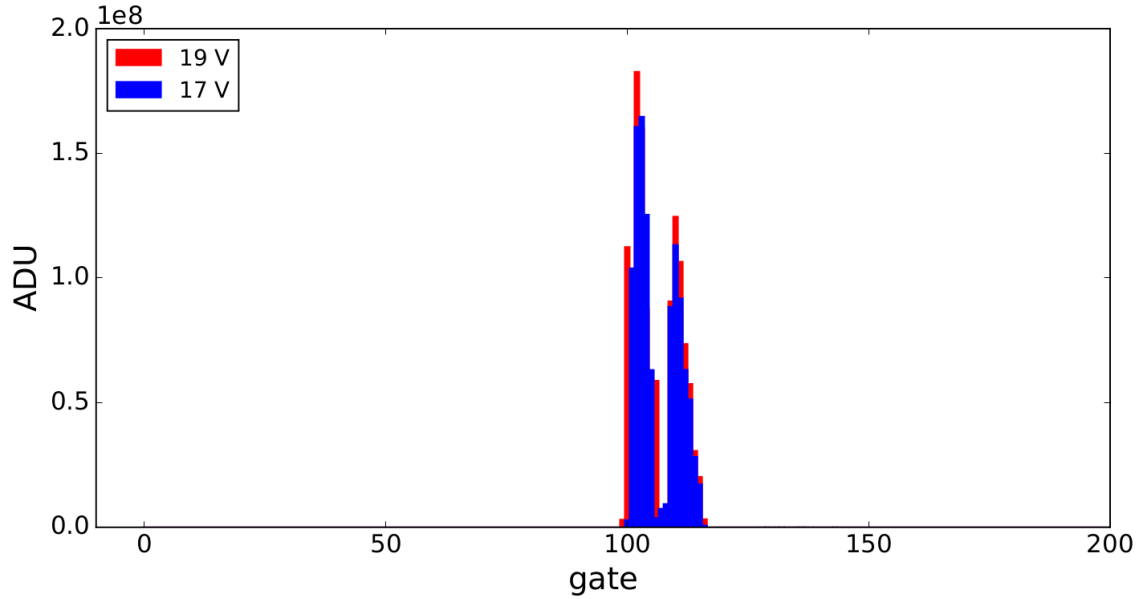
- zs-data with threshold 0
  - Linear rise due to too large occupancy
  - Reduced number of hits during the GM at gate 54 (6 gates long) due to bug of pedestal offset
- Fake hits for overshoot drain lines
- Lost hits for undershoot drain lines
- Influence on resolution/fake hit rates must be further investigated

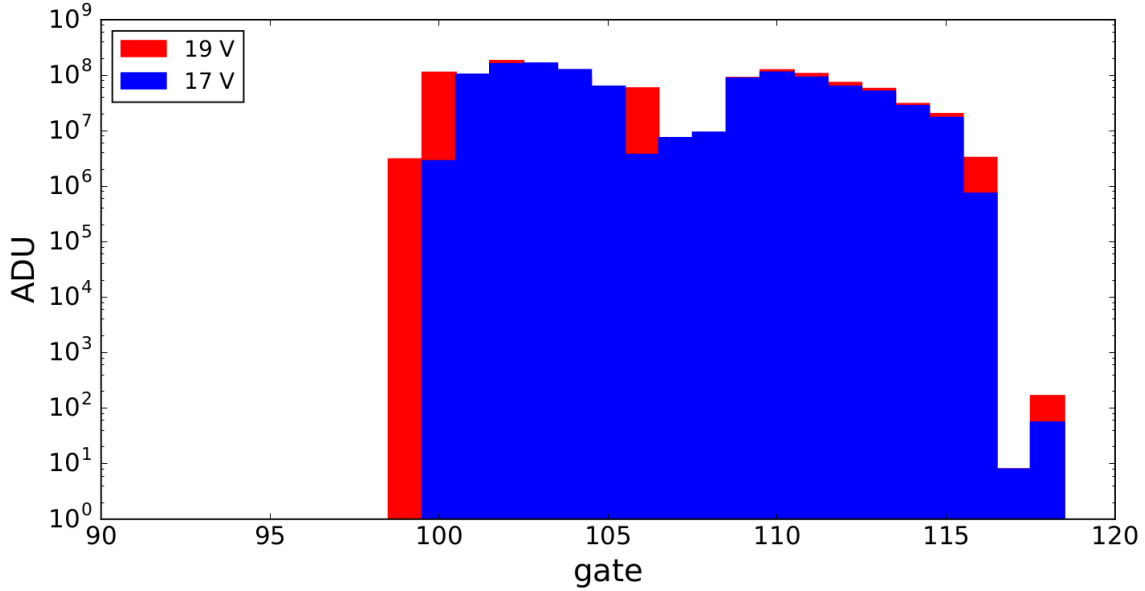




Lowering Clear-on.

- Christian suggested to use 17 V Clear-on instead of 19 V to reduce pedestal fluctuation
- Only small change in pedestal fluctuation time
- Additional charge visible at gate 99 for 19 V measurement
  - Reproducible or software/firmware effect?





KEK.

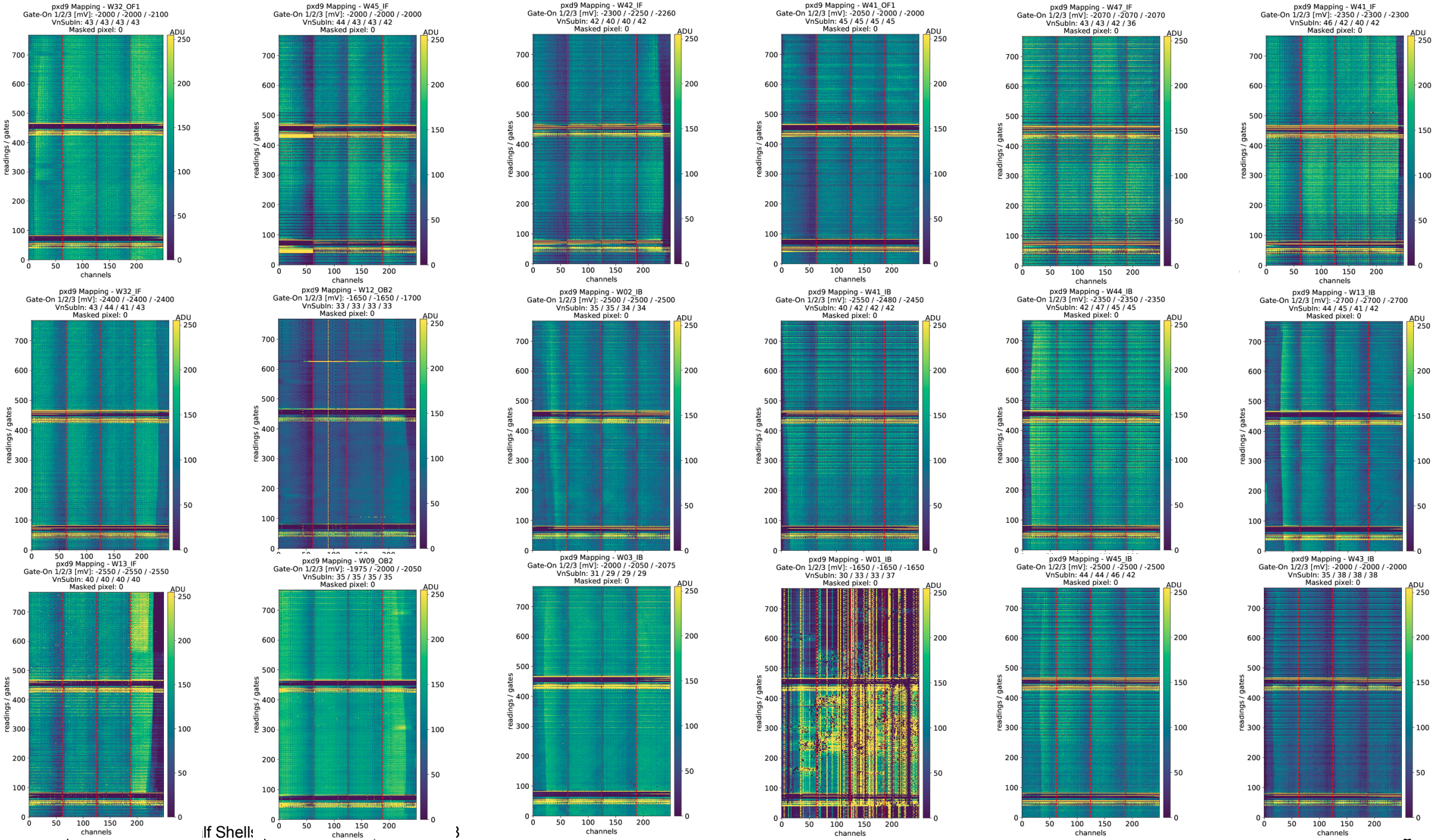
KEK Tests.

- Longer struggle with slow-control/readout/epics
  - Why different behavior compared to DESY setup?
- Implementation of hot-fixes
  - Epics shows values for DHC & DHI which are set as PVs but are not applied to hardware

    → included state machine for DHC & DHI
  - Clock programming by the DHH-sequencer caused problems in the DHH

    → manual programing of the clocks and removal from DHH-sequencer
  - Automatic check of the GM switcher sequence in the DHH-sequencer failed

    → introduced longer timeout after writing of the GM switcher sequence
- Finally: 18 Modules running in GM at the same time
  - H1011 (W03_IF) excluded due to high clear currents
    - Which limits are acceptable? Currently: 100 mA for clear-off/clear-on
  - H1081 (W02_IF) excluded due to a problem with the DHE


pxd9 Mapping - W32_OF1
Gate-On 1/2/3 [mV]: -2000 / -2000 / -2100
VnSubIn: 43 / 43 / 43 / 43
Masked pixel: 0
pxd9 Mapping - W45_IF
Gate-On 1/2/3 [mV]: -2000 / -2000 / -2000
VnSubIn: 44 / 43 / 43 / 42
Masked pixel: 0
pxd9 Mapping - W42_IF
Gate-On 1/2/3 [mV]: -2300 / -2250 / -2260
VnSubIn: 42 / 40 / 40 / 42
Masked pixel: 0
pxd9 Mapping - W41_OF1
Gate-On 1/2/3 [mV]: -2050 / -2000 / -2000
VnSubIn: 45 / 45 / 45 / 45
Masked pixel: 0
pxd9 Mapping - W47_IF
Gate-On 1/2/3 [mV]: -2070 / -2070 / -2070
VnSubIn: 43 / 43 / 42 / 36
Masked pixel: 0
pxd9 Mapping - W41_IF
Gate-On 1/2/3 [mV]: -2350 / -2300 / -2300
VnSubIn: 46 / 42 / 40 / 42
Masked pixel: 0
pxd9 Mapping - W32_IF
Gate-On 1/2/3 [mV]: -2400 / -2400 / -2400
VnSubIn: 43 / 44 / 41 / 43
Masked pixel: 0
pxd9 Mapping - W12_OB2
Gate-On 1/2/3 [mV]: -1650 / -1650 / -1700
VnSubIn: 33 / 33 / 33 / 33
Masked pixel: 0
pxd9 Mapping - W02_IB
Gate-On 1/2/3 [mV]: -2500 / -2500 / -2500
VnSubIn: 35 / 35 / 34 / 34
Masked pixel: 0
pxd9 Mapping - W41_IB
Gate-On 1/2/3 [mV]: -2550 / -2480 / -2450
VnSubIn: 40 / 42 / 42 / 42
Masked pixel: 0
pxd9 Mapping - W44_IB
Gate-On 1/2/3 [mV]: -2350 / -2350 / -2350
VnSubIn: 42 / 47 / 45 / 45
Masked pixel: 0
pxd9 Mapping - W13_IB
Gate-On 1/2/3 [mV]: -2700 / -2700 / -2700
VnSubIn: 44 / 45 / 41 / 42
Masked pixel: 0
pxd9 Mapping - W13_IF
Gate-On 1/2/3 [mV]: -2550 / -2550 / -2550
VnSubIn: 40 / 40 / 40 / 40
Masked pixel: 0
pxd9 Mapping - W09_OB2
Gate-On 1/2/3 [mV]: -1975 / -2000 / -2050
VnSubIn: 35 / 35 / 35 / 35
Masked pixel: 0
pxd9 Mapping - W03_IB
Gate-On 1/2/3 [mV]: -2000 / -2050 / -2075
VnSubIn: 31 / 29 / 29 / 29
Masked pixel: 0
pxd9 Mapping - W01_IB
Gate-On 1/2/3 [mV]: -1650 / -1650 / -1650
VnSubIn: 30 / 33 / 33 / 37
Masked pixel: 0
pxd9 Mapping - W45_IB
Gate-On 1/2/3 [mV]: -2500 / -2500 / -2500
VnSubIn: 44 / 44 / 46 / 42
Masked pixel: 0
pxd9 Mapping - W43_IB
Gate-On 1/2/3 [mV]: -2000 / -2000 / -2000
VnSubIn: 35 / 38 / 38 / 38
Masked pixel: 0
ADU
readings / gates
channels

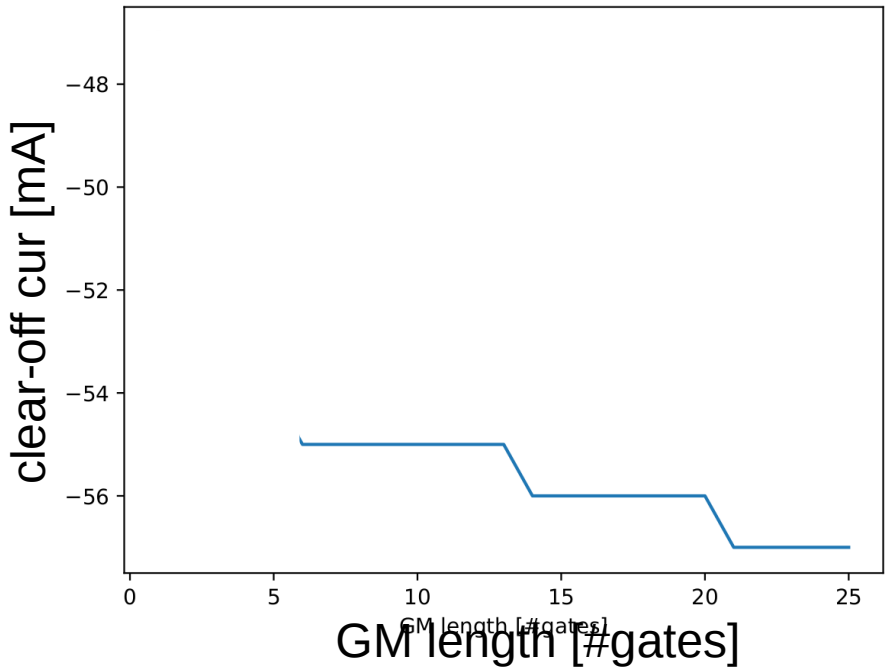
Summary.

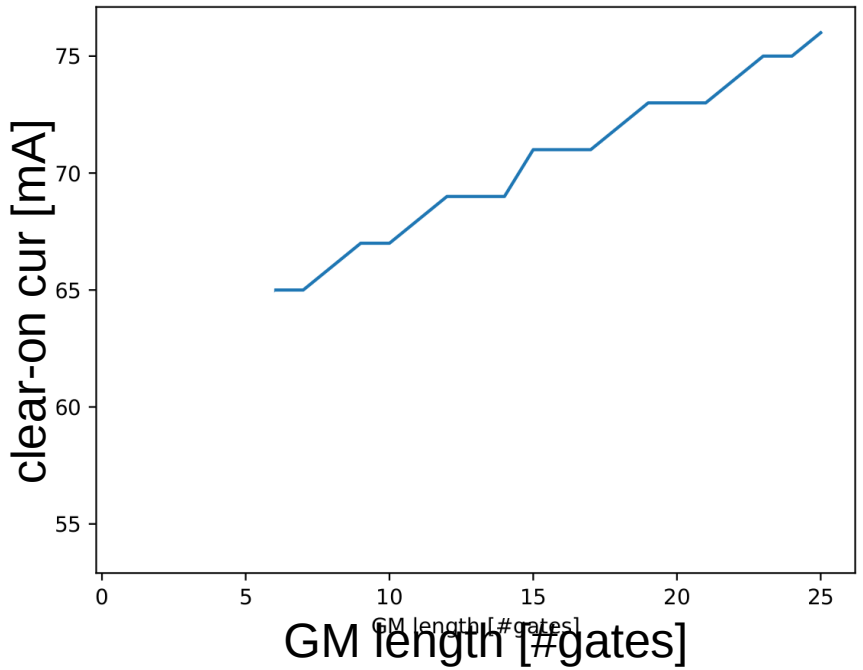
- All but one module were operated successfully with 2 GM per frames
  - System is in a state where GM tests can be done everywhere with ATCA DHH crate
  - We have to decide how to handle H1011
- Conducted first qualitatively measurements to get experience with GM operation
- Make a detailed plan on what we need to measure
  - Which parameters?
  - Measurements with GM and a source (at DESY)?
  - Test outer start/stop signal?
  - How much time for GM test and cosmic runs?

Backup.

Influence on Currents.

- Two GM per frame for module W05_OB1
- w/o GM:
  - Clear off -21 mA
  - Clear on 27 mA





Influence on Currents.