Upgrade of the PreProcessor System for the ATLAS LVL1 Calorimeter Trigger: From ASICs to FPGA

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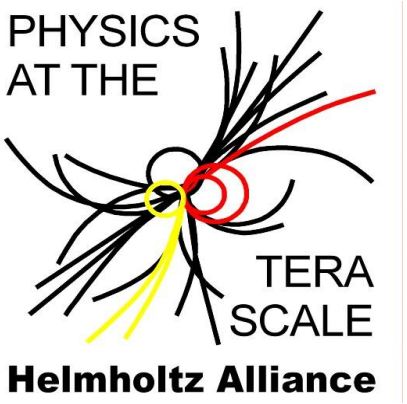

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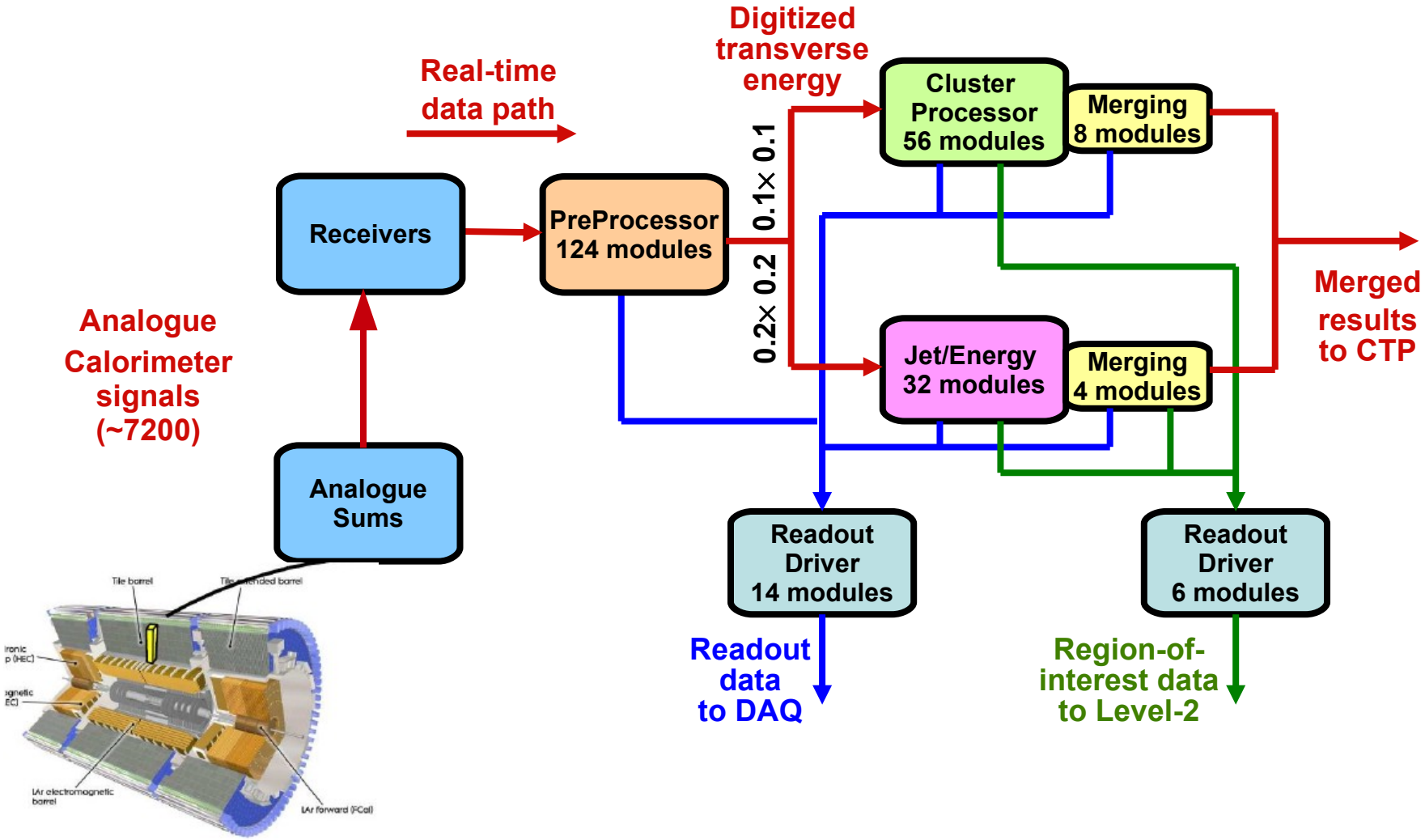
Outline

- ATLAS Level-1 calorimeter trigger
- PreProcessor Module
- “Phase 0” Upgrade. New MCM: from ASICs to FPGA
  - Motivation and Ideas
  - FPGA Development board for testing
  - PHOS4 replacement: FPGA for time-adjustment
  - FPGA as LVDS serialiser
- Conclusions

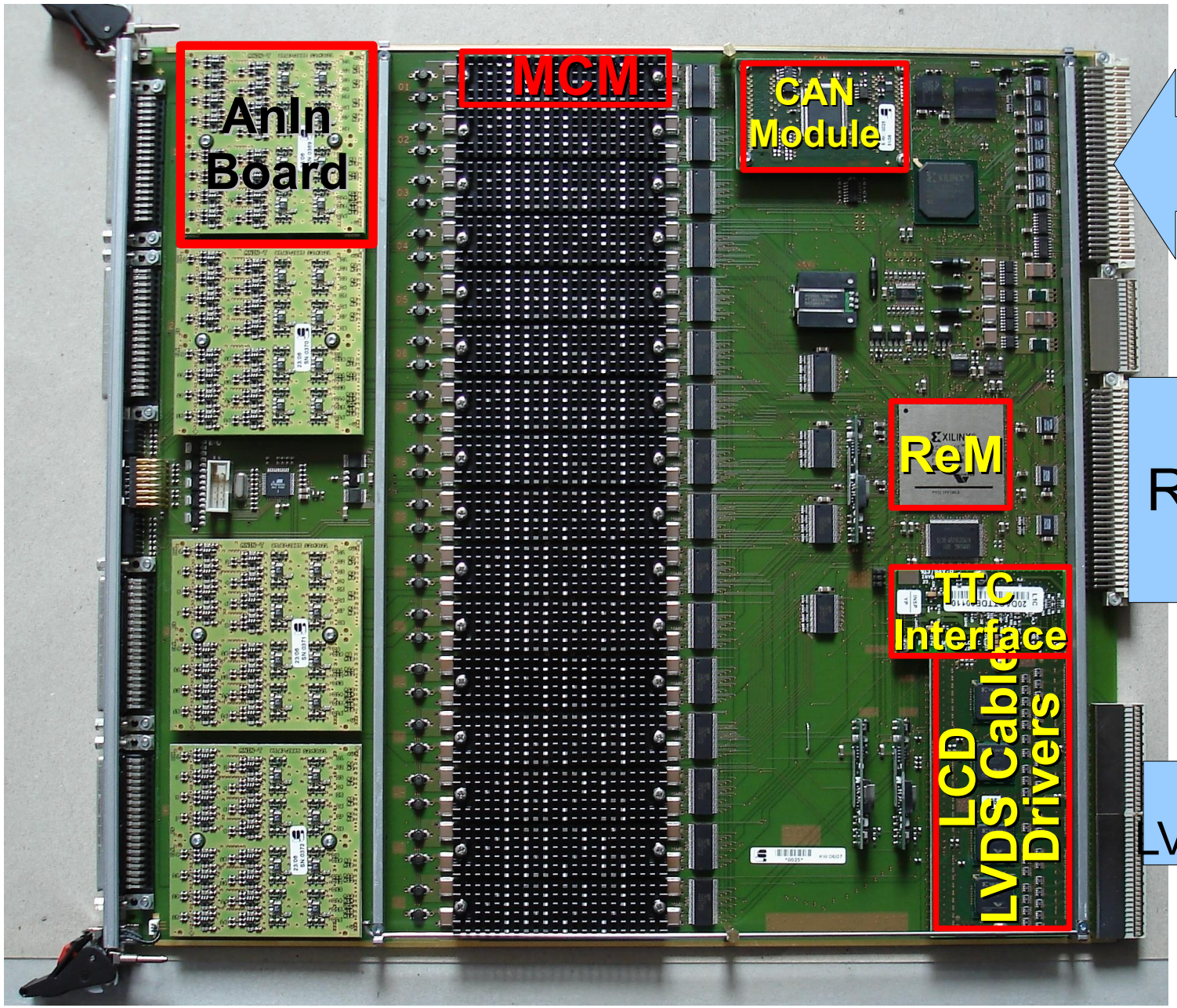
ATLAS Level-1 Calorimeter Trigger (L1Calo)



Features:

Real-time Path: Fixed Latency (~1μs); Pipeline processing; Massive parallelism; FPGA and ASIC based

Preprocessor Module

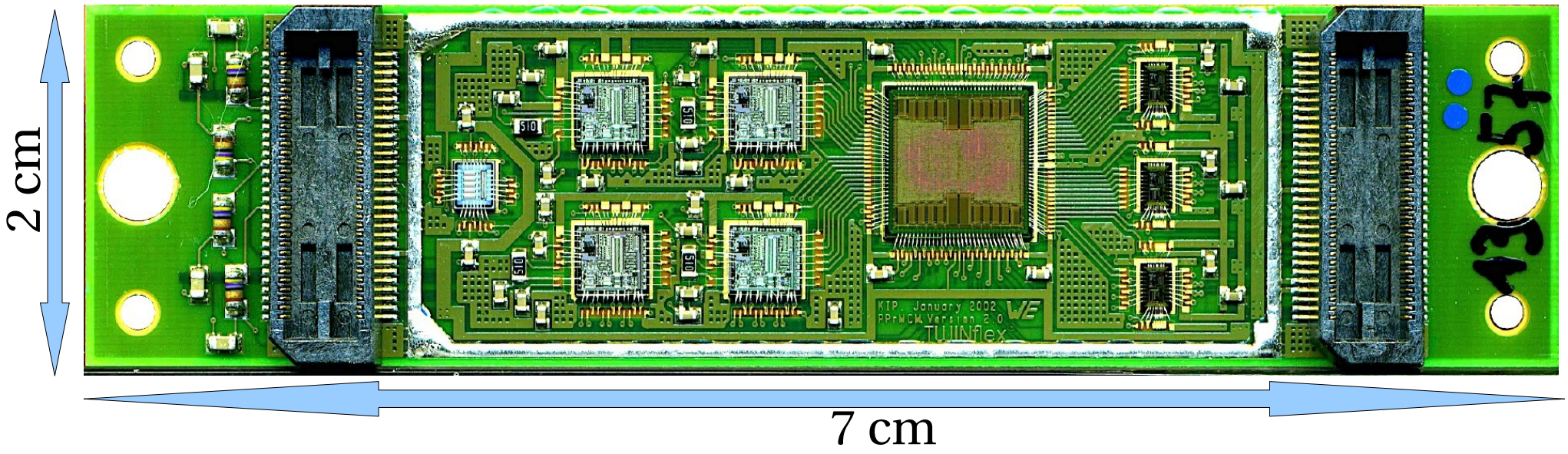


VME

RGTM to DAQ

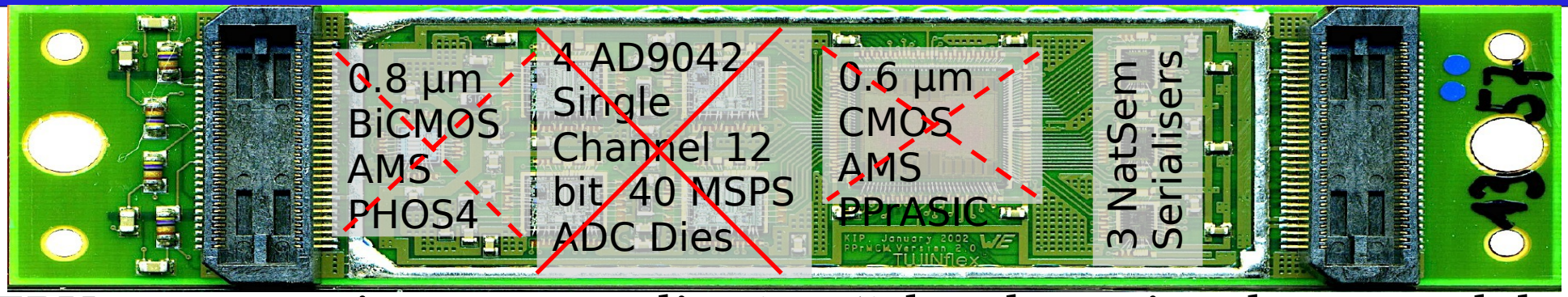
Electrical LVDS to CP/JEP

PPr Multichip Module (MCM)



- 10(12)-bit, 40 MHz, 3 BC delay, 595 mW per channel digitisation
- 1 ns sampling time adjustment
- BCID (2 methods)
- Look-up table based calibration
- Histogramming, playback
- Jet-summing
- 400(480) Mbit/s serialisation
- 13 BC ticks from analog in to Jet (summed) serial output

New MCM. Motivation



VERY conservative spare policy(50%) has been implemented, but, if we would like to produce more MCMs

9 ASIC Dies on each of 2048 MCMs in the System

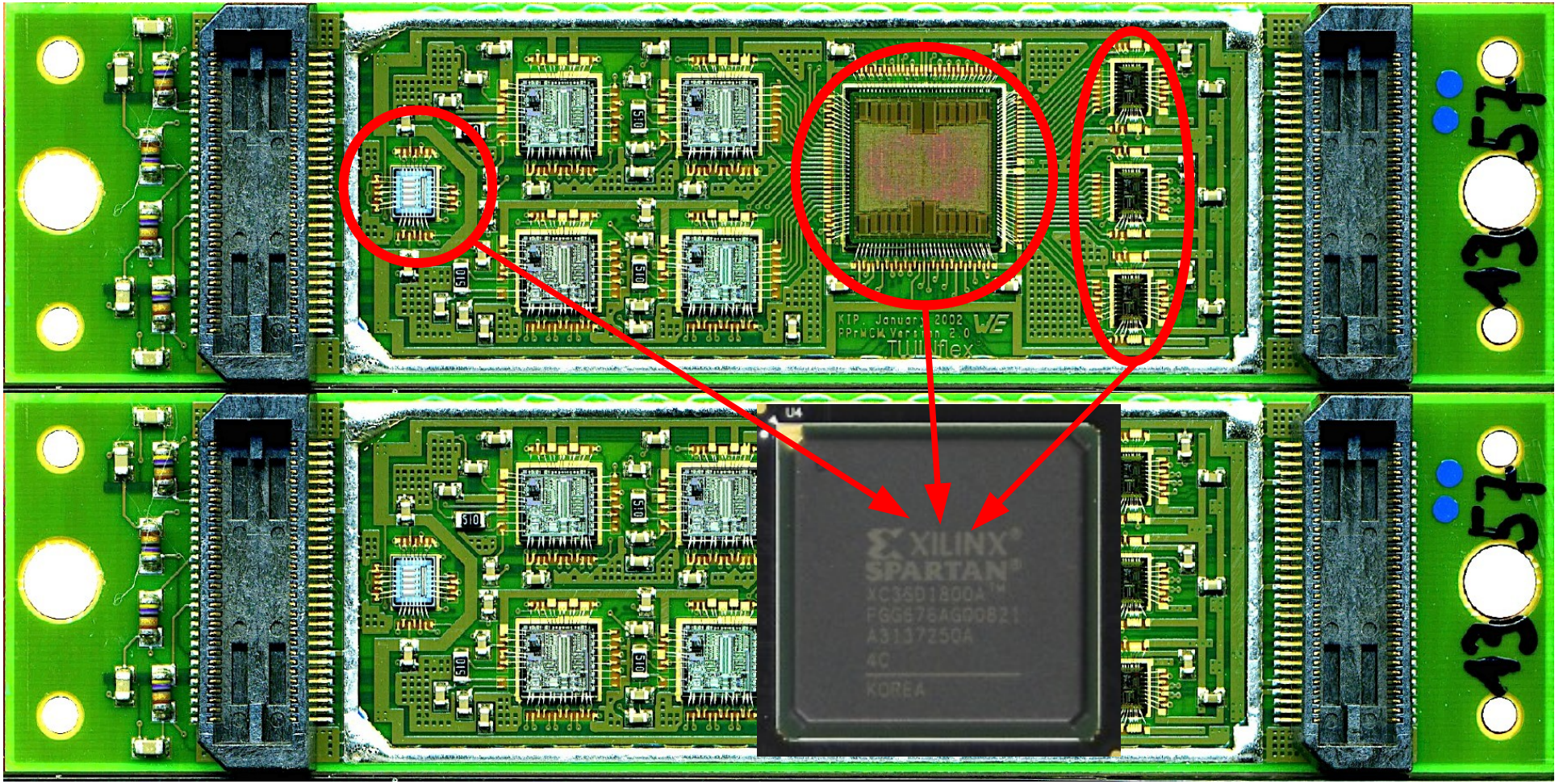
- PHOS4 (time-adjustment chip with 1ns resolution): GDSII available, process (still) available, success uncertain, no support
- AD9042: n/a as unpackaged die anymore, packaged version prohibitive size
- PPrASIC: Verilog available, process (still) available, GDSII available, outdated technology (0.6 µm)
- Serialisers: available, new pin compatible DS92LV1023E recommended by NatSem

“Phase 0” – New MCM

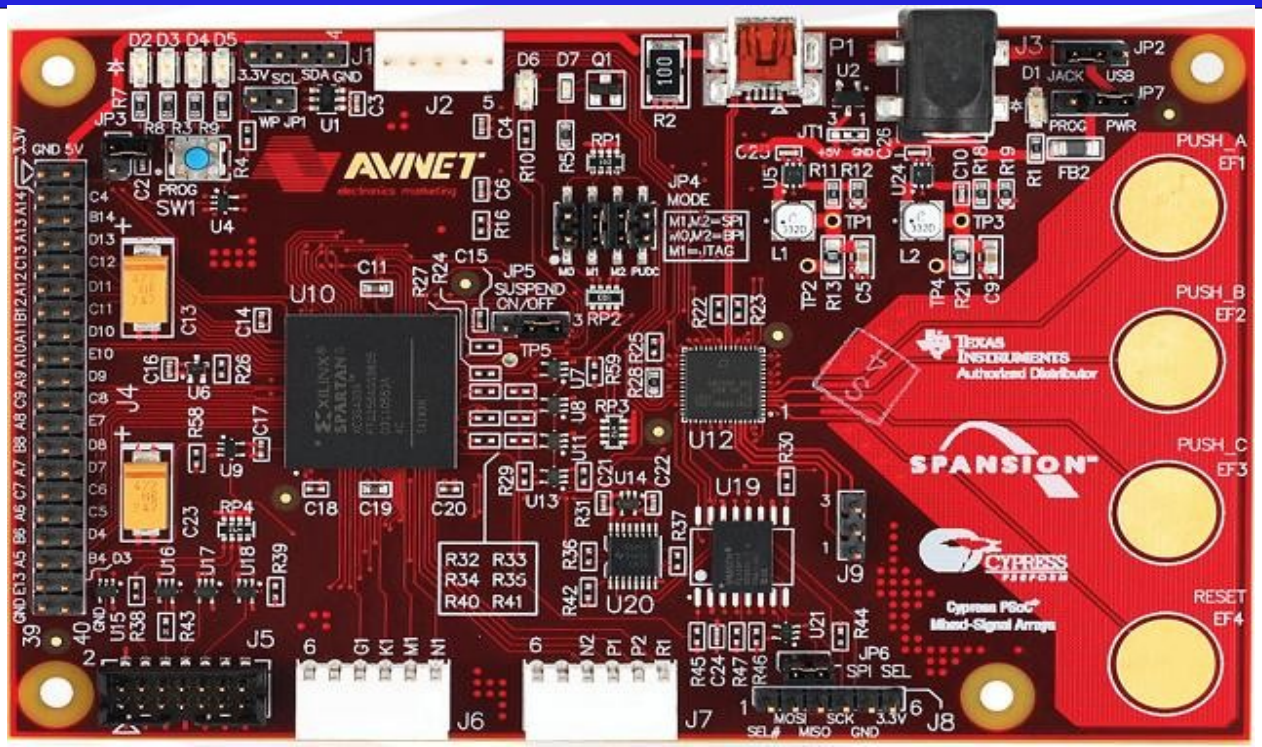
- We would like to develop a pin-, size- and latency-compatible substitute for the MCM based on today’s components.
- Candidates for the main parts are two AD9218 (dual 105 Mhz FADC) and a Spartan-3A(or 6)
  - Spartan-6 currently has limited availability
  - Spartan-3A (for ex. XC3S1400A) can be used for design and tests now
- I will not touch analog part and ASIC itself in this talk

FPGA on MCM

- PHOS4 functionality and LVDS serialisers inside FPGA?



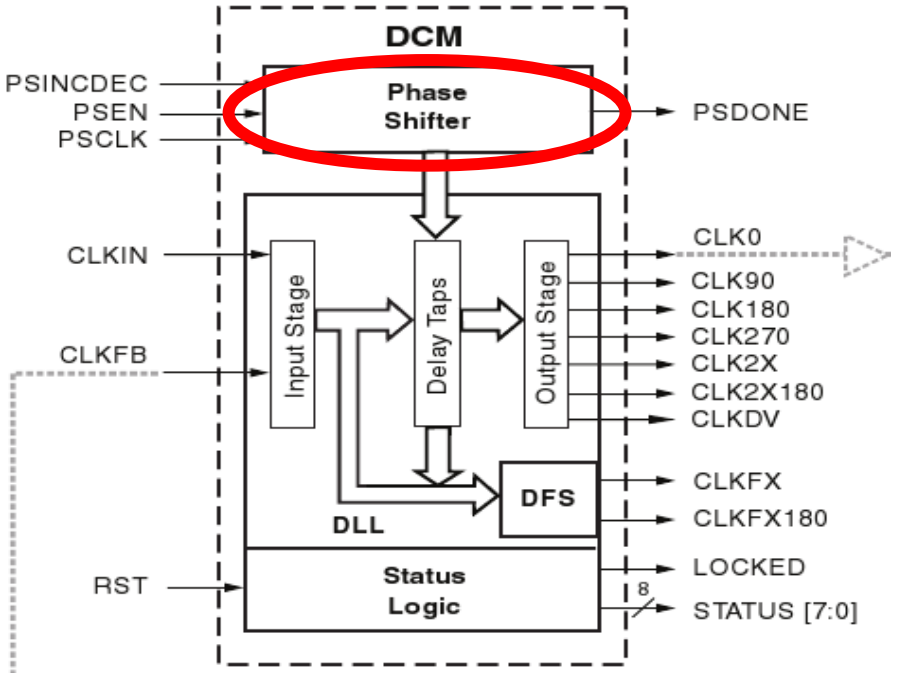
FPGA Development board for testing

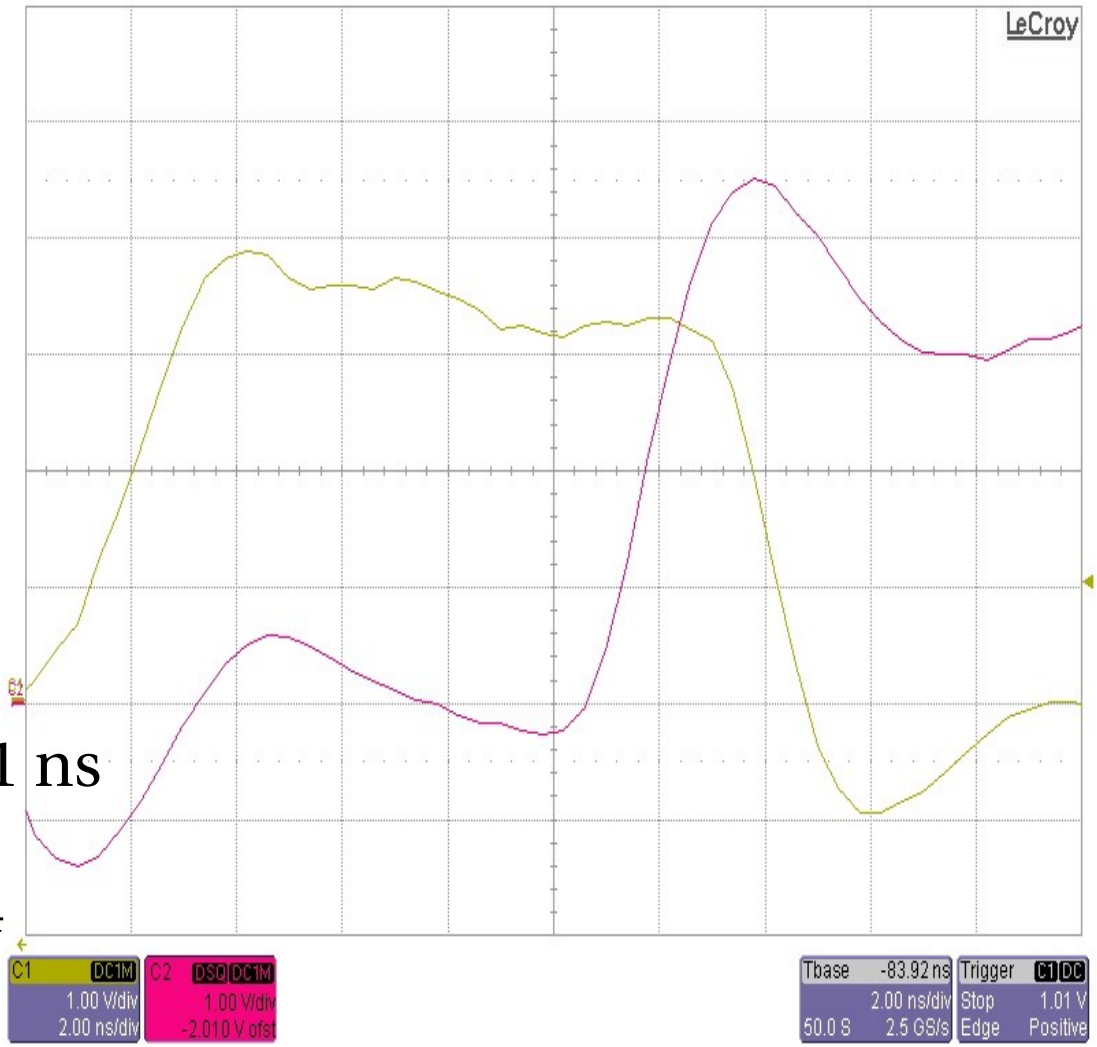


- AVNET development board is used for testing
  - XC3S400A-4FTG256C Spartan-3A FPGA in the suitable for MCM package (small in terms of the available resources, but can be replaced)
  - MC with USB interface for board-PC connection

PHOS4 Functionality in FPGA

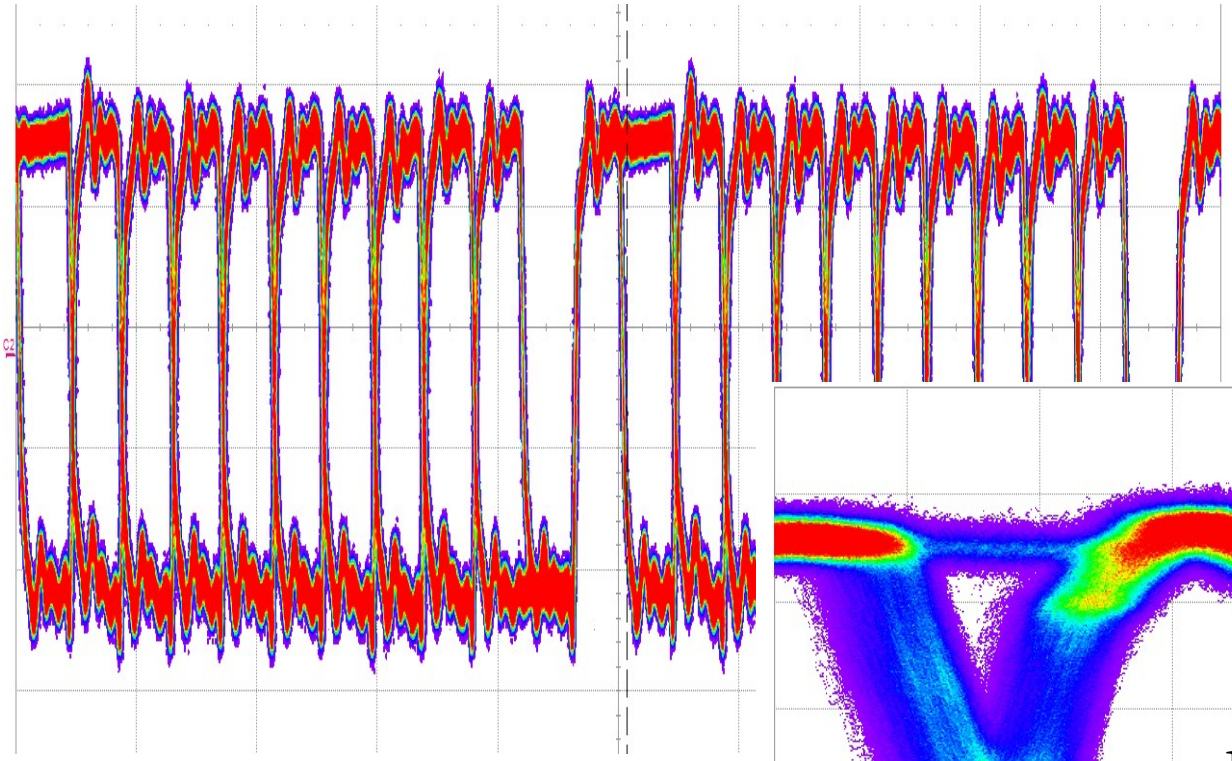
- PHOS4 chip task – fine time adjustment (resolution: 1 ns)
- This job can be done by FPGA's Digital Clock Manager (DCM)





- Phase Shifter step is well bellow 1 ns
- 8 DCMs are in the XC3S1400A
- 4 of them can be used for PHOS4 replacement (4 channels)

LVDS serialisers in FPGA

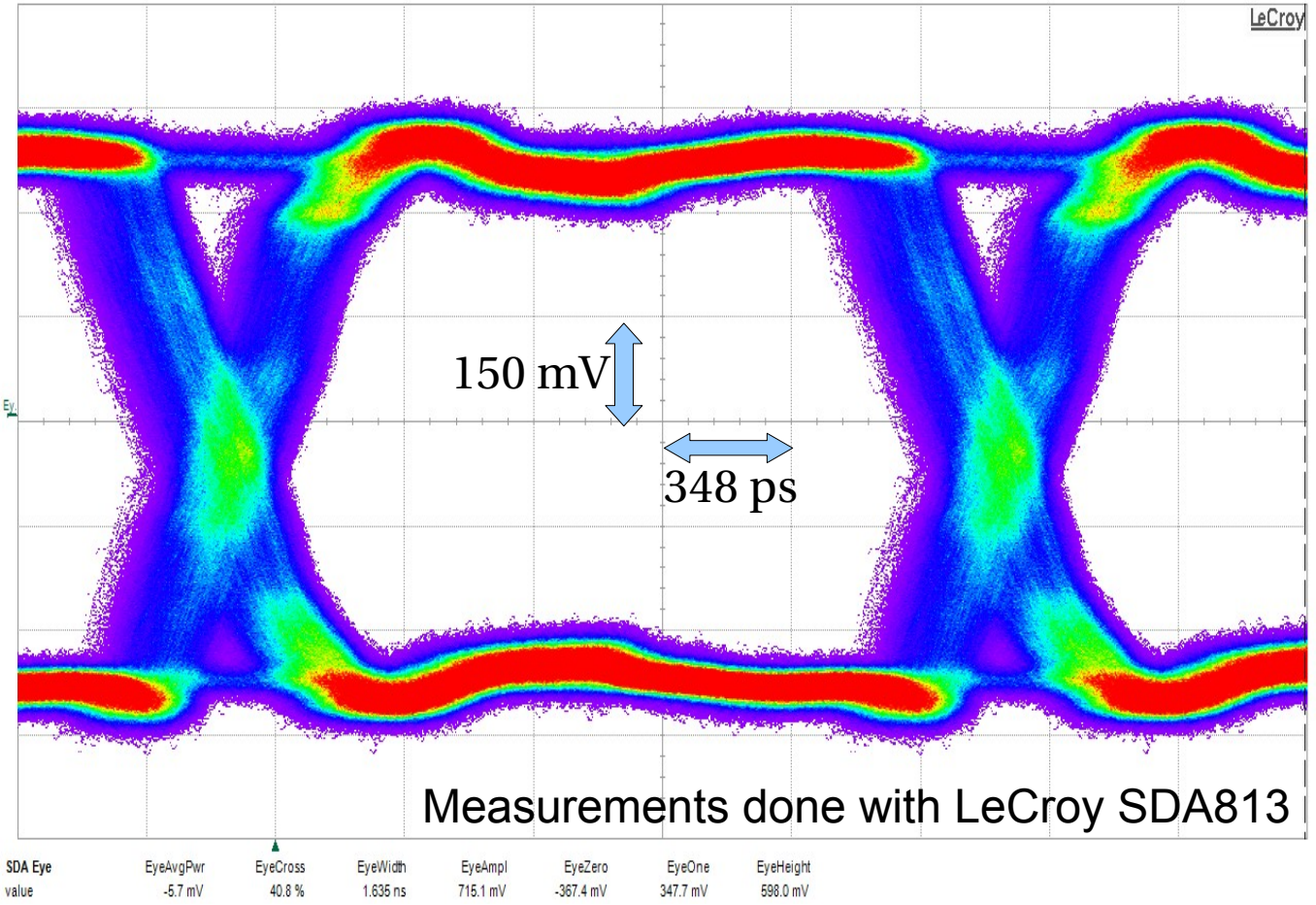


480 MBit/s

10 data bits

+ 1 start bit @ 40 MHz

+ 1 stop bit



- Close to the speed limit of the Spartan-3
- Is implemented using DDR I/O
- 3 serialisers: <2% of the XC3S400A

Conclusions

- New MCM (nMCM) can be built with the same form-factor and functionality
- Having a reconfigurable component (FPGA) we will gain in flexibility
- PHOS4 functionality and LVDS serialisers can be implemented inside FPGA => less components on the module
- Various FPGA evaluation boards, together with existing equipment for current MCM testing is used for development and tests before actual layout of the nMCM will be ready.