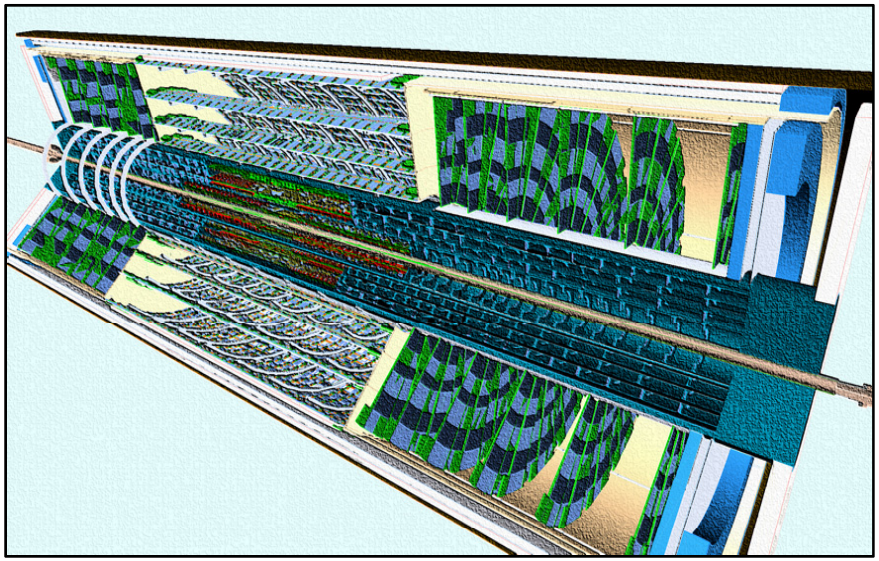
The Inner Tracker for the Phase-II upgrade of ATLAS

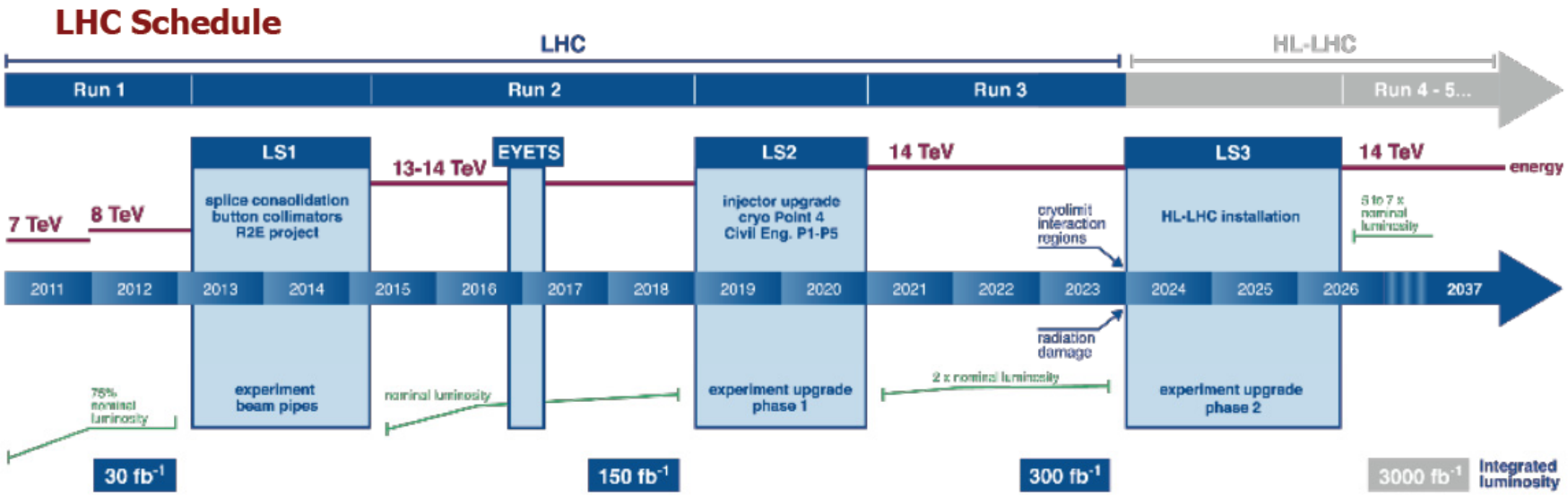
Sergio Díez Cornell

Deutsches Elektronen-Synchrotron (DESY)



DESY LHC physics discussions, 18th Feb 2019

LHC schedule and HL-LHC



High-Luminosity upgrade of the LHC and its detectors envisioned for 2024-2026

Frédérick Bordry, Chamonix Workshop 2017
https://indico.cern.ch/event/580313/

Increased instantaneous luminosity
$10^{34}\ cm^{-2}s^{-1} \rightarrow 5\text{-}7.5x\ 10^{34}\ cm^{-2}s^{-1}$
and pp interaction per BC
$25 \rightarrow 200$

Increased integrated luminosity
$300\ fb^{-1} \rightarrow 3000\text{-}\ 4000\ fb^{-1}$

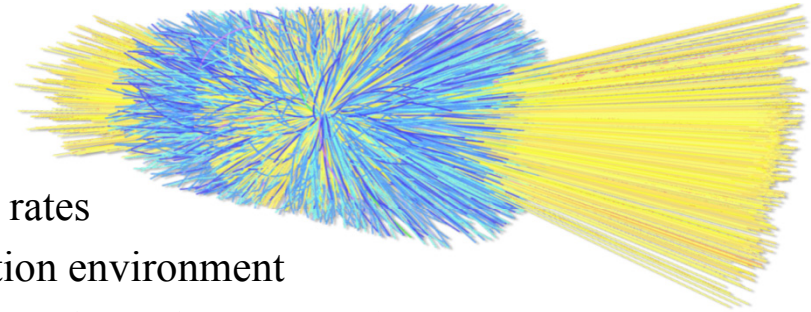
Higher data rate

Increased detector occupancy

Increased radiation environment

The new ATLAS Inner Tracker (ITk)

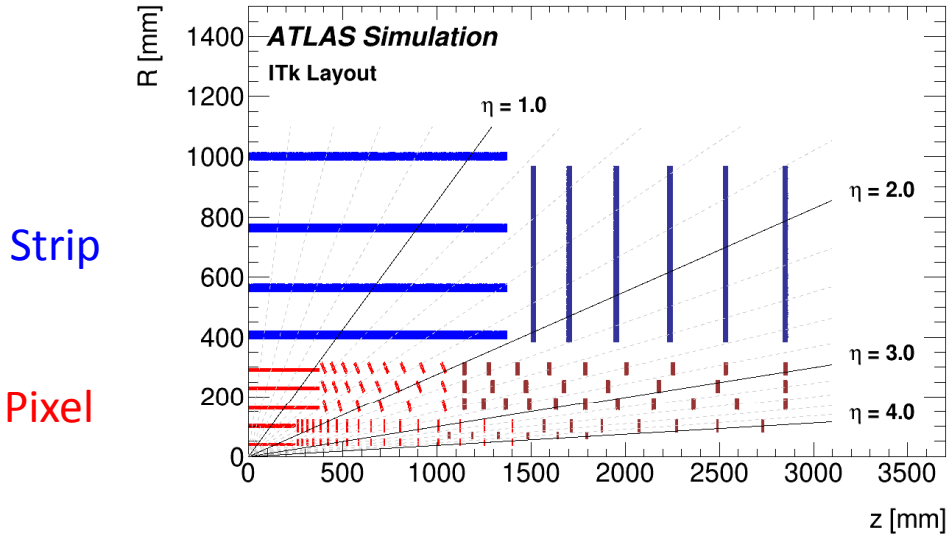
Challenges for silicon trackers



- Higher granularity to keep same low occupancy
- Reduced pitch to improve performance at high p_T
- Improved readout and triggering to deal with high data rates
- Higher radiation tolerance to deal with increased radiation environment
- Reduce material and cable count in the tracking volume to keep detector performance
- Reduce cost per sensor to cover larger area (~ 175 m^2)

Replacement of ATLAS Inner detector by an **all-silicon tracker**

Current Layout for the Phase-II Inner Tracker (Sept 2018)

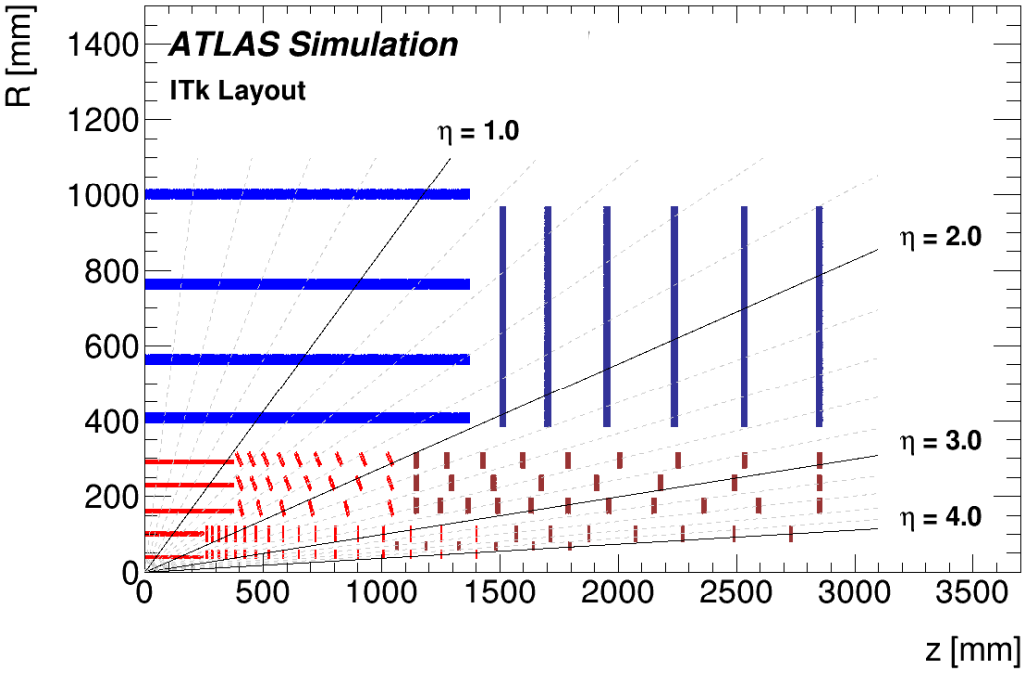


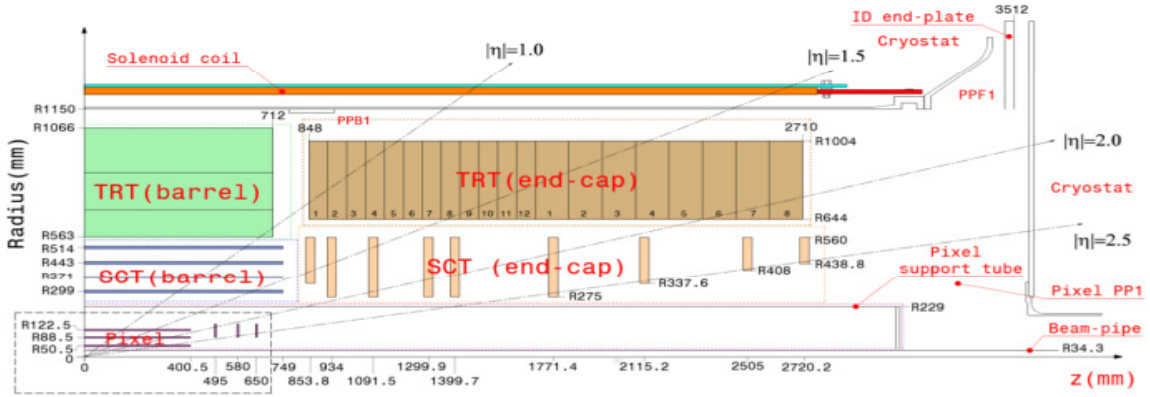
5 pixel barrel layers and 5 pixel rings

4 strip barrel layers and 6 endcap disks

	Silicon Area	Channels [10^6]
Pixel	~13 m^2	580
Strip	160 m^2	50

Why η<4?





Improved identification of the correct hard-scatter vertex

Reject pile-up jets

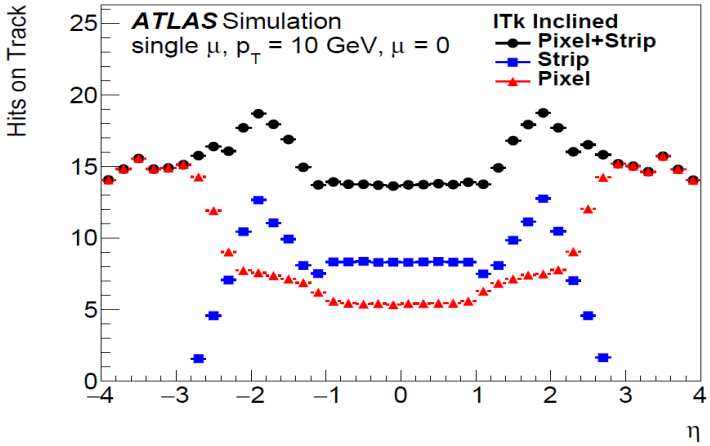
Improved identification or suppression of b-jets

Extend lepton coverage

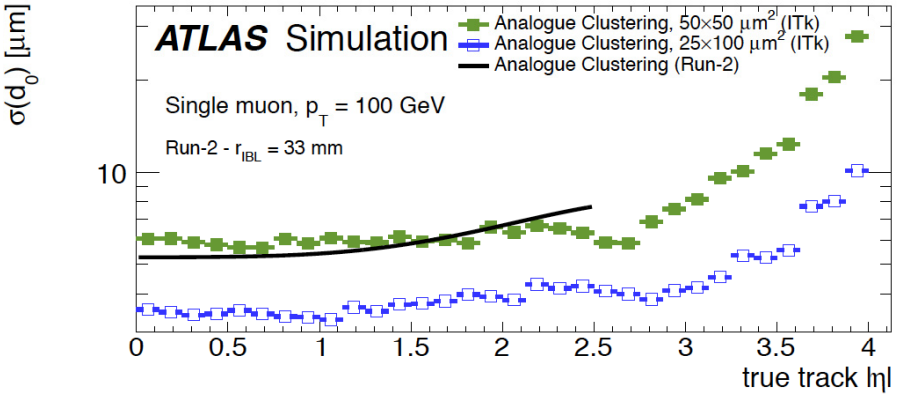
ITk layout performance

Layout goal: Maintain or improve tracking resolution and particle identification performance from Run-2

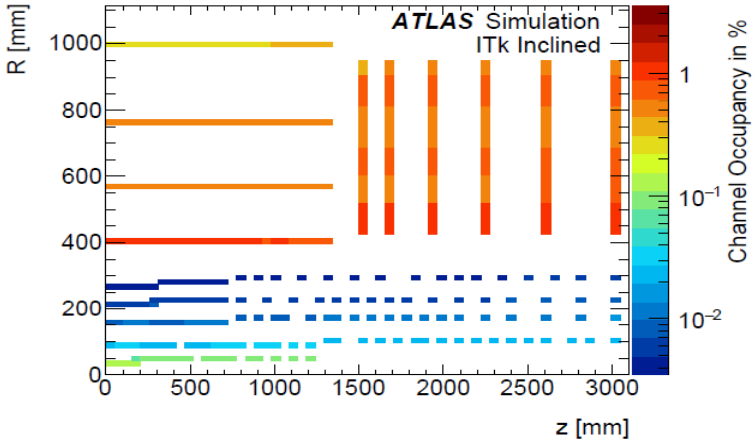
Mean number of hits per track

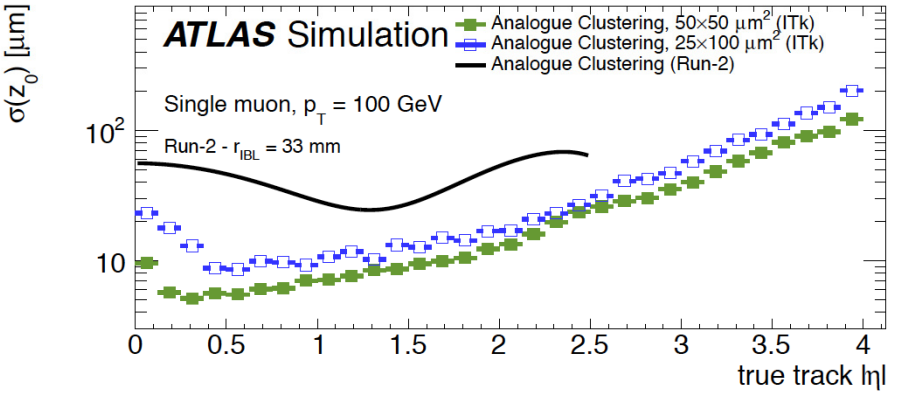


Transverse and longitudinal impact parameter resolution

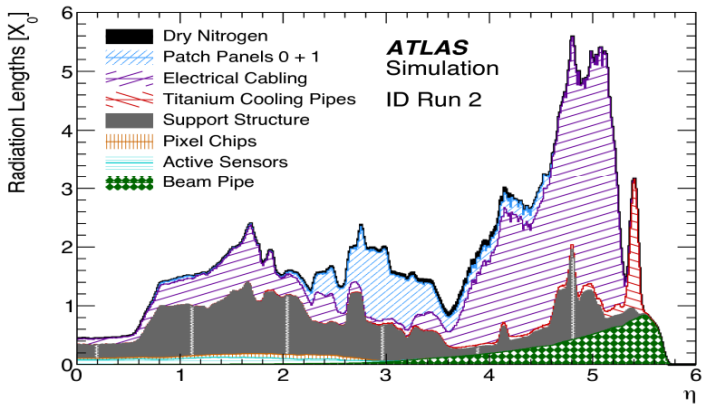


Average channel occupancy at <μ> = 200

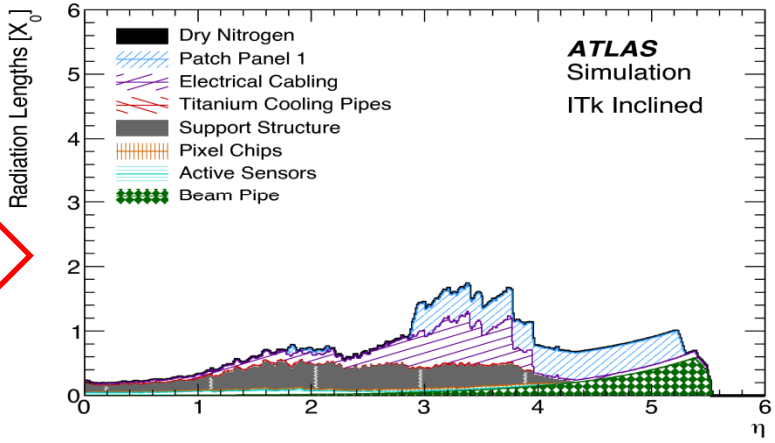




ITk X0 profile and radiation environment



50% lower than ID at η<4

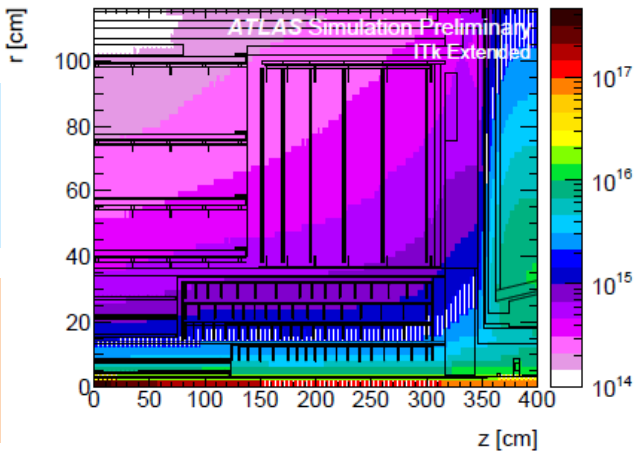


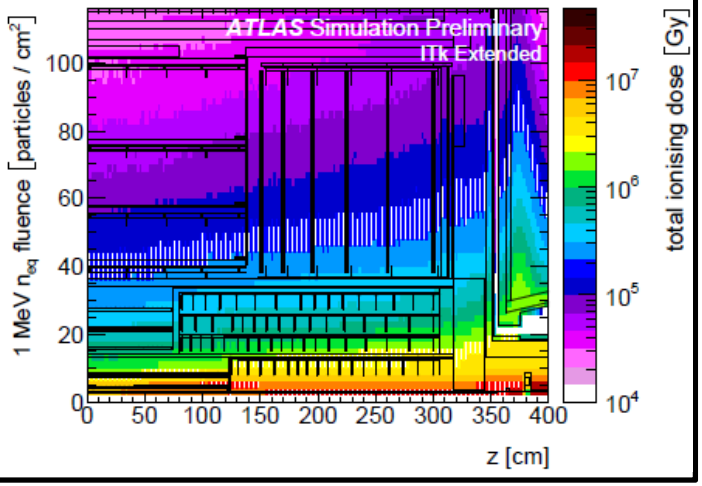
< 1 X0 for the active tracker volume
< 1.5 X0 before the calorimeter incl. moderator

Maximum values (without Safety Factors):

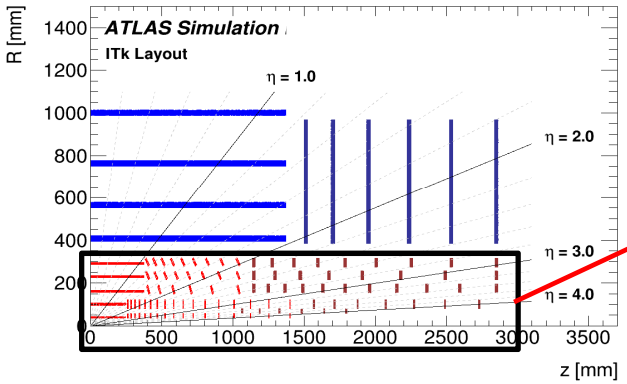
Strips
8.2 x 10^{14} neq/cm^2
33.2 Mrad

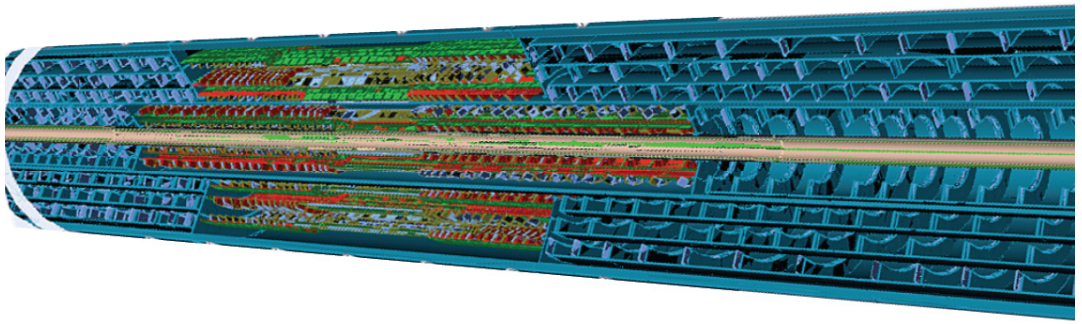
Pixels:
1.5x10^{16} neq/cm^2
1.1 Grad





The pixel tracker





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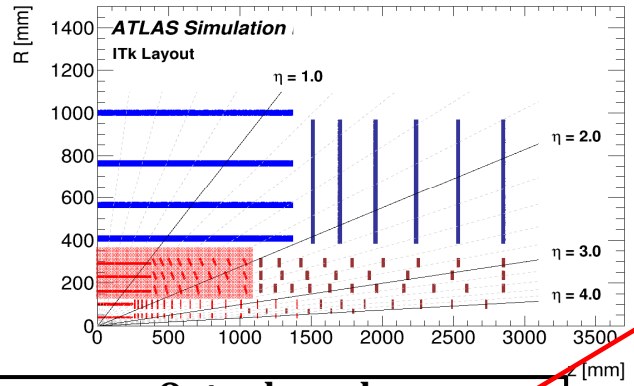
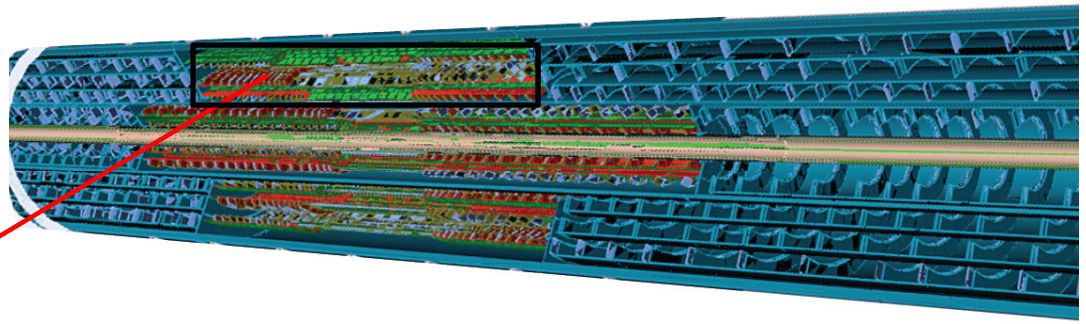
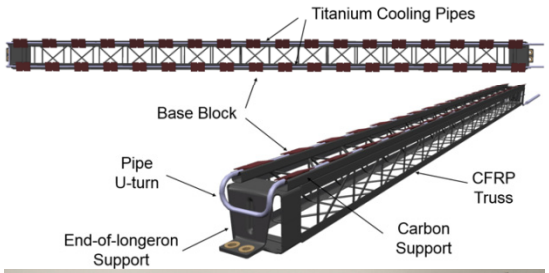


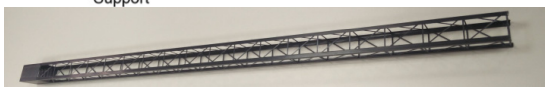


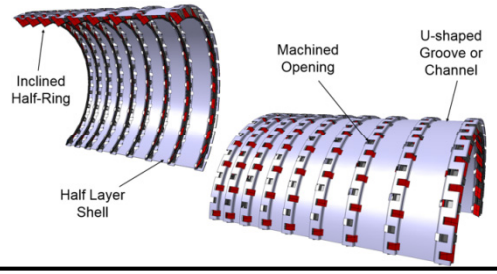
Outer barrel:

Truss prototype for Longeron design

Inclined modules in half shells







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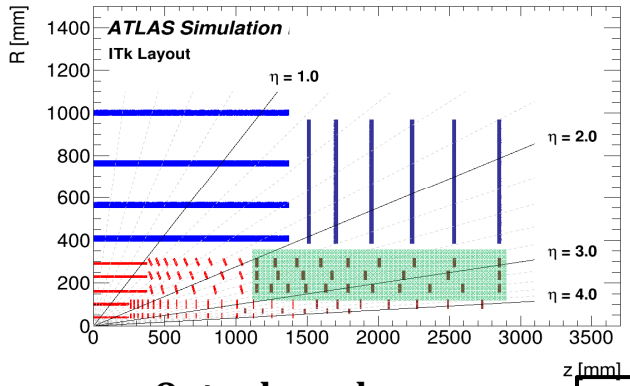
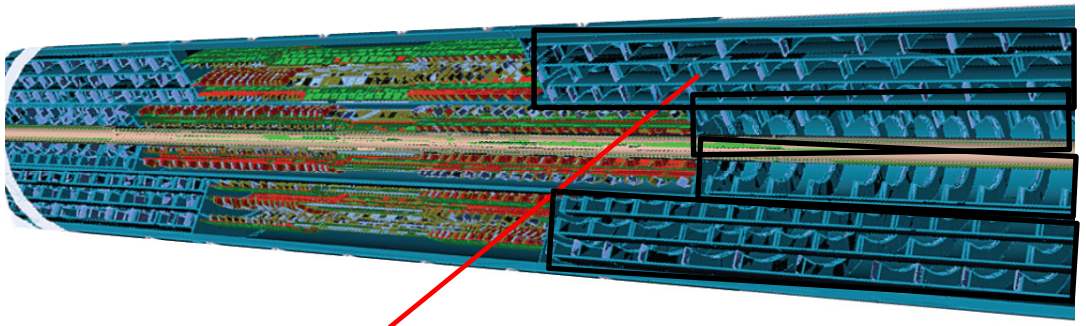
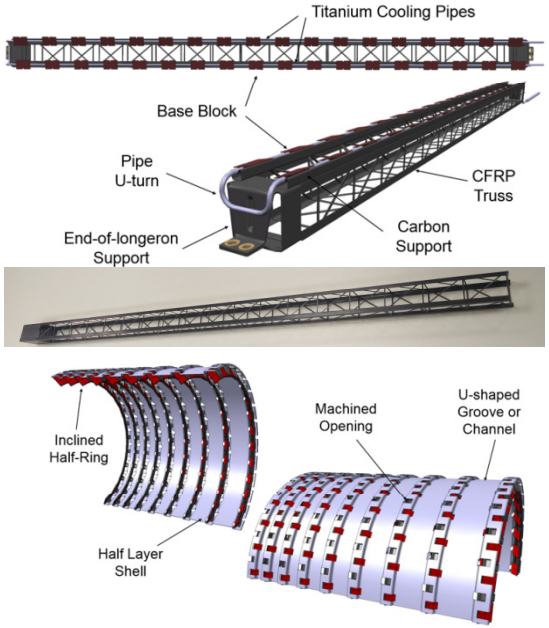
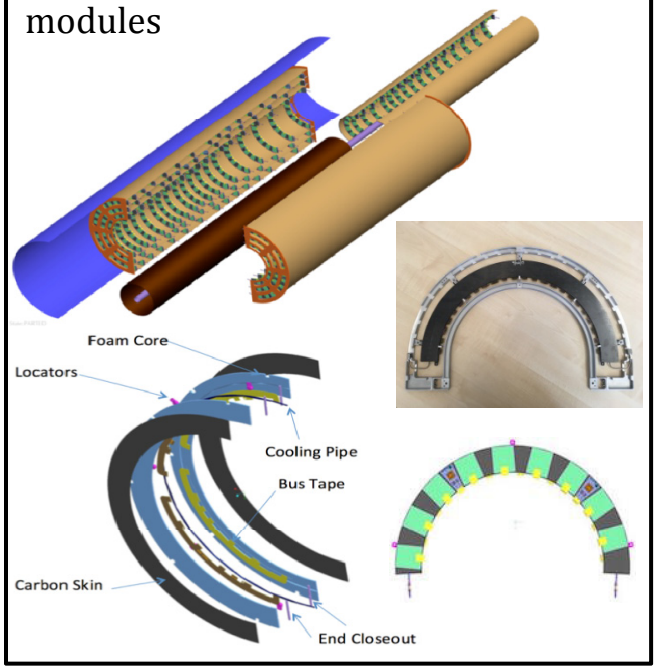




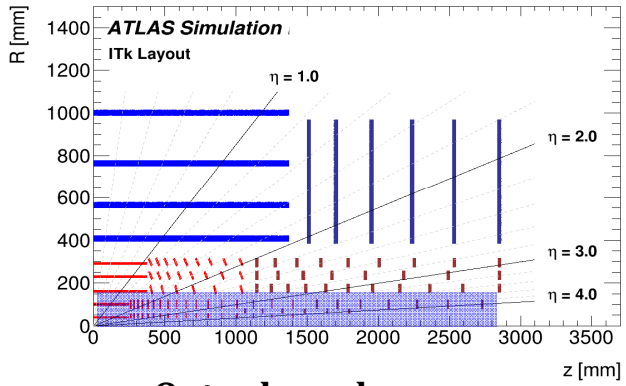
Outer barrel:
Truss prototype for Longeron design
Inclined modules in half shells

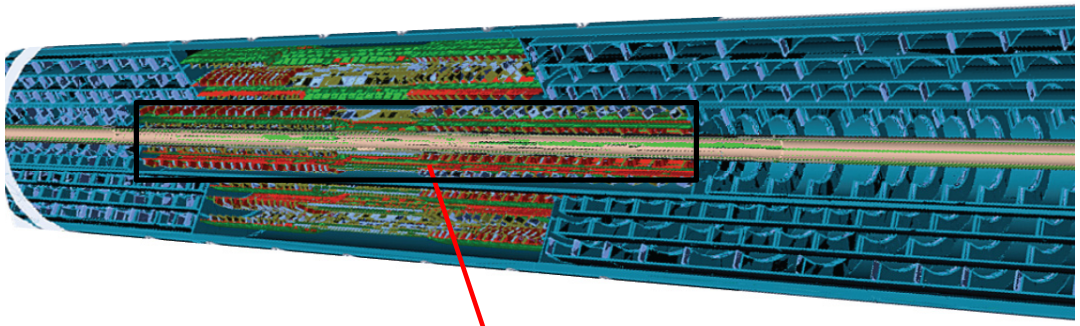


Pixel endcap:
Half-cylindrical cells supporting quad modules



Pixel tracker structures





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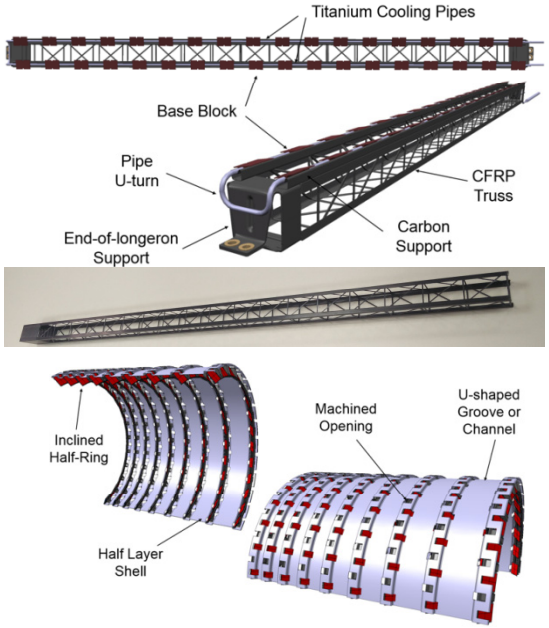

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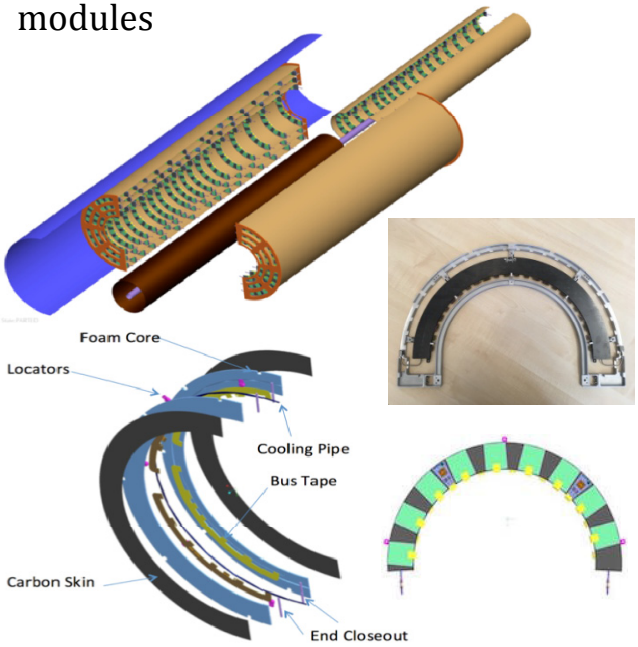
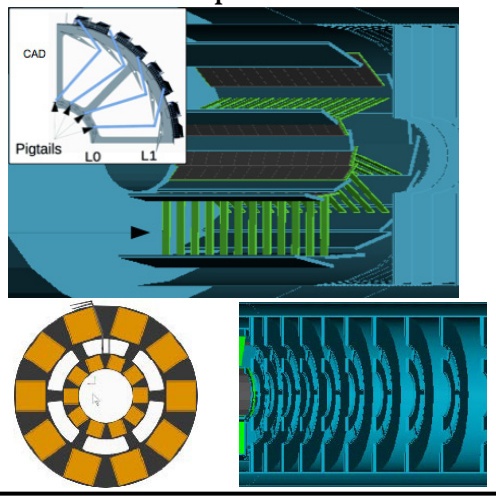
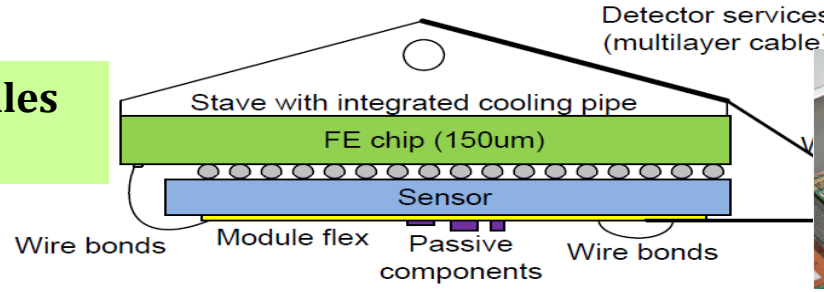


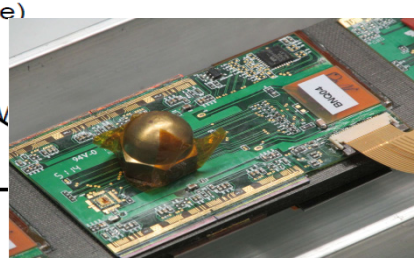
Removable inner pixel system:
Quarter shells for joint L0/L1
Flat staves on barrel region
Coupled rings with 90° inclination
End-cap rings at high eta similar to the outer end-caps



Pixel modules and sensor technology

Hybrid pixel technology for modules
Single, double, and quad modules





Prototype quad module

Pixel modules and sensor technology

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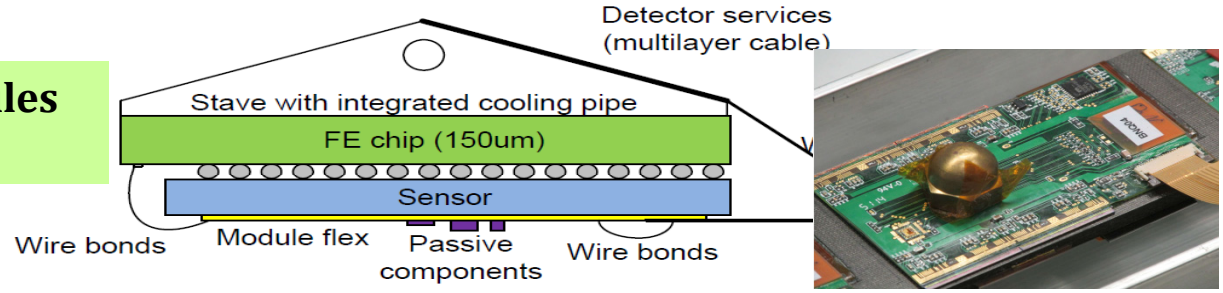
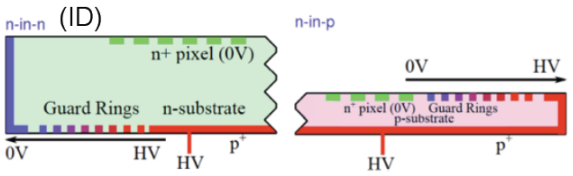
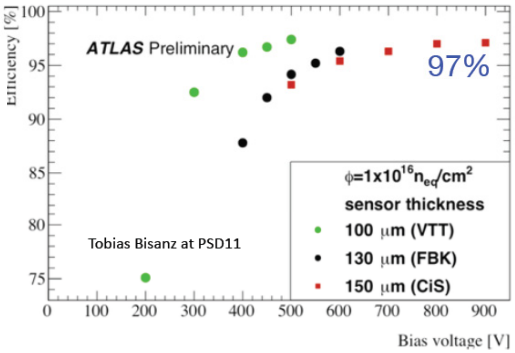


Prototype quad module

Planar sensors for outer layers
High yield and lower costs
Well proven technology
Reduced thickness: goal is 100-150 μm
Move to n-in-p technology





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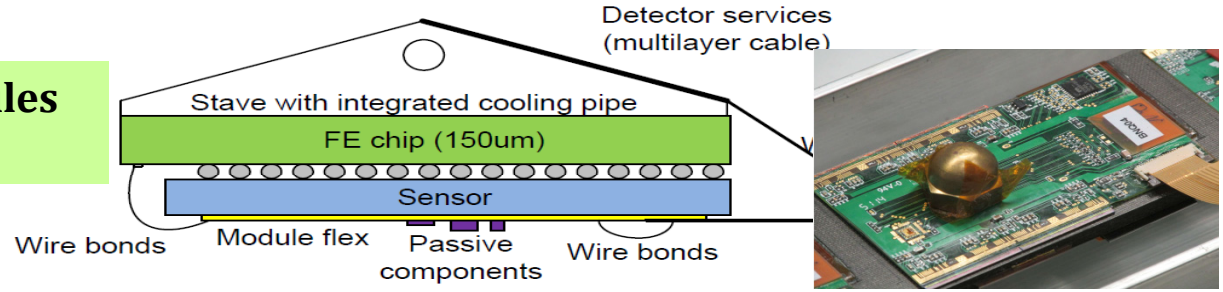

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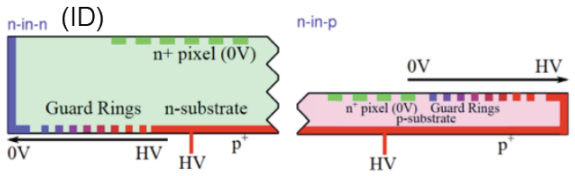
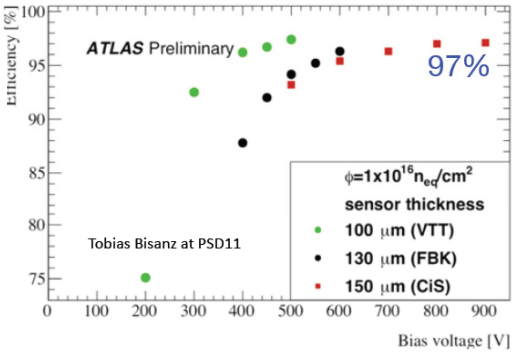
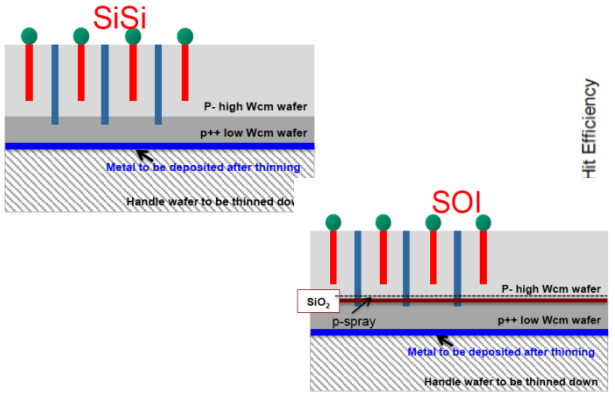
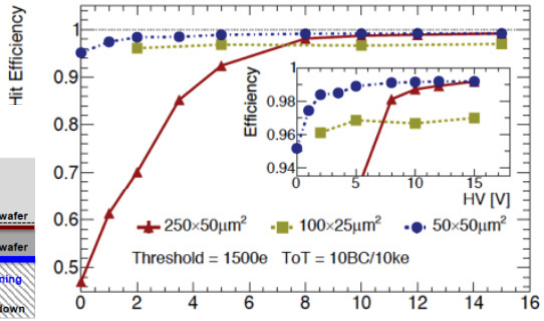




3D sensors for innermost layers
Excellent radiation hardness
Low power dissipation
Optimization of process for small pixels and thinned sensors in progress

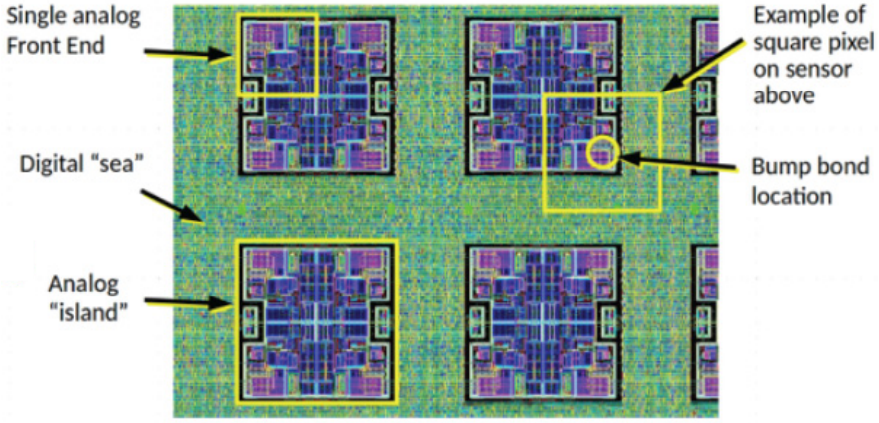




Pixel readout electronics

- Synergic development with CMS (RD53)
- Increased radiation hardness using **65 nm technology** in TSMC (target 1 Grad)
- First large prototype fabricated and tested:
  - 50x50 μm^2 with 4-pixel analogue section
  - 50 μm minimum pitch to allow standard flip-chip
  - Shunt LDO implementation for compatibility with serial powering
  - Highest data rate per ASIC: 5 Gbps
- RD53A is fully functional with very promising test results within or close to the specifications
- Test results confirm that RD53A is a fundamental and solid baseline for final ATLAS/CMS chip development

Technology	65nm CMOS
Pixel size	**50x50 um^2**
Pixels	192x400 = 76800 (50% of production chip)
Detector capacitance	< 100fF (200fF for edge pixels)
Detector leakage	< 10nA (20nA for edge pixels)
Detection threshold	<600e-
In -time threshold	<1200e-
Noise hits	< 10^{-6}
Hit rate	**< 3GHz/cm^2 (75 kHz avg. pixel hit rate)**
Trigger rate	Max 1MHz
Digital buffer	12.5 us
Hit loss at max hit rate (in-pixel pile-up)	≤1%
Charge resolution	≥ 4 bits ToT (Time over Threshold)
Readout data rate	**1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s**
Radiation tolerance	**500Mrad at -15°C**
SEU affecting whole chip	< 0.05 /hr/chip at 1.5GHz/cm^2 particle flux
Power consumption at max hit/trigger rate	**< 1W/cm^2 including SLDO losses**
Pixel analog/digital current	4uA/4uA
Temperature range	-40°C ÷ 40°C

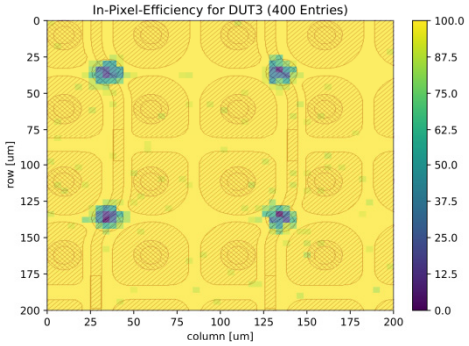


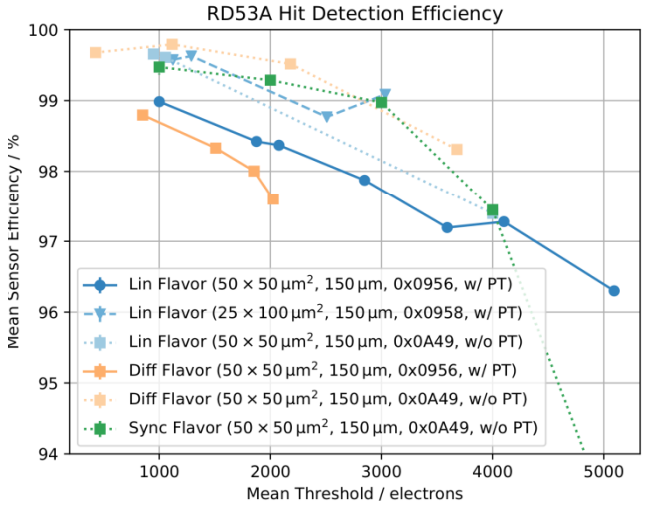
Pixel module assembly and system tests

Pixel assembly: ~200 RD53A assemblies with a large variety of sensor types have flip-chipped and under test

Test beams and irradiations to evaluate the sensor performance

- Have reached ~99.7 % Efficiency @ 1000 e- with all three analog FEs for unirradiated sensors





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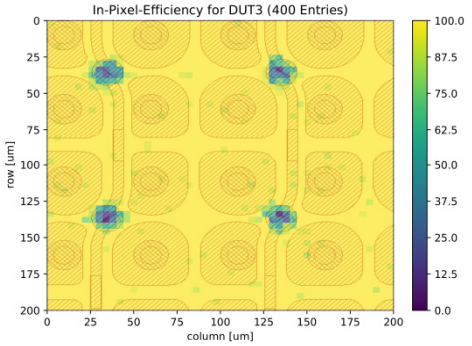
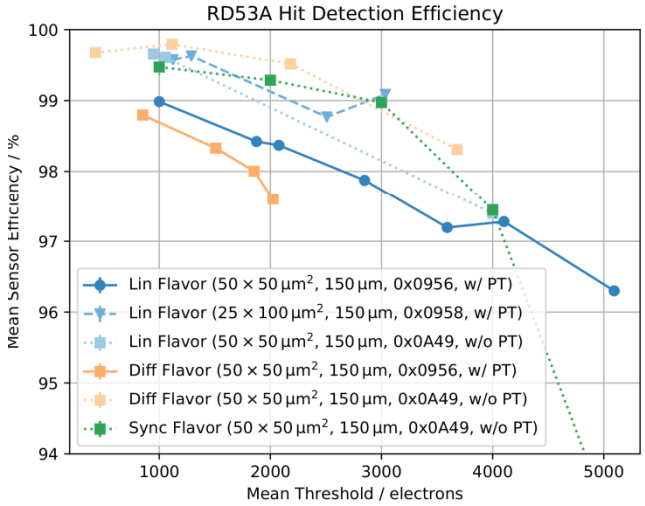




System tests:

Several serial powering test setups, test with up to 7 FE-I4 modules

Powering, noise introduction, cross-talk, …

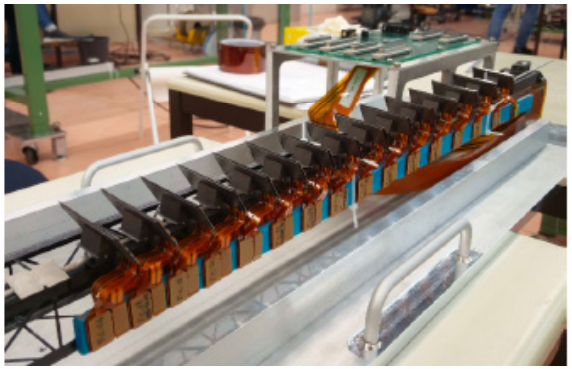
All tests show a safe operation with no distortion from noisy modules

Thermo-mechanical prototypes for thermo-fluidic and thermal tests with CO2 cooling

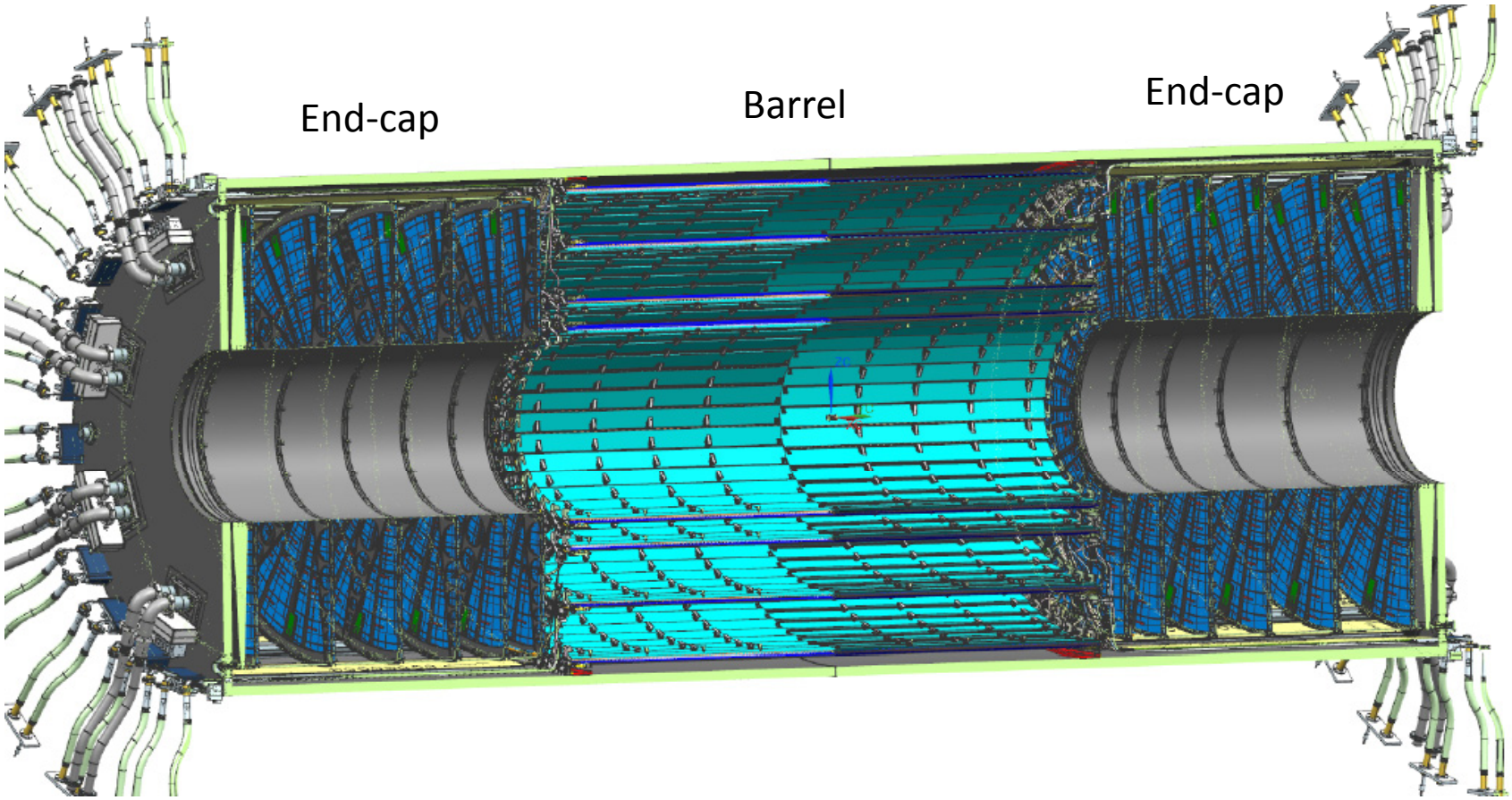
Thermal figures of merit achieved

Electrical outer barrel prototype with 7 FE-I4 quads

TM prototype of inclined section



The ITk strip detector: the stave/petal concept



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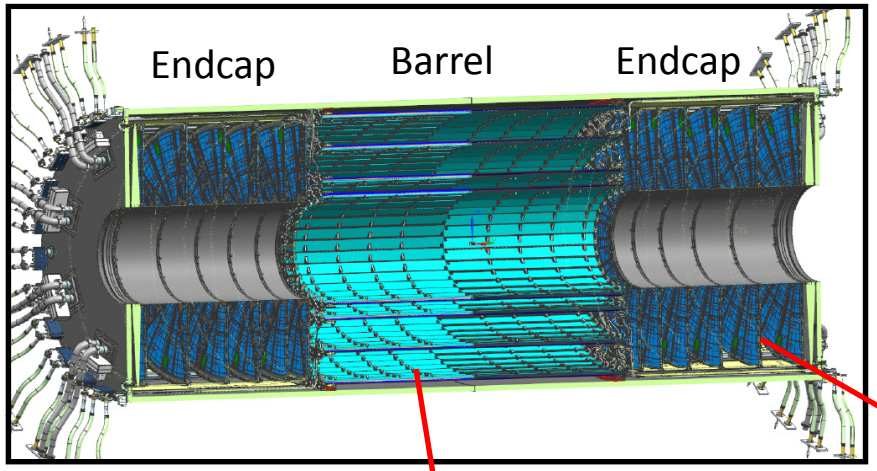
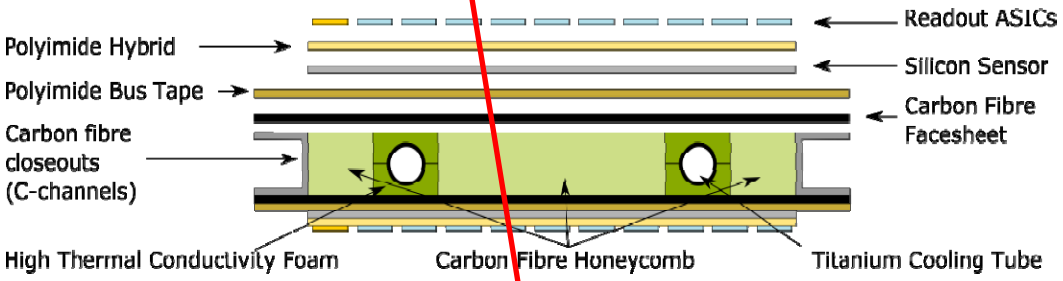


- Modules directly glued to CF support structures
- No substrate or connectors, hybrids glued to sensors
- Shortened cooling paths
- Minimized cable count
- Simplified build procedure

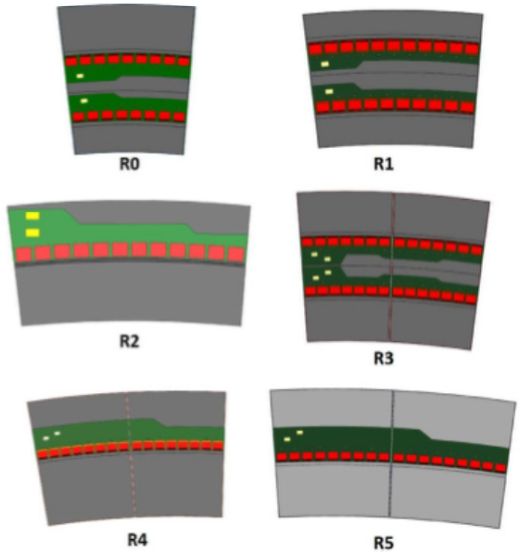


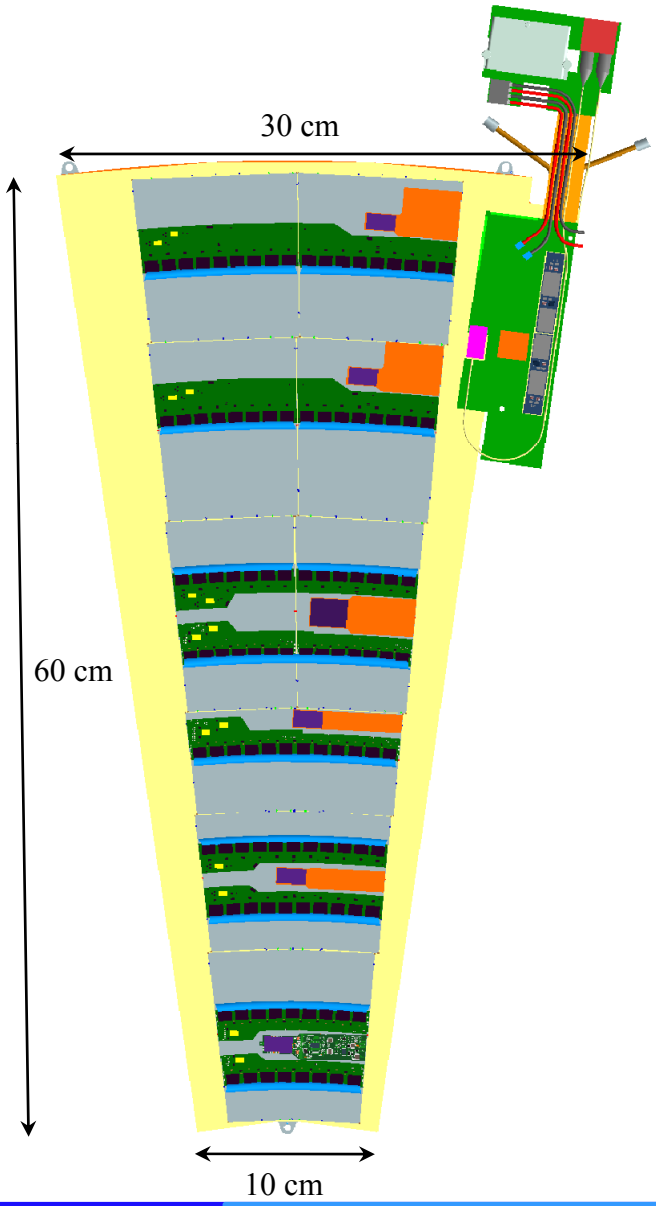
Petal geometry

- Hermetic η coverage in disk geometry
- Optimal phi resolution
- Stereo angle built into the petal (20 mrad)
- Straight edges parallel to strips to avoid truncated strips
- Curved inner and outer edges and curved gaps between strips
- Biggest Si strips sensor manufactured on 6” wafers (reliable proven technology)
- Strip pitch as close as possible to 75 μm as in barrel
- Number of rows (strip lengths) chosen to cope with increased occupancy

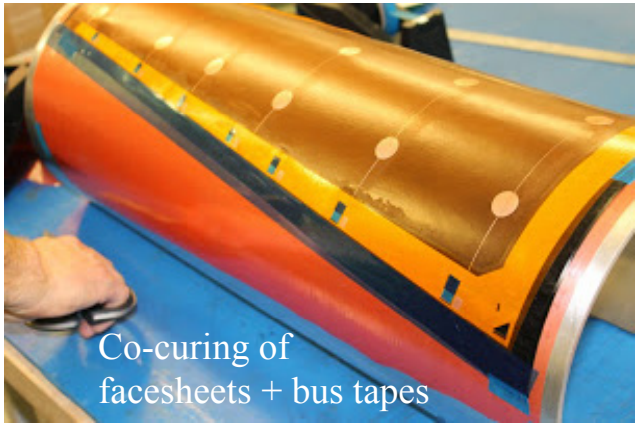
6 different types of wedge-shaped modules

Identical electronics components, readout, and build procedure for all of them, and for barrel modules





Local support manufacture

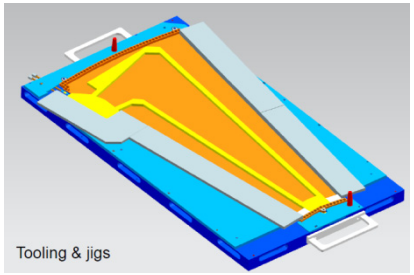


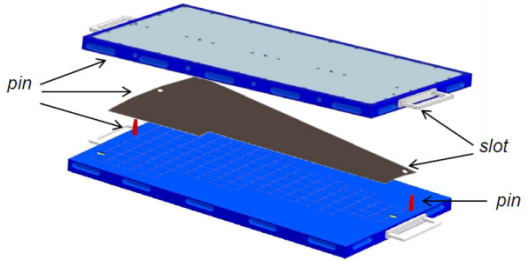
Supports manufacture performed with precision tools :

Accuracy

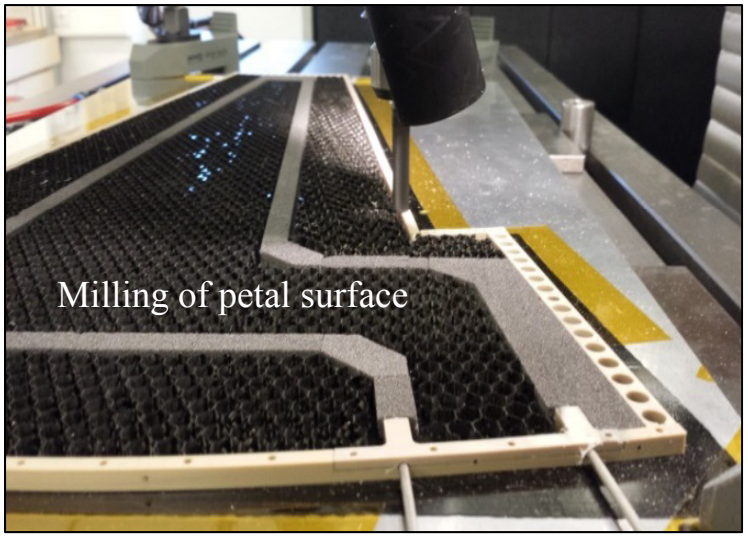
Repeatability

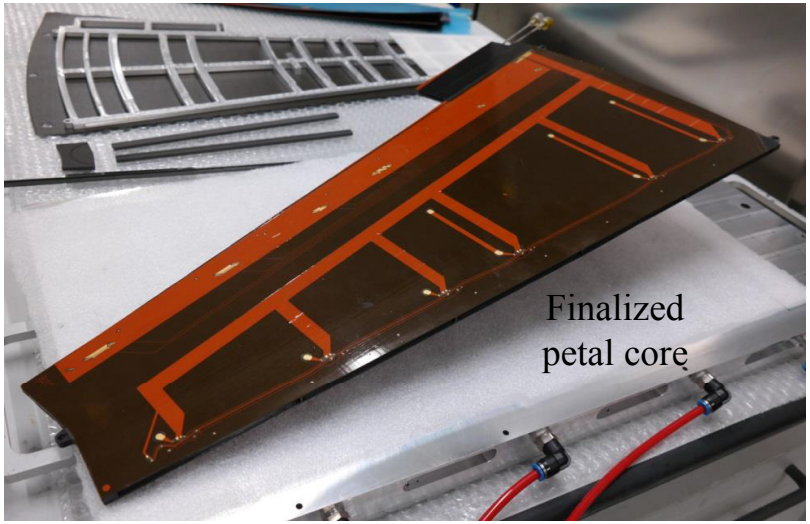
High throughput



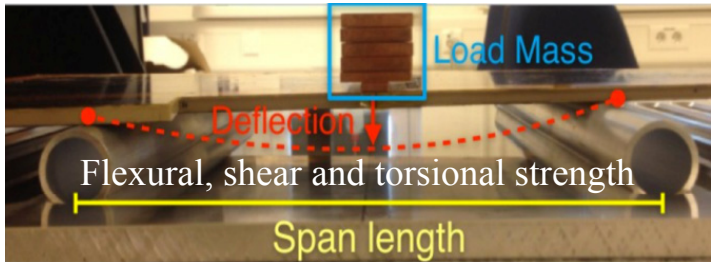


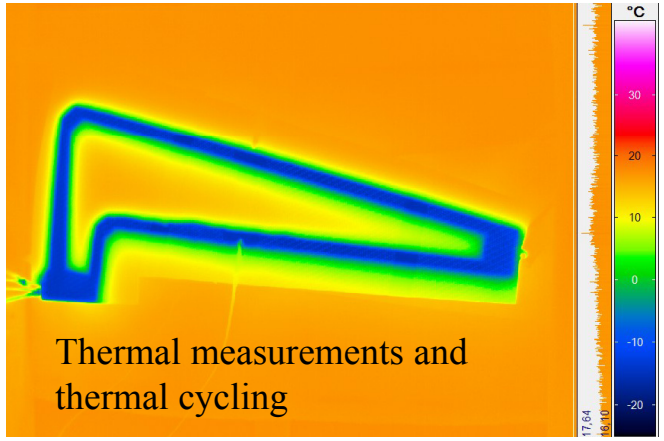
Sketch of main baseplates

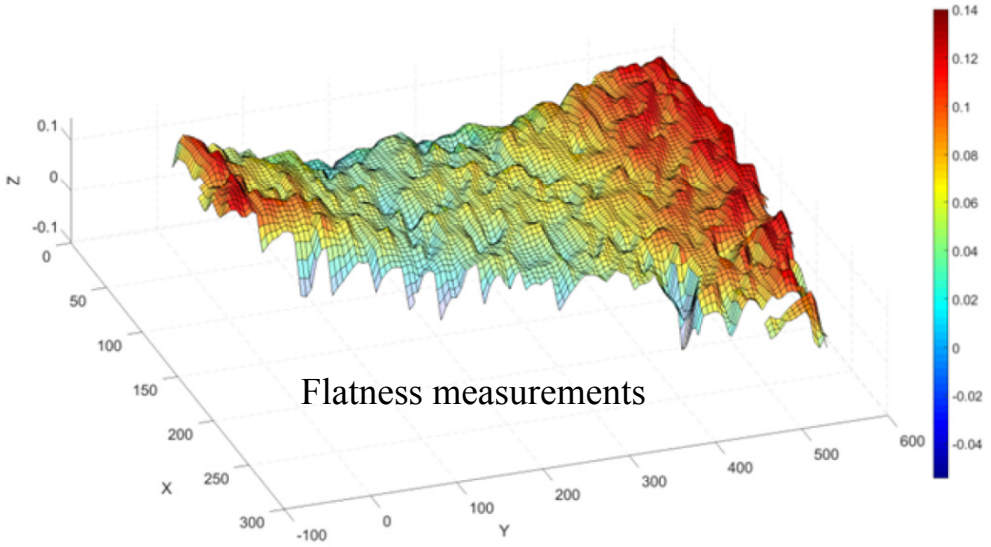


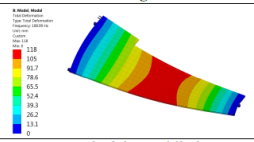
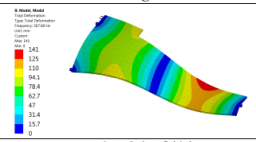
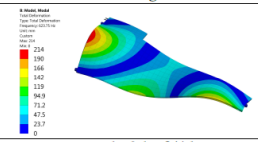


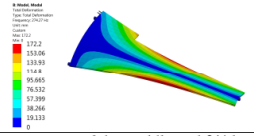
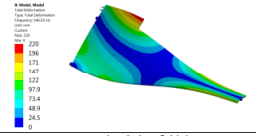
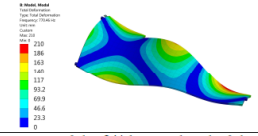
QA/QC and FEA



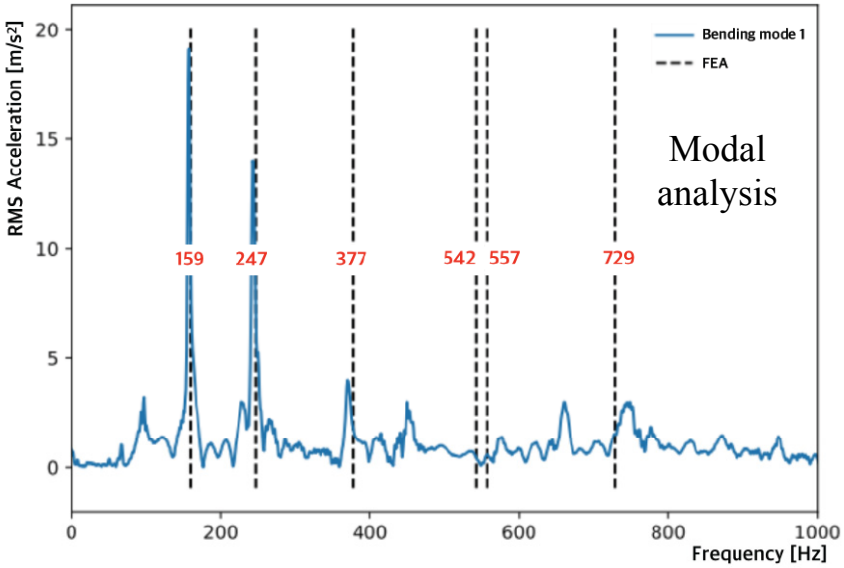




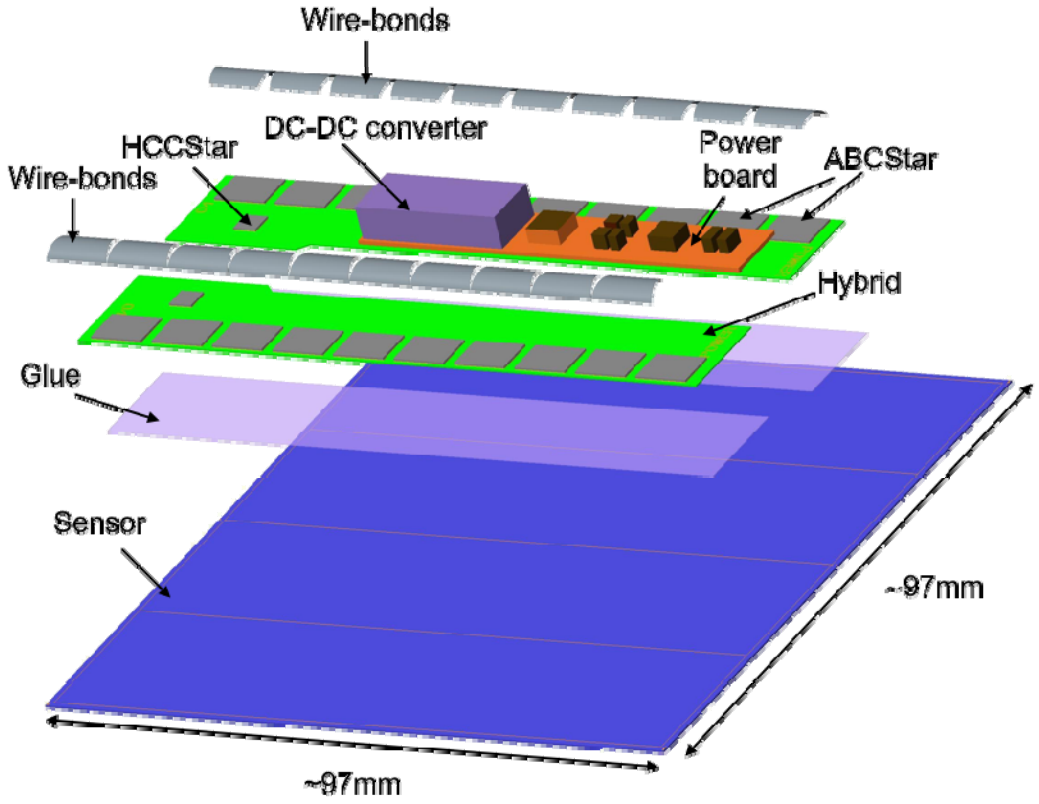
	Bending mode 1	Bending mode 2	Bending mode3
Motion			
Hitting Point	end of the middle line	ends of the 3/4 line	end of the 3/4 line
Sensor Position	end of the middle line	end of the 3/4 line	center of the petal width

	Torsional mode 1	Torsional mode 2	Torsional mode 3
Motion			
Hitting Point	center of the middle and 3/4 line	end of the 3/4 line	center of the 3/4 line and end of the petal
Sensor Position	center of the middle and 3/4 line	end of the 1/4 line (the ear of petal core)	center of the middle and 3/4 line

Mechanical FEA



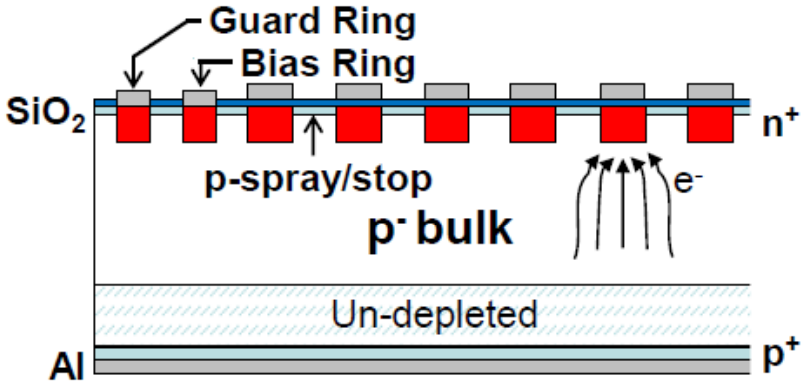
Silicon strip modules

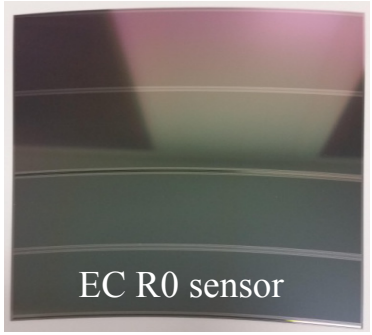


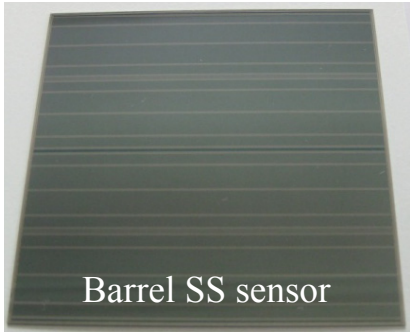
Silicon strip sensors: technology choice

n^+ strips in p-type substrate (n-in-p)

- 6" wafer technology (~10x10 cm^2)
- Strip lengths from 1.7 to 5 cm
- 320 µm thick, ~ 75 µm pitch
- High resistivity (~4 kΩ/cm)
  $\Rightarrow$ V_{dep}~200 V
- P-stop isolation in between strips
- Spatial resolution ~ 20 µm
- Time resolution ~3 ns







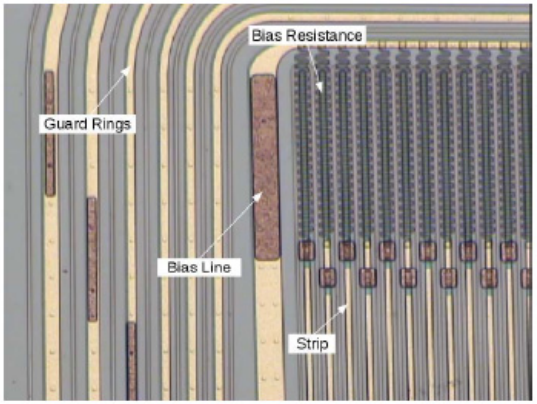
Why n-in-p?

Collects electrons (as opposed to p-in-n)
- Faster signal, reduced charge trapping

Depletes from segmented side
- Good signal even under-depleted

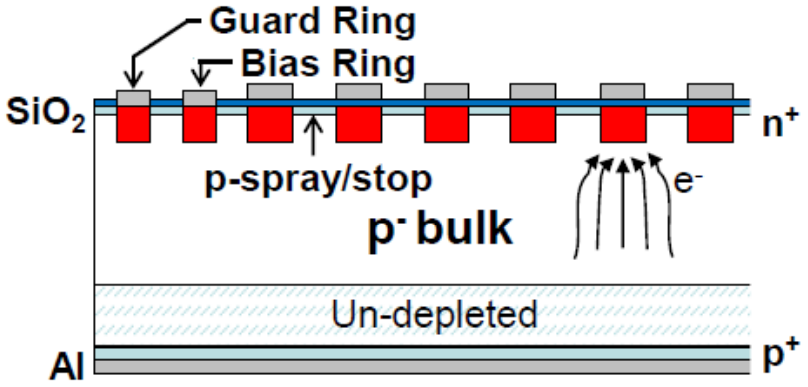
Single-sided process
- Significantly cheaper than n-in-n
- More foundries and available capacity worldwide

Lack of patterned back-side implant
- Easier handling and testing



Silicon strip sensors: technology choice

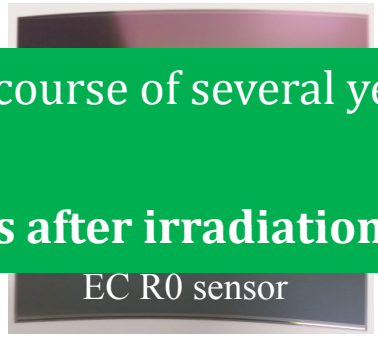
n^+ strips in p-type substrate (n-in-p)

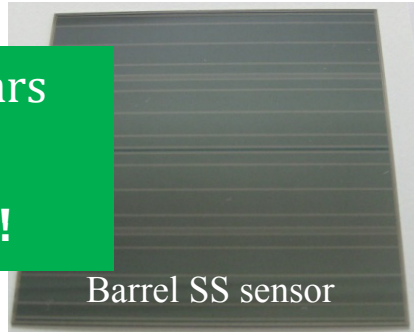


- 6" wafer technology (~10x10 cm^2)
- Strip lengths from 1.7 to 5 cm
- 320 µm thick, ~ 75 µm pitch
- High resistivity (~4 kΩ/cm)
  $\Rightarrow$ V_{dep}~200 V
- P-stop isolation in between strips
- Spatial r
- Time re

Very detailed studies over the course of several years

Sensors meet specifications after irradiations!


EC R0 sensor


Barrel SS sensor

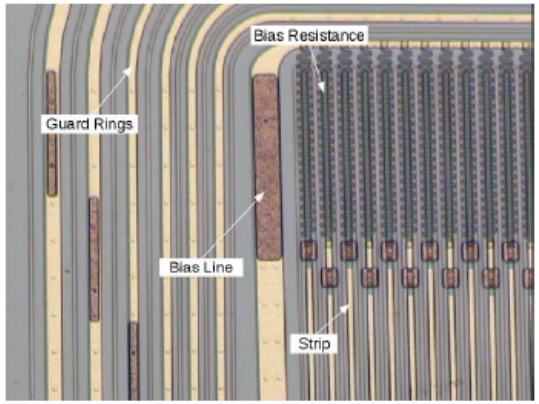
Why n-in-p?

Collects electrons (as opposed to p-in-n)
- Faster signal, reduced charge trapping

Depletes from segmented side
- Good signal even under-depleted

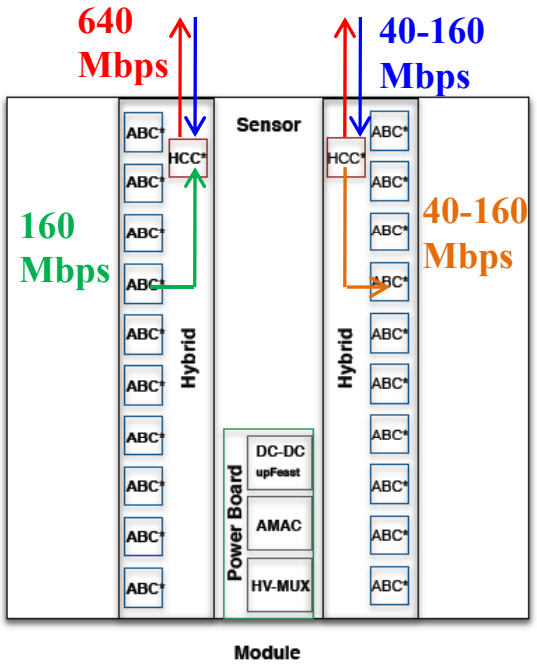
Single-sided process
- Significantly cheaper than n-in-n
- More foundries and available capacity worldwide

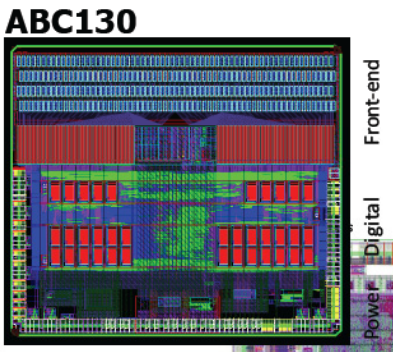
Lack of patterned back-side implant
- Easier handling and testing

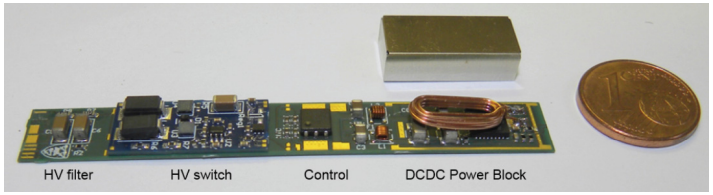


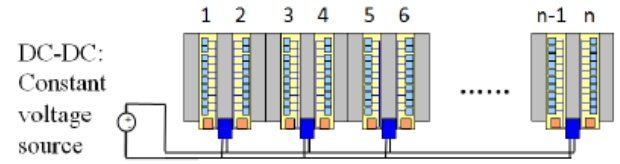
On-module readout, power and control electronics

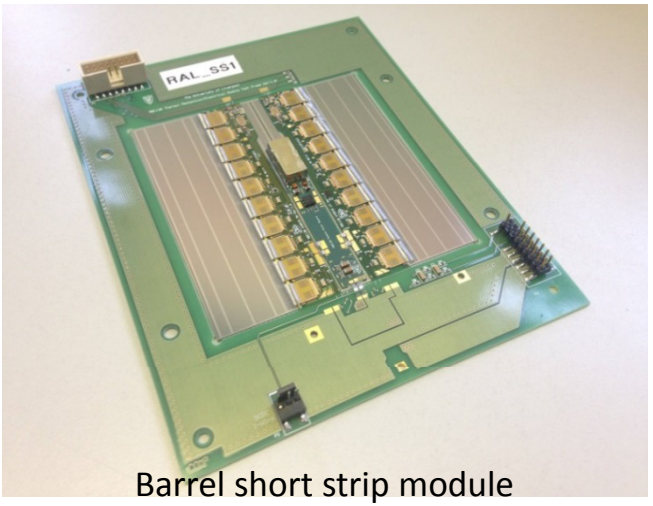
- ABC130
  - ATLAS Front-End readout chip for **binary readout**
  - Fabricated in 130 nm CMOS technology
  - 256 channels/chip, connected to sensor strips via wire-bonds
- HCC
  - Digital interface chip between ABC and bus tape
  - Handles incoming TTC signals, multiplexes readout data on-module and sends it to the outside world
- DC-DC powering









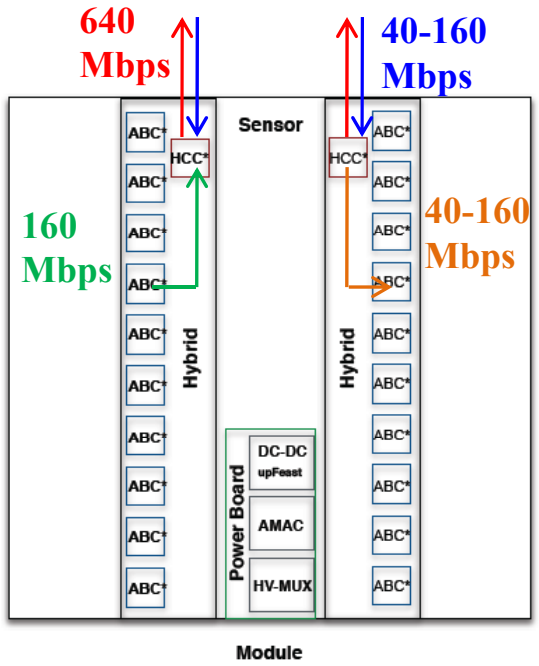


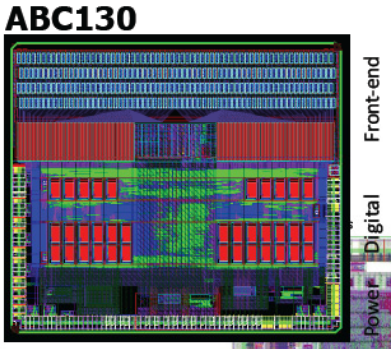
Barrel short strip module

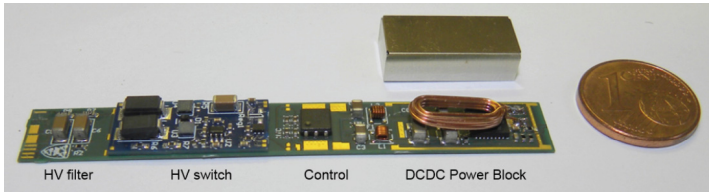
On-module readout, power and control electronics

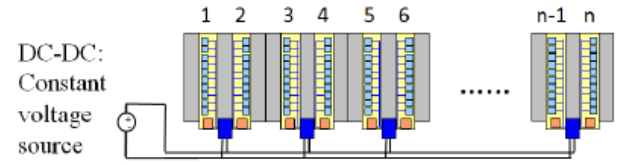
- ABC130
  - ATLAS Front-End readout chip for **binary readout**
  - Fabricated in 130 nm CMOS technology
  - 256 channels/chip, connected to sensor strips via
  - Digital interface chip between ABC and bus tape
  - Handles incoming TTC signals, multiplexes readout data on-module and sends it to the outside world
- DC-DC powering

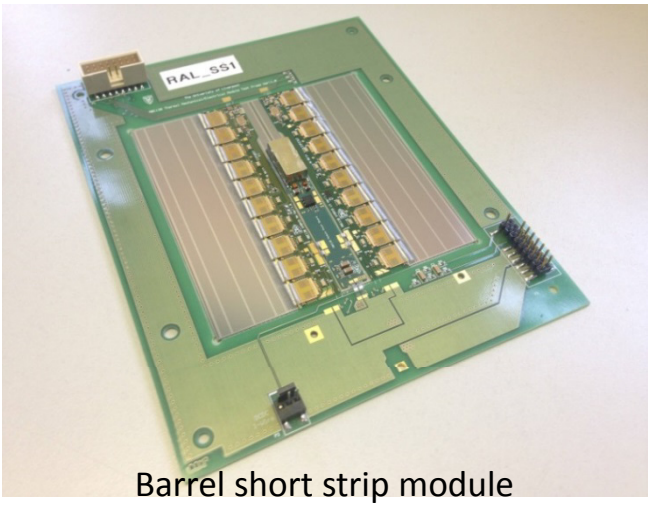
>100 fully operational ABCN250 modules
A dozen of ABCN130 barrel and EC modules produced during the last year







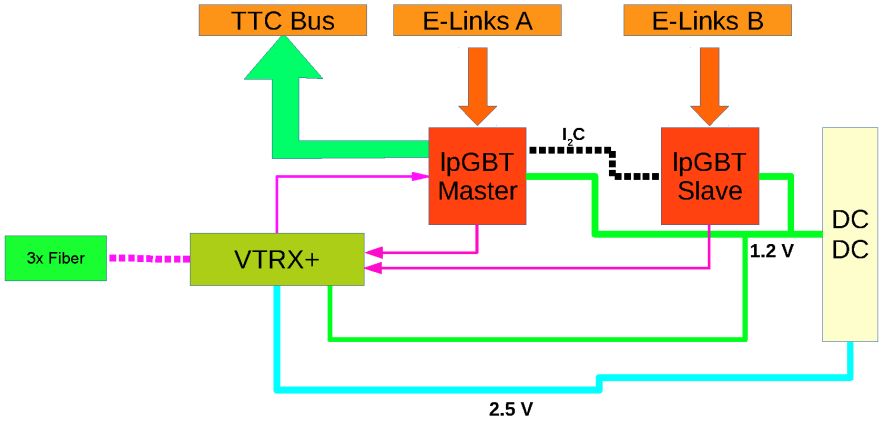


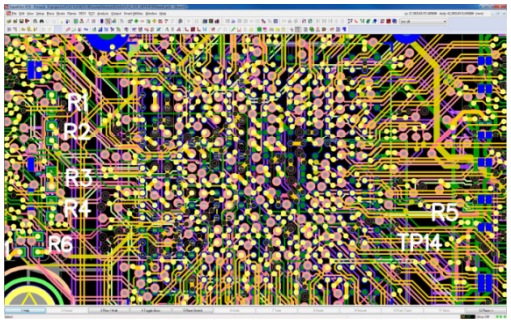


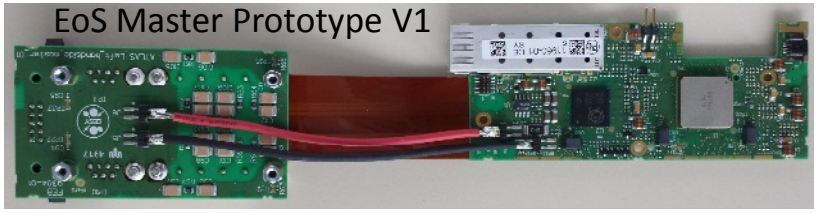
Barrel short strip module

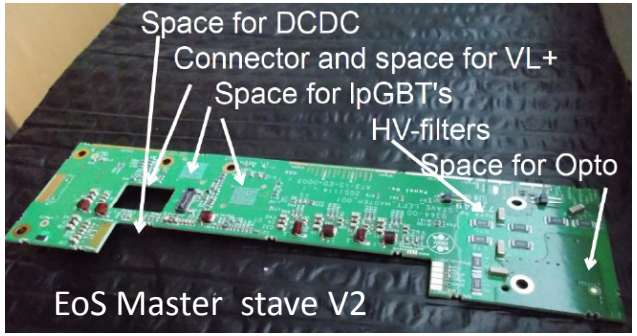
End of substructure (EoS) board

- Interface between Staves/Petals and Off-Detector
  - Incoming: Power & Commands, DCS signals
  - Outgoing: Data, DCS (10/20 Gbps)
- Key components
  - **lpGBT**: High-speed, data aggregator (MUX/DMUX), transceiver, rad-hard ASIC
  - **VTR+**: rad-hard optical link
  - **DCDC2s**: Power converters with single input and 2 power outputs
  - None of those components are still available
- First prototypes in hand with earlier versions of ASICs (GBTx, SFP transceiver)
  - V2 Master and V0 Slave prototypes
    - Electrical characterization successful
    - Material Budget Studies at the DESY Test Beam







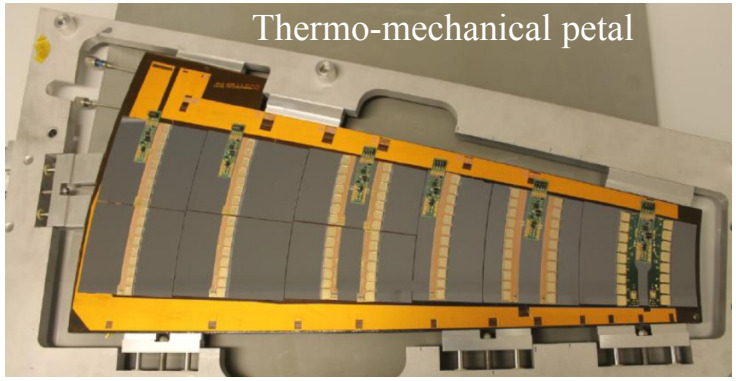


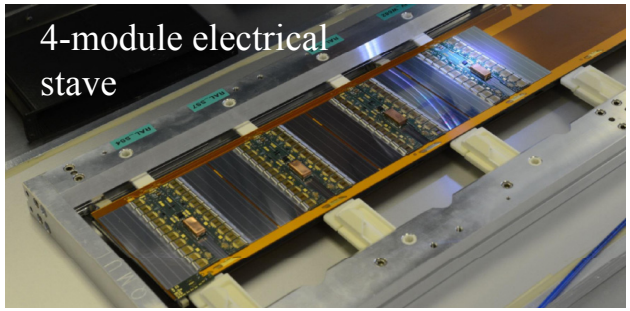
Full-size stave/petal prototypes

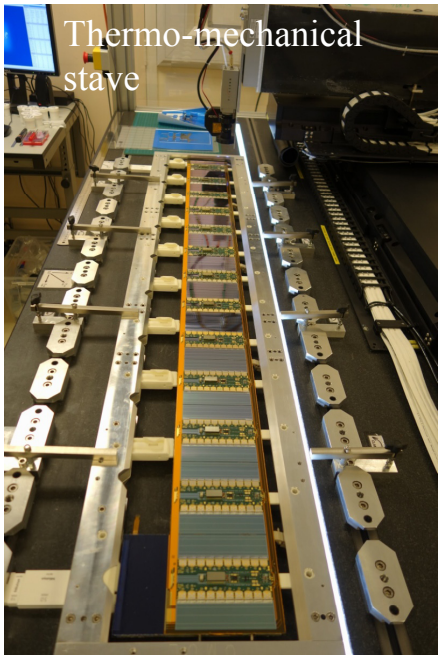
Fully loaded thermo-mechanical stave and thermo-mechanical petal

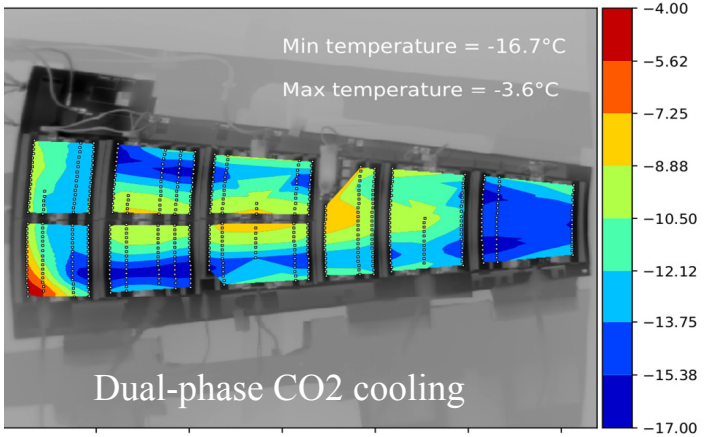
- Thermal testing (cold CO2 tests, thermal cycling, comparison to FEA)

First electrical staves (4 modules per side) assembled, first electrical results recently obtained

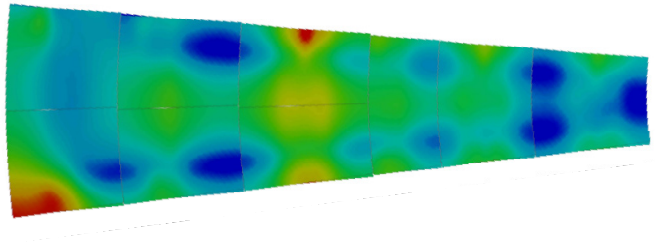






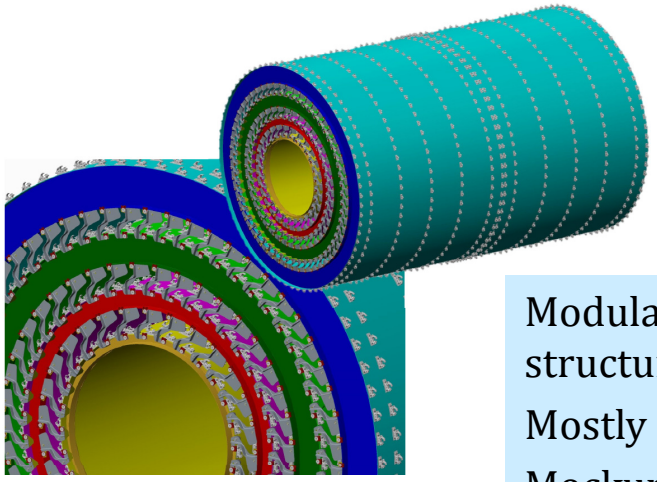


Good agreements between infrared measurements and FEA simulations

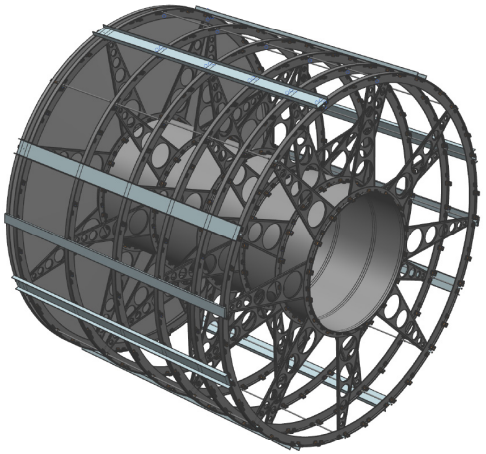


Global structures

Barrel: 4 concentric cylinders connected at the end by interlinks



Endcap: 6 concentric disks supported by the inner tube (low R) and rods and service trays (outer R)

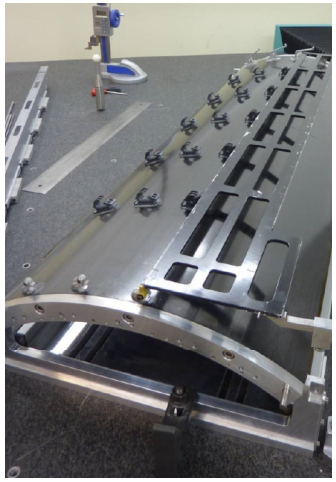


Modular cooling and electrical services implemented within the structures

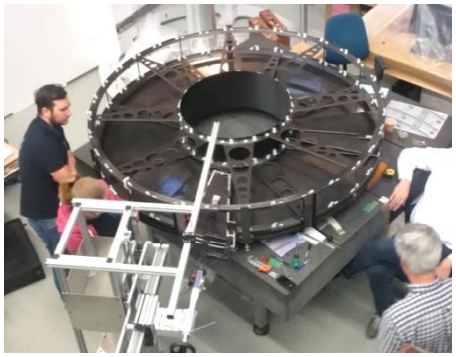
Mostly carbon fiber composite materials, extensively simulated

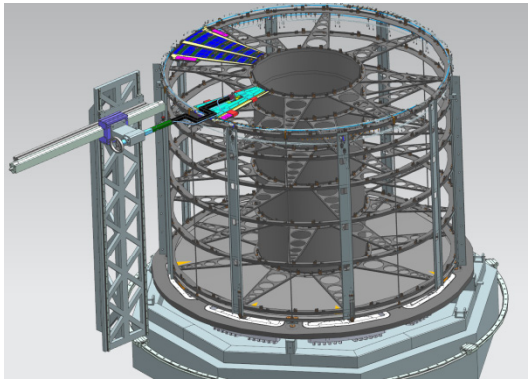
Mockup sectors/wheels already existing for both structures

End-insertion methods both for barrel staves and end-cap petals



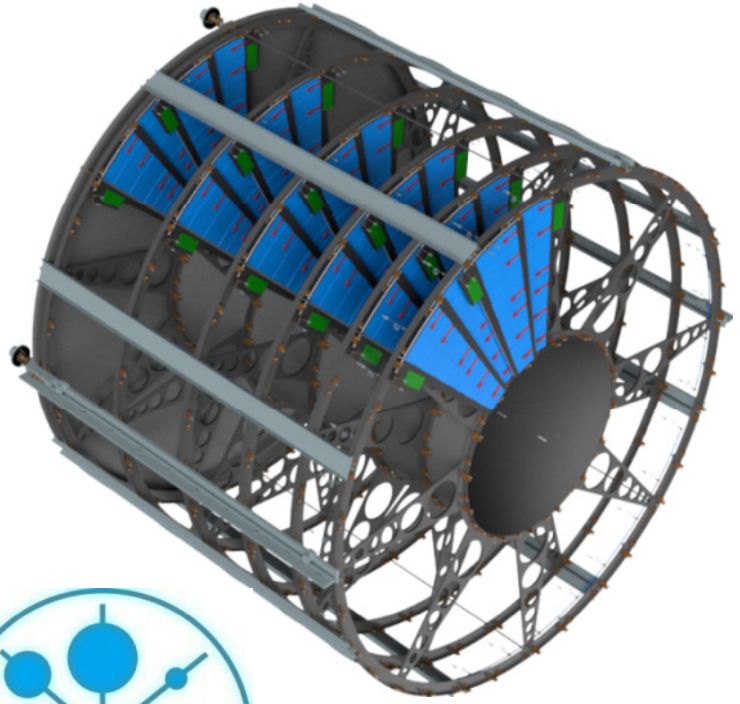
CF Service trays for endcap mockup





DESY involvement the ITk

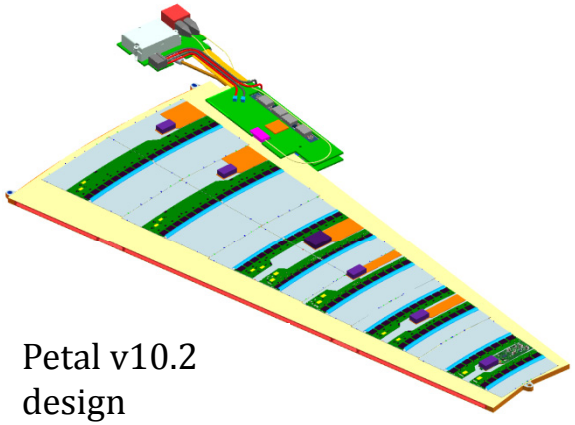
- Mostly focused on EC strips
  - EC Module assembly and test
  - Test beam and irradiation campaigns
  - EoS design and test
  - Overall petal design
  - Petal core manufacture and test
  - Bus tape tests
  - Petal assembly and test
  - End-Cap integration methods and test
  - Development of 1.5 kW CO2 system



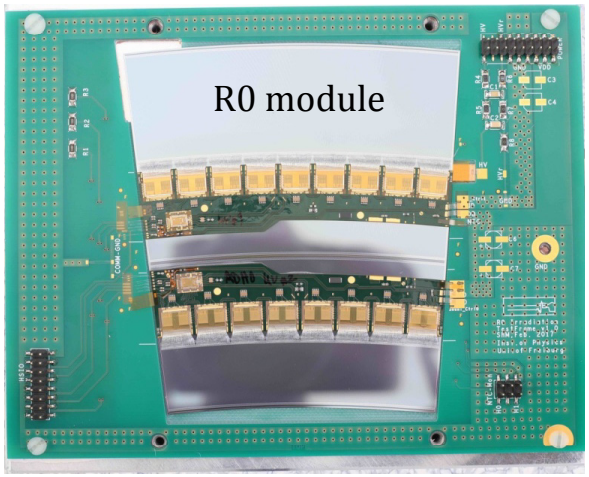
- Representation in the layout task force (N. Styles)
- FTK activities (S. Schmidt)
- ITk strips activity coordinators (I. Gregor, P. Goettlicher, I. Bloch, S. Díez)

Ultimately, DESY will deliver a fully instrumented strips endcap

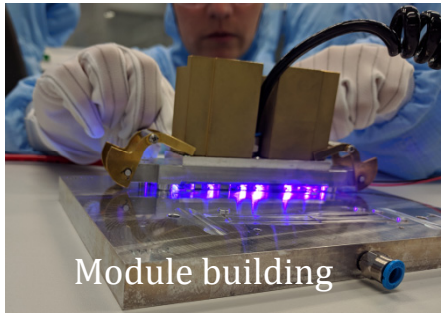
DESY activities

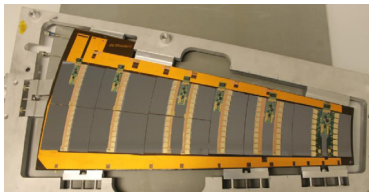


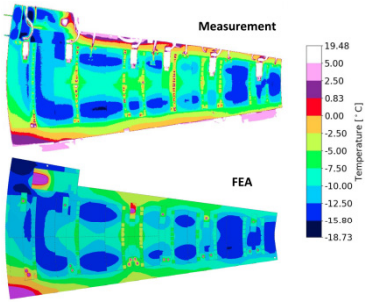
Petal v10.2 design



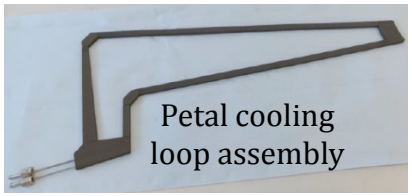
Bus tape co-curing

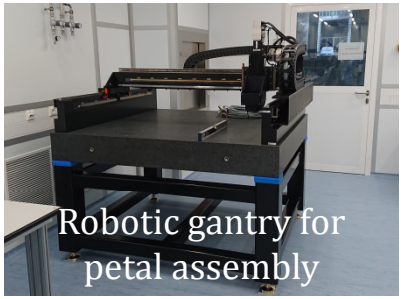




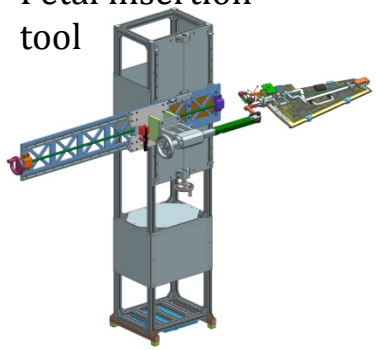


TM petal assembly and test





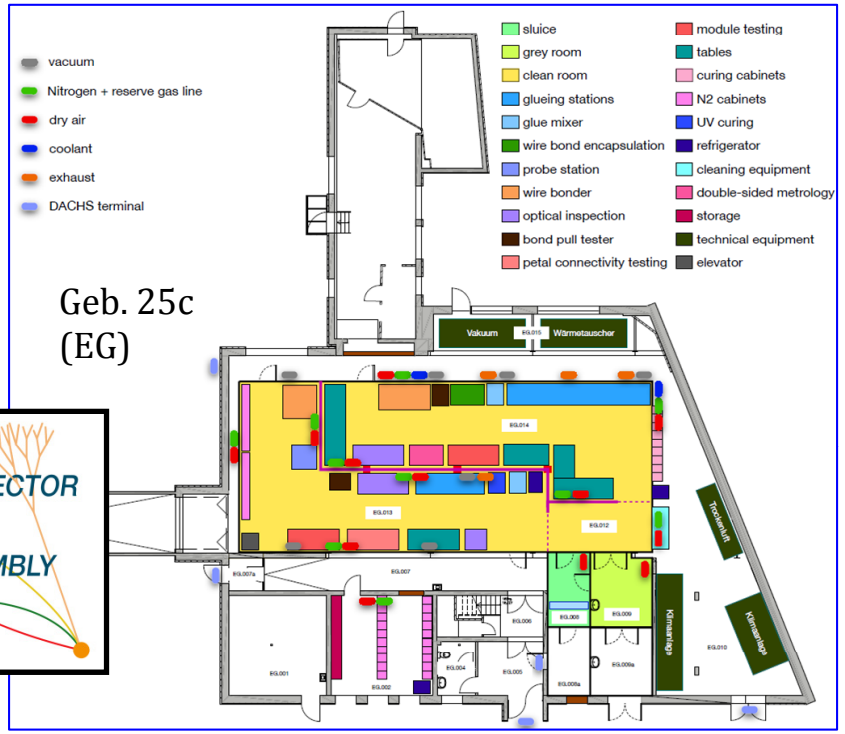
Petal insertion tool

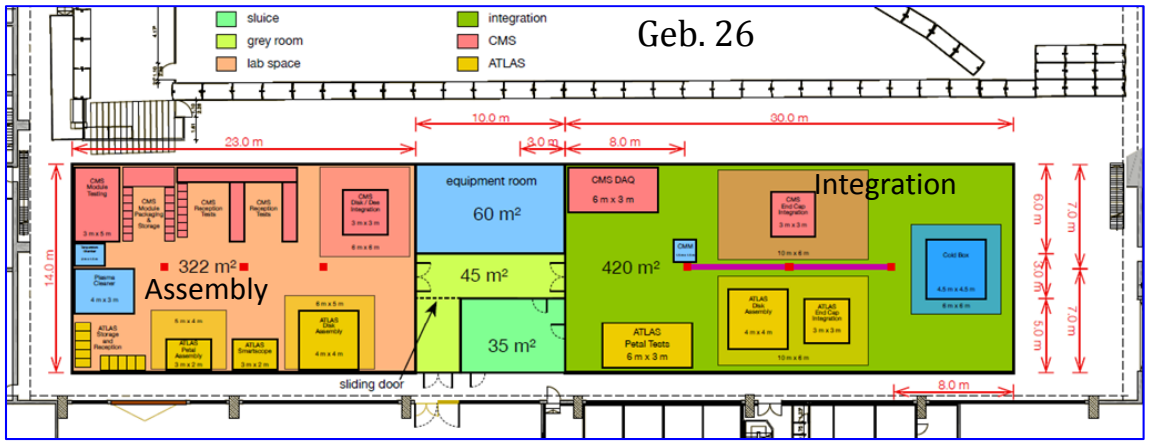


Facilities: DESY Hamburg

- **Geb. 25c**
  - ISO6 clean room and ISO7 labs
  - Module and Petal assembly, Module and EoS reception tests, validation and QC
- **Geb. 26**
  - ISO7 clean room
  - Test and QC for Petal cores, full petals
  - Endcap assembly, integration, system test
- **Geb. 43a**
  - Composites workshops for CFRP R&D
  - Petal core assembly

DETECTOR ASSEMBLY FACILITY





Facilities: DESY Hamburg

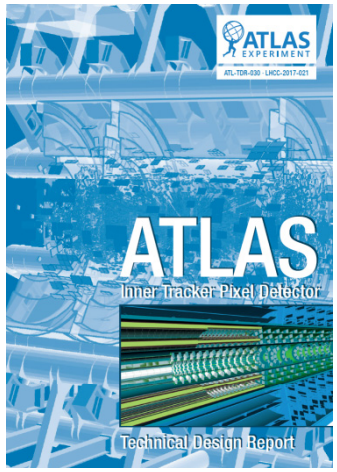
- **Geb. 25c**
  - ISO6 clean room and ISO7 labs
  - Module and Petal assembly, Module and EoS reception tests, validation and QC
- **Geb. 26**

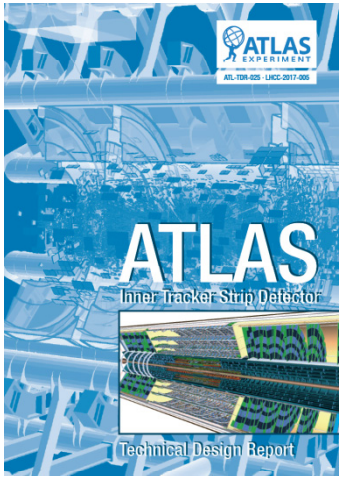
Shared with CMS group
All laboratories fully operational

  - Endcap assembly, integration, system test
- **Geb. 43a**
  - Composites workshops for CFRP R&D
  - Petal core assembly

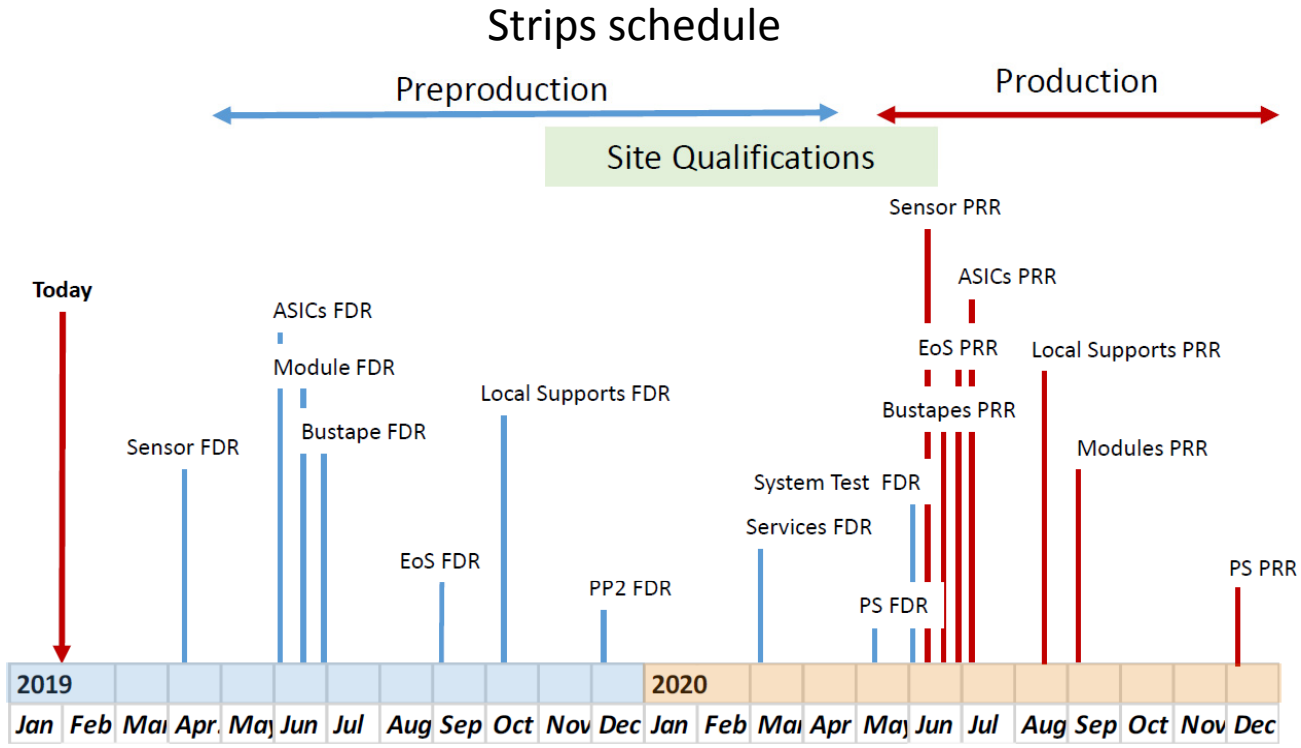

Autoclave at composites lab

ITk schedule





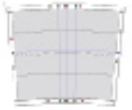
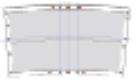
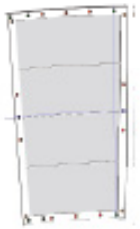
Strips and pixels TDR already public
Strips PDRs finalized last year
MoUs under approval



FDRs mark the beginning of pre-production

Backup slides

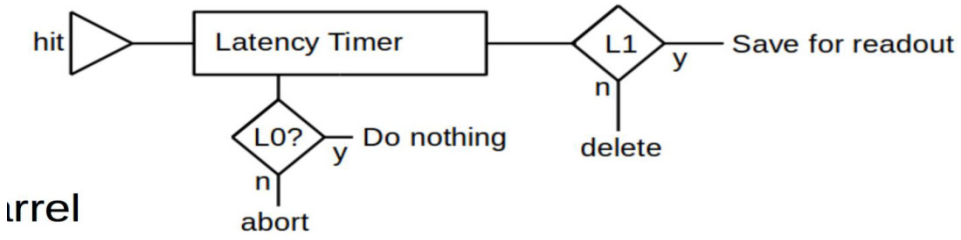
Endcap sensor geometries

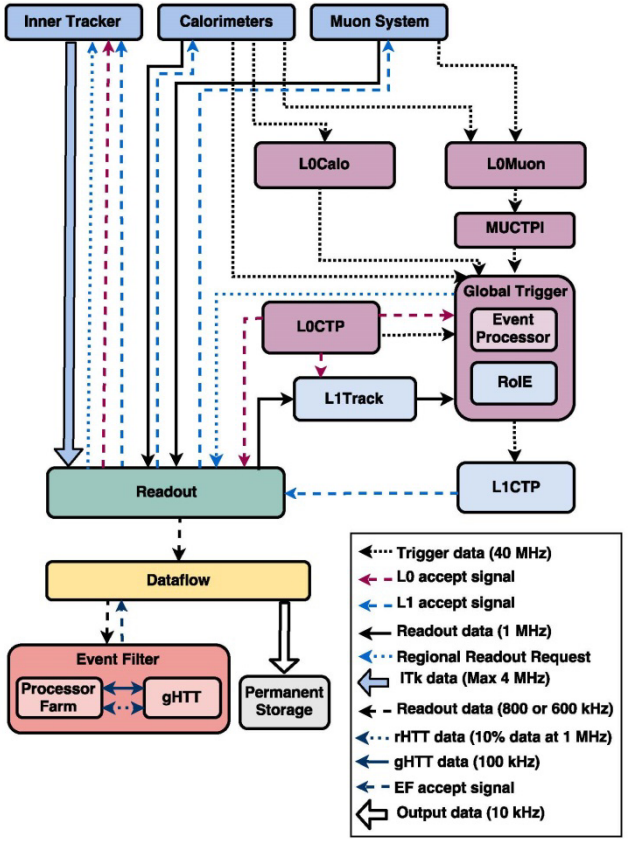
Sensor type	Number of sensors	Shape	Number of rows	Channels per sensor	Min/max pitch (μm)
Short-strips	3808	Square	4	5128	75.5
Long-strips	7168	Square	2	2564	75.5
EC Ring 0	768		4	4360	73.5/84
EC Ring 1	768		4	5640	69/81
EC Ring 2	768		2	3076	73.5/84
EC Ring 3	1536		4	3592	70.6/83.5
EC Ring 4	1536		2	2052	73.4/83.9
EC Ring 5	1536		2	2308	74.8/83.6

Trigger concept

- Complete ITk readout on L0 with 1 MHz rate and 10 µs latency or
- Partial ITk readout on L0 with 4 MHz/10 µs and full readout at L1 with 800 kHz/35 µs
  - outer pixel layers can provide full data on L0
  - inner layers can't due to bandwidth limitation of 5 Gb/s

→ fast clear on L0, wait for L1

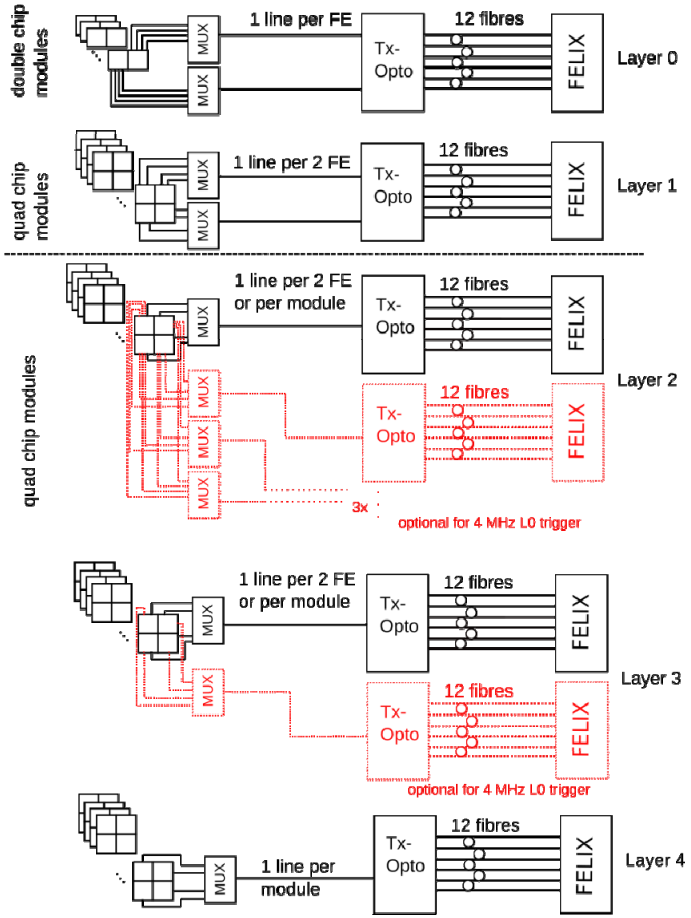




F. Hügging - ATLAS-D Freiburg 2018

Pixels bandwidth strategy

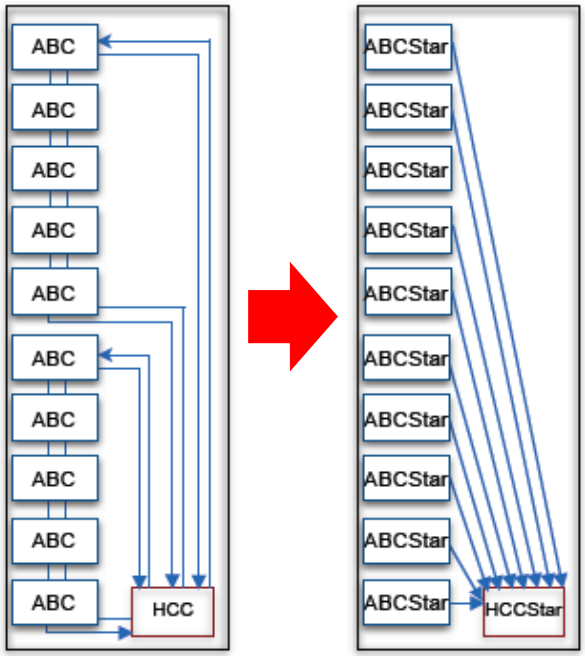
- Rates and bandwidths vary:
  - inner layer: 1 cable per FE
  - outer layer: combines links to make use of bandwidth
- For Command/Clock (TTC):
  - use GBT
  - 160 Mb/s between GBT and FE for all chips per module

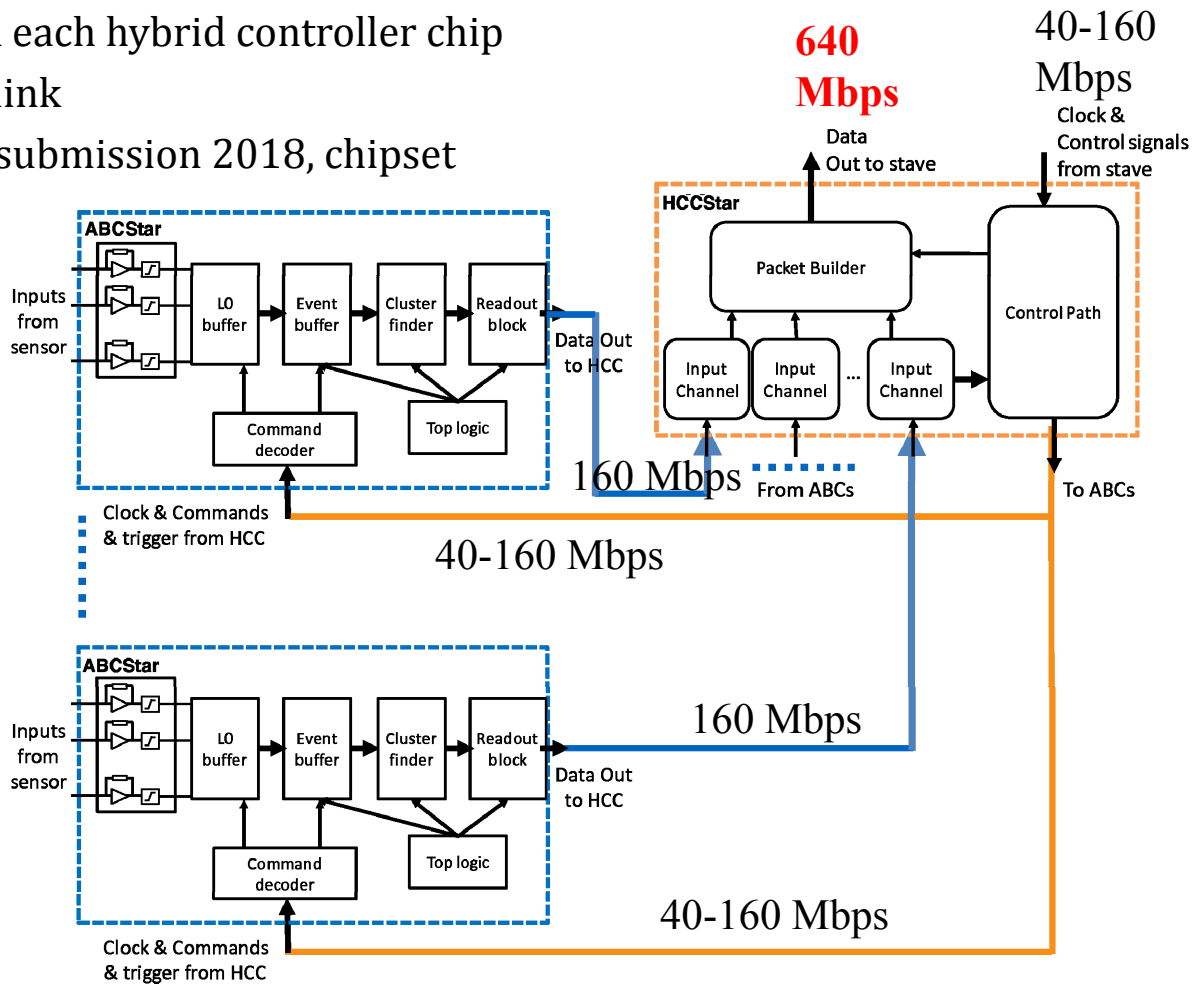


F. Hügging - ATLAS-D Freiburg 2018

1MHz L0 trigger rate: strips

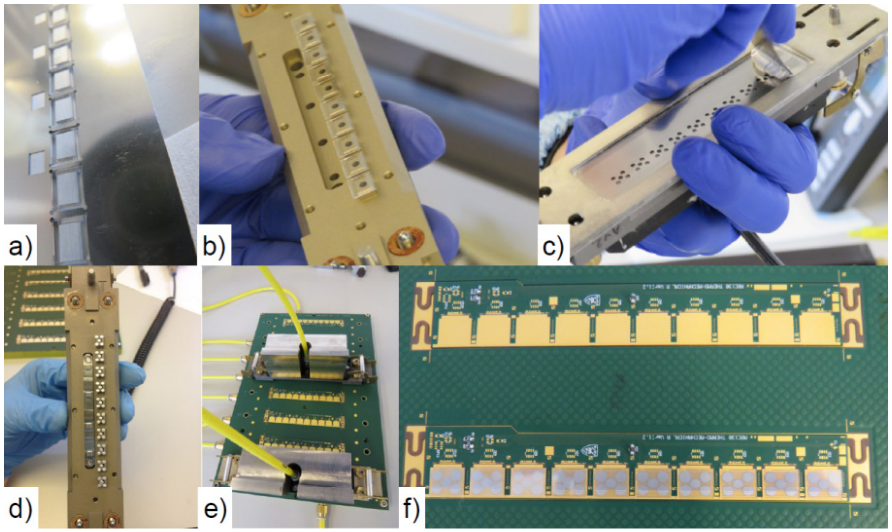
- Baseline 1MHz trigger rate requires new readout architecture: STAR
  - 640Mbit/s downlinks from each hybrid controller chip
  - Shared 160Mbit/s control link
  - ABCStar and HCCStar first submission 2018, chipset currently under test

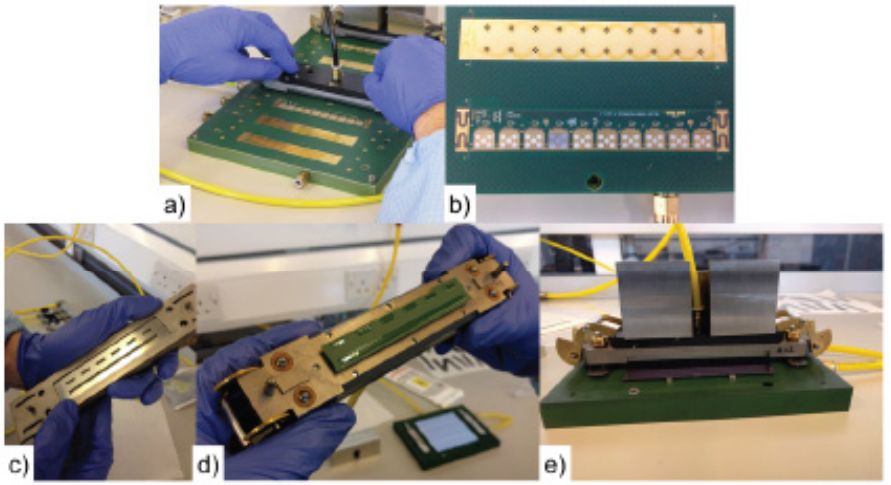




Module assembly

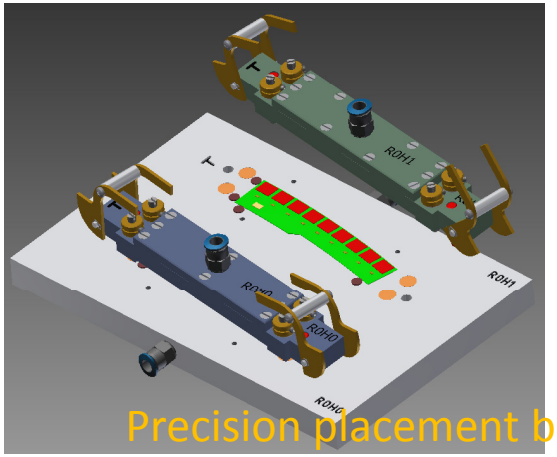
- Scalability for large scale production even at prototyping stage
  - Panelization of laminated hybrids
    - Designed for machine placement of passives and solder reflow
    - Tools developed for controlled gluing and wire bonding of ABCNs
    - Conservative design rules for high yield and volume, and low cost
    - Final hybrids testable on panels, ready for module assembly
  - Automated wire bonding of ASICs to sensor and hybrids to test frames
  - **Fully testable modules, ready for stave/petal assembly**



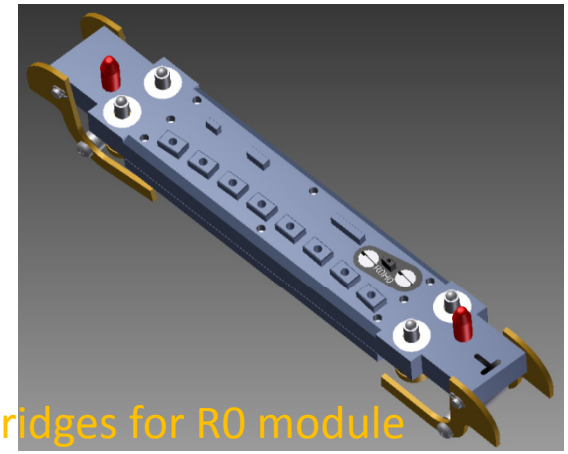


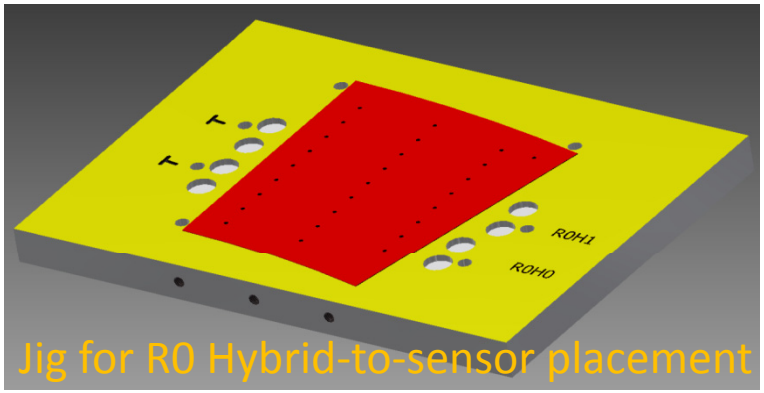
Harmonized tooling

- Test frames for all modules have identical connectors and size, to be tested in common multi-frame test stand (used also for hybrid panel test)
- Tooling outer dimensions harmonized and made to fit gluing and bonding stations
- Tools for all modules the same with only small geometrical adjustments reflecting the geometrical differences between the modules



Precision placement bridges for R0 module





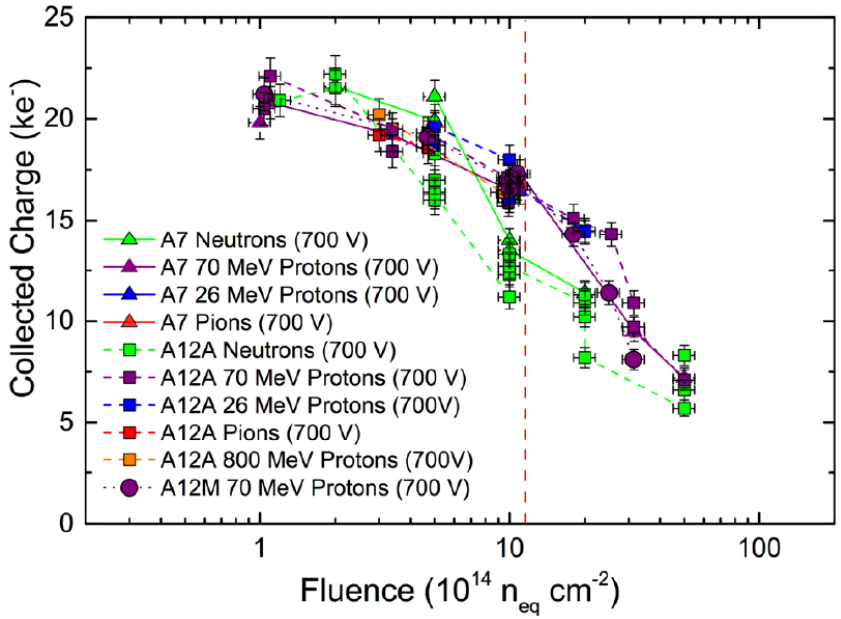
Jig for R0 Hybrid-to-sensor placement

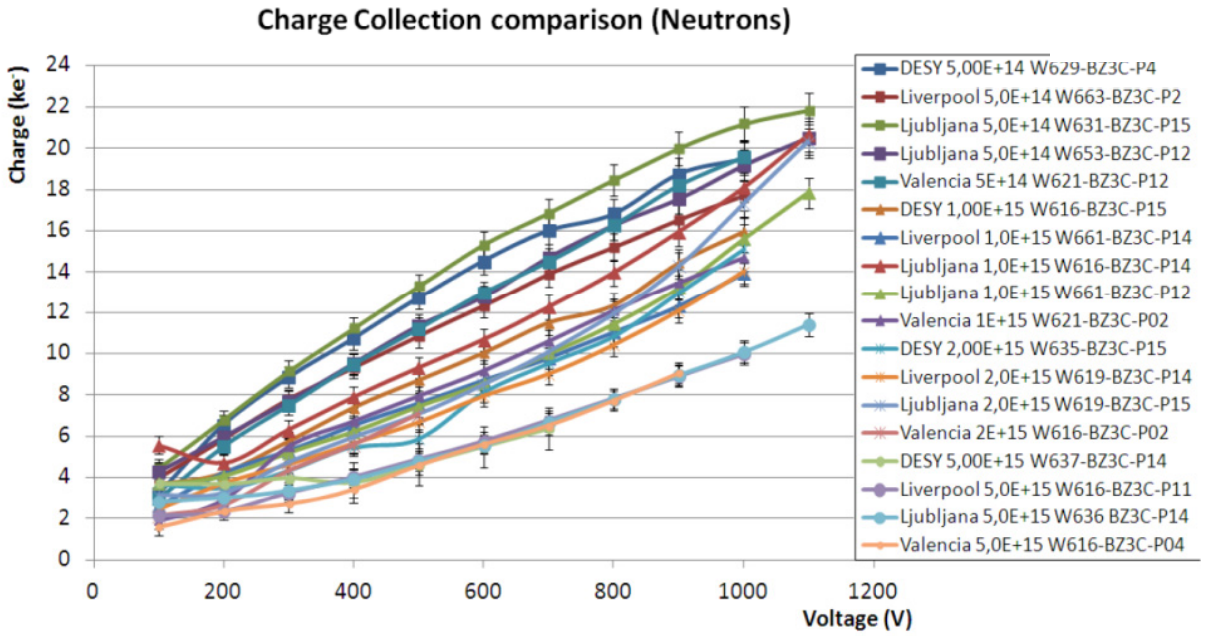
- Dedicated effort to keep end-cap and barrel tooling very similar to avoid individual learning curve for each type
- Target: every module site can, with short transition time, come to the aid of a struggling site, be it EC or barrel
- **This is true for every aspect in the ITk strips system**

Strip sensors performance

Very detailed studies over the course of several years

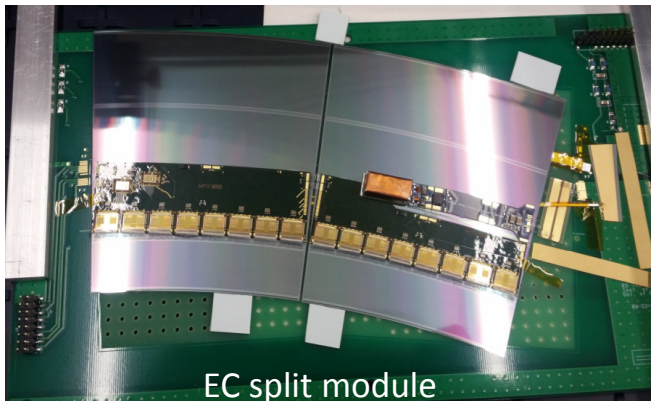
- Sensors meet specifications after irradiations!

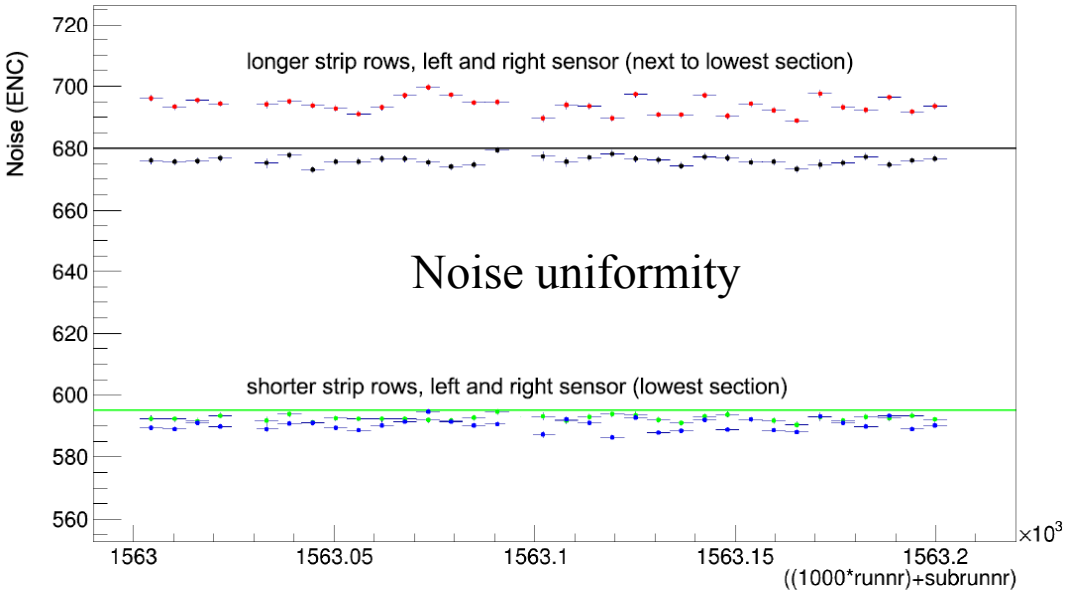


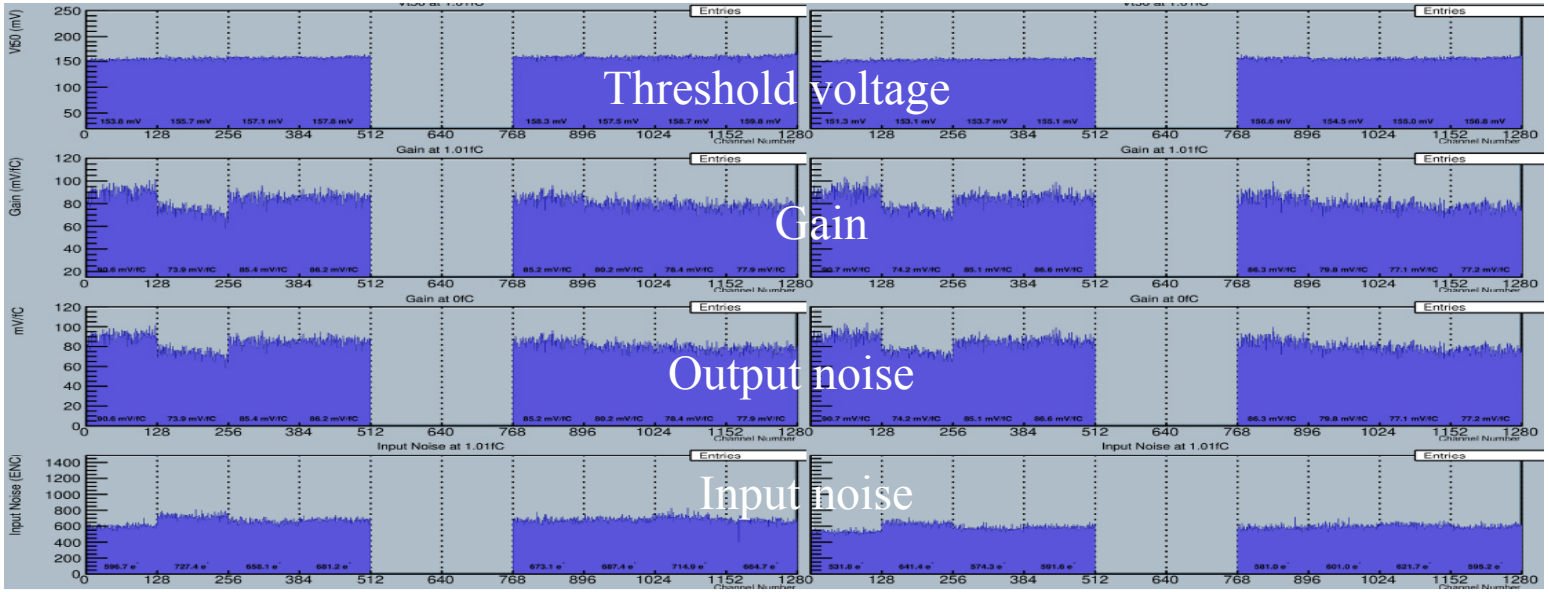


Module prototyping

>100 fully operational ABCN250 modules
A dozen of ABCN130 barrel and EC modules produced during the last year

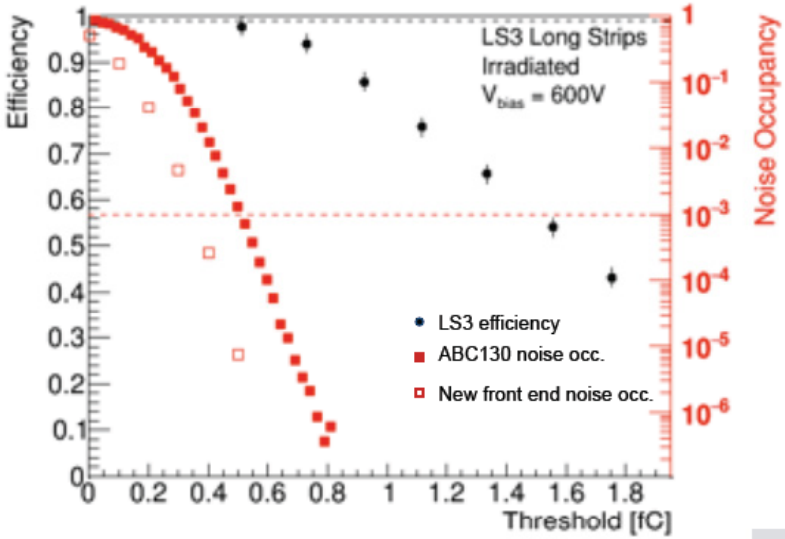






Strips test beam

most important and most discussed plot ...



- First measurements of front-end stage prototype for ABCStar indicate much improved noise behaviour

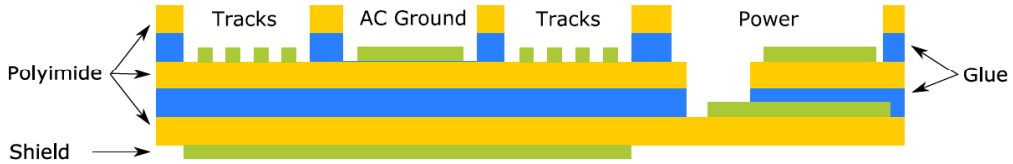
- Performance at end-of-lifetime is marginal with the used prototype components.
- Caveats:
  - Sensors were not annealed (+20% in signal)
  - Final sensor will have higher resistivity (+ 10% in signal)
  - Old front-end stage -> polarity fix (-20% in noise)
  - Enclosed transistors (-30% in noise)
- Extrapolated results to be confirmed with final prototypes

Module Type	Fluence (x E14)	Charge (500 V)	Charge (700V)	Noise (e^-)	S/N (@500 V)	S/N (@700 V)
SS	8,07	13,73	16,12	630,25	21,79	25,58
LS	4,13	17,28	19,47	748,96	23,08	26,00
R0	12,26	11,52	14,04	652,14	17,67	21,53
R1	10,11	12,54	15,00	640,33	19,59	23,43
R2	8,72	13,33	15,74	657,26	20,28	23,95
R3	8,01	13,77	16,16	643,93	21,39	25,10
R4	6,80	14,64	16,98	795,68	18,40	21,34
R5	6,00	15,30	17,60	835,36	18,32	21,07

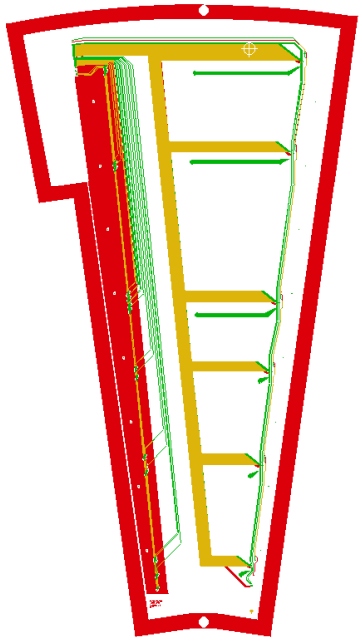
Bus tapes

Flexible, low-mass printed circuits that provide readout, power and control lines to the modules along the staves/petals

Total thickness: 180 um



Data traces + shield layer



125 um track-and-gap differential lines

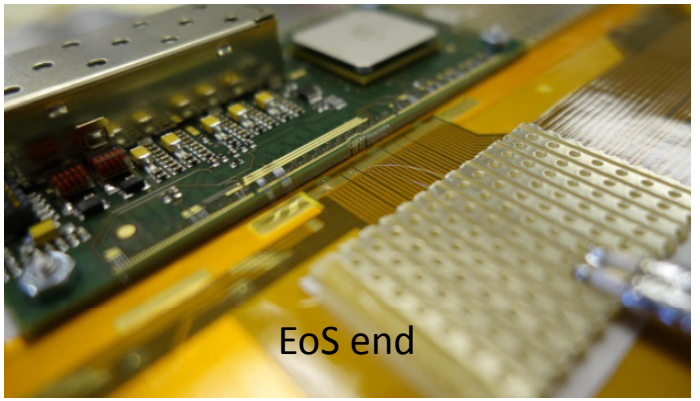
Design optimized for 640 Mbps signals

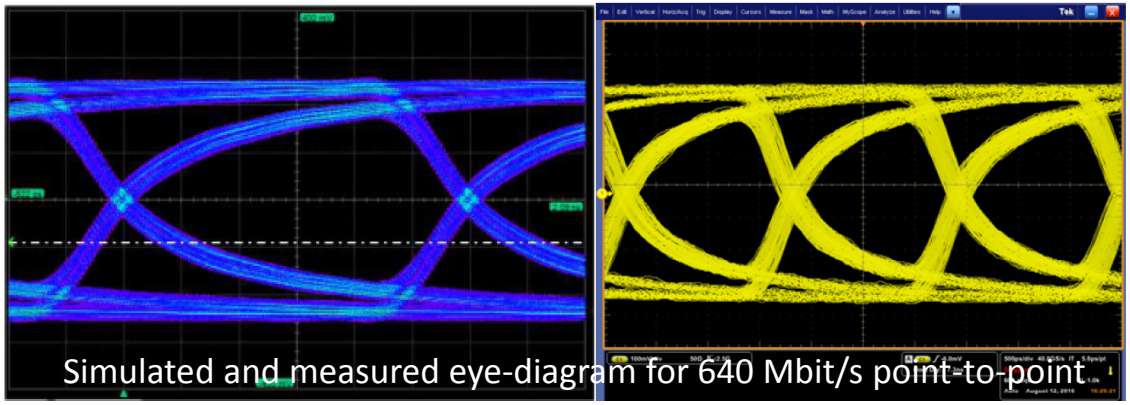
Al material discarded due to excessive deformation during co-curing

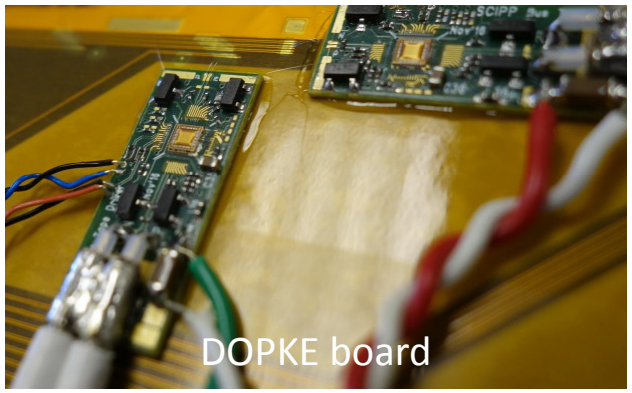
Gold-plated pads to facilitate bonding

Bus tape electrical tests

- S-parameters measurements
  - 1.4 m long test tape
  - Test chips containing drivers and receivers of the type expected in the HCC130 ASIC
  - Point-to-point eye-diagram at 640Mbps measured and simulated
  - Bit Error Ratio (BER) for 10 loads at 640 Mbps: < 10^{-12}

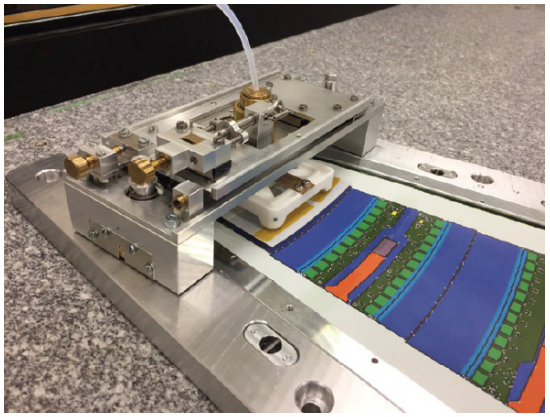


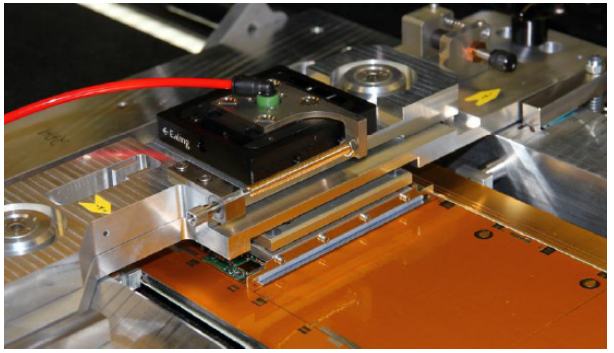

Simulated and measured eye-diagram for 640 Mbit/s point-to-point

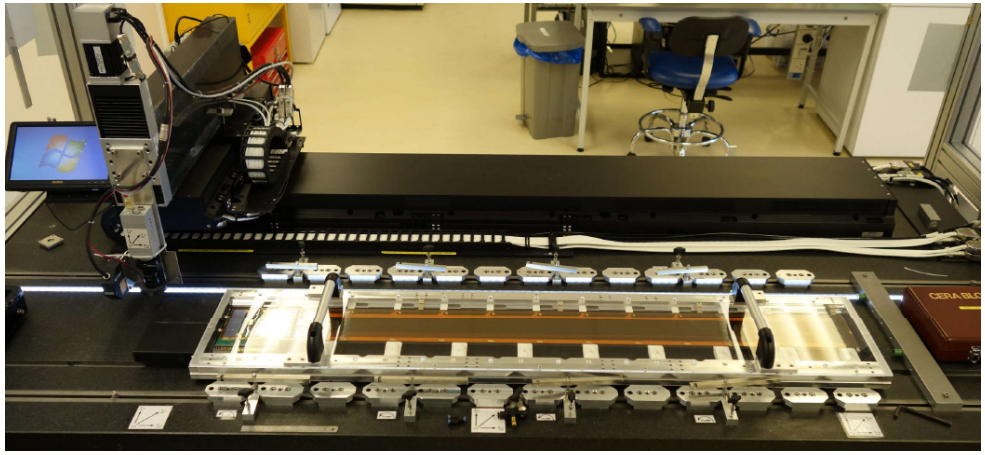


Module loading on core structures

- Accurate placement of modules on cores and good cooling connection
- Common procedure
  - Survey precision fiducials to determine stave/petal reference frame
  - Load module from loading station onto bridge
  - Survey module fiducials and (iteratively) position module
  - Apply glue pattern of SE4445 adhesive
  - Place module – cure glue, held in place by bridge – repeat 14/9 times
  - Perform post-mounting stave/petal metrology survey
  - Wire bonding to bus-tape and EoS + electrical acceptance test



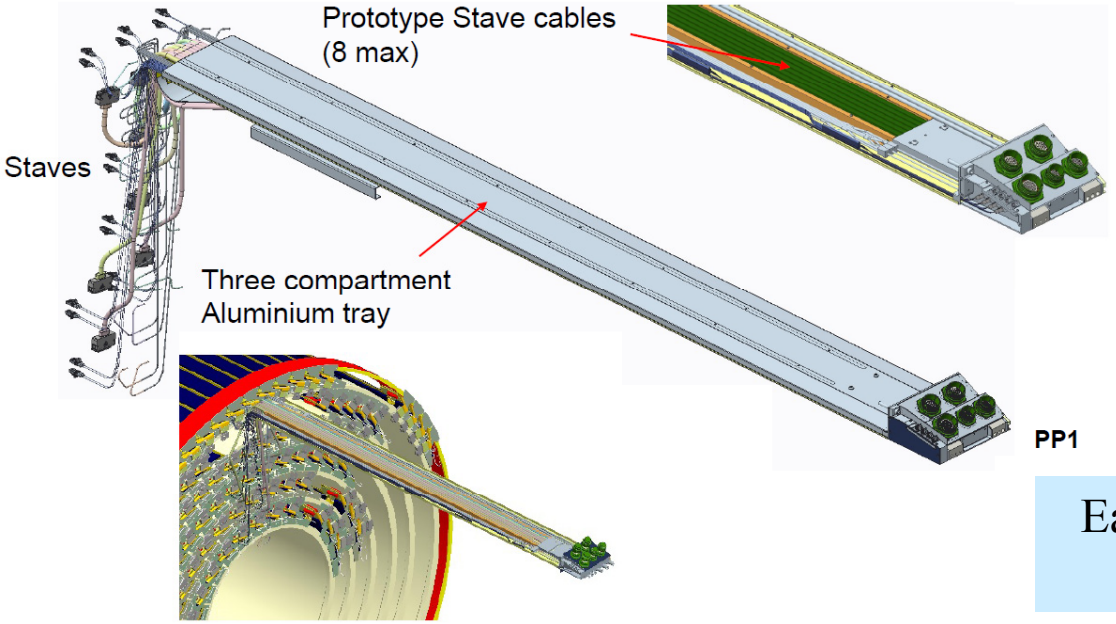




Performance target:
Lateral accuracy ± 50 µm
Average distance between module and core = 150 µm

Service modules

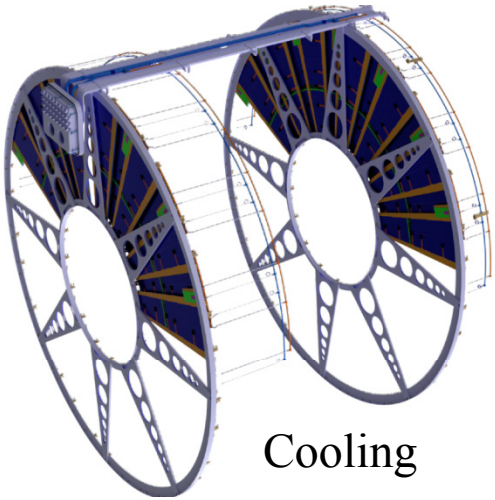
- Both barrel and end-caps aim for modularity of services
  - Service modules consist of compact structures that provide electrical and cooling services to several staves and petals in the structures
  - Barrel services:
    - Each service modules reaches several staves within each cylinder, or preferably a bigger single cylinder sector (max. of 8)
    - Service tray hooks up to the Outer Cylinder, runs on top of end-cap structure and reaches PP1 at the edge of the end-caps structural bulkheads (the "lids" of the ITk)



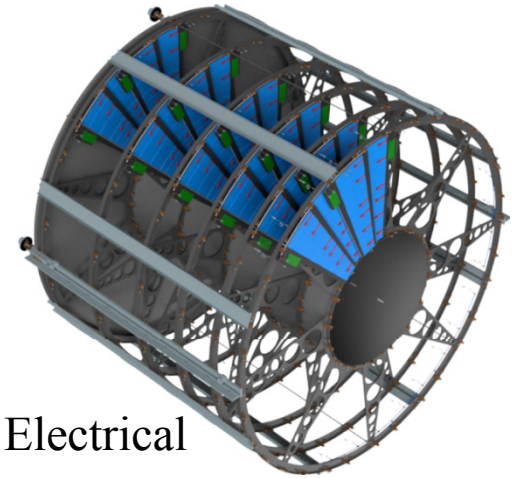
Early prototype, design slightly outdated

Service modules

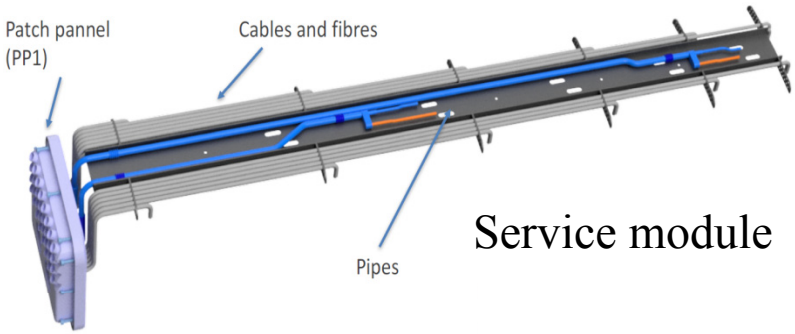
- Both barrel and end-caps aim for modularity of services
  - Service modules consist of compact structures that provide electrical and cooling services to several staves and petals in the structures
  - En-cap services:
    - Service module runs on top of end-cap structure
    - De-coupled electrical and cooling services
    - Minimizing damage in case of a catastrophic cooling failure (one loses single hits on multiple tracks instead of losing full tracks)
    - Not enough space for electrical services to follow cooling segmentation
      - Cooling module serves half-disks (16 or 32 petals), electrical module serves phi sector (24 petals)



Cooling



Electrical



Service module

Facilities: DESY Zeuthen

- Hall for module construction in Zeuthen (**ZModuleHall**)
  - Planning ongoing, Cleanroom of ISO6 or better, Dec 2017