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SILICON DETECTORS II

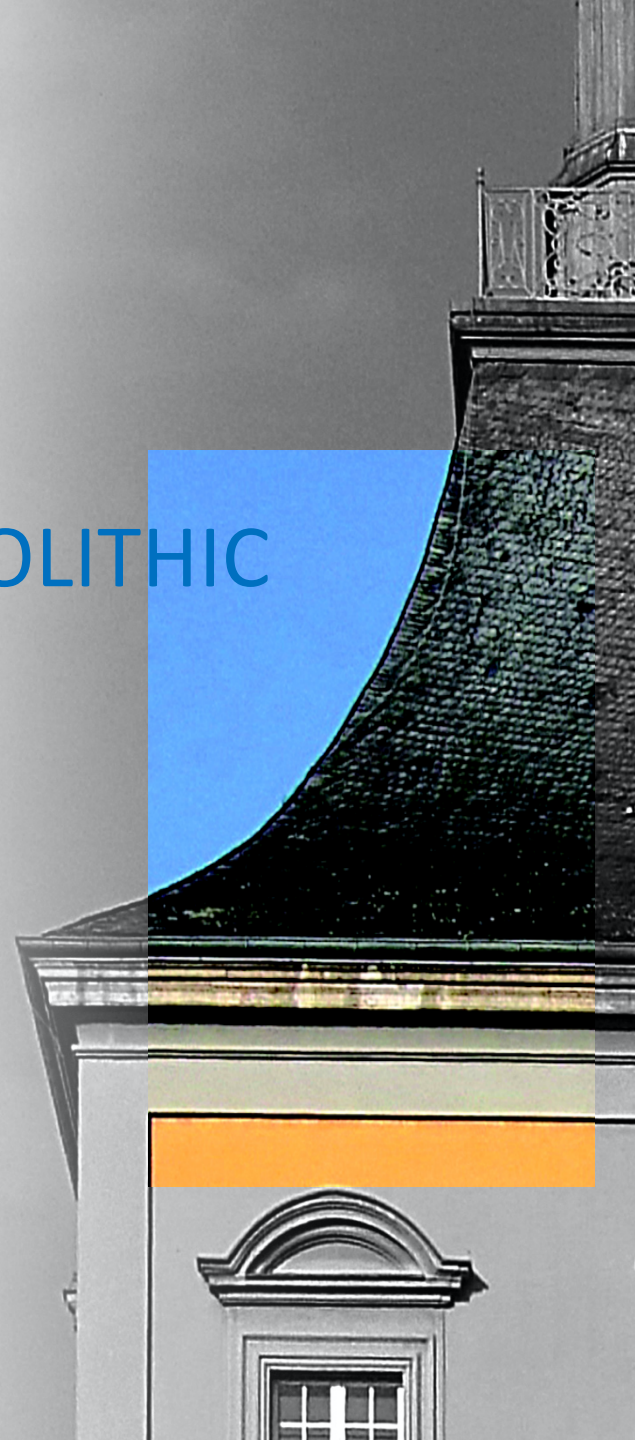
PIXEL DETECTORS – HYBRID & MONOLITHIC

LECTURE AT EDIT2020 SCHOOL

DESY HAMBURG

FEBRUARY 19, 2020

NORBERT WERMES
UNIVERSITY OF BONN



Outline

- A somewhat longer intro: Why pixels? and How ?
- How to make a (hybrid) pixel detector?
- Hybrid pixel detectors
  - The pixel “sensor”
  - The pixel readout chips
  - Hybridization
- Monolithic pixel detectors
  - Large electrode approach
  - Small electrode approach
- DEPFET pixels
- Conclusions / Take-home messages

apologies: I know ATLAS developments much better than CMS&ALICE

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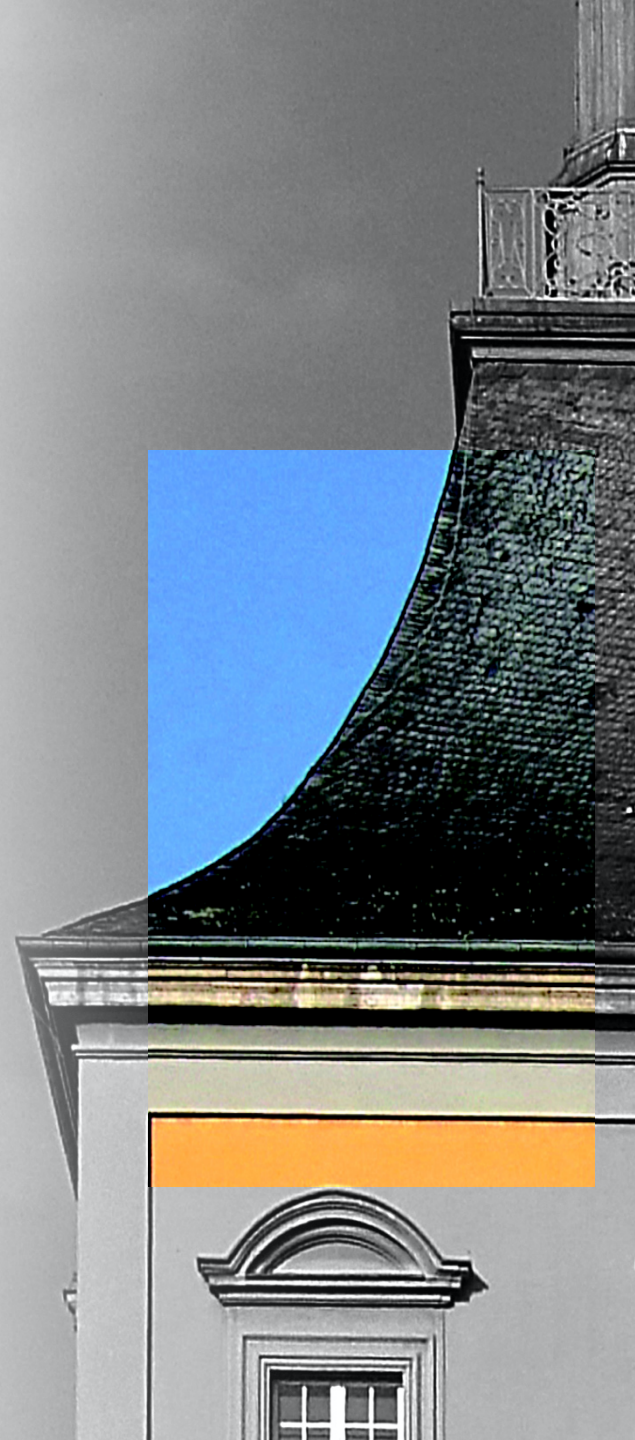
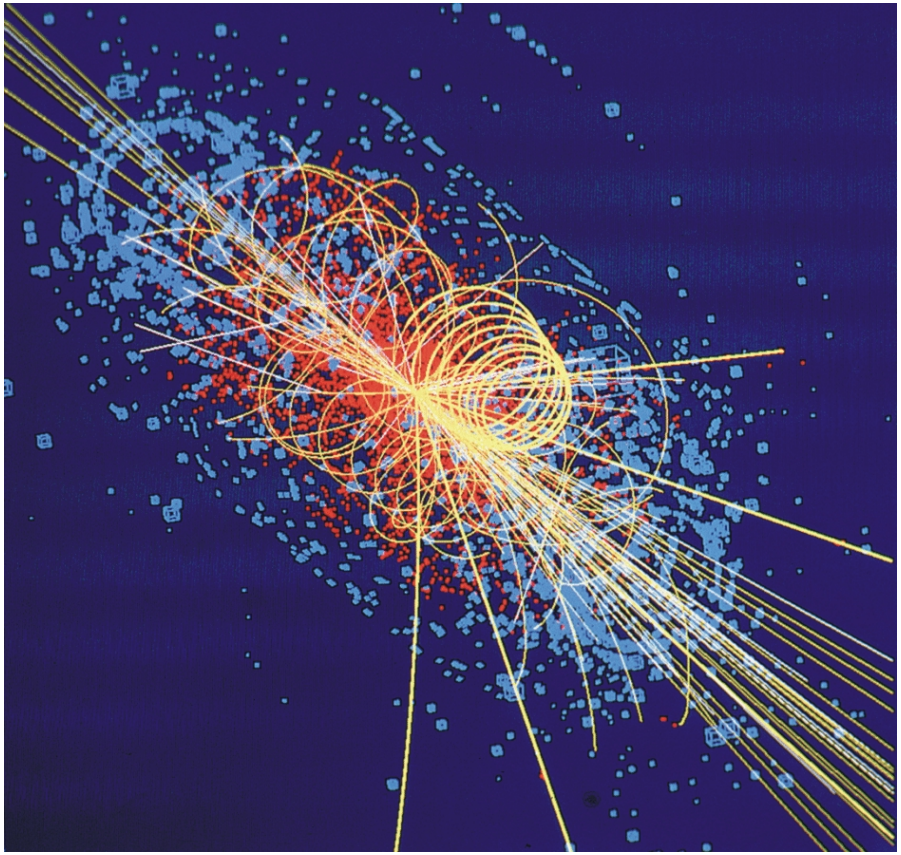
WHY PIXEL DETECTORS?



Collisions at the LHC



proton-proton collisions (ATLAS, CMS)

40 MHz, L=10^{34}cm^{-2} s^{-1}

$\Rightarrow$ every 25 ns have 25 interactions with 1600 tracks

$\Rightarrow$ **10^{11} tracks / s**

Ion + Ion collisions (ALICE)

300 kHz, L=10^{29}cm^{-2} s^{-1}

$\Rightarrow$ dN/dη ~ 8000 for central collisions

$\Rightarrow$ $10^{9\text{-}10}$ tracks / s

LHC (pp) = 10^6 x LEP in track rate !

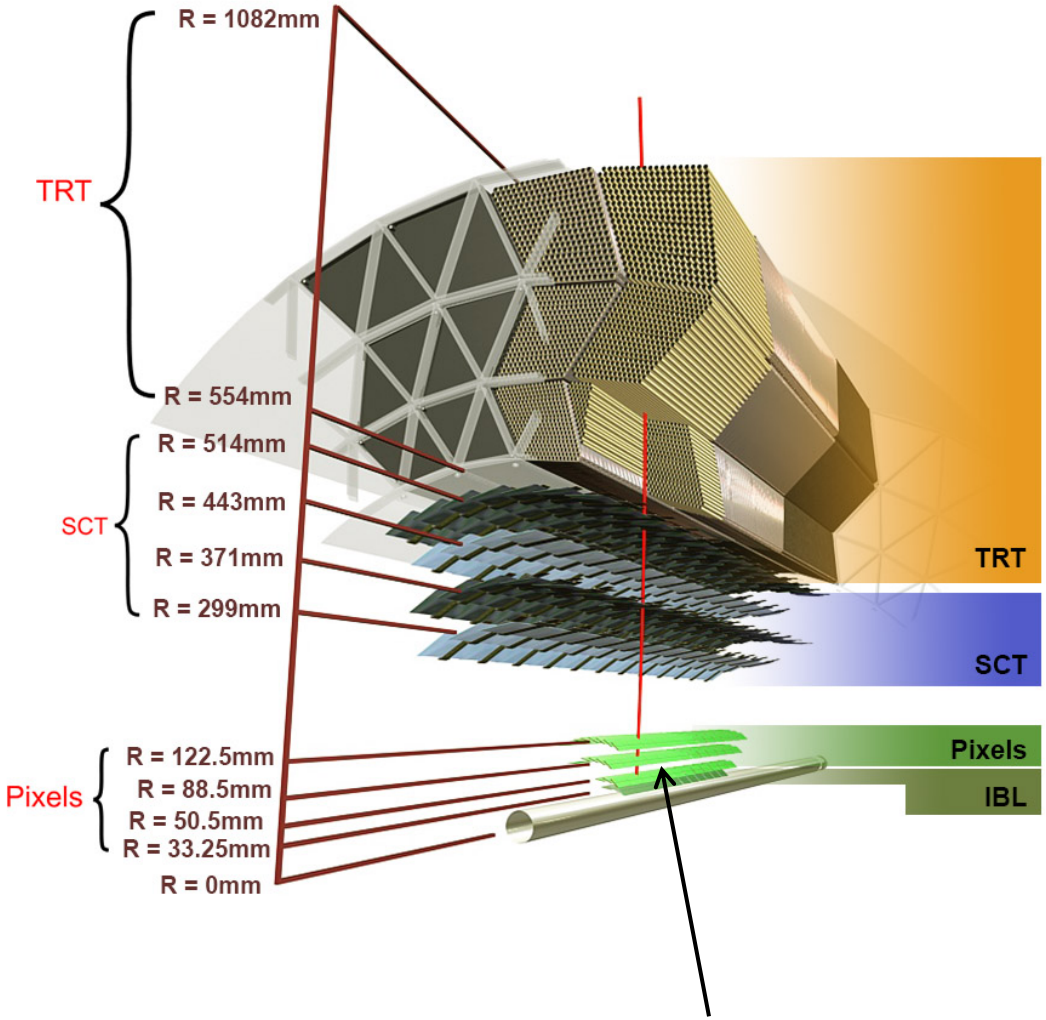
HL-LHC $\approx 10^7$ x LEP

The dominant challenges therefore are

- particle hit rate (up to 2 GHz/cm^2)
- radiation damage

… and **only pixels** can live up to this

Tracking detectors in ATLAS (4 pixel layers)



50 x 400/250 μm^2 cells
~100 x 10^6 pixels

Transition Radiation Tracker ~ 300 m$^2_{eq}$

Silicon Strip Detector ~ 60 m^2

Silicon Pixel Detector ~ 2 m^2

	points	σ (Rϕ) (μm)	σ (Rz) (μm)
TRT	36	170	-
SCT	4	17	580
PIXELS	4	10	115

ATLAS IBL in operation

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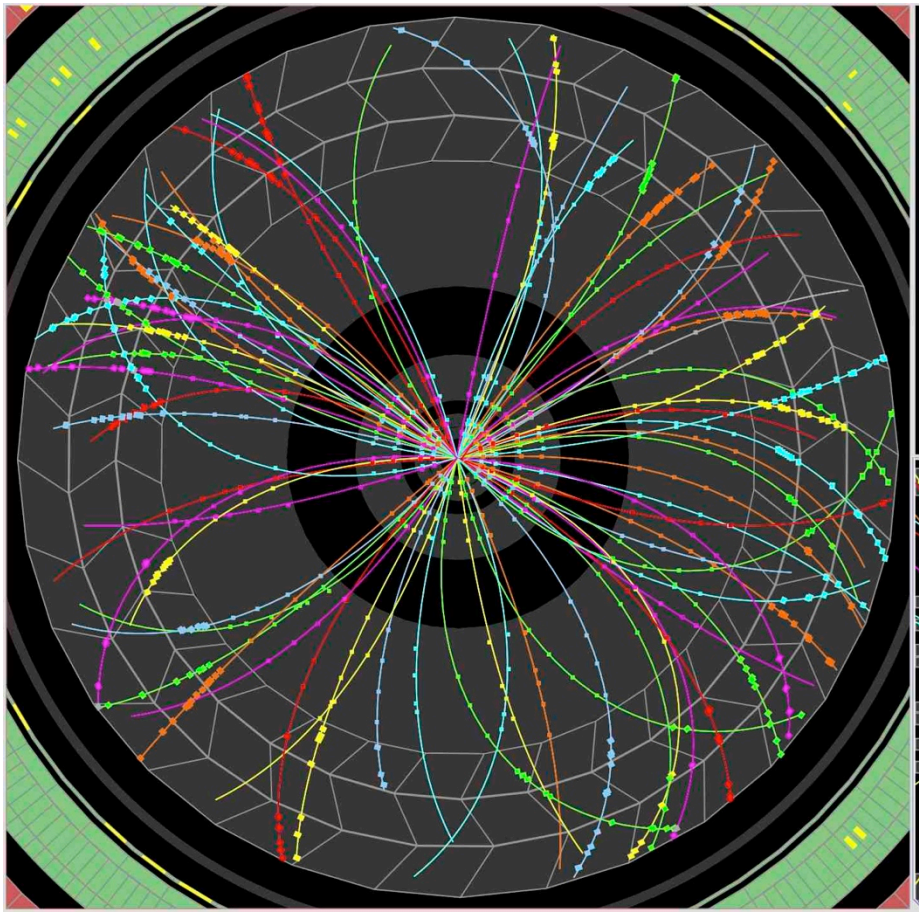
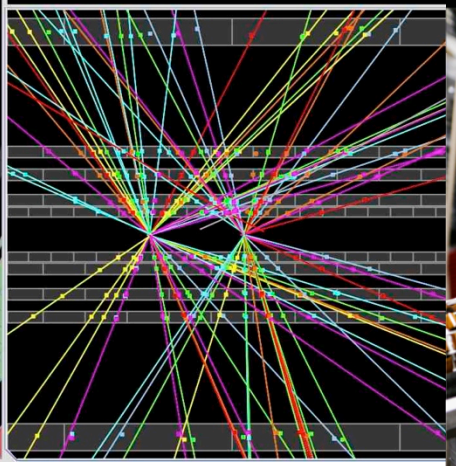
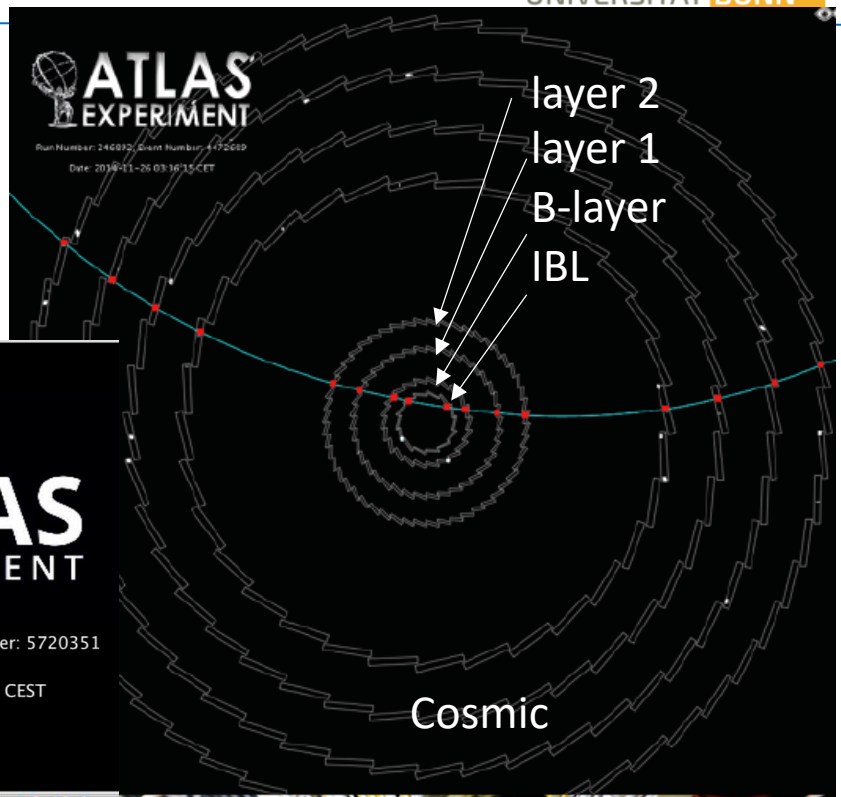
A 4-hit pixel system!

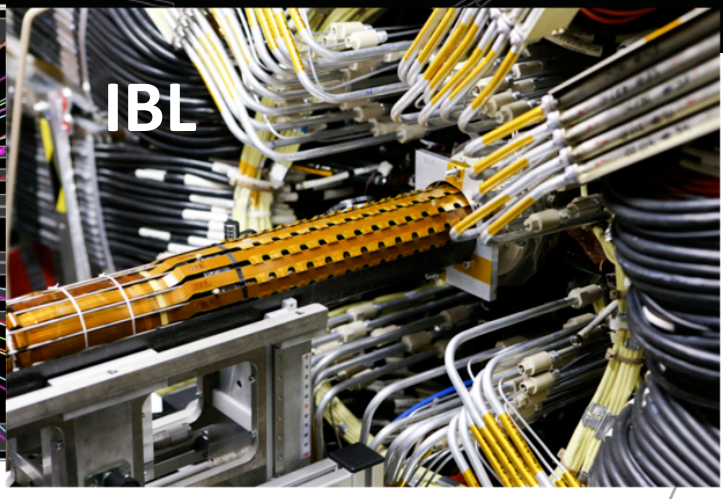
important for b-quark tagging

13 TeV pp collision, low luminosity, 2 interactions

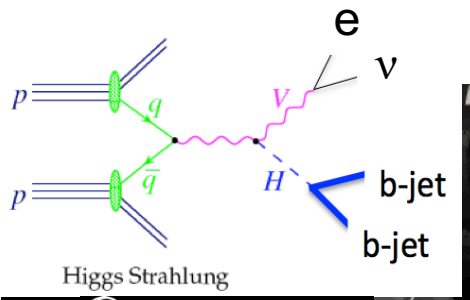


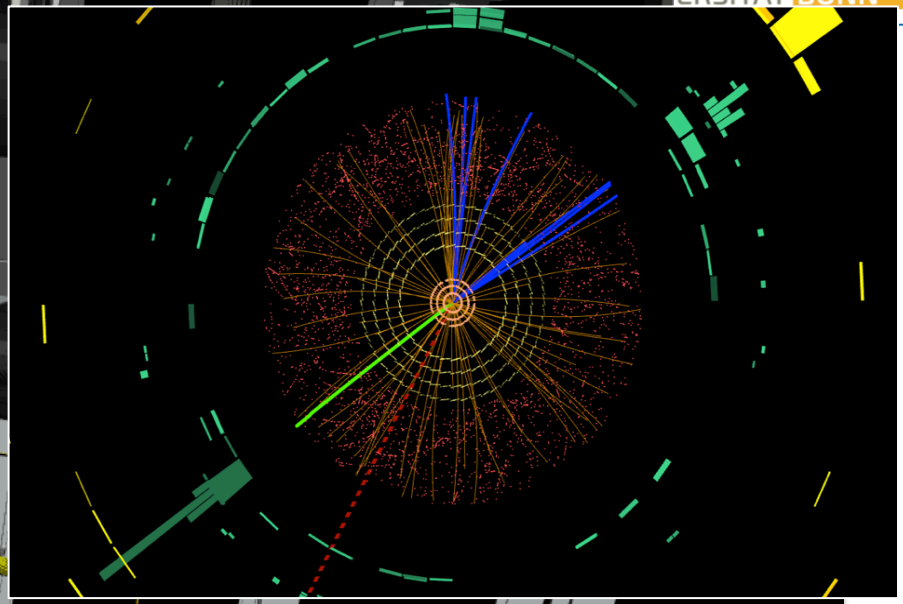


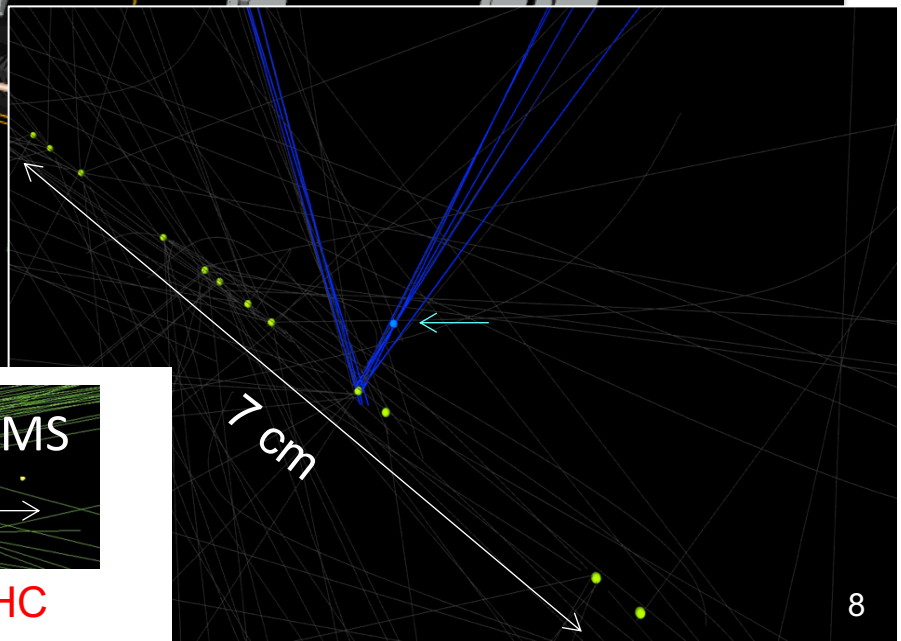


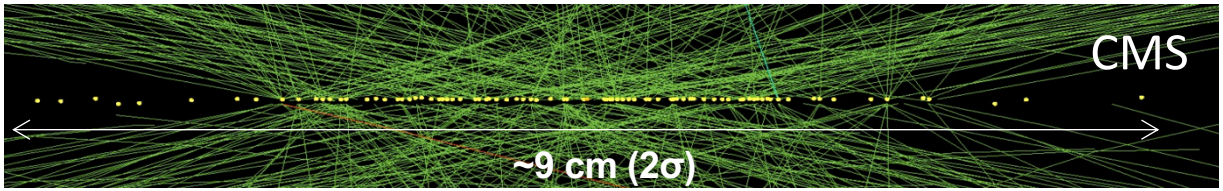


pp -> WH -> νl + bb









78 interactions piling up in one collision → 200 @ HL-LHC

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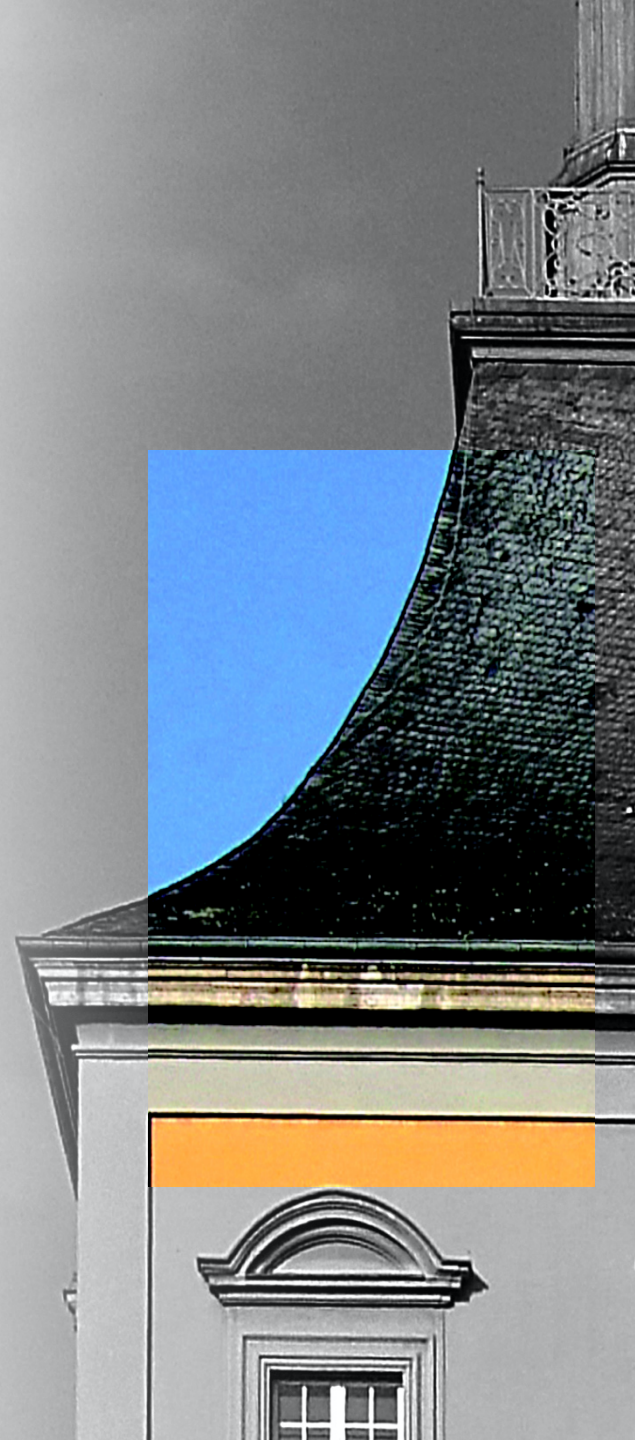
HOW TO … ?



Patterned Semiconductor Detectors

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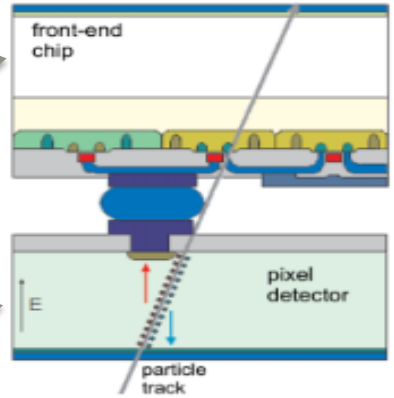
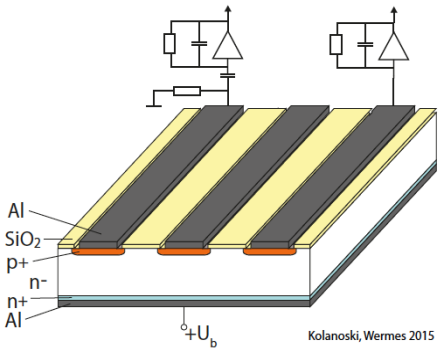
readout chip

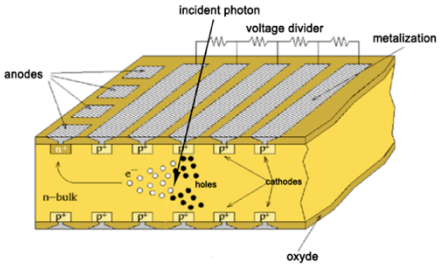
Hybrid pixel detector

sensor chip

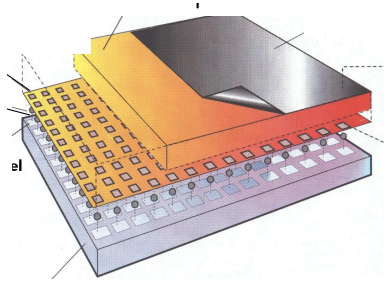




Microstrip Detector
-> Lecture 1



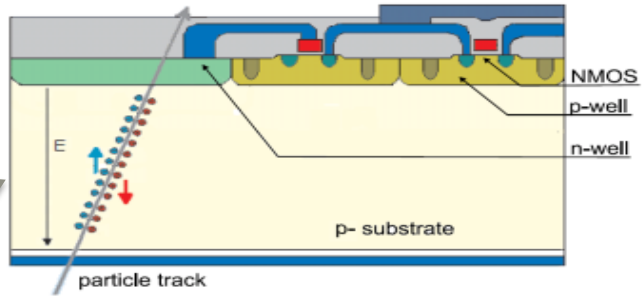
Silicon Drift Detector



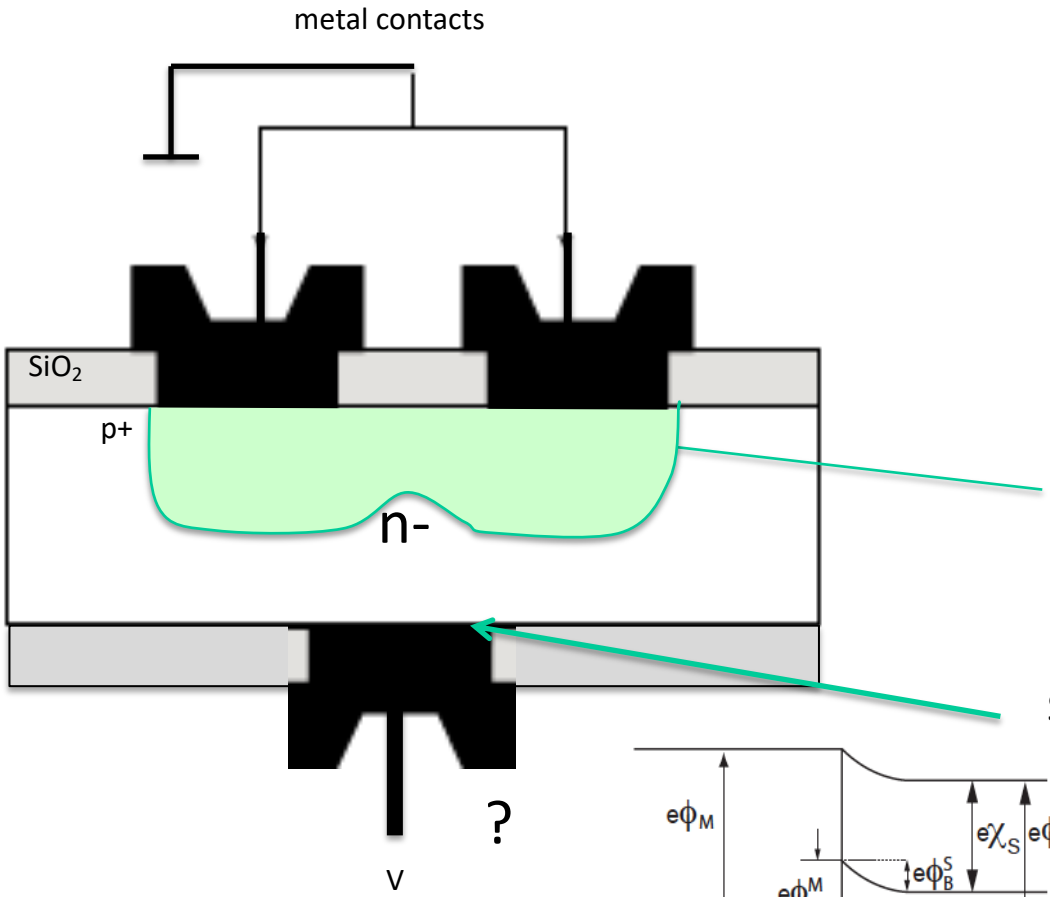
Pad -> Pixel Detector

Monolithic active pixel sensor (CMOS)

Sensor & readout

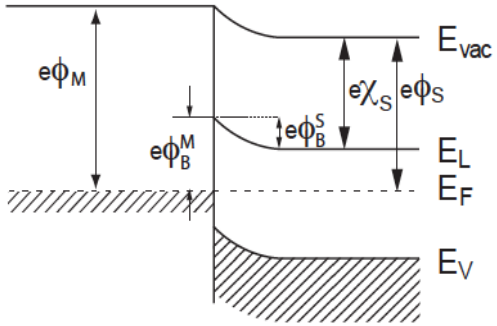


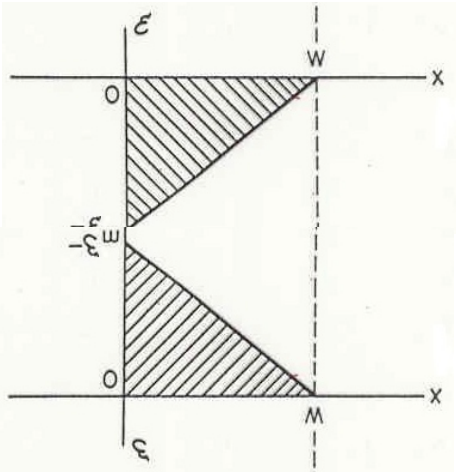
Contacting a silicon detector



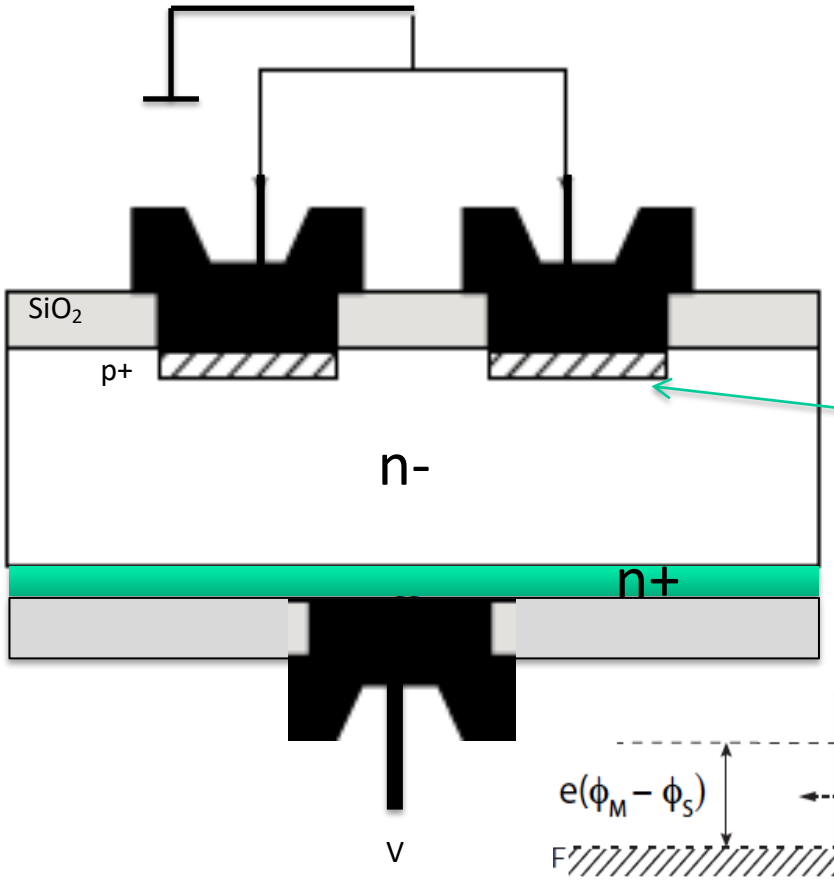
pn - junction

Schottky contact

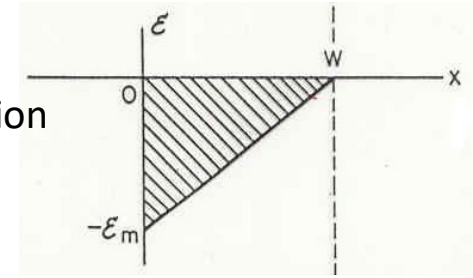


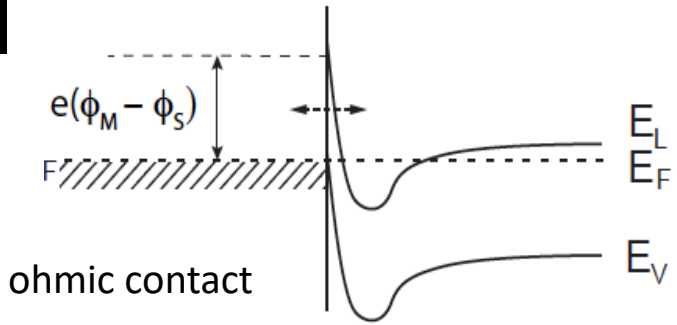


Contacting a silicon detector

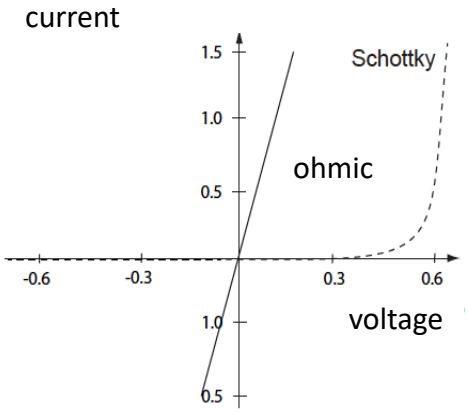


pn - junction

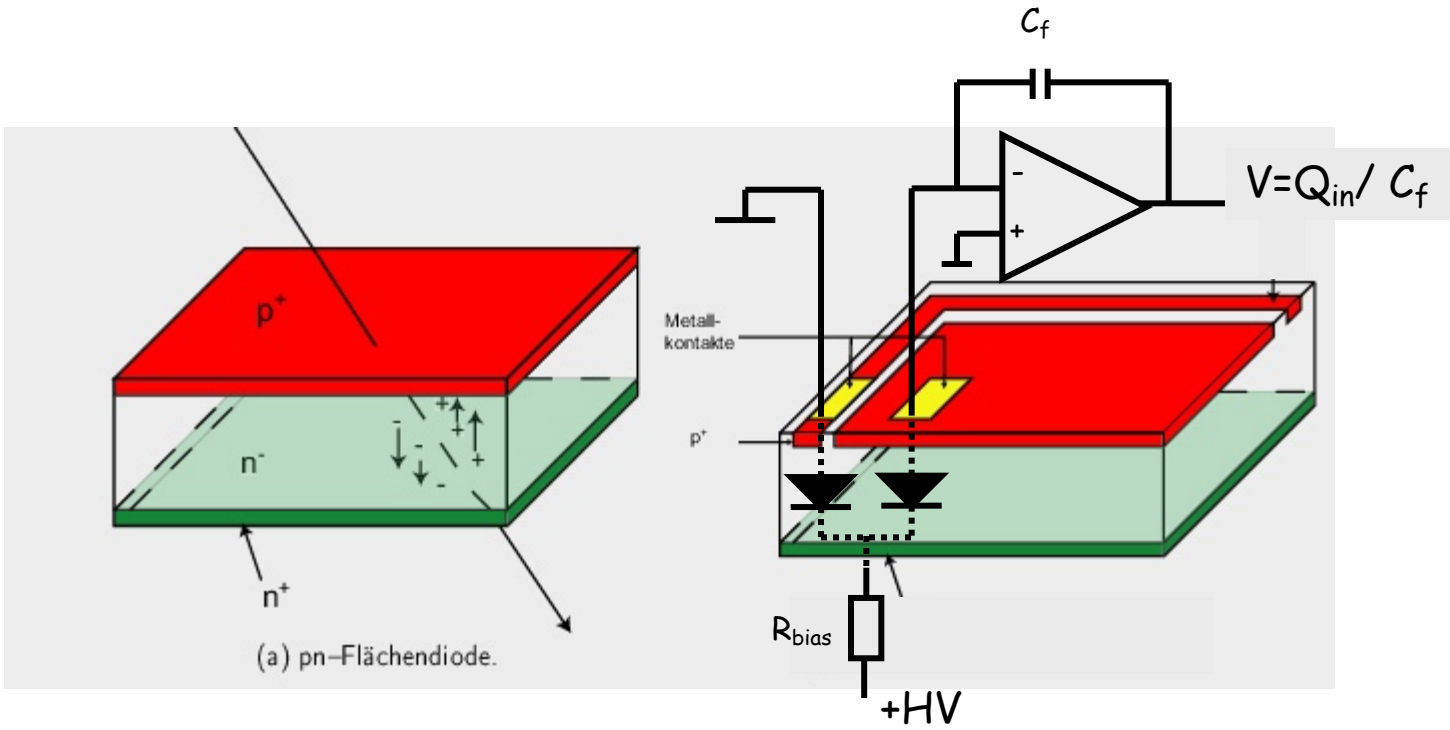




ohmic contact

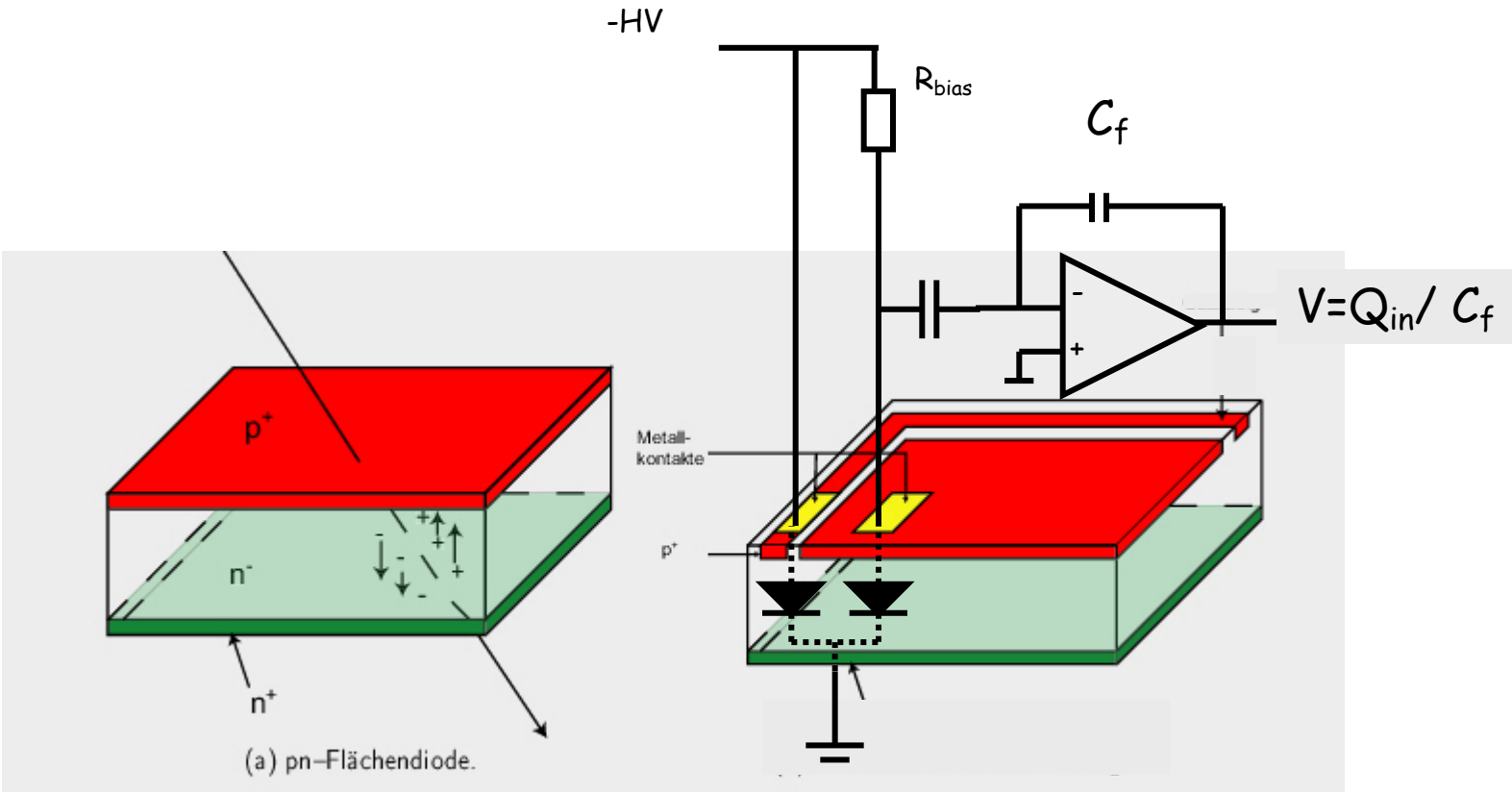


BIASING



DC - Coupling

BIASING



AC - Coupling

Biasing (a strip) or - even worse - a pixel detector

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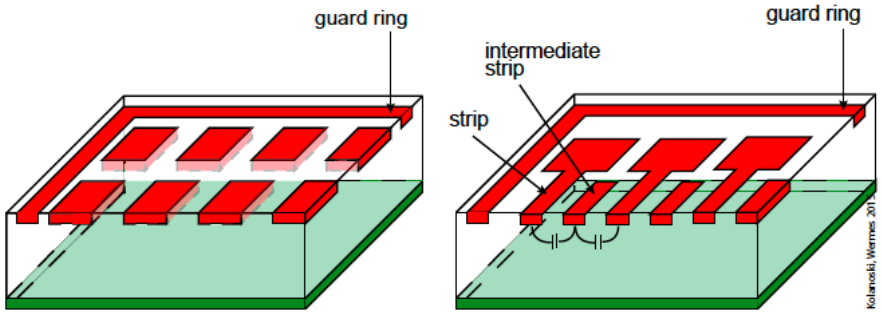
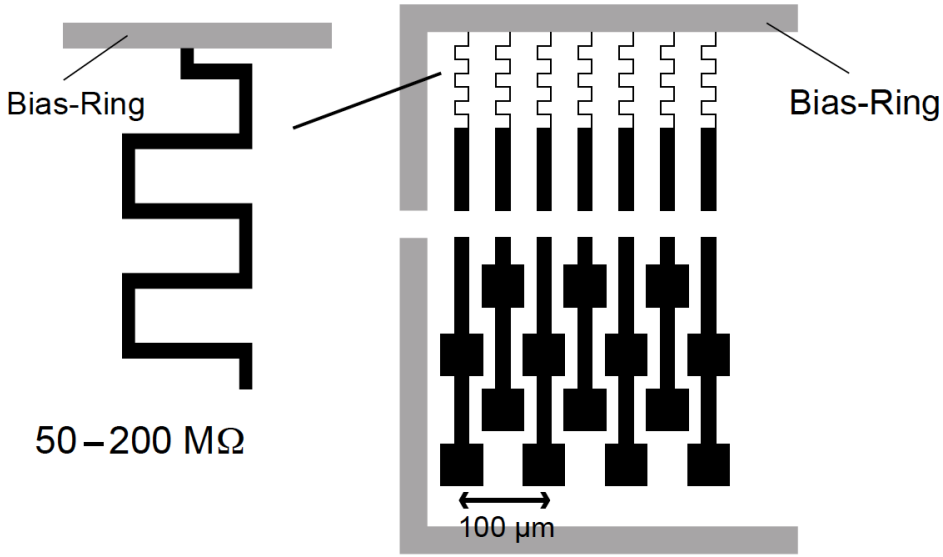
- where is the problem?
  - the problem comes with the many channels



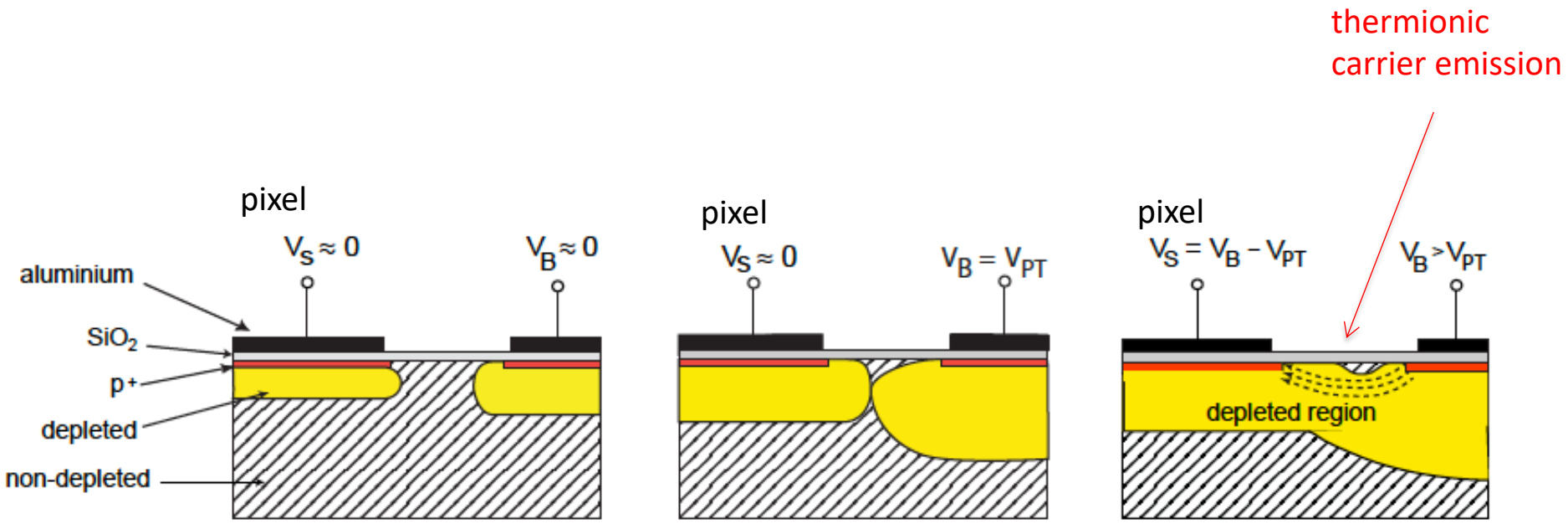
- resistive poly silicon biasing
  - polycrystalline Si on SiO_2 has area resistance of ~100 kΩ/□
  - meander structures can reach 50 – 200 kΩ (for space reasons)

☹ variations

☹ extra processing step



Punch through biasing



(a) Detector without applied bias.

(b) Reverse bias voltage as large as *punch-through* voltage.

(c) Reverse bias voltage larger than *punch-through* voltage.

V

below

$V_{punch\ through}$

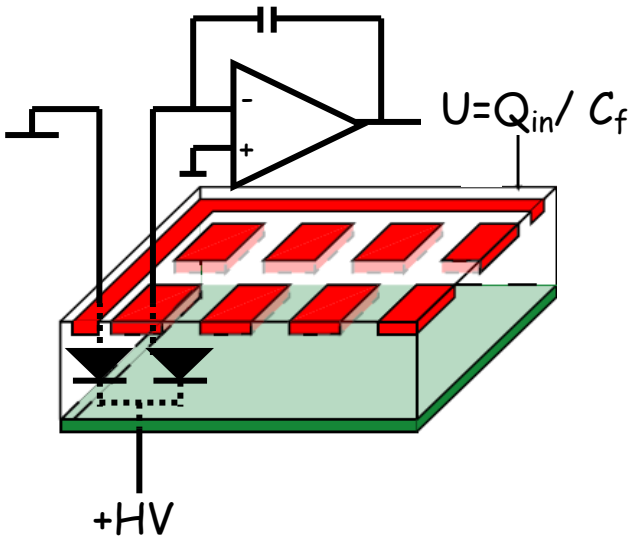
equal

$V_{punch\ through}$

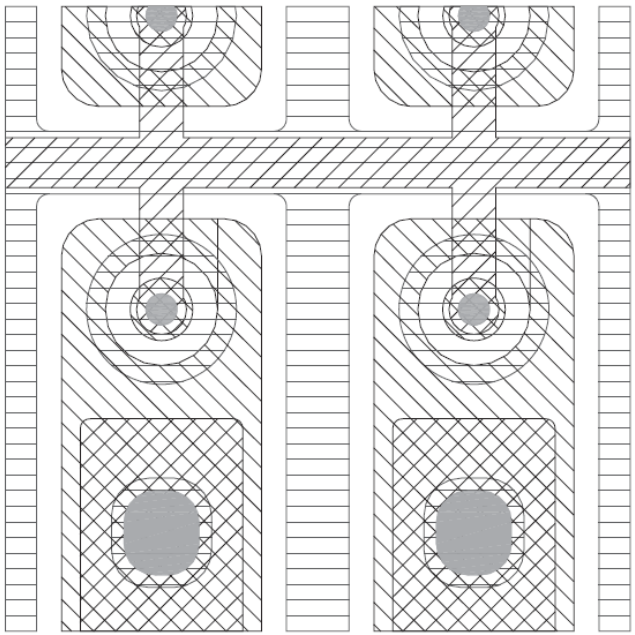
above

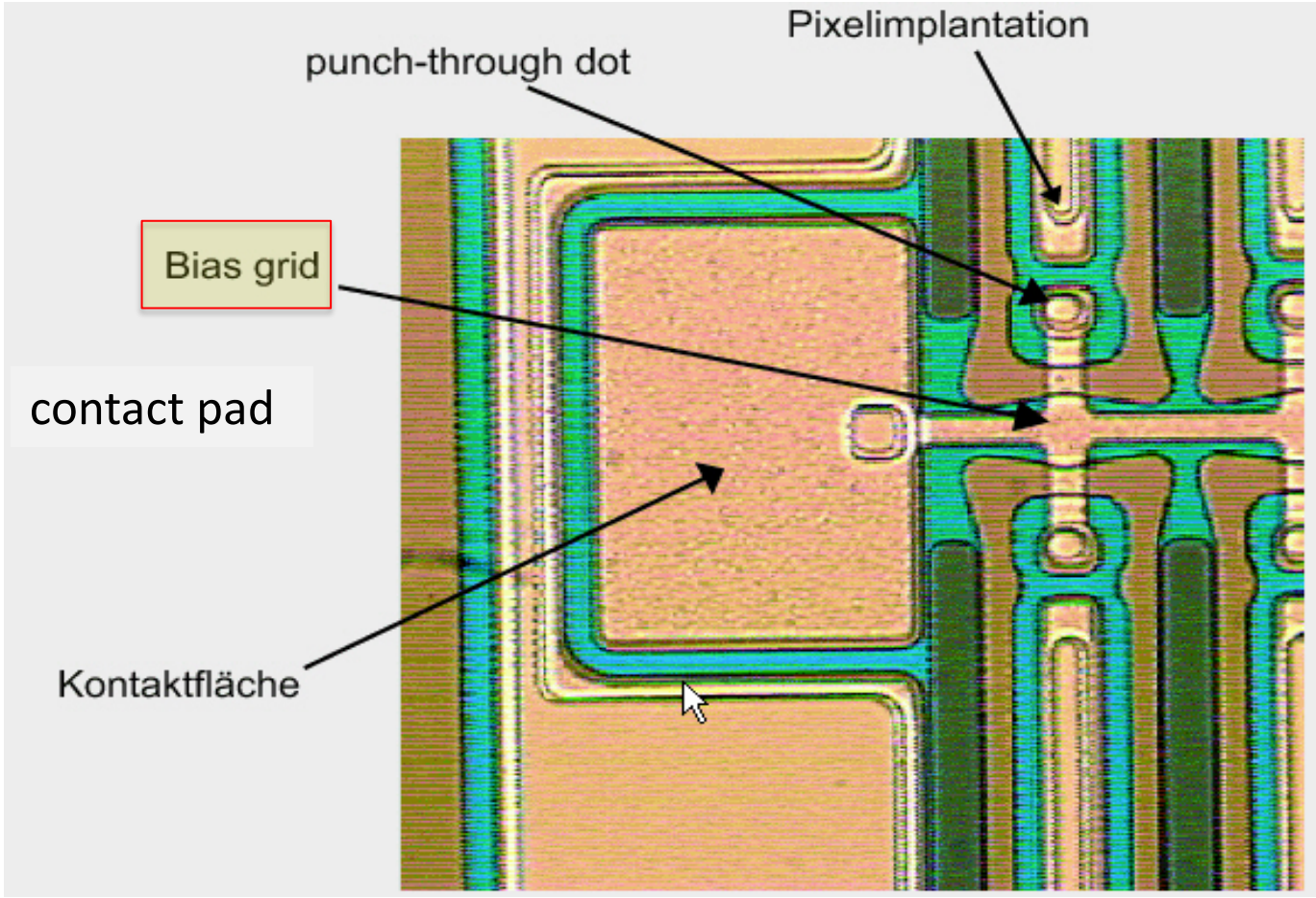
$V_{punch\ through}$

How to bias a pixel detector … with many many channels?



- answer: through the virtual ground of the preamplifier
- but one wants to test the sensor w/o chip, i.e. before you put (many) chips on (yield!)





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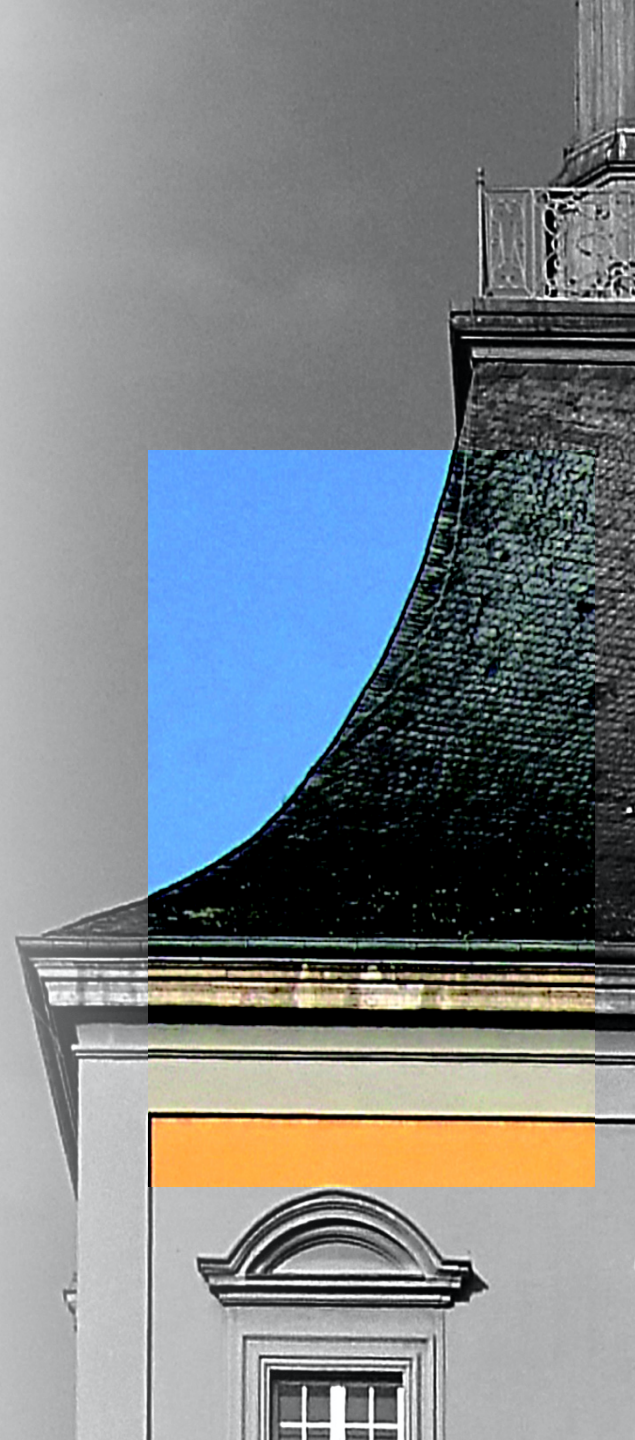
HOW DOES THE SIGNAL DEVELOP?



Weighting field in a pixel detector (1-dim)

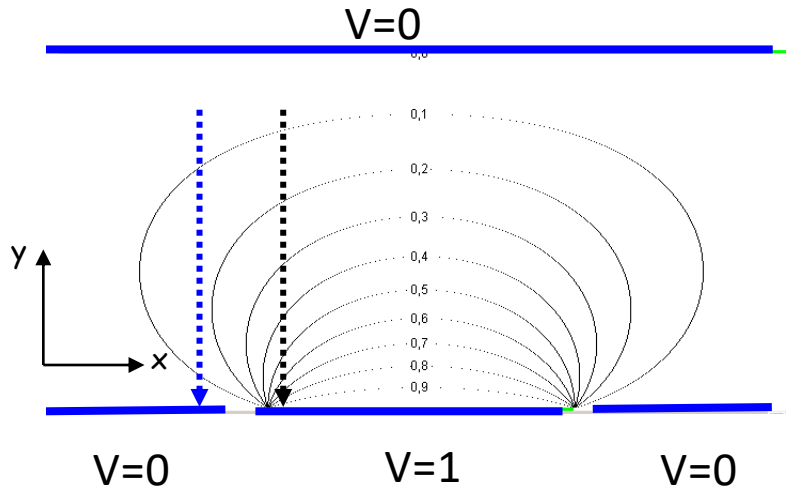
Shockley-Ramo theorem

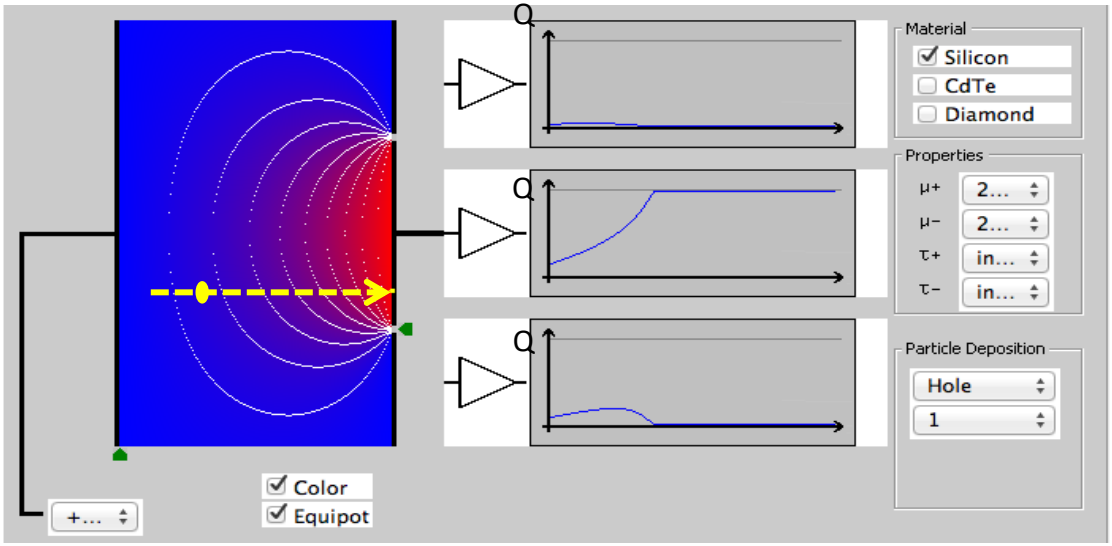
$$dQ_i = -q\vec{\nabla}\Phi_{w,i}d\vec{r}$$

$$i_{S,i} = q\,\vec{E}_{w,i}\,\vec{v}$$

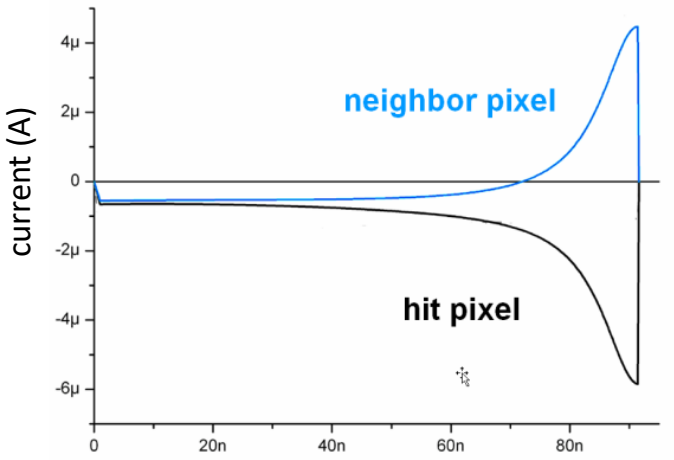
Φ_W for a strip/pixel geometry

$$\phi_w(x,y) = \frac{1}{\pi}\arctan\frac{\sin(\pi y)\cdot\sinh(\pi\frac{a}{2})}{\cosh(\pi x)-\cos(\pi y)\cosh(\pi\frac{a}{2})}$$

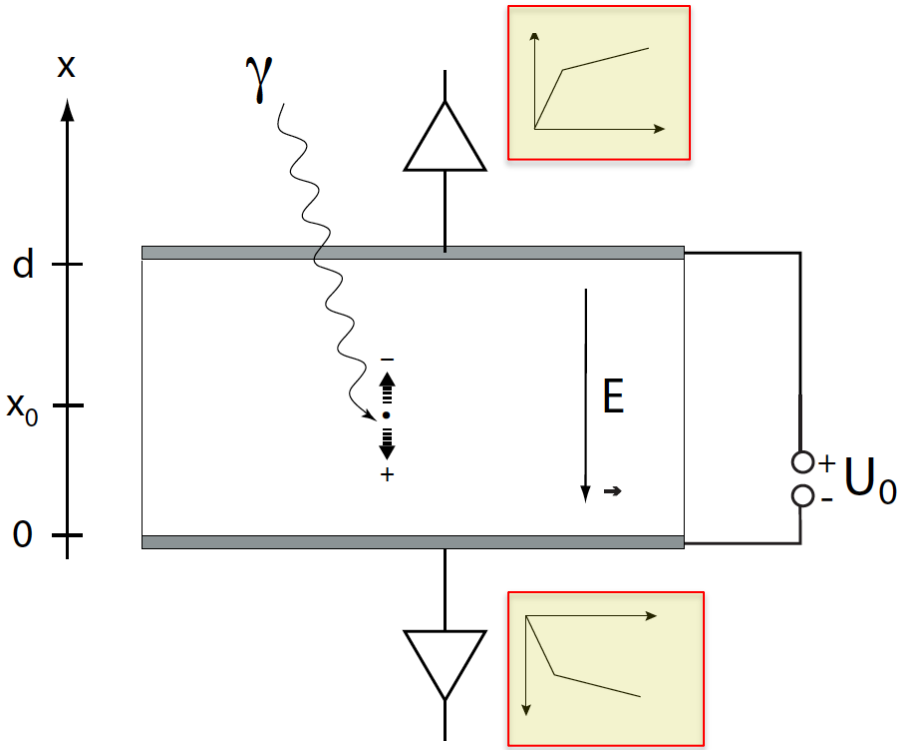




"small pixel effect" !



Note!

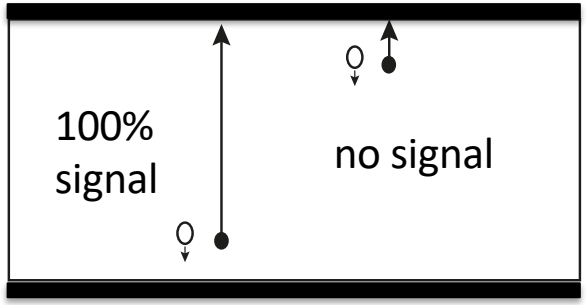


- movement of both charges create signals on both electrodes.
- on every electrode a total charge of

$$Q_S^{tot} = Q_S^- + Q_S^+ = -Ne$$

is induced.

- if a material the produced charges have very different mobilities (like CdTe) e.g. with $\mu_h \approx 0$, then part of the signal is lost and the signal becomes dependent on where the charge was deposited.



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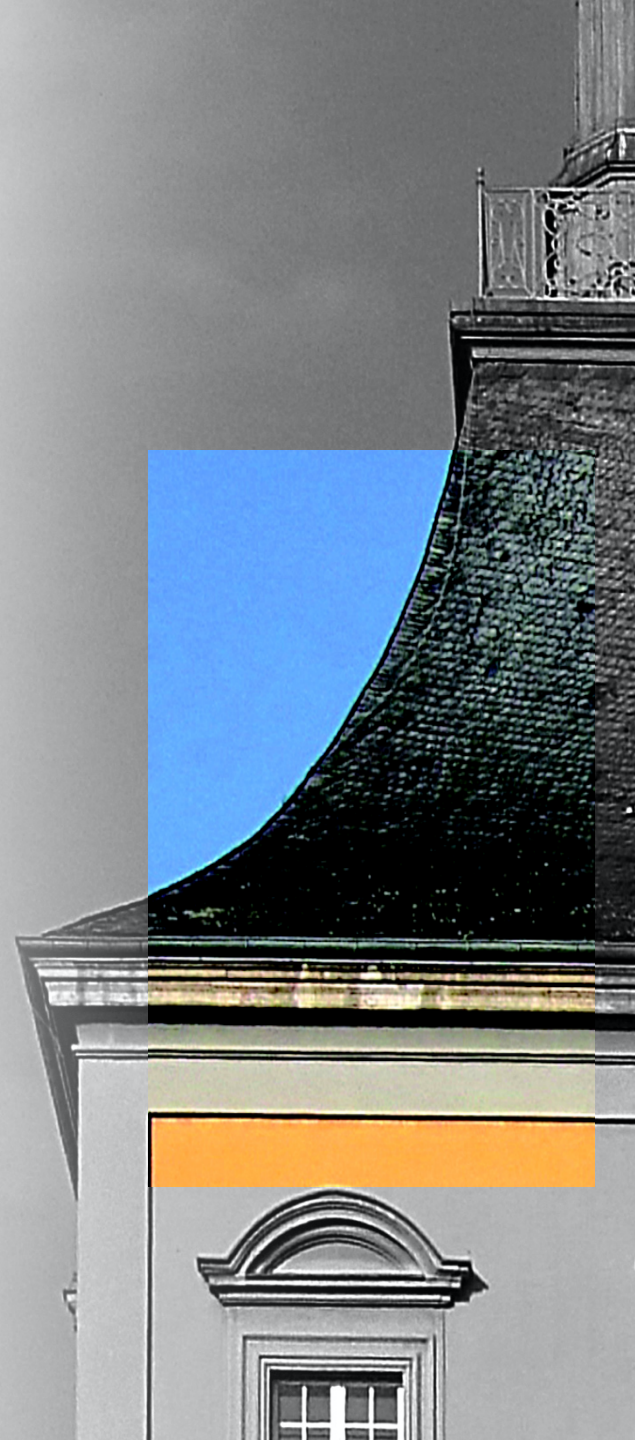
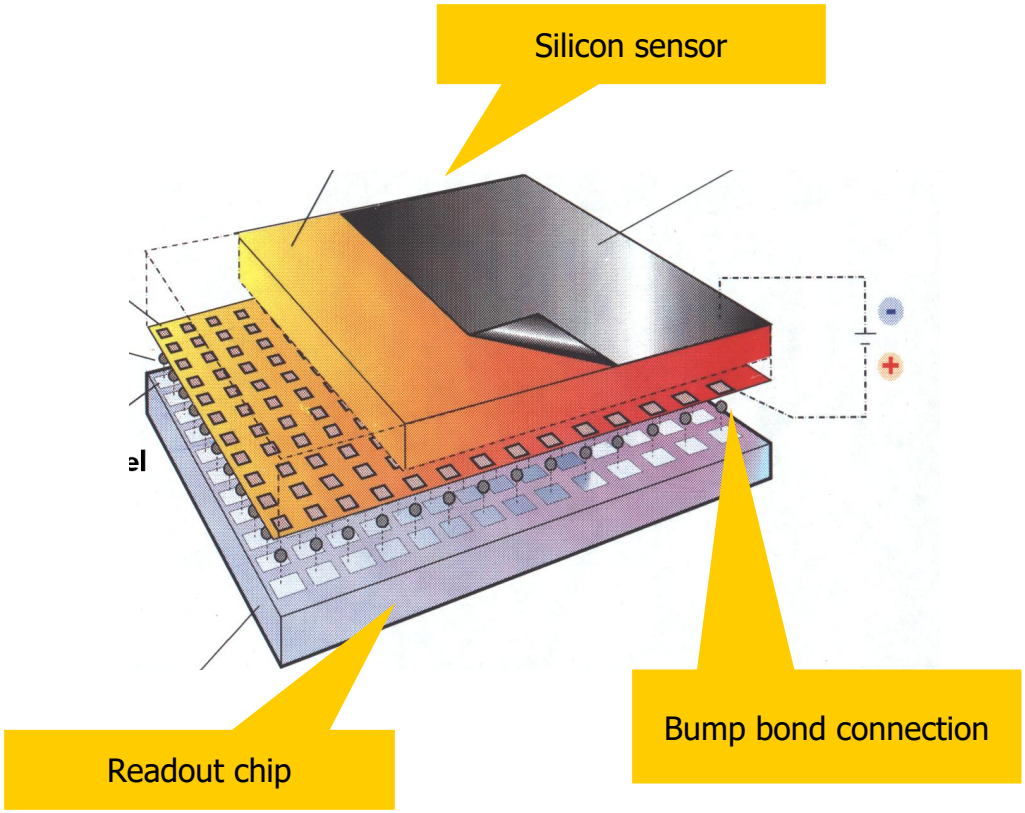
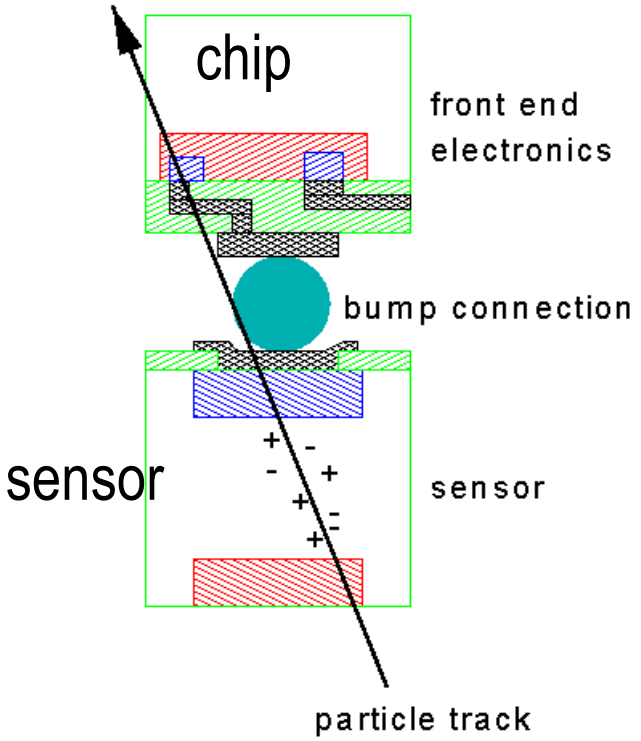
HOW TO MAKE A …

“HYBRID” PIXEL DETECTOR



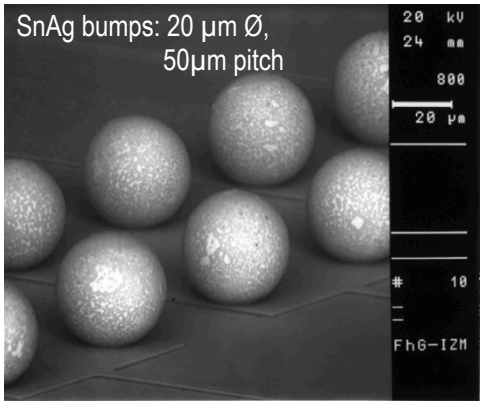
Hybrid Pixel Detectors = current state of the art / standard @ LHC





- amplification by a dedicated R/O chip
- 1-1 cell correspondence

ATLAS: 50 x 250 µm pixel cells
amplifier for every pixel



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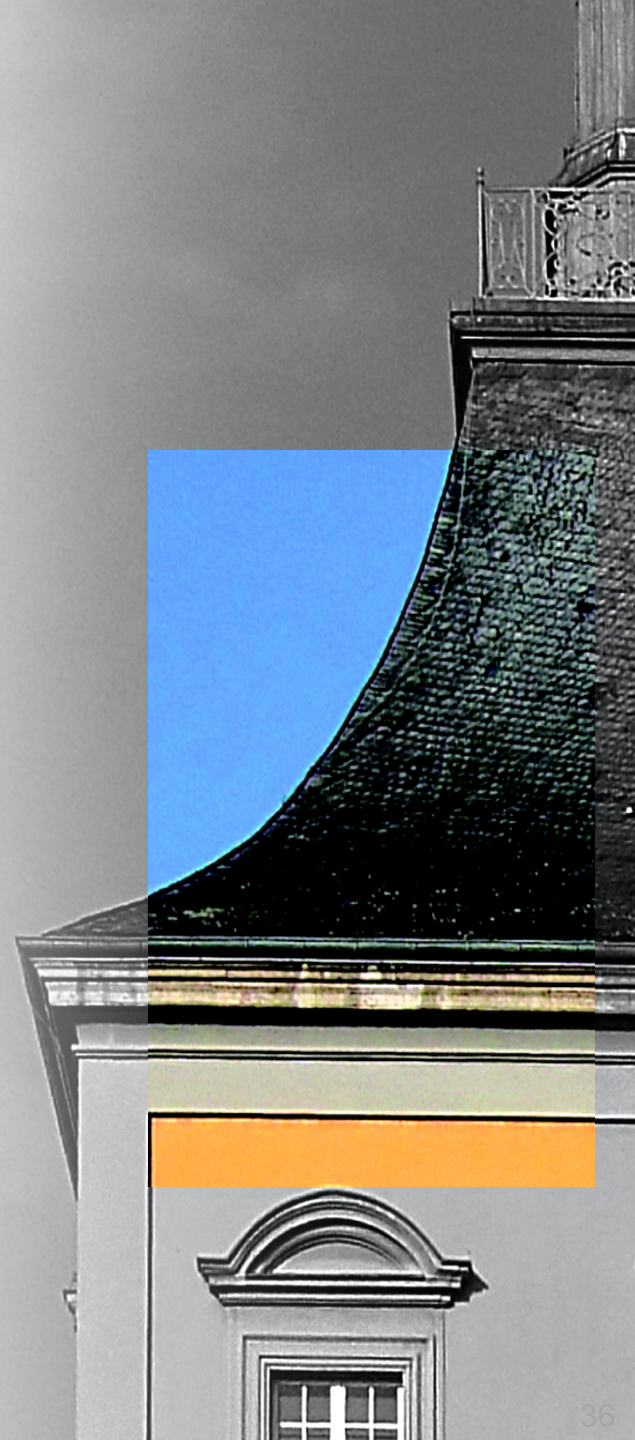
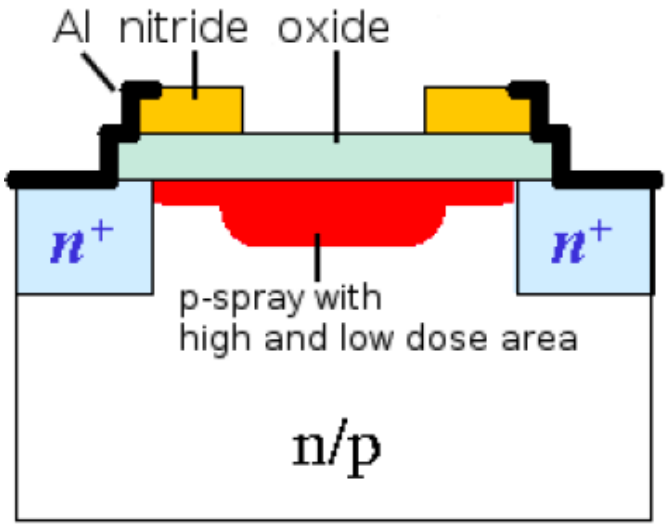
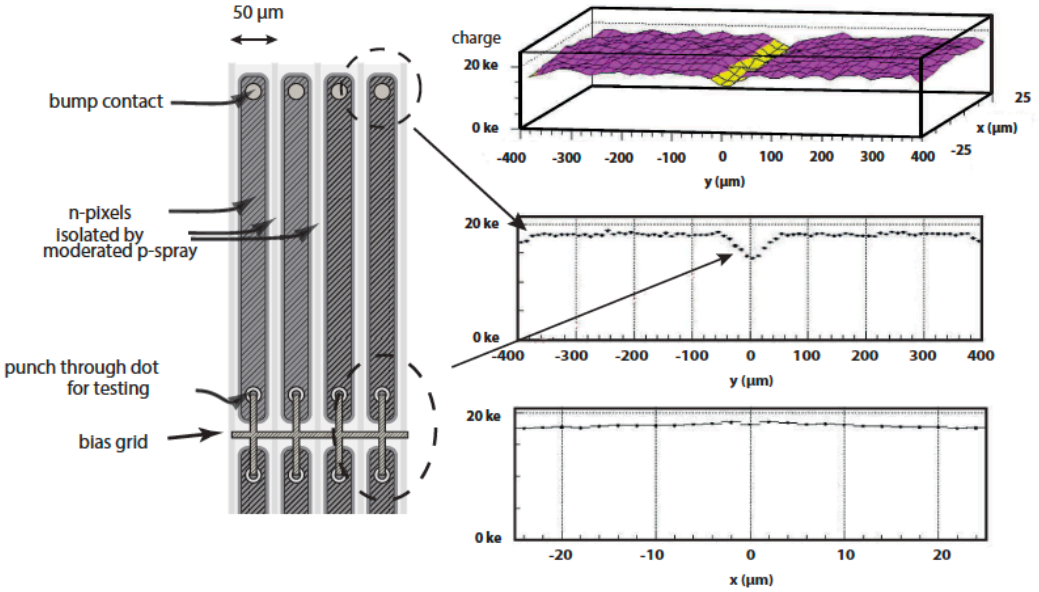
PIXEL “SENSOR”

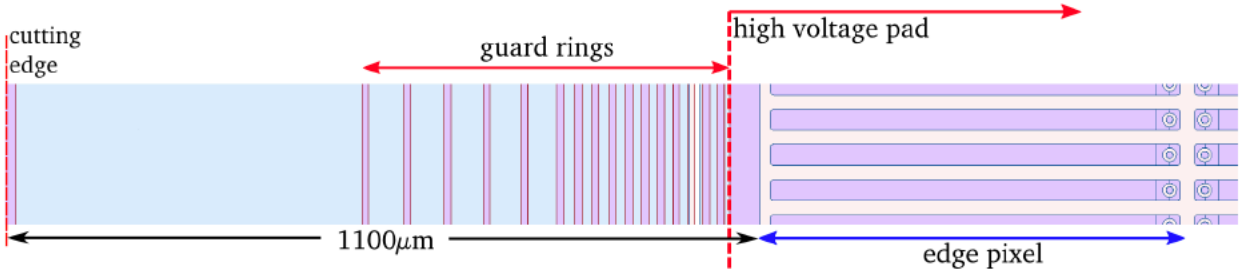


Planar sensors

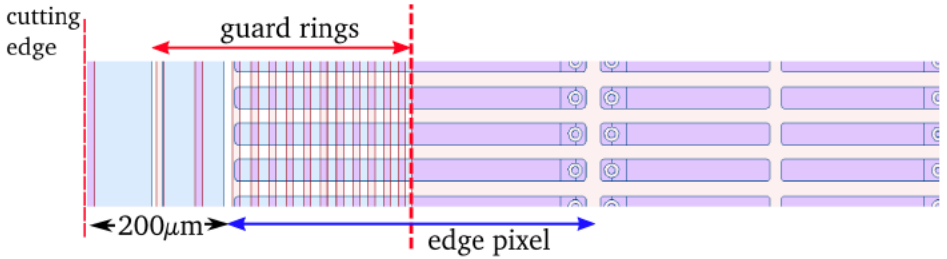




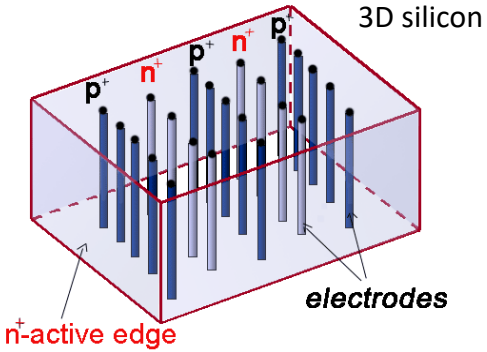
ATLAS Layers 1-3

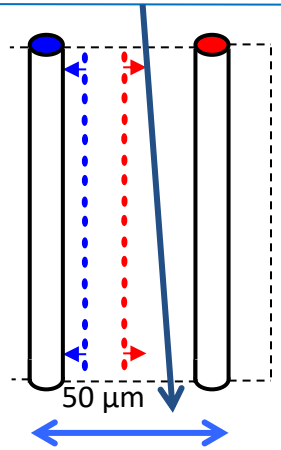


ATLAS IBL

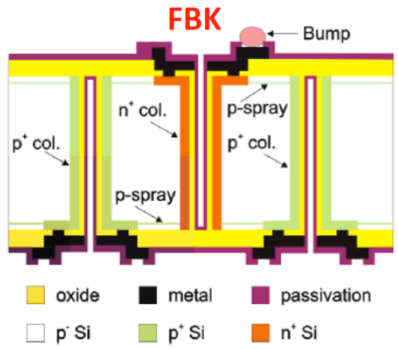


3D-Si sensors for the innermost pixel layer(s)

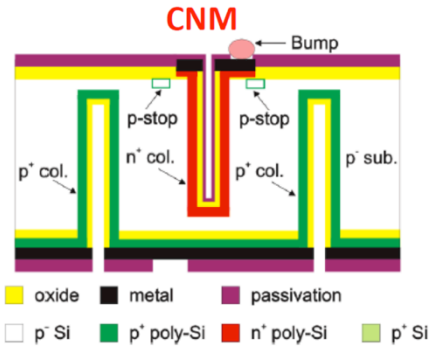




S. Parker, C. Kenney , J. Segal, ICFA Instrum.Bull. 14 (1997) 30-50
C. Da Via, et al., NIM A49 (2005) 122-125 and NIM A 699 (2013) 18



G.F. Della Betta et al.,
PoS Vertex2012 (2013) 014



G. Pellegrini et al..
NIM A731 (2013) 198-200

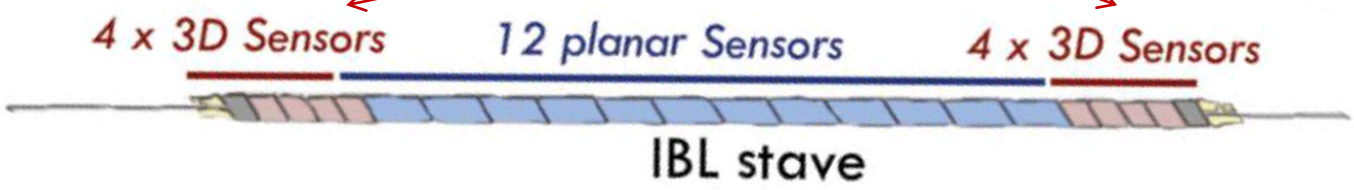
- particle path (signal) different from drift path
- high field w/ low voltage

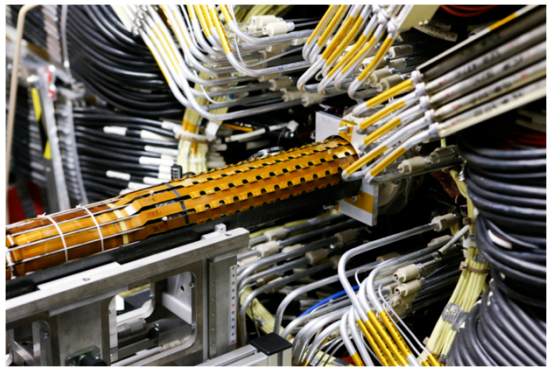
-> radiation tolerance

- good for inclined tracks

- slightly larger C_{in} (noise)

- now also in diamond, CdTe





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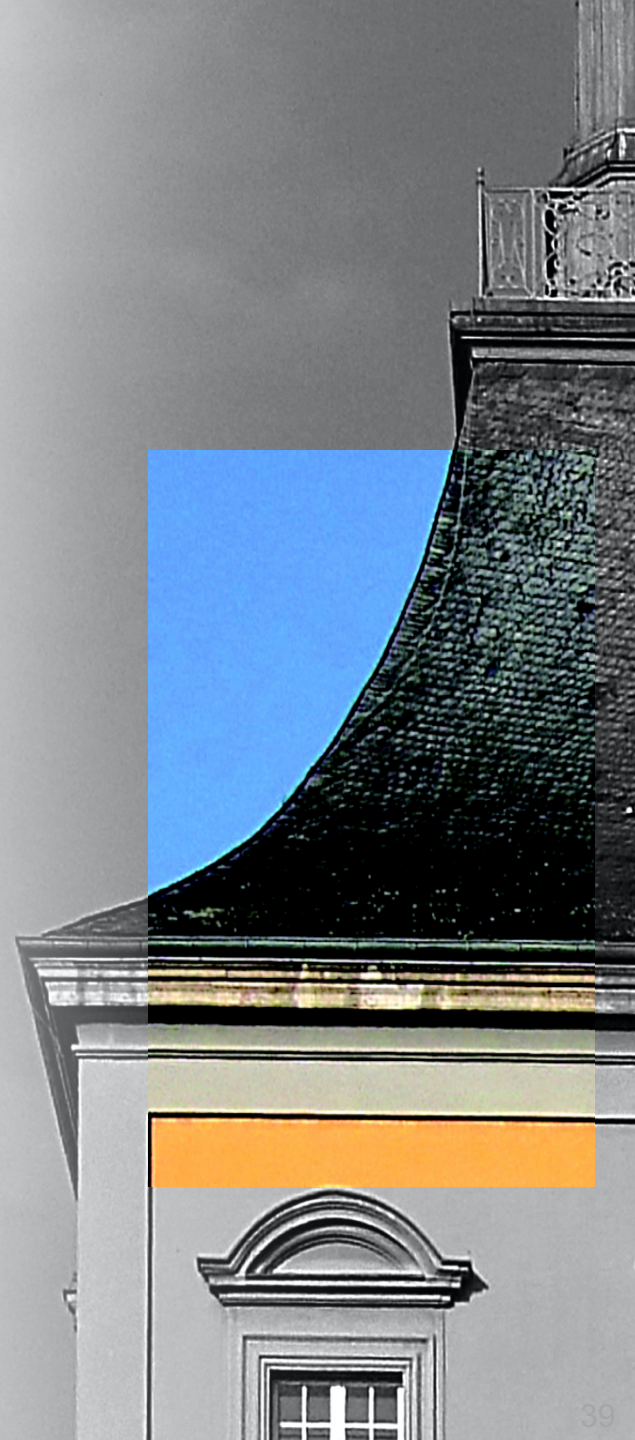
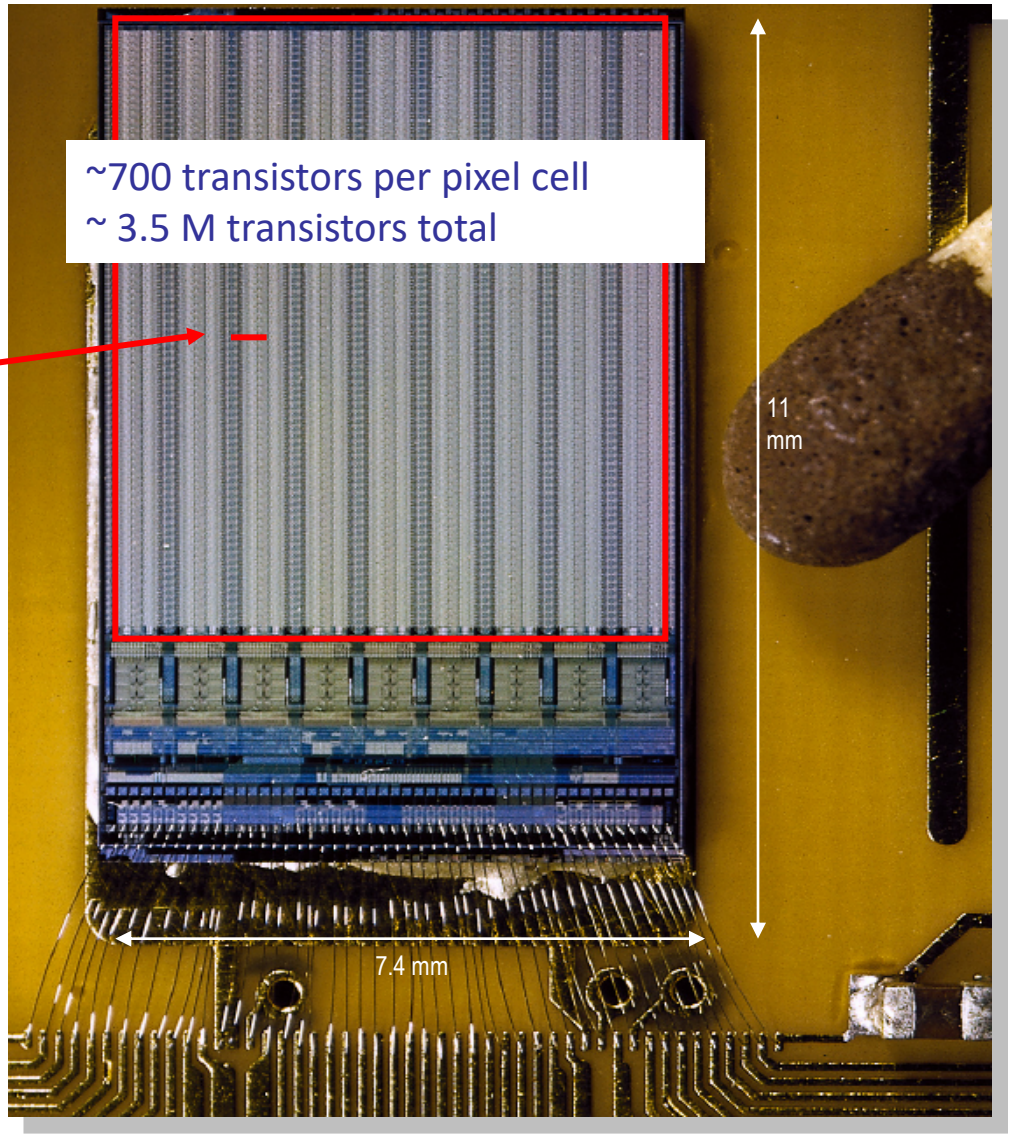
PIXEL READOUT CHIP

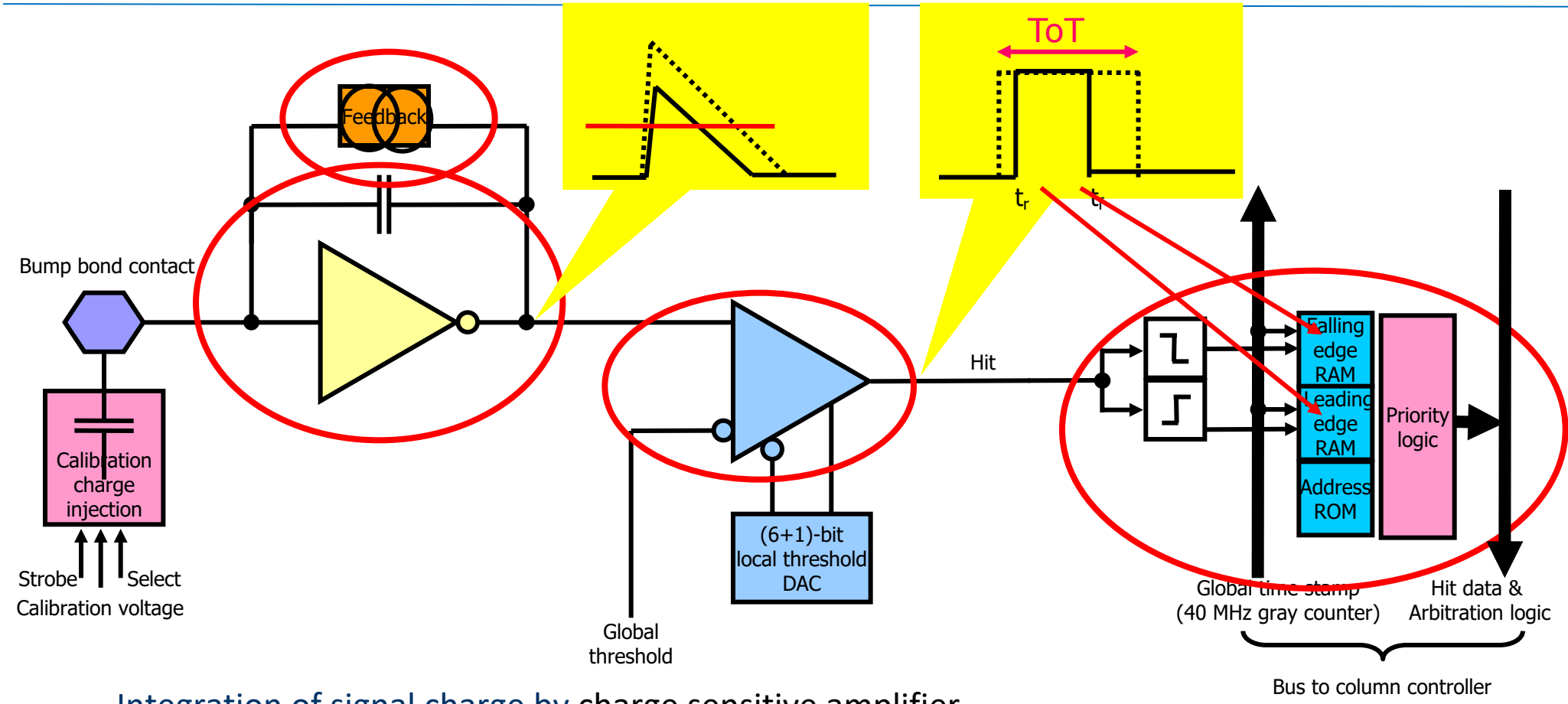


Pixel Frontend Chip

- ATLAS FE chips (FE-I3 and FE-I4)
  - 250 nm (IBL 130 nm) CMOS technology
  - pixel cell size: 50 x 400 µm^2
  - 18 columns x 160 rows = 2880 cells
  - parallel processing in all cells
    - - amplification
    - - zero suppression



Functions in the cell (binary readout + „poor man‘s“ analog)



- Integration of signal charge by charge sensitive amplifier
- Pulse shaping by feedback circuit with constant current feed back
- Hit detection by comparator
- ~5 bit analog information via „time over threshold“
- storage of address and time stamps in RAM at the periphery

L. Blanquart et al., NIM-A565:178-187, 2006

Pixel Frontend Chip

- ATLAS FE-I3
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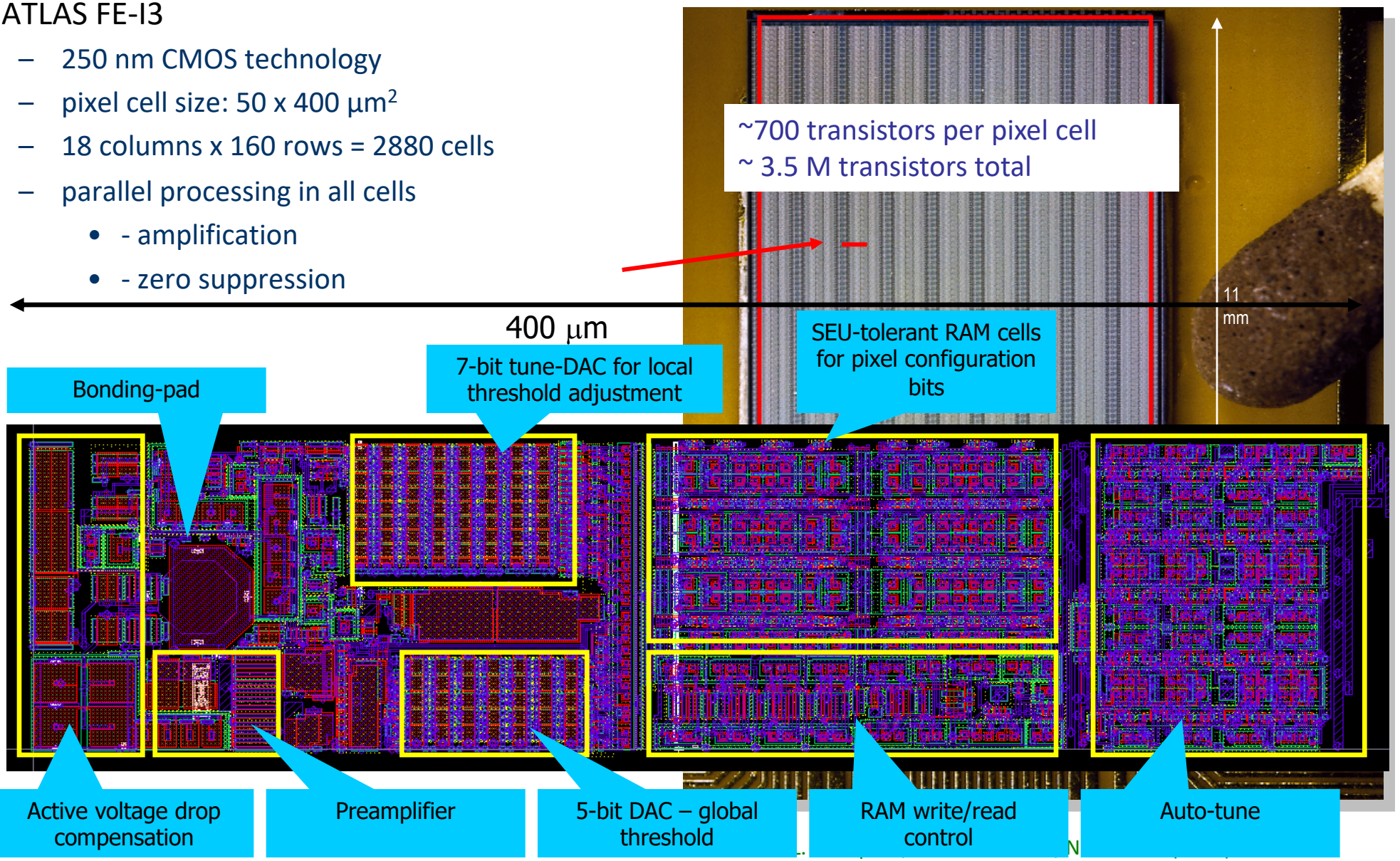
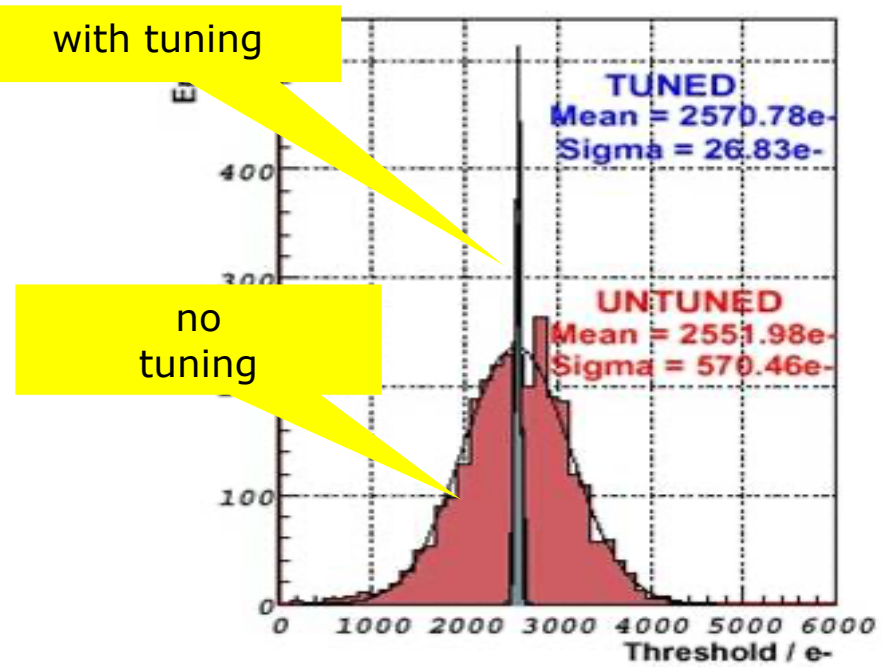
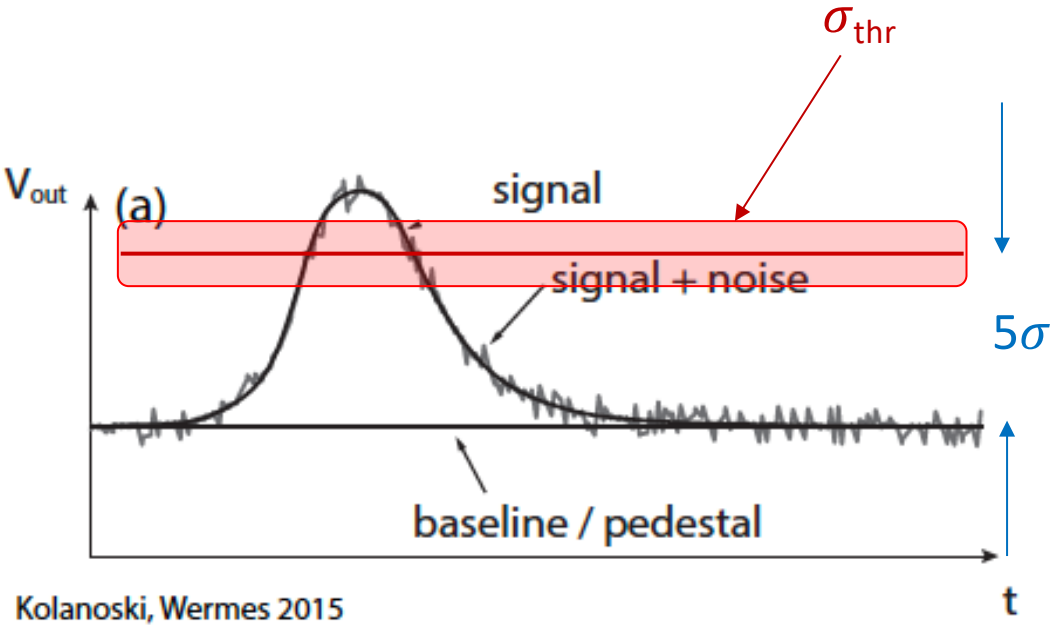


Requirements on the electronics performance

- small noise hit rate → low noise and small threshold dispersion
- $\sigma_{noise} \oplus \sigma_{threshold}$ < 500 e^- @ a threshold of 2500 e^-
- time stamping < 20 ns after BX for all signal heights



Distribution of pixel cell thresholds

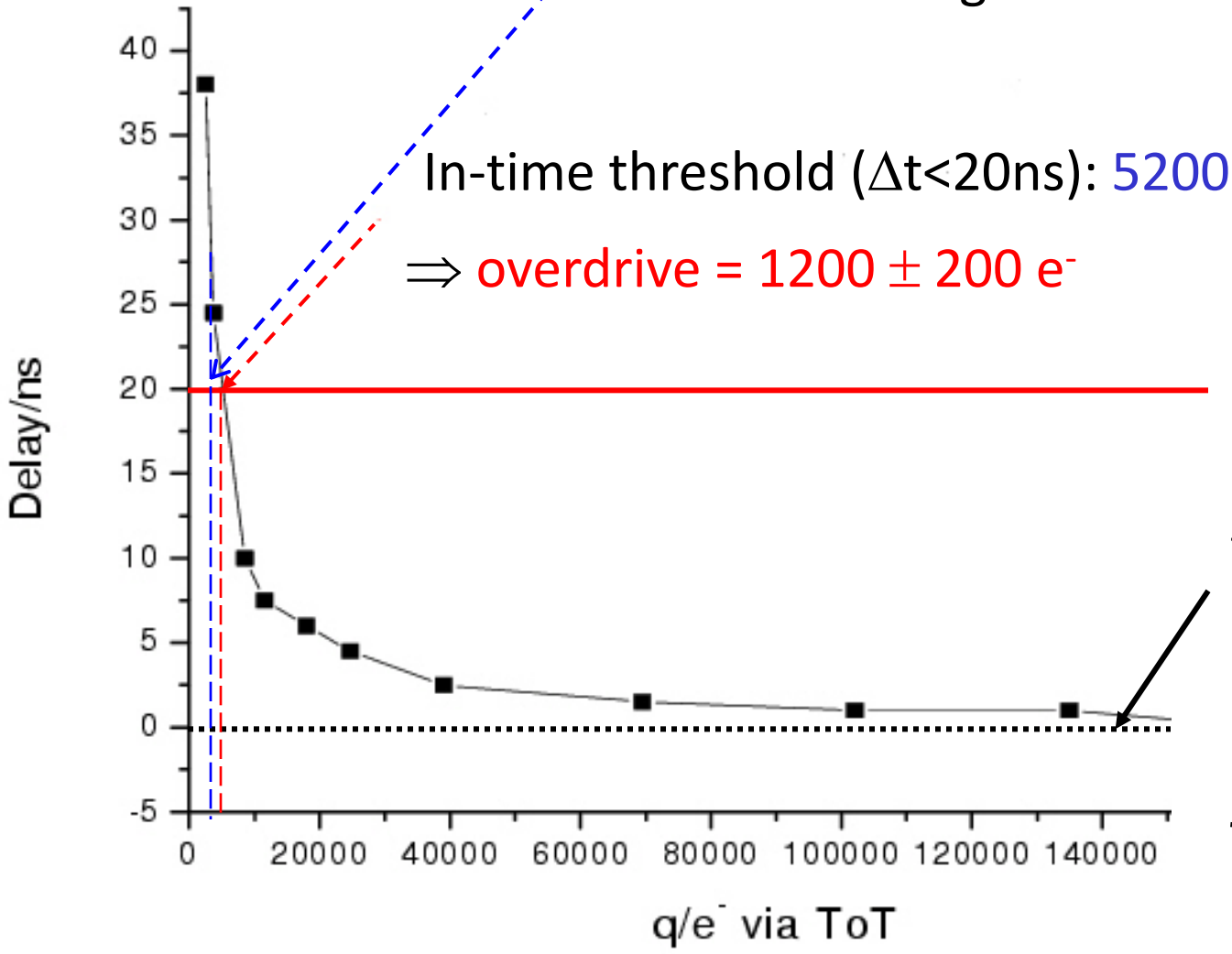


Important / in-time threshold & efficiency

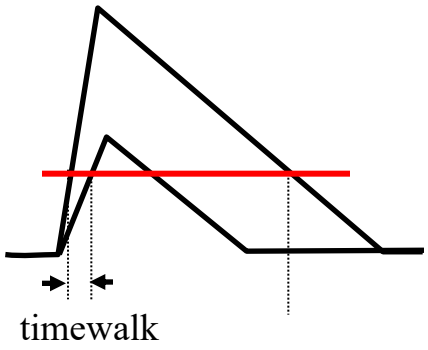
set threshold e.g. to 4000 ± 200 e⁻

In-time threshold (Δt<20ns): 5200 ± 200 e⁻

⇒ overdrive = 1200 ± 200 e⁻



zero time walk line for large signals

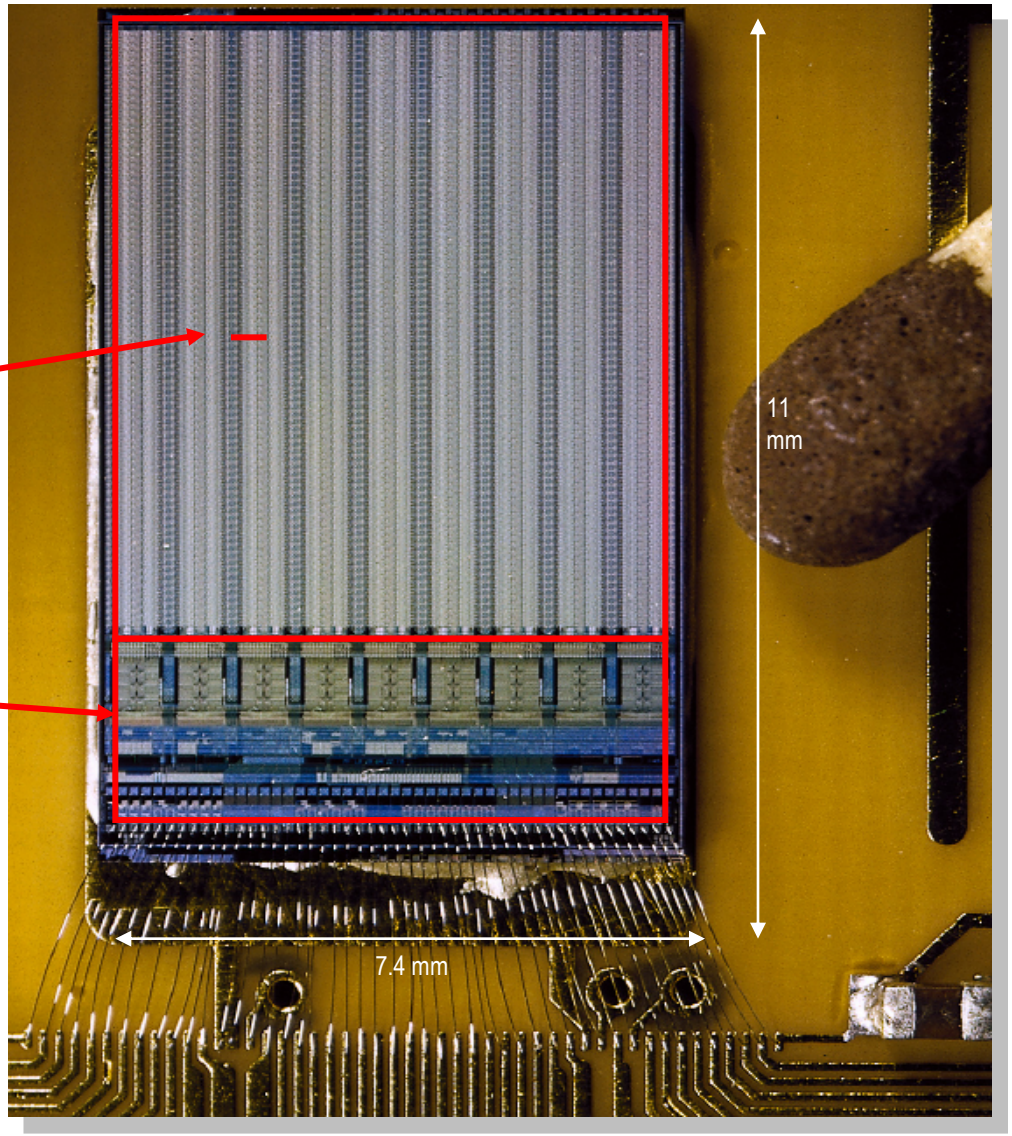


➔ in-time efficiency ~99% wanted and achieved !

Pixel Frontend Chip

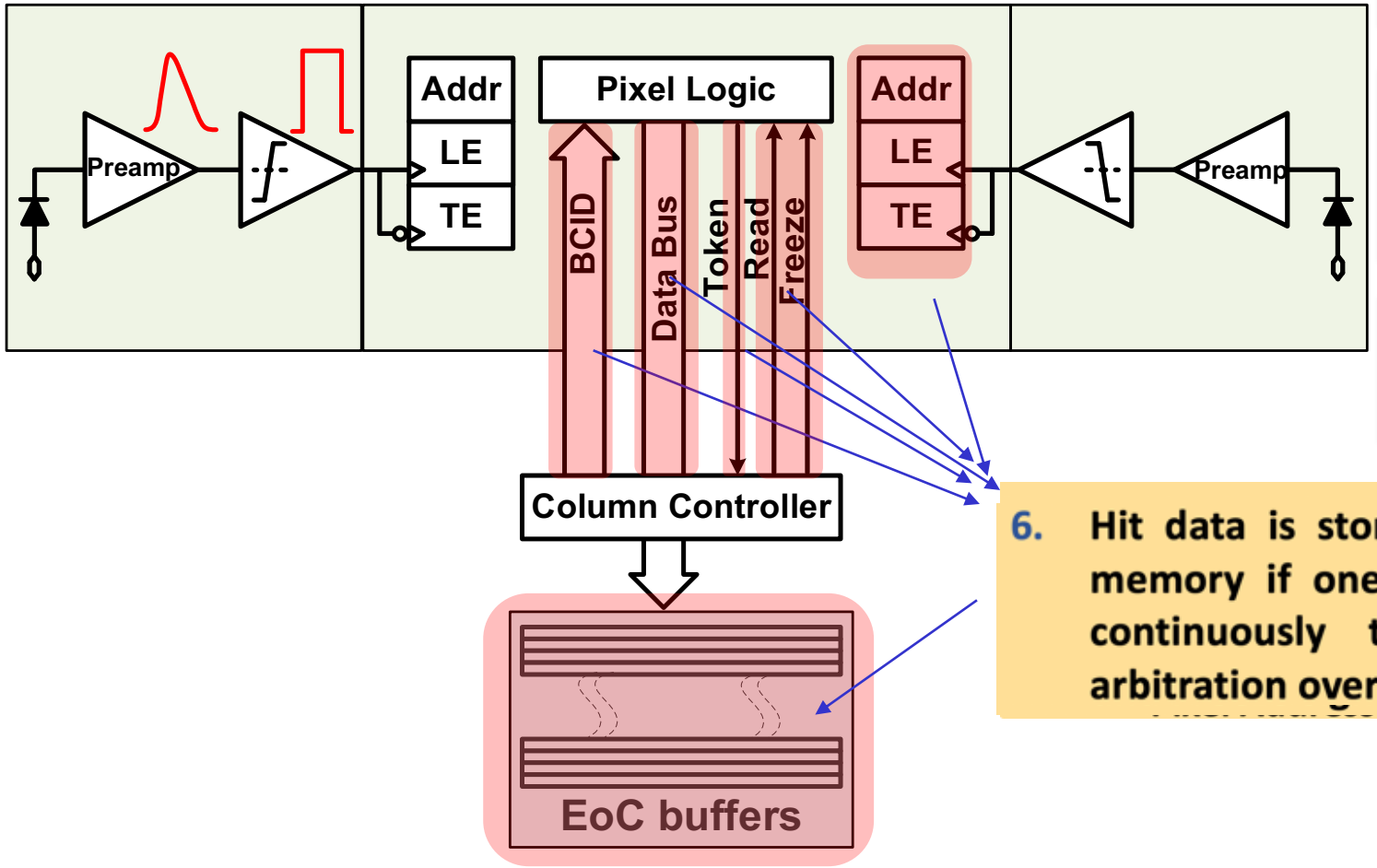
- ATLAS FE-Chip
  - 250 nm CMOS technology
  - pixel cell size: 50 x 400 µm^2
  - 18 columns x 160 rows = 2880 cells
  - parallel processing in all cells
    - amplification
    - zero suppression

- end of column logic
  - storage of hit information during trigger latency (2.5 µs)
  - hit selection upon L1 trigger



A readout architecture (“column drain”)

Synchronous readout => time stamping in matrix



- BC ID (40 MHz) distributed in the column
- Hit timing stamped in pixel
  - LE: leading edge
  - TE: trailing edge

  => Time of arrival: LE

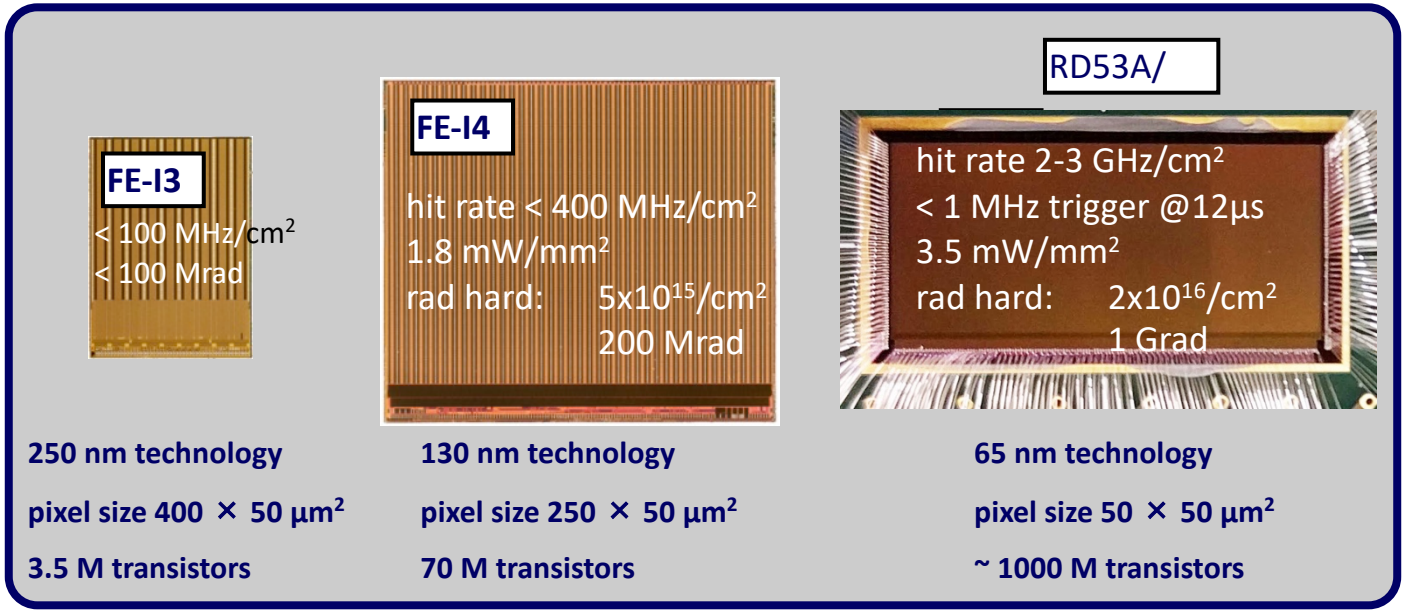
  => Ana. info. from ToT
- Hits read out sequentially, following a token passing scheme on a shared column bus

6. Hit data is stored in the trigger memory if one exists or else is continuously transmitted after arbitration over different columns

- Hits are removed if no trigger conicidence occurs.
- Hit information agreeing with L1 trigger time are read out.

Pixel R/O-Chip for HL-LHC rates (and radiation)

- Effort and costs so large that joint approach (cross experiments) is needed -> **RD53** (20 Institutes)
- Higher hit rate (not smaller pixel size) requires higher logic density **-> 65nm TSMC**



Pixel R/O philosophy changes -> better architectures

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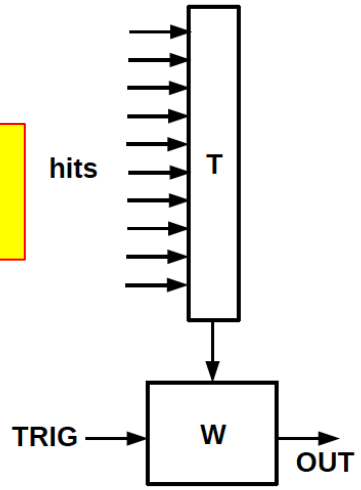
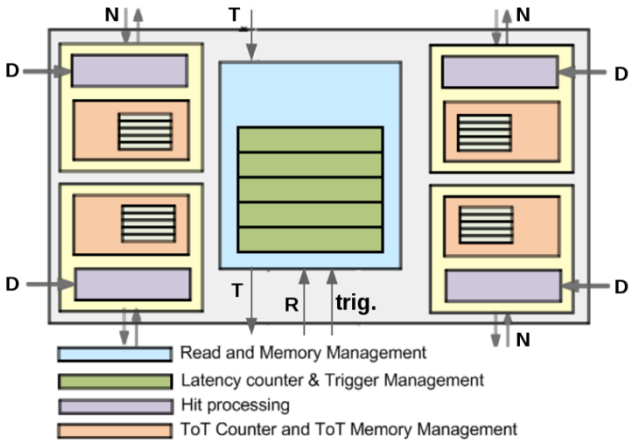
1st generation

- column drain R/O
- FE-I3 like



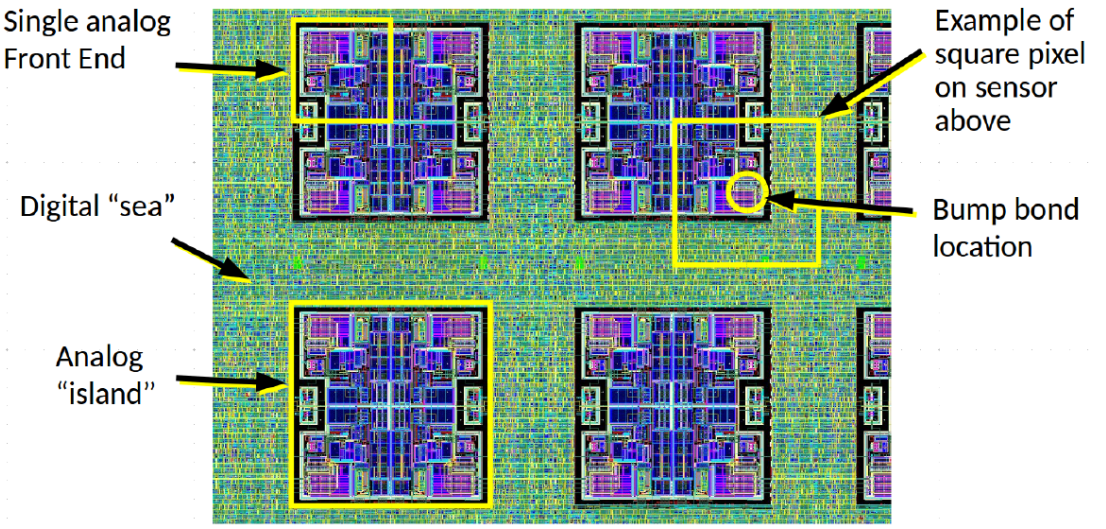
2nd generation

- 4-pixel region logic
- efficient for clusters
- FE-I4 like



3rd generation

- region architectures with grouped logic -> regional hit draining
- surrounded by synthesized logic (“digital sea”)
- RD53 like



“analog islands in digital sea”

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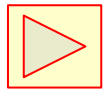
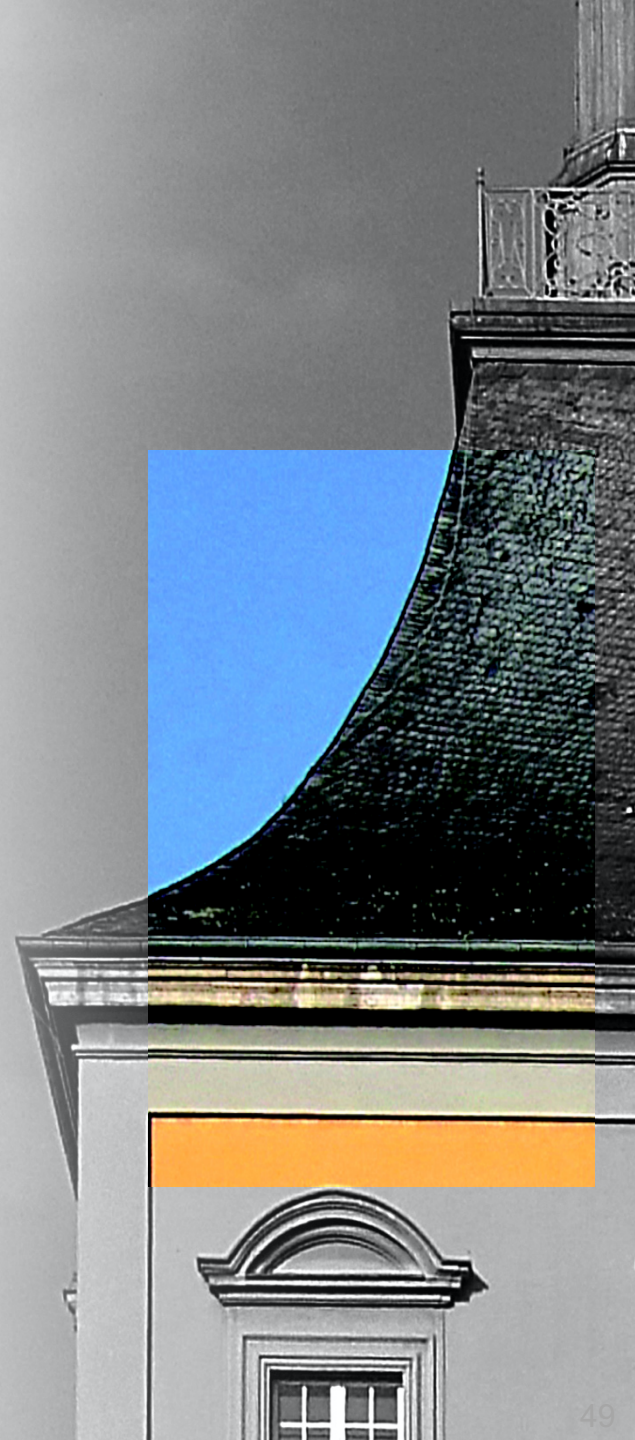
HYBRIDISATION

25





Hybrid Pixel Assembly

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Sensors

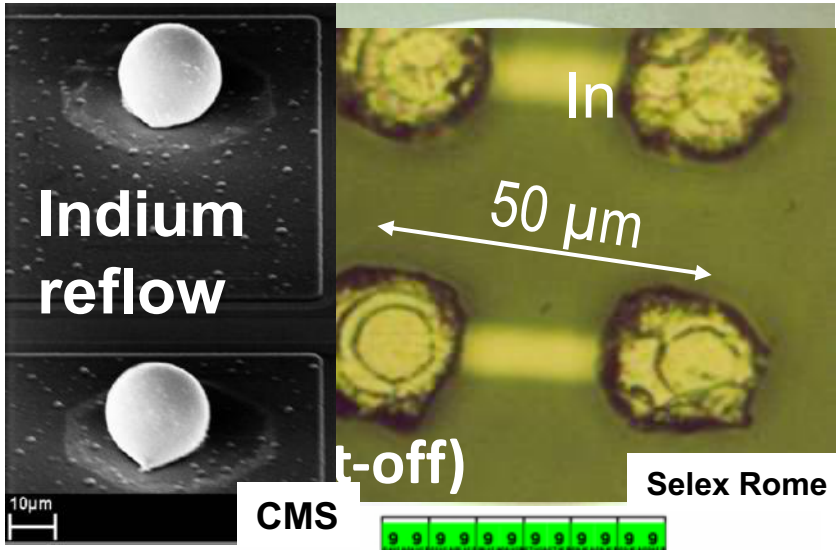
- n^+ in n (oxygenated Si)
- 200 µm thick

Readout – Chip (FE-I3 -> FE-I4)

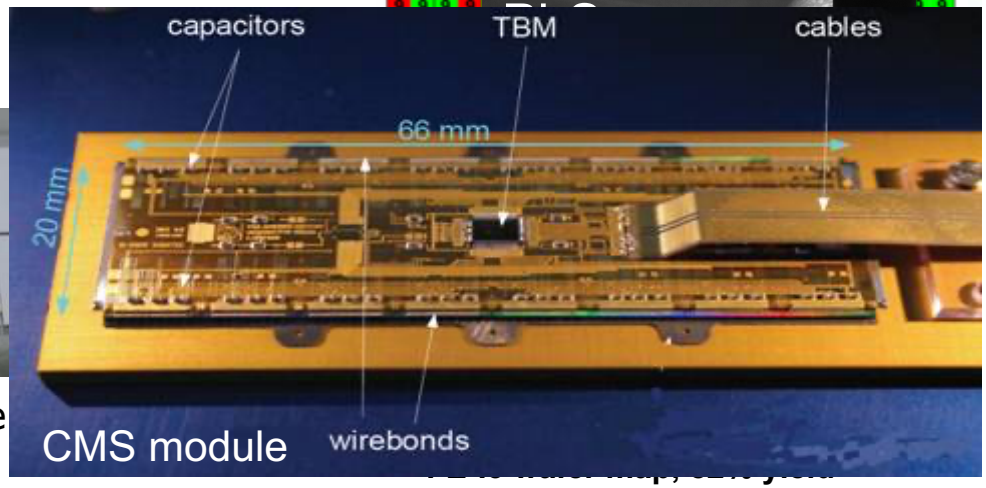
- chip size limited by yield ~1-2.5 cm^2
- wafer size (Ø 20 cm)

Hybridization

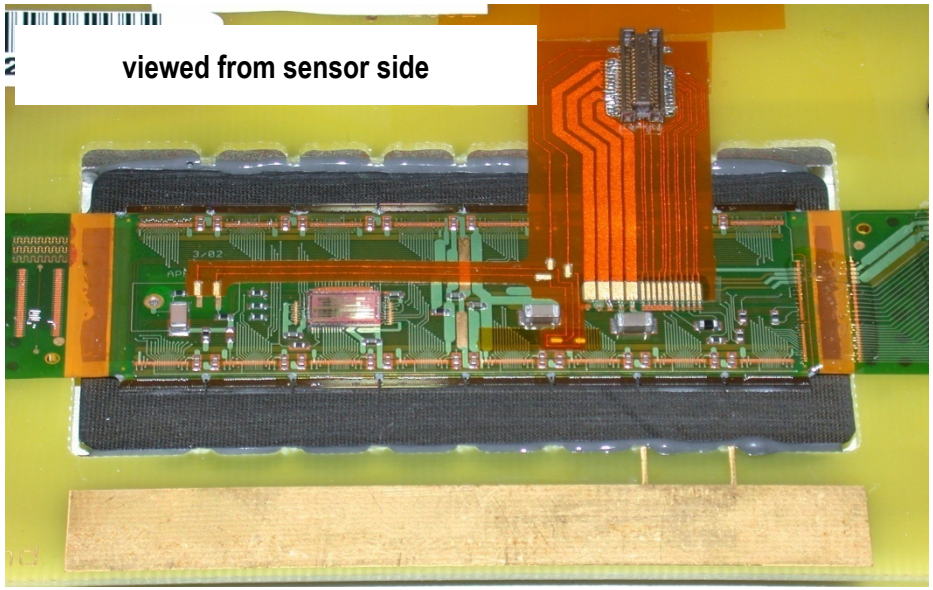
- PbSn, SnAg or Indium bumps (applied on wafer)
- IC wafers thinned after bumping to ~180 µm
- ‚flip-chipping' to mate the parts
- ~3000 bumps/chip, ~50000 bumps/module

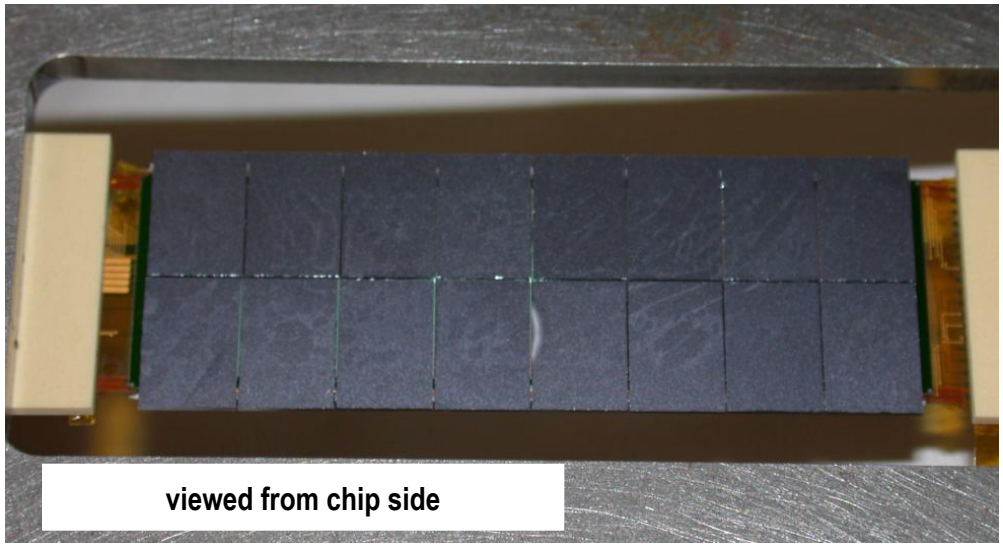


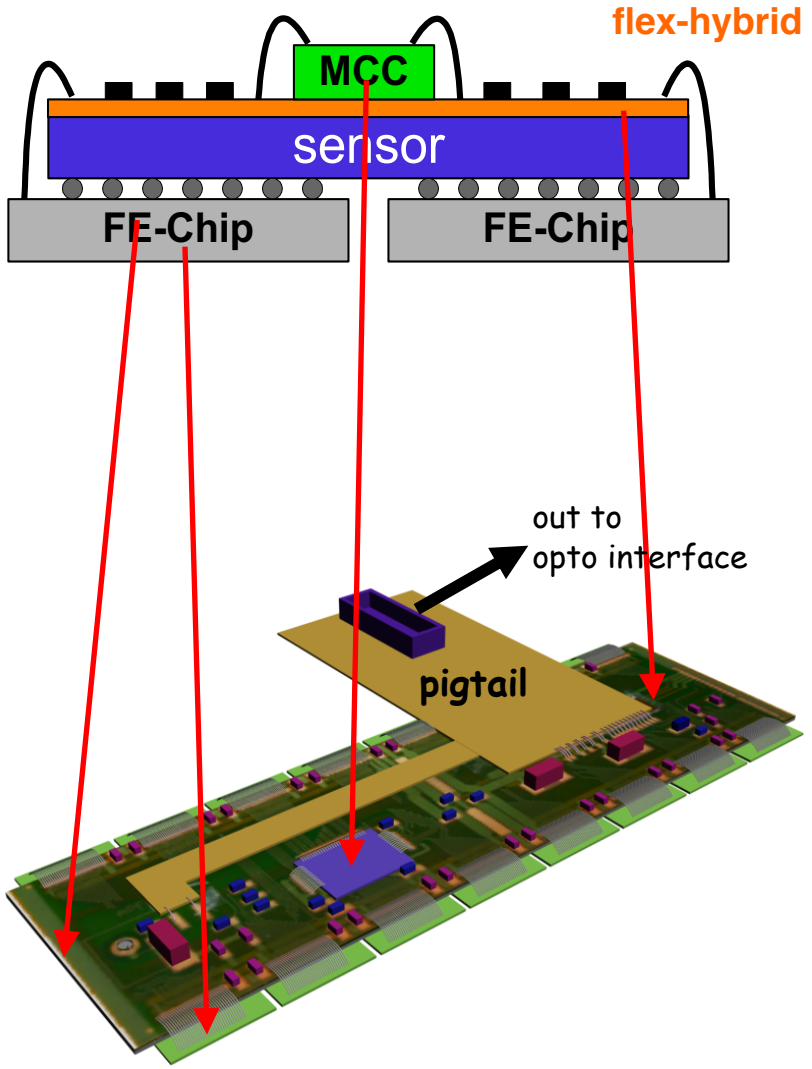
ATLAS Modul, Foto:IZM, Berlin



The Pixel Module

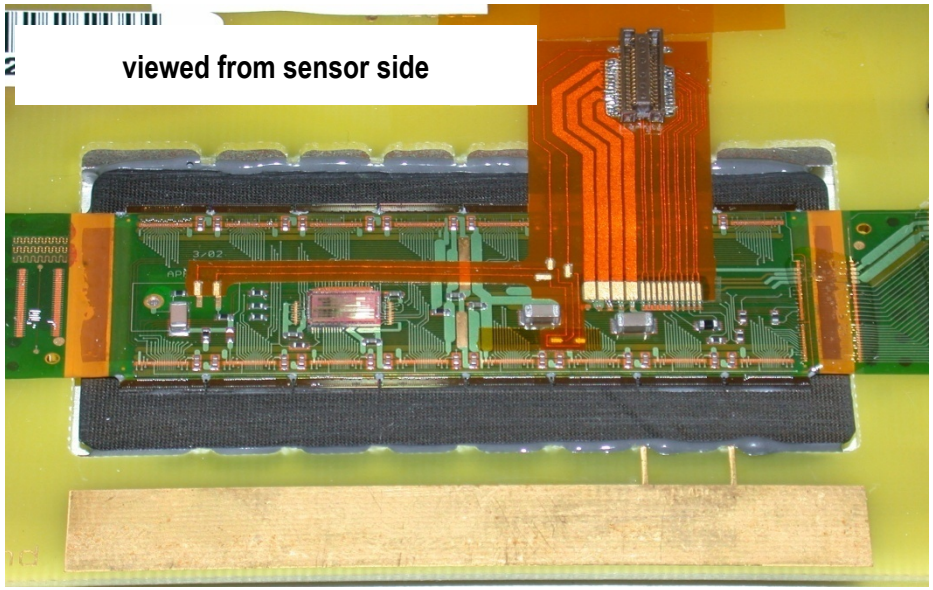


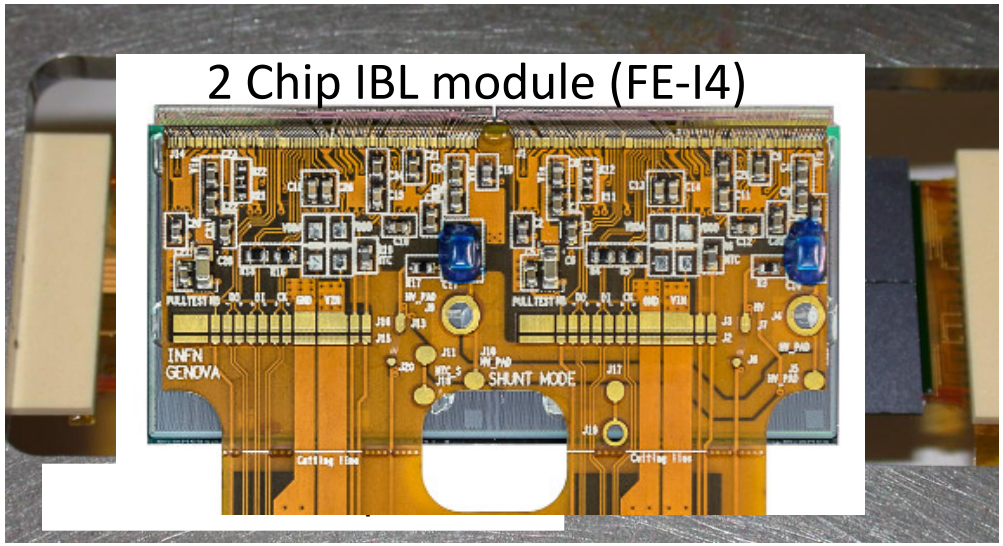


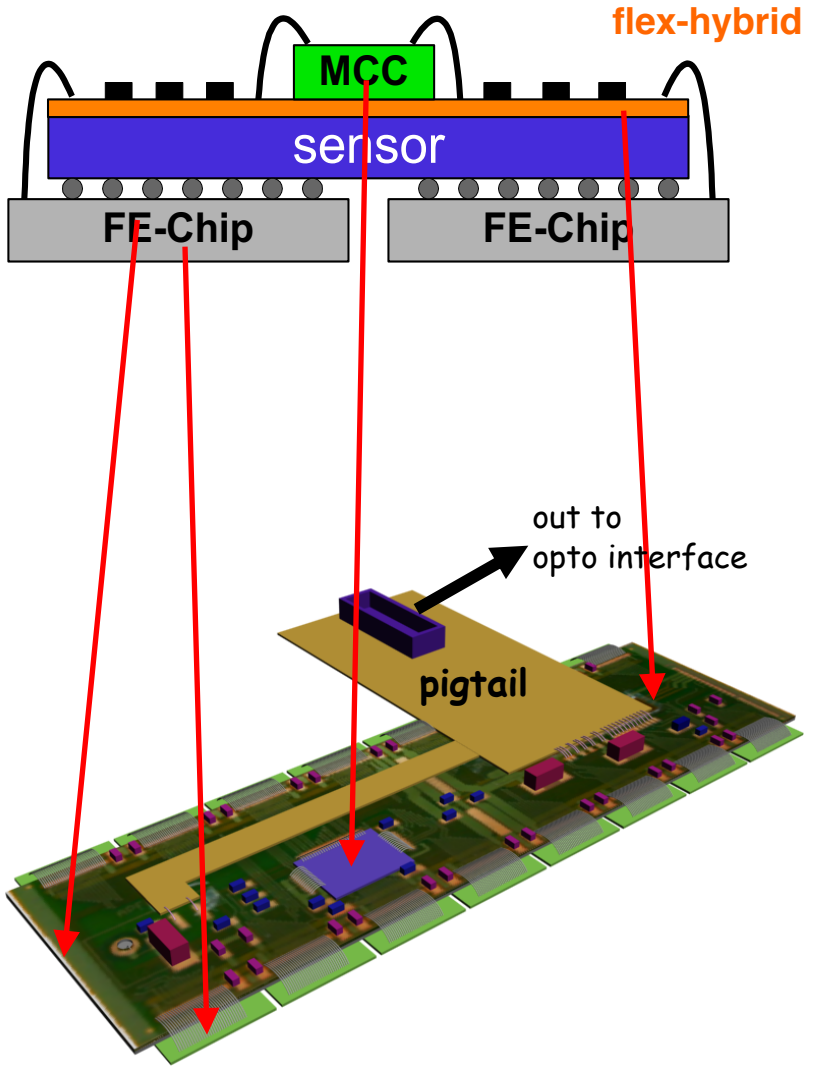


16 ICs, 46080 pixels

The Pixel Module







16 ICs, 46080 pixels

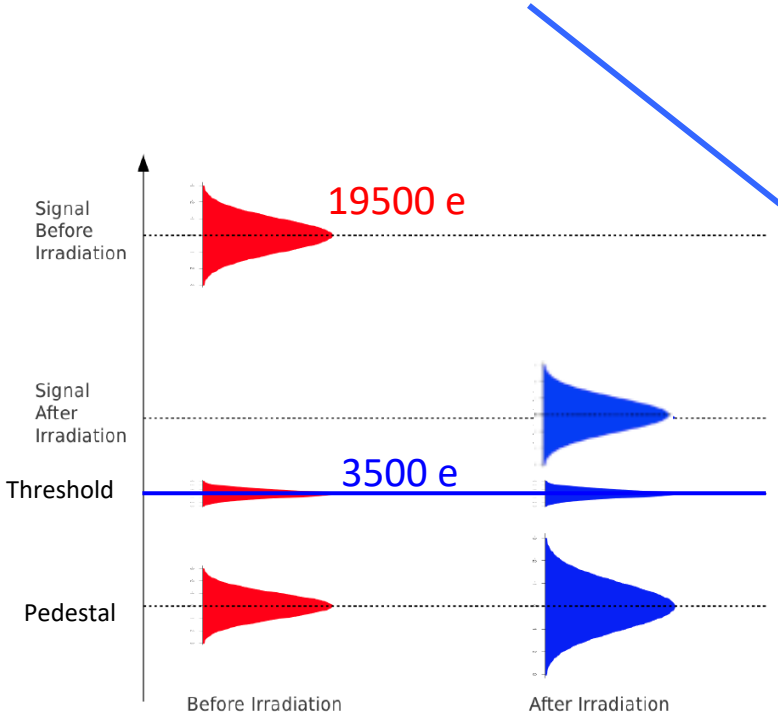
Full Pixel Detector

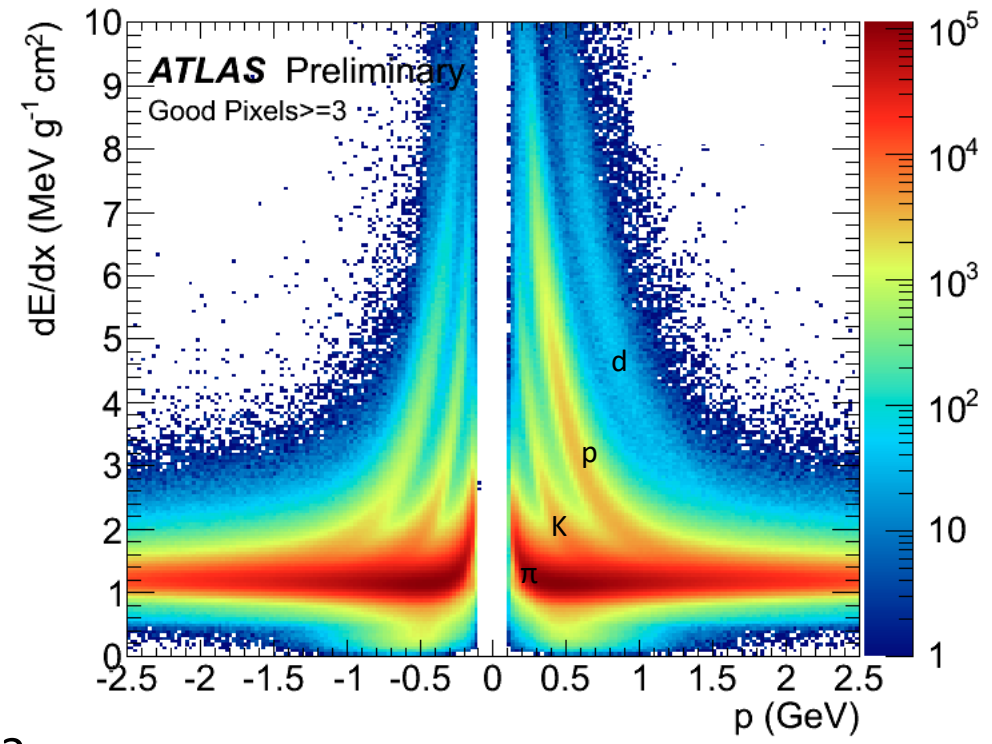
The operation challenge

Signal of a mip in 250µm Si ≙ 19500 e^- → <10000 e^- after irradiation

Charge on more than 1 pixel => S/N > 30 → S/N ~ 10

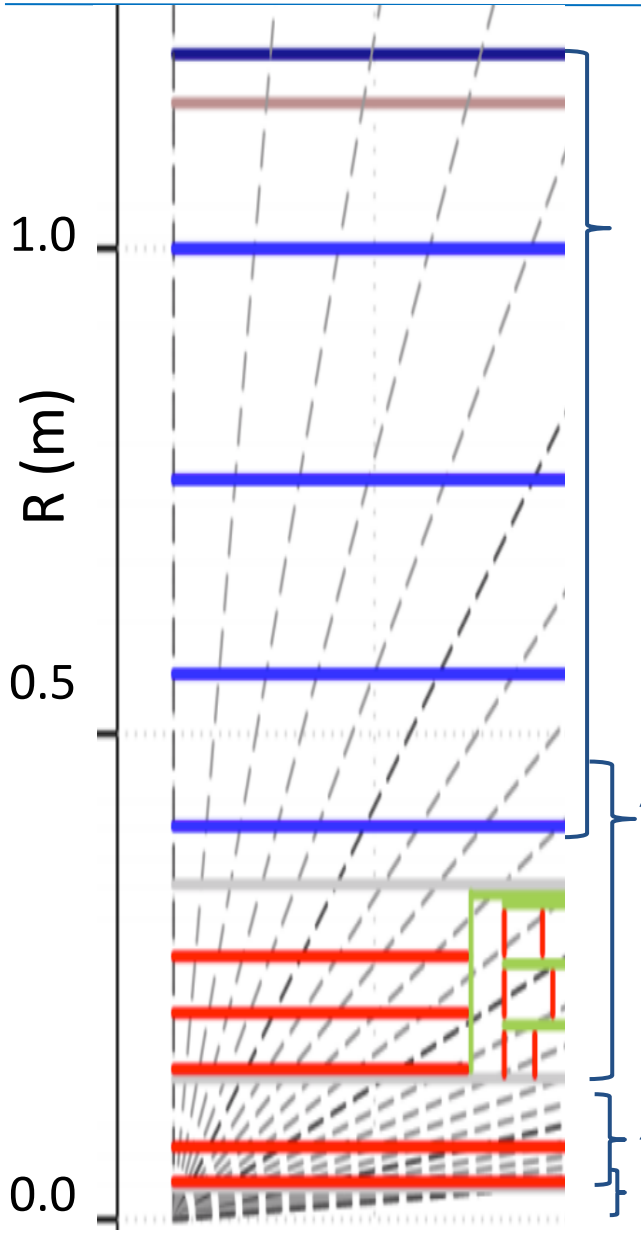
- ❑ Discriminator thresholds = 3500 e, ~40 e spread, ~170 e noise
- ❑ ca. 10 µm x 100 µm resolution (track angle dependent)
- ❑ 12% dE/dx resolution





35?

ATLAS upgrade for HL-LHC: tracker layout

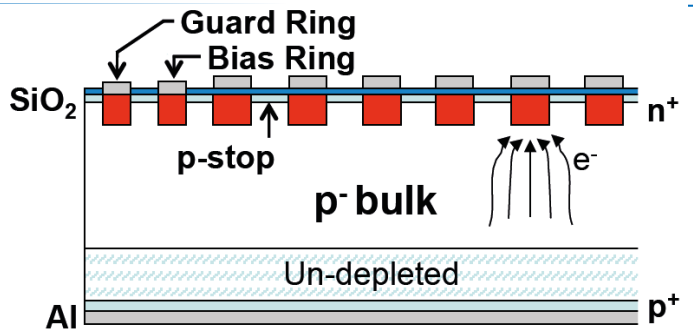


strips

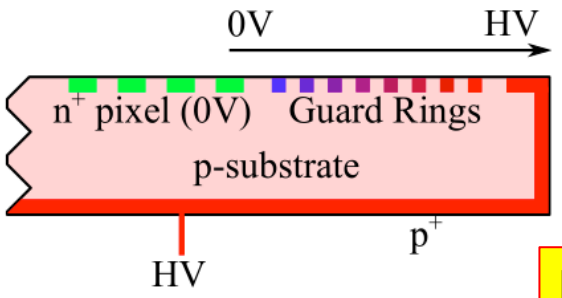
outer pixel

inner pixel

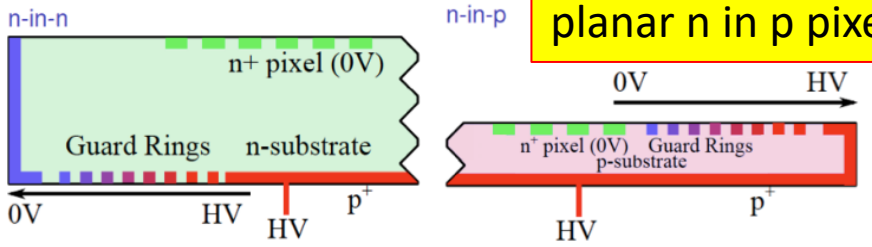
innermost pixel



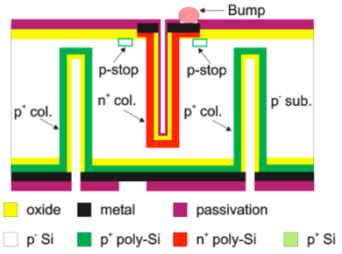
n in p
strip modules



large modules
planar n in p pixels

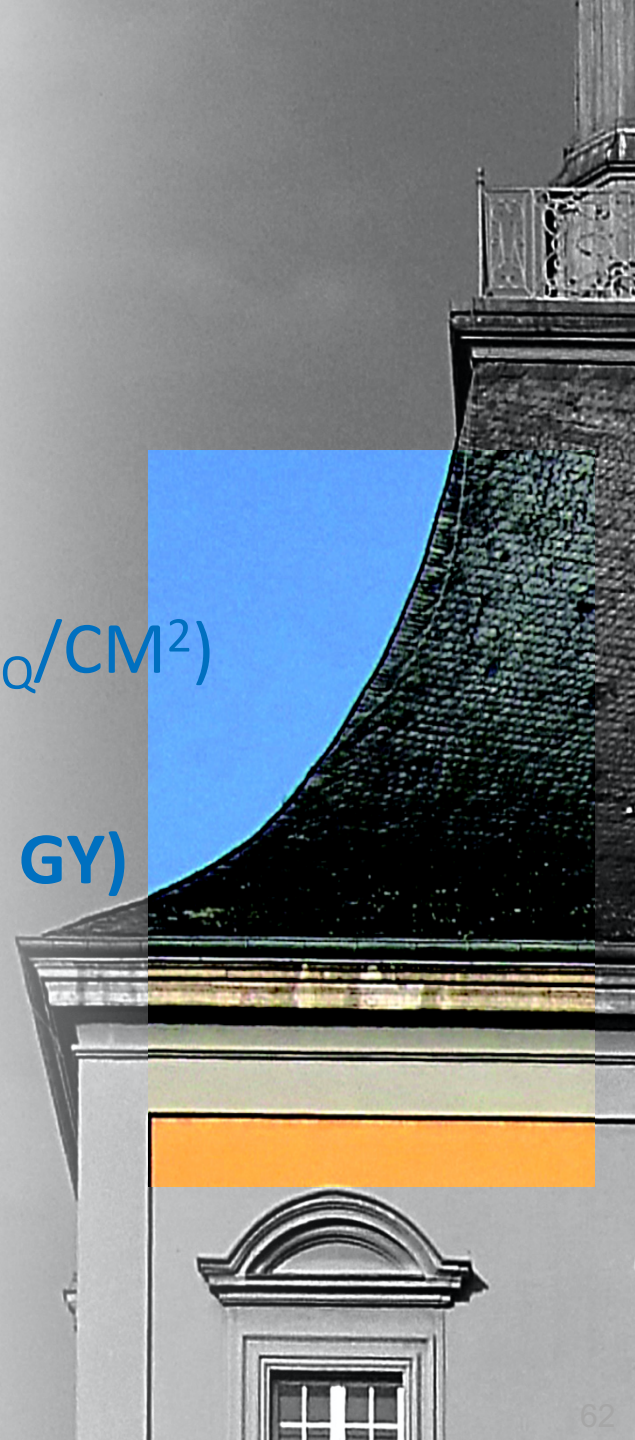


3D silicon



dedicated
rad.-hard
detectors

35?

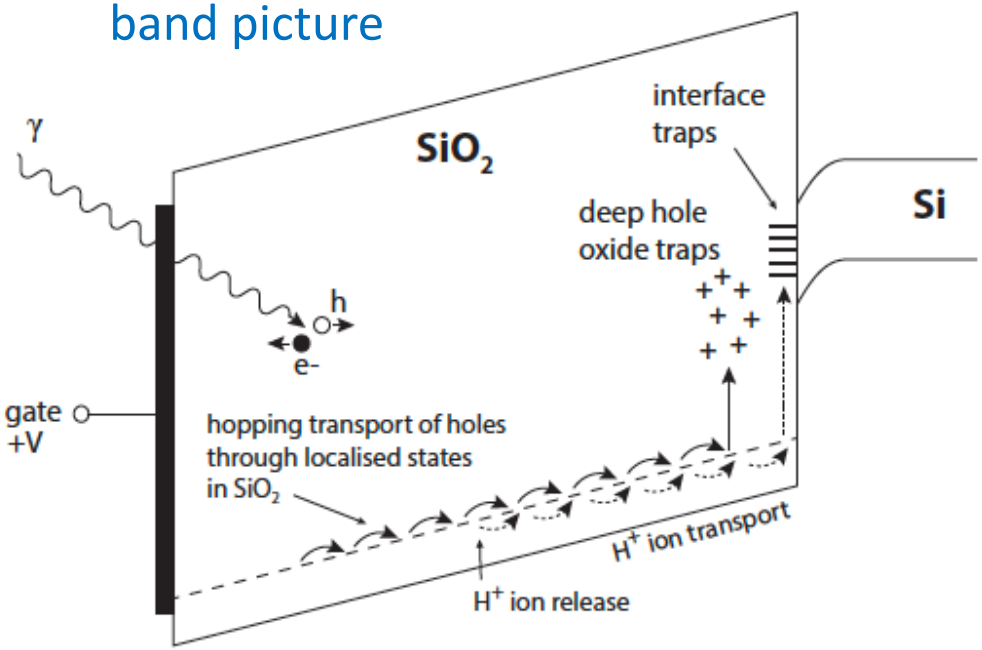


RADIATION DAMAGE

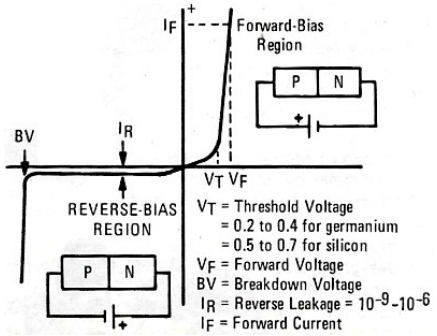
- BULK DAMAGE BY NIEL -> FLUENCE (N_{EQ}/CM^2)
  -> SEE LECTURE 1
- **OXIDE DAMAGE BY IEL -> TID (RAD OR GY)**

Surface damage (TID)

band picture



- net effects:
  threshold shifts
  parasitic currents



1)

- In SiO_2 μ_h **is low**
- Holes can be **(self) trapped**
- If a positive bias is applied at the gate the **holes will move towards the interface** where they will be trapped for long times
  => transistor threshold shifts

2)

- Formation of charges near the interface from defects (dangling bonds) created inside the Si gap.
- They can become charged (+ or -) depending on the carrier type of the channel (nMOS or pMOS).
  => transistor threshold shifts
  (both directions possible)

Radiation damage to the FE-electronics … and cure

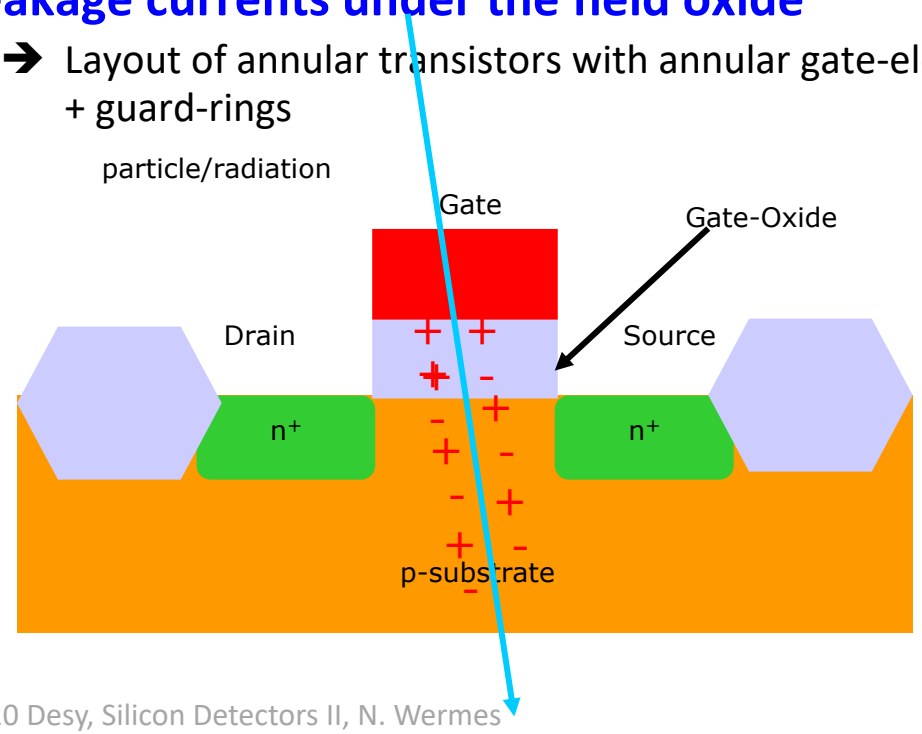
Effects: generation of positive charges in the SiO_2
and defects in Si - SiO_2 interface

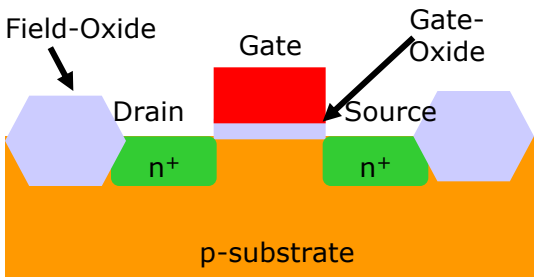
1. Threshold shifts of transistors

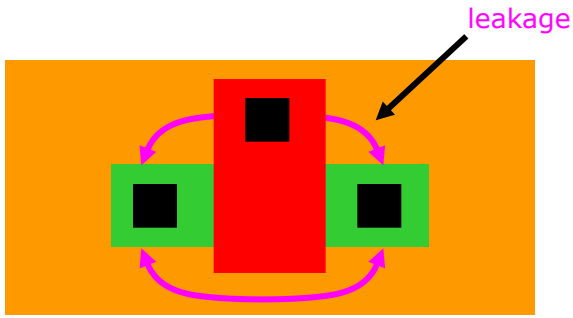
➔ Deep Submicron CMOS technologies with small structure sizes (≤ 350 nm) and thin gate oxides (d_{ox} < 5 nm) → holes tunnel out

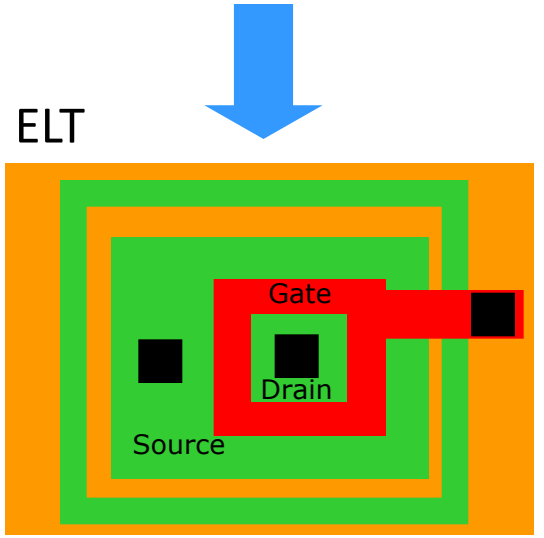
2. Leakage currents under the field oxide

➔ Layout of annular transistors with annular gate-electrodes + guard-rings







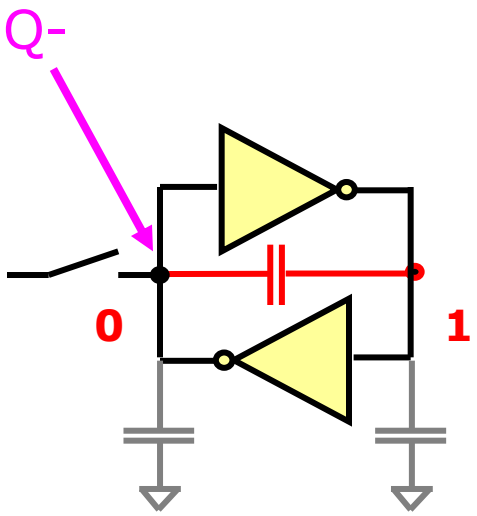


Radiation damage to the FE-electronics … and cure

radiation induced bit errors

(“single event upsets“ SEU)

large amounts of charge on circuit nodes
- by nuclear reactions, high track densities -
can cause “bit-flip“



standard SRAM cell

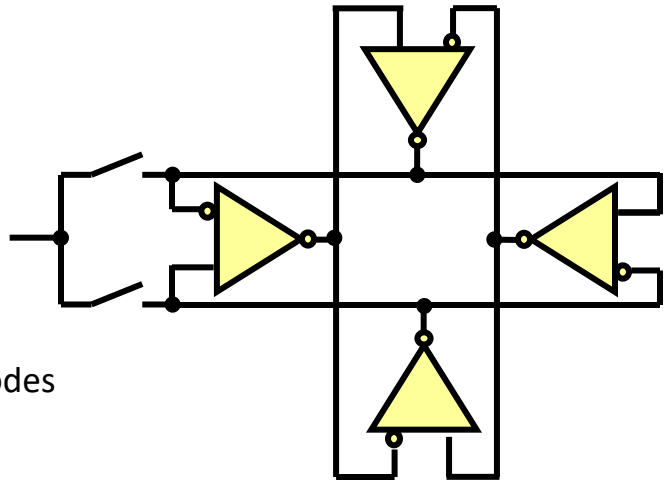
2 examples of error resistant logic cells

➔ enlarge storage capacitances in SRAM cells:

$Q_{crit} = V_{threshold} \cdot C$

➔ storage cells with redundancy (DICE SRAM cell)

information and its inverse stored on 2+2 independent and cross-coupled nodes
→ temporary flip of one node cannot permanently flip the cell.


SEU tolerant DICE SRAM cell

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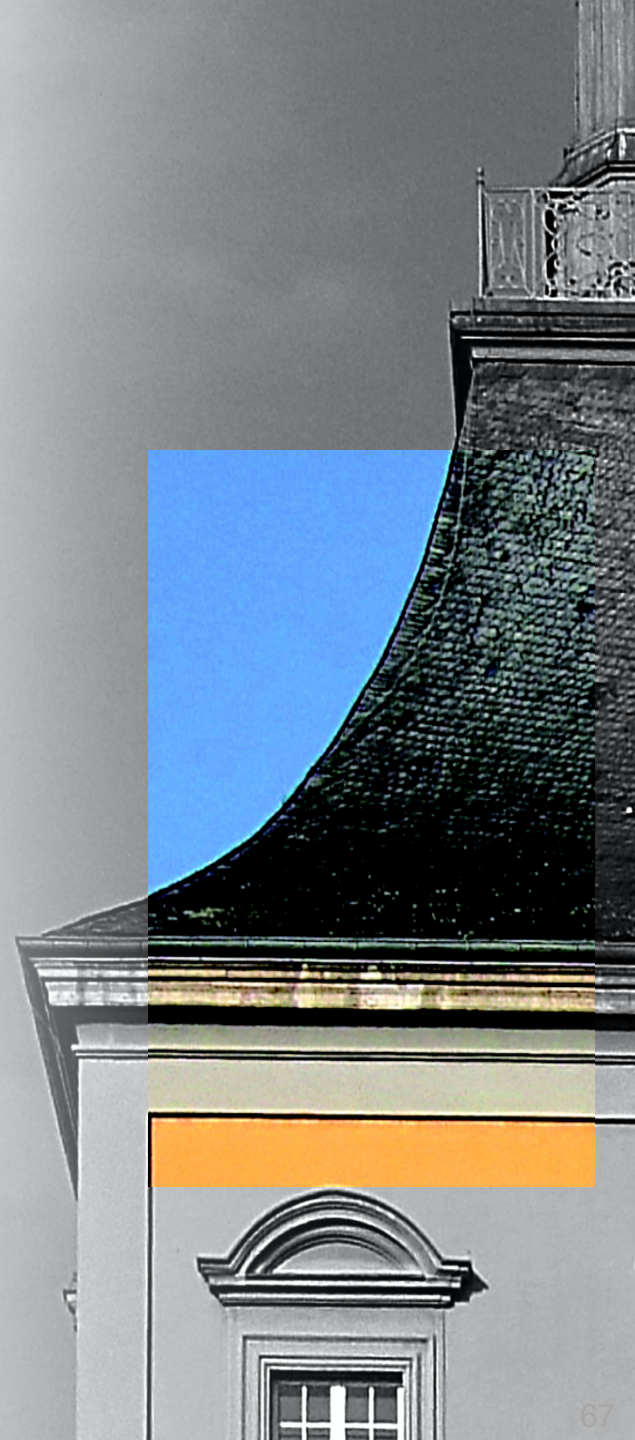
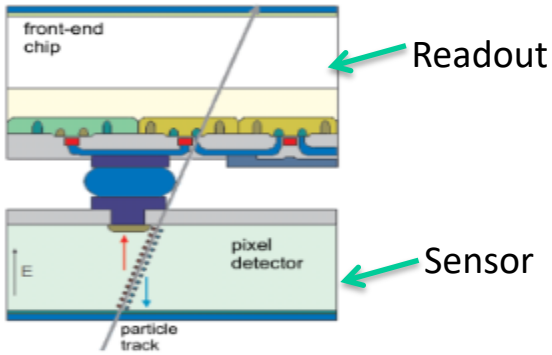
New Developments Monolithic CMOS Pixels

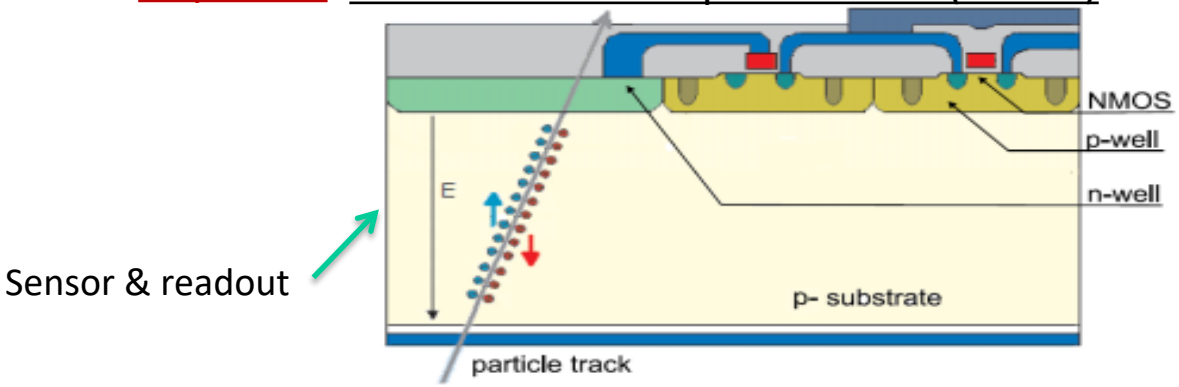


Introducing DMAPS

Hybrid detector



Depleted monolithic active pixel sensor (CMOS)



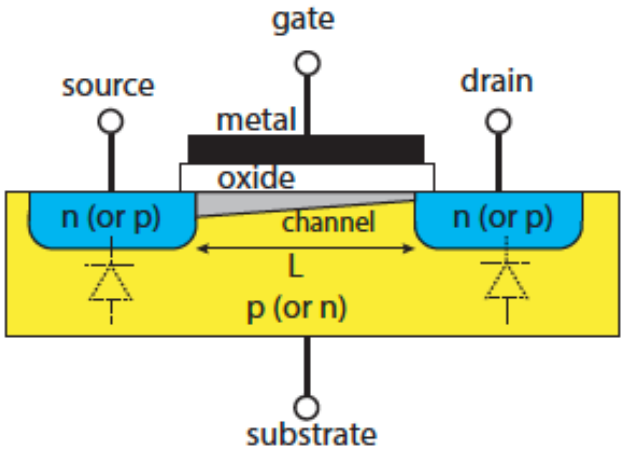
No need for fine pitch bump bonding between sensor and readout circuitry.

→ **Easier to produce and easier to test**

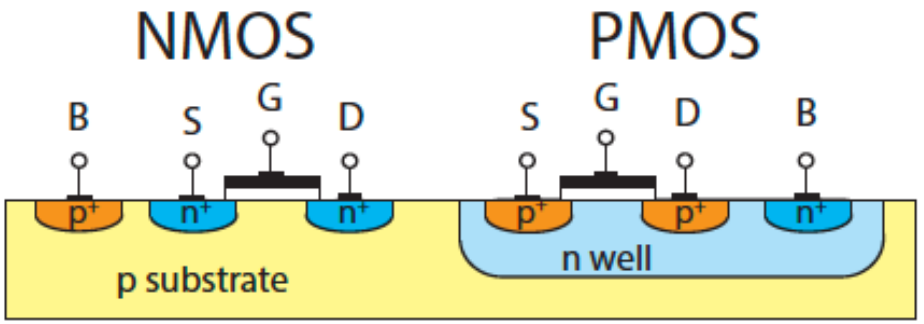
→ Large cost reduction (sensor + R/O chip + BB → one chip)

→ Plus all advantages that large CMOS Fabs may offer, including fast turn around, large wafer sizes, large throughput

fresh-up: MOSFET -> NMOS, PMOS, CMOS



(a) MOSFET.

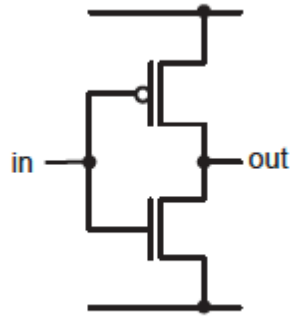


(b) CMOS.

- reminder: transistors operate in “inversion”

- NMOS: transistor channel current are electrons
- PMOS: transistor channel current are holes

- CMOS: both transistor types are realised in the same substrate.
  IMPORTANT for electronic circuits



(a) CMOS inverter.

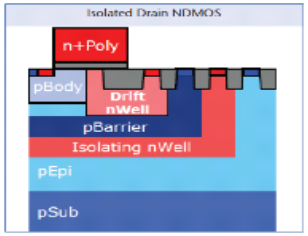
What is needed to realise (radhard) depleted CMOS pixels?

$$d \sim \sqrt{\rho \cdot V}$$

1 **"High" Voltage add-ons to apply 50 – 200 V bias**

I. Peric, DOI: 10.1016/j.nima.2007.07.115

2 **"High" Resistivity Substrate Wafers (100 Ωcm – kΩ cm)**



from: www.xfab.com

3

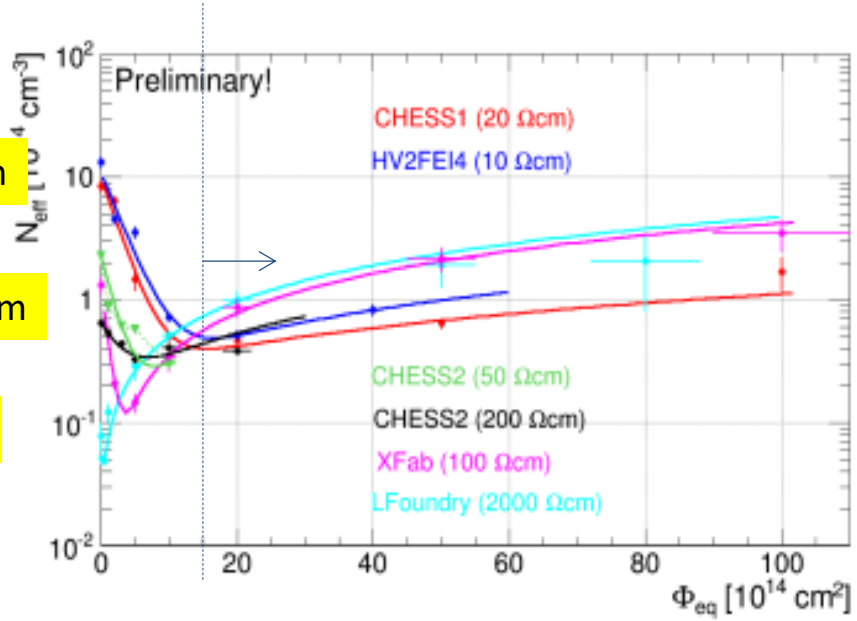
Multiple (3-4) nested wells (for shielding and full CMOS)

4 **Backside Processing (for thinning and back bias contact)**

~10 Ωcm

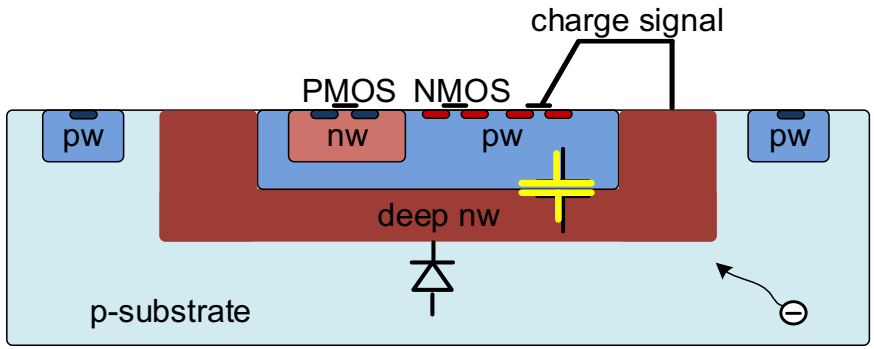
~100 Ωcm

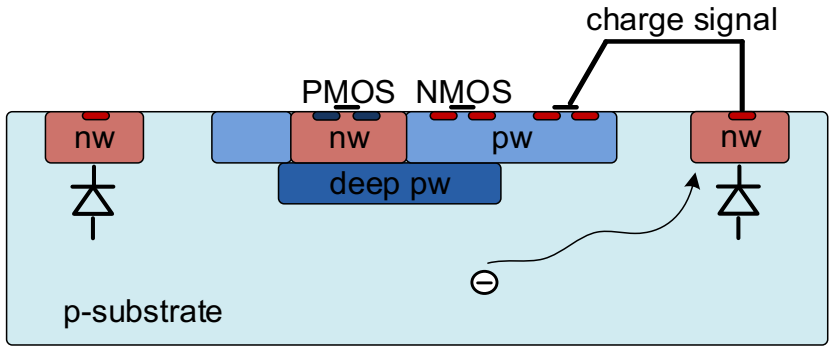
kΩcm



I. Mandic et al., JINST 12 (2017) no.02, P02021

Large versus small collection electrode (fill factor)





Electronics **inside** charge collection well

- **large** collection electrode
  => little low field regions
  => on average **short(er) drift** paths
  => less trapping -> **radiation hard**
- **Larger** sensor **capacitance** (pw & dnw!)
  => noise & speed/power penalty
  => possible x-talk (digital to sensor)

$$\tau_{CSA} \approx \frac{1}{g_m}\frac{C}{C_f}$$

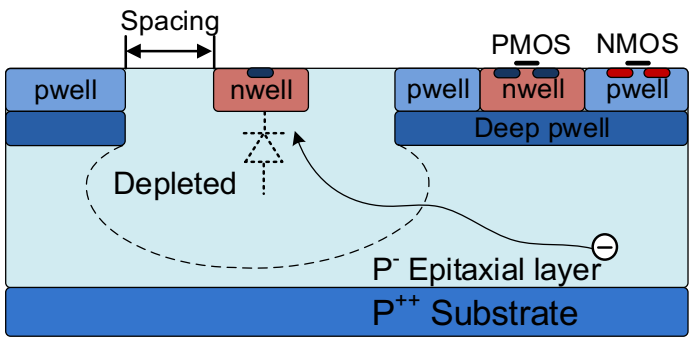
$$ENC^2_{\text{thermal}} \approx \frac{4}{3}\frac{kT}{g_m}\frac{C}{\tau_f}$$

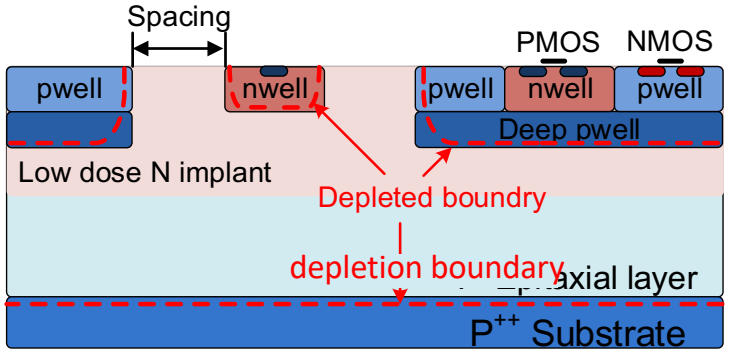
power

Electronics **outside** charge collection well

- **small** electrode
  => **very small sensor capacitance (< 5fF)**
  => lower analog power budget (noise, speed)
  => less prone to x-talk
- on average long(er) drift distances and potentially low field regions
  → **radiation hardness needs process mods**

e.g. Process modification – TowerJazz 180 nm CMOS





Standard process

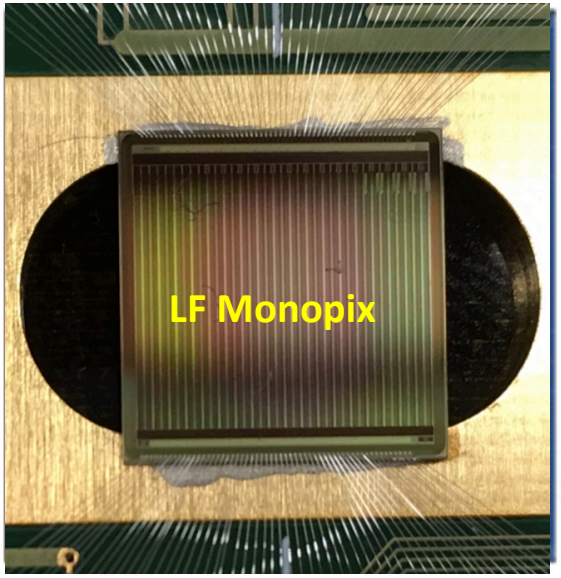
- **ALICE ITS type**
- **High res. p**-type epi. (> 1 kΩ·cm)
  => thickness typ. **25 µm**
- Quadruple-well
  => deep pwell shields nwell => **full CMOS**
- **Reverse bias** typ. -6V
  => enhanced (but not yet full) depletion
  => some charge collected by diffusion only => slow

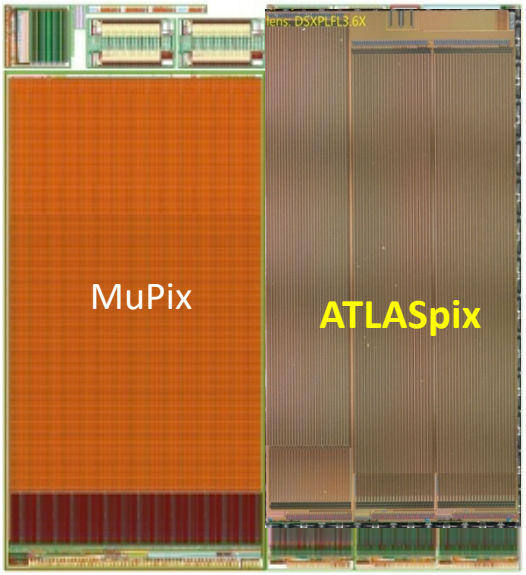
Modified process

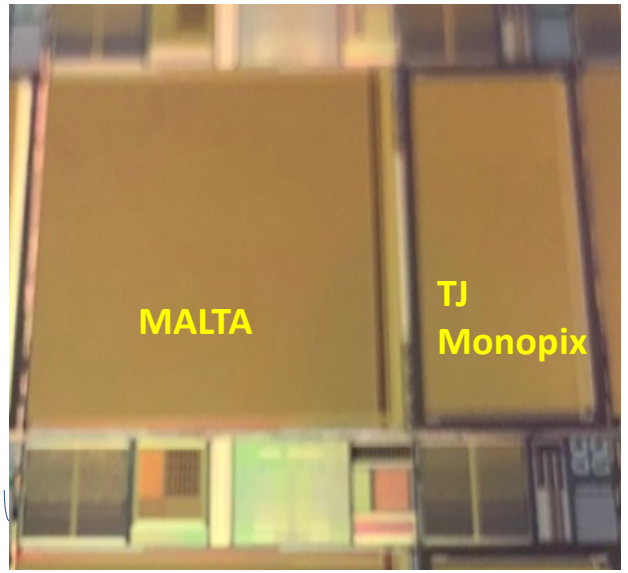
- Additional planar medium dose **N implant**
  => depletion from two junction boundaries
  full volume can be depleted
  better charge collection in lateral direction
- Maintain small capacitance
- No significant circuit/layout changes

W. Snoeys et al. DOI: 10.1016/j.nima.2017.07.046

Large (~1 cm^2) full CMOS chips (=modules) w/ readout



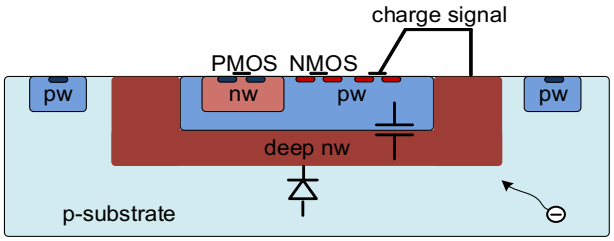




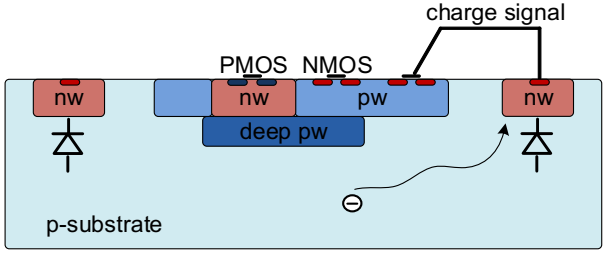
LFoundry 150 nm
substrate ρ > 2 kΩcm

ams 180 nm
substrate ρ ~ 0.08 - 1 kΩcm

TowerJazz 180 nm epitaxial (25 µm)
substrate ρ > kΩ cm



large electrode



small electrode

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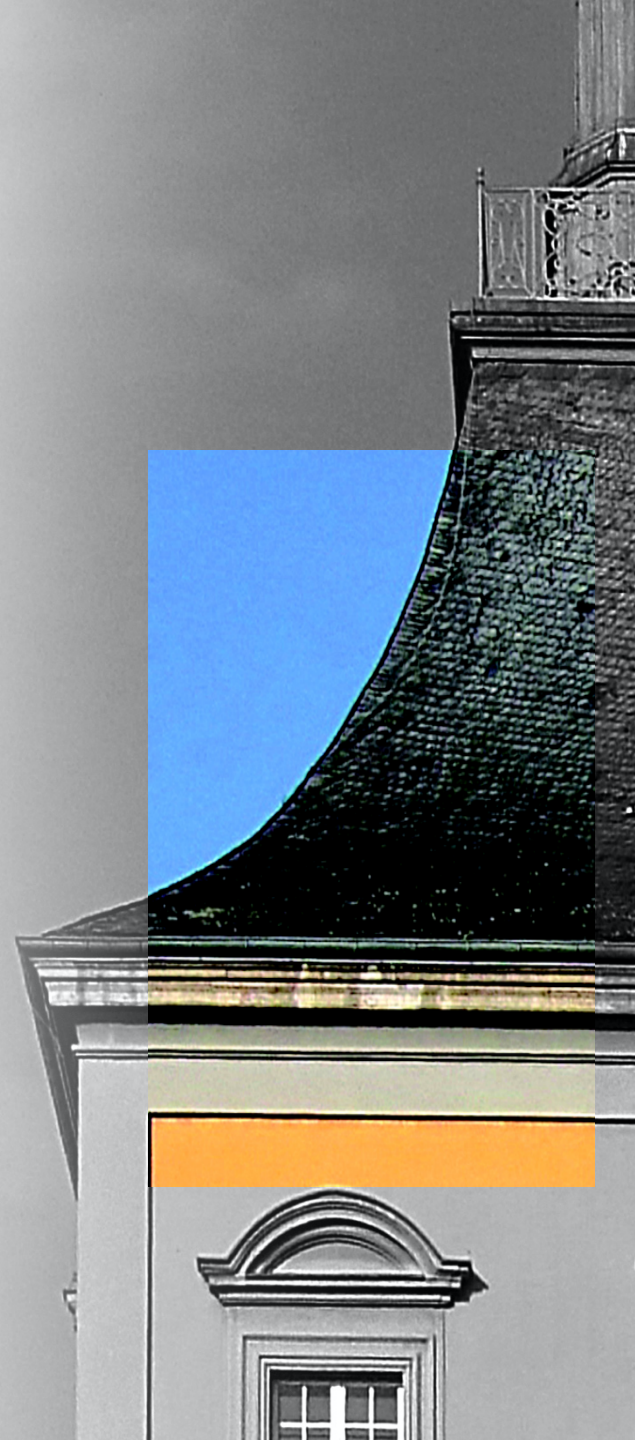
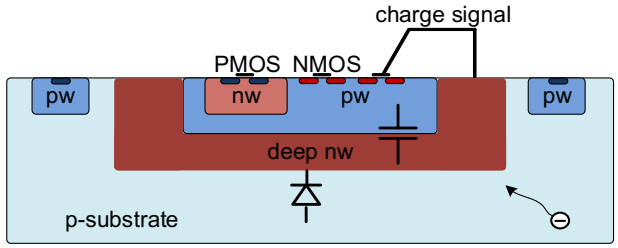


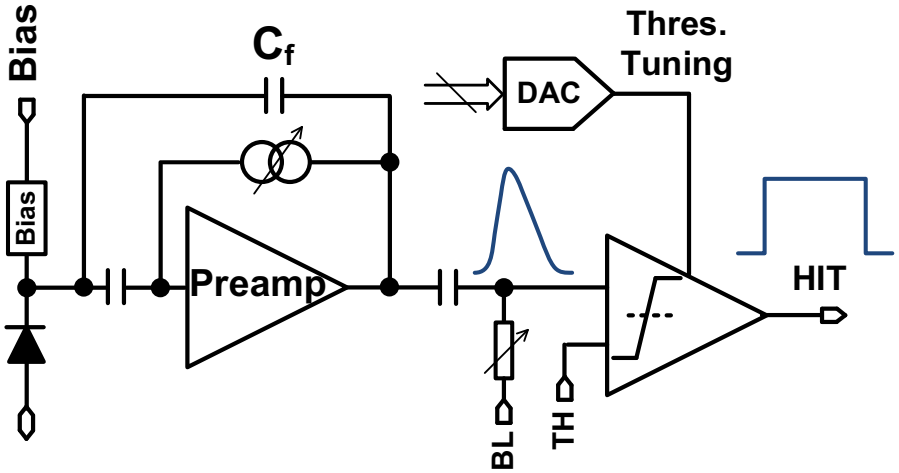
DIFFERENT ELECTRODE (LARGE/SMALL)
APPROACHES LEAD TO DIFFERENT

ANALOG FRONT END CHOICES

Analog front-ends - CSA vs. voltage amplifier

- large electrode



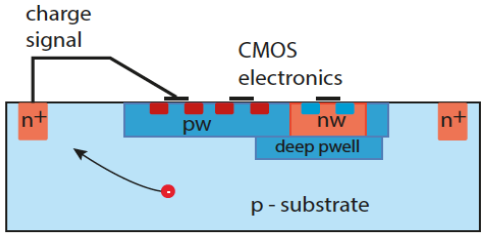


Charge Sensitive Amplifier

- Choice for large electrode design
- Gain (ideally) independent of C_D
  => G ~ $1/C_f$ (typ. C_f ~ 5 fF)
- $\tau_{CSA} \propto \frac{C_D}{g_m \cdot C_f}$, $ENC^2_{therm} \propto \frac{kT}{g_m}\frac{C_D^2}{\tau}$
  => requires larger g_m (power) for large C_D
  => typ. power 30 – 40 µW per pixel
- threshold trimming is advised and a standard in typical implementations

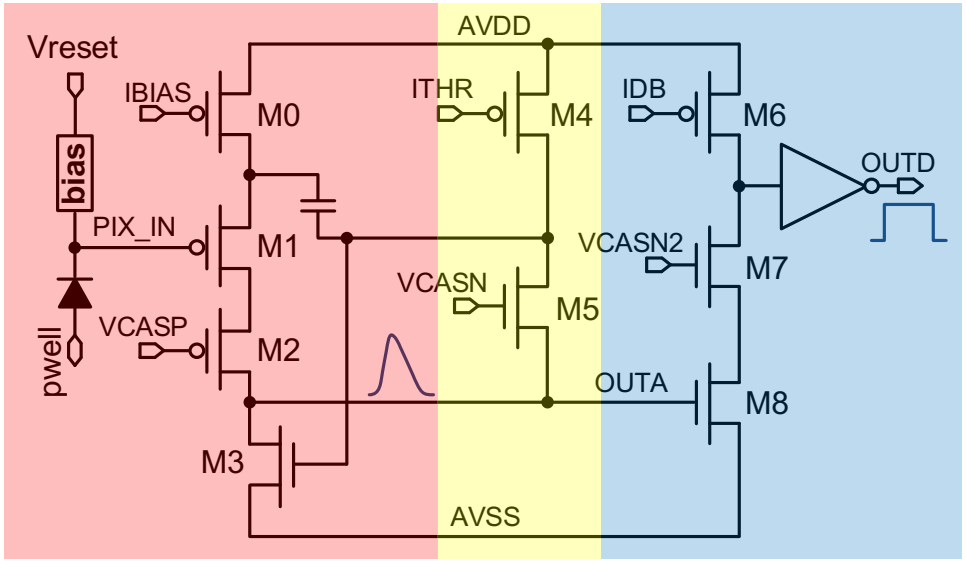
Analog front-endS - CSA vs. voltage amplifier

- small electrode



(b) Small fill-factor

W. Snoeys, DOI: 10.1016/
j.nima.2013.05.073



D. Kim et al., doi 10.1088/1748-0221/11/02/C02042

Voltage amplifier (ALPIDE like)

- => Profit from small sensor capacitance
  => large voltage signal Q/C_D @ input node
- Very compact design
  => amplification + shaping in one stage
  => simple inverter as discriminator
  => no threshold trimming used (see later)
- Optimized power for required timing
  => ~1 µW/pixel for 25 ns peaking time

$$\frac{S}{N} \propto \frac{Q}{C_D}\sqrt{g_m} \propto \frac{Q}{C_D}\sqrt[m]{P}, \quad P \propto \left(\frac{C_D}{Q}\right)^m$$

$2 \lesssim m \lesssim 4$

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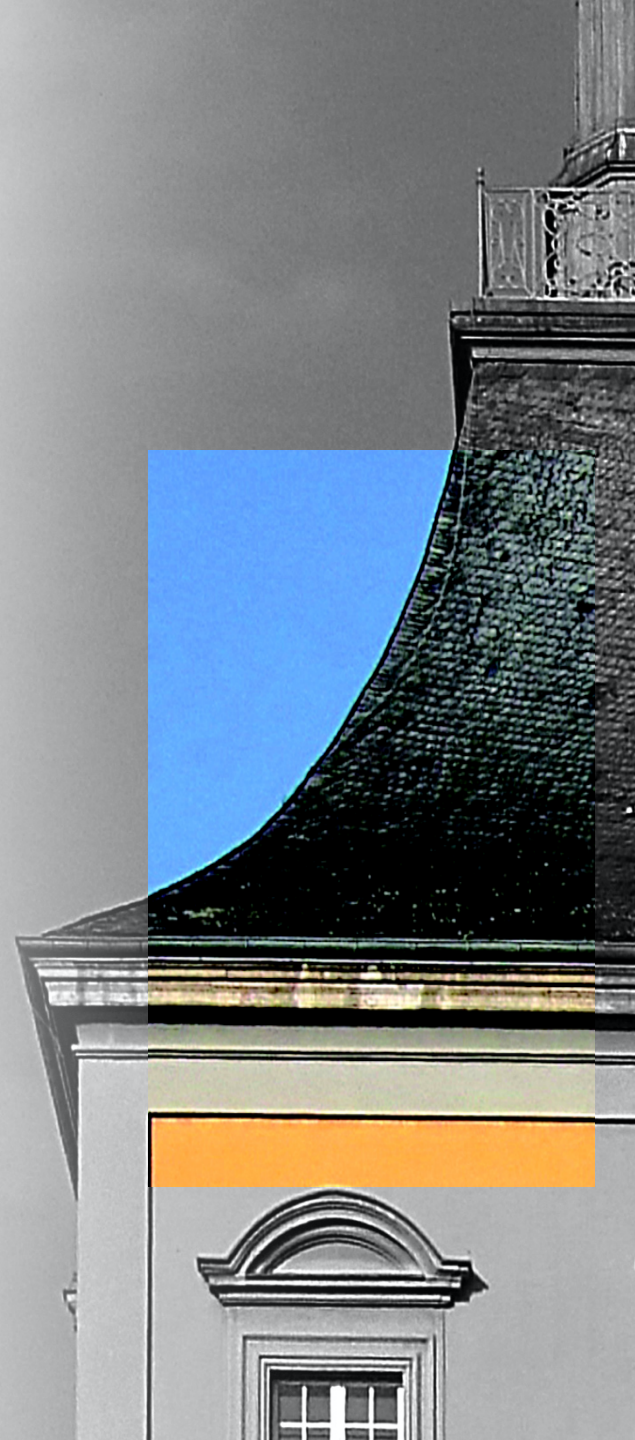


DMAPS

READOUT ARCHITECTURE CHOICES

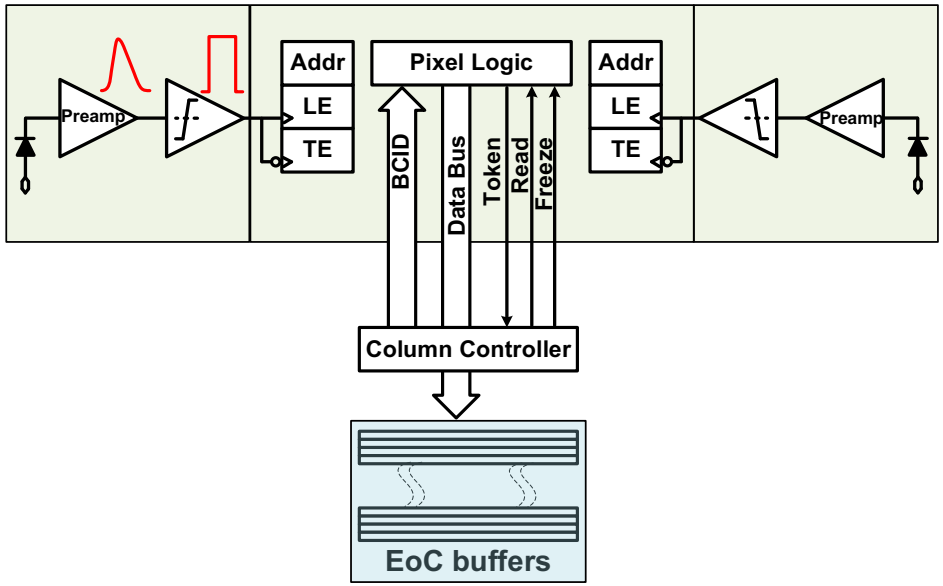
wanted

- Small pixels
- High logic (memory) density

- Fast shaping
- High data transmission bandwidth

“Column drain” Architecture

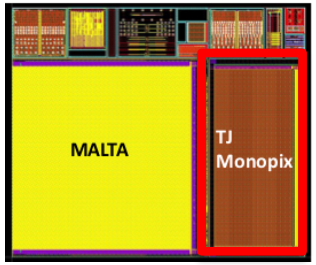
Synchronous readout => time stamping in matrix



- BC ID (40 MHz) distributed in the column
- Hit timing stamped in pixel
  - LE: leading edge
  - TE: trailing edge

  => Time of arrival: LE

  => Ana. info. from ToT
- Hits read out sequentially, following a token passing scheme on a shared column bus



- Well established scheme in ATLAS – FE-I3 like (current pixel detector)
- Demonstrated rate capability for the addressed goal (ITk outer pixel layers)
- Affordable in-pixel logic (storage & digital R/O)
- Challenges: preventing digital cross talk, pixel size, C_D (for large electrode design)

ALTERNATIVE: Asynchronous readout schemes

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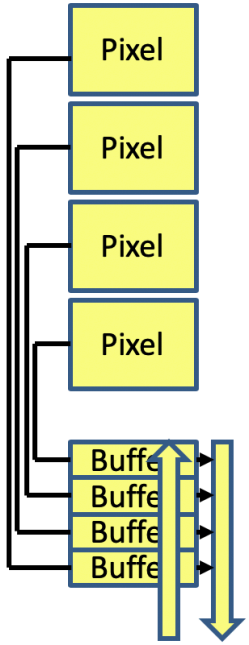
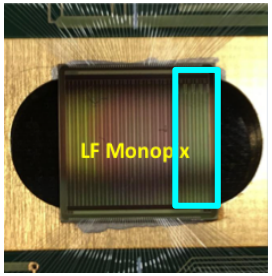
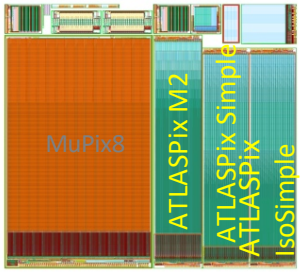
DMAPS with asynchronous matrix => time stamping at periphery

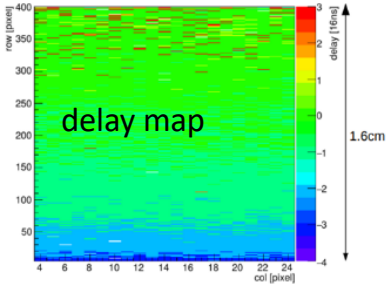
=> Hits transferred to periphery immediately => calls for massive parallelism

A) One to one connection



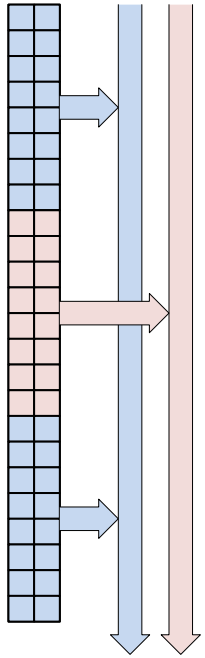


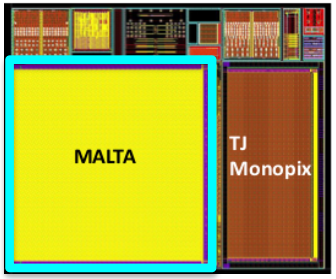




o(400) lines in two metal layers; larger periphery

B) Shared bus by pixel groups





- Two high speed buses w/ short pulses (~1ns)
- Complicated balancing for multibit data to arrive simultaneously at bottom
- GHz synchronization needed

- Challenge: avoid data collisions

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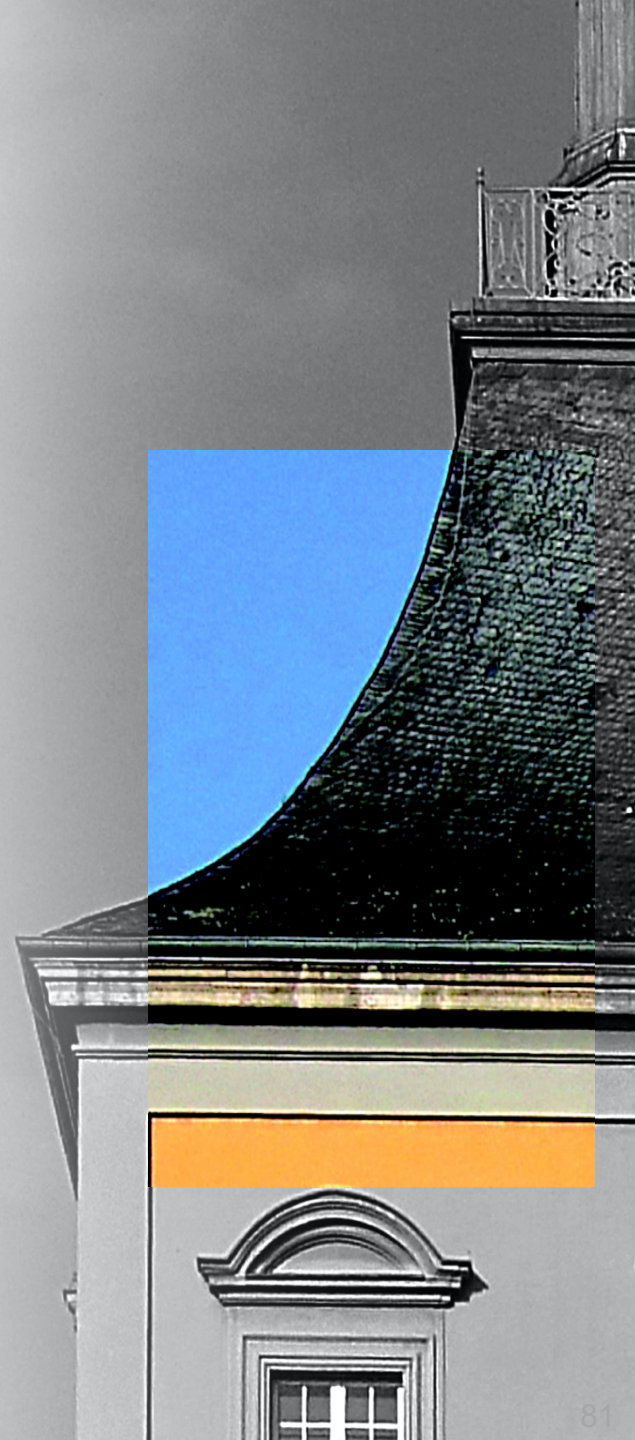
Results
Large Electrode Design



LF-Monopix1: Results

M. Barbero et al.,
arXiv:1911.01119,
submitted to JINST

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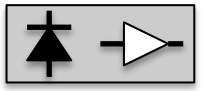
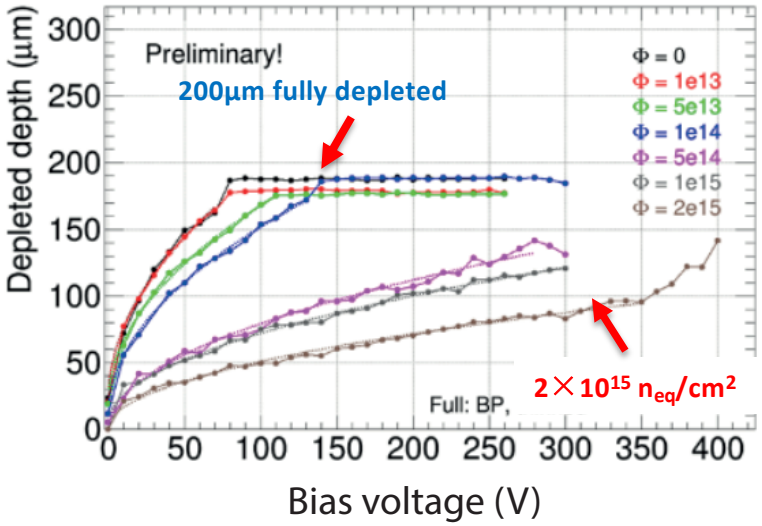
- High and uniform efficiency even after irradiation

Active sensor

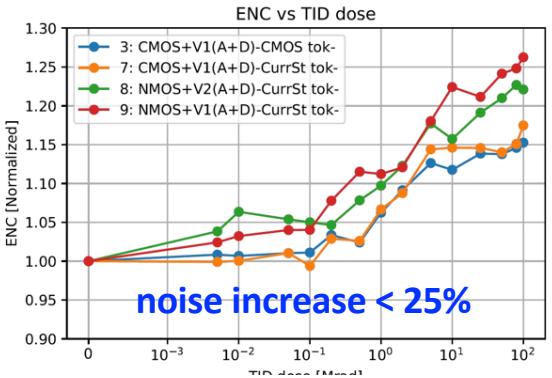


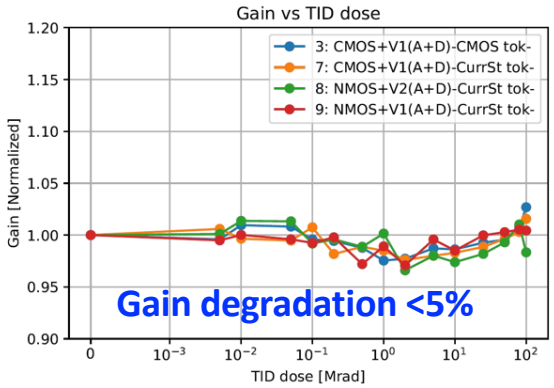
- NIEL (2 × 10^{15} n_{eq}/cm^2) ✓



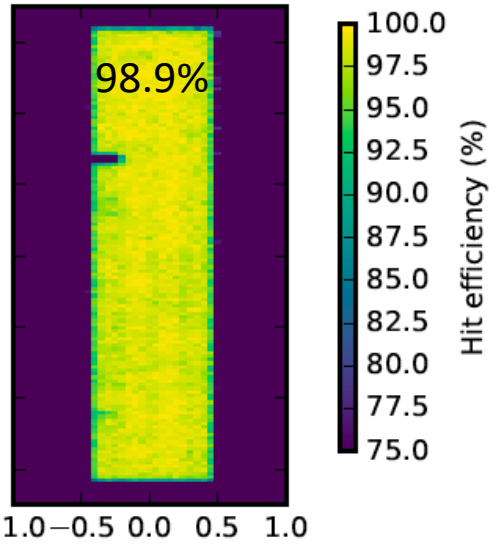
I.Mandić et al.,
DOI: 10.1016/j.nima.2018.06.062

- TID (100 Mrad) ✓





After $10^{15}n_{eq}/cm^2$ (neutrons)



- Noise occ. < 0.1 Hz/pix
  < 10^{-7}/25 ns/pixel
- 0.2% masked pixels
- Dry ice cooling
- Bias -130 V (this sensor!)
- Thres ~1700 e-
- **ε = 98.9 ± 0.1 %**

T. Hirono et al., DOI: 10.1016/j.nima.2016.01.088
P. Rymaszewski et al., DOI: 10.1088/1748-0221/11/02/C02045

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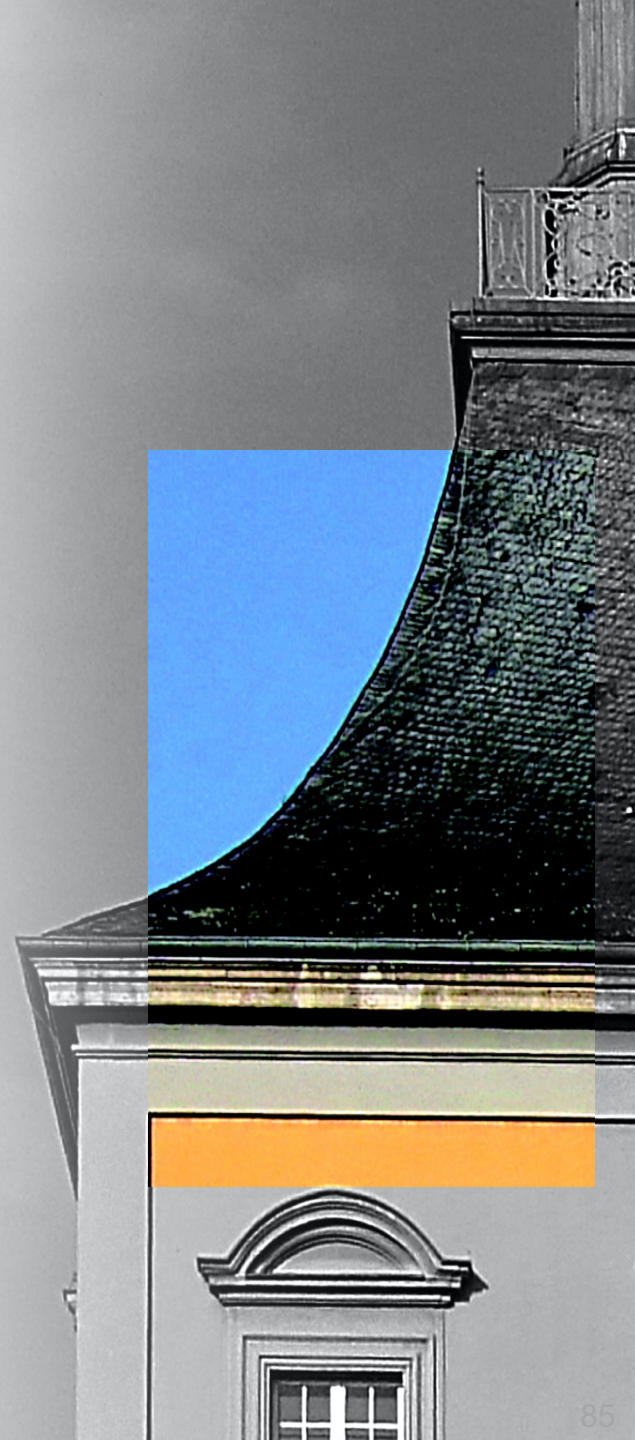
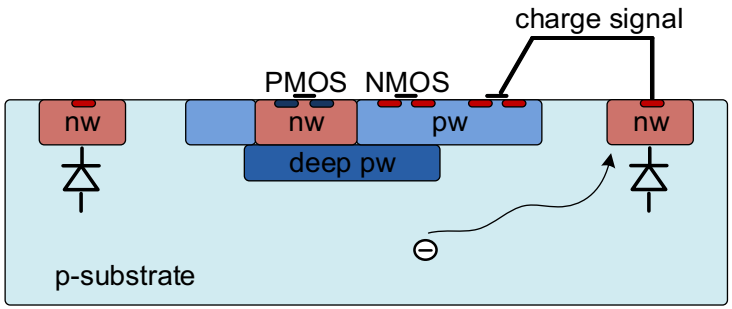
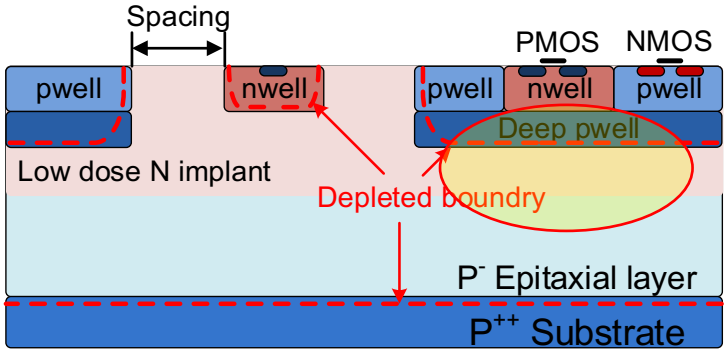
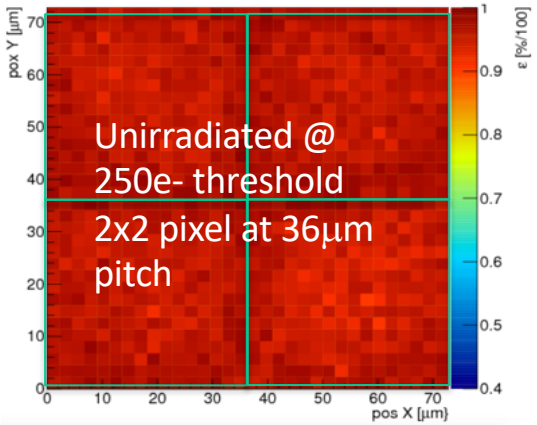
Results
Small Electrode Design



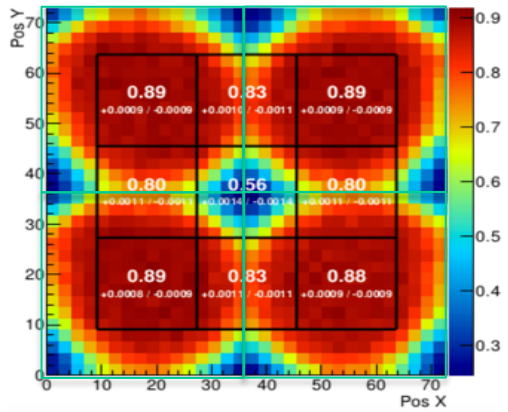
Charge collection with small electrodes







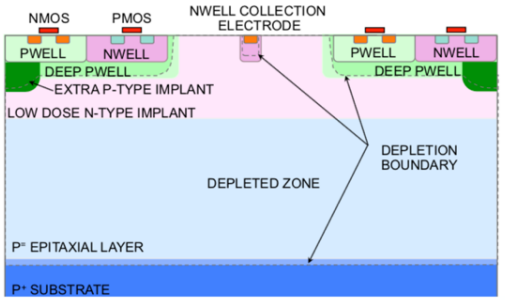
Irradiated 10^{15}n/cm^2 @ 350e- threshold
2x2 pixel at 36 µm pitch

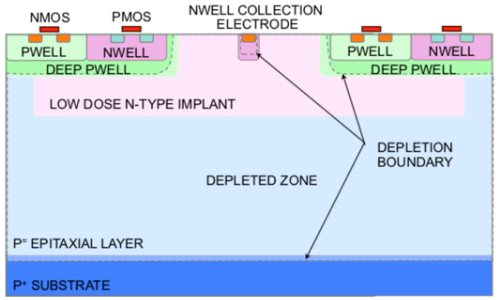


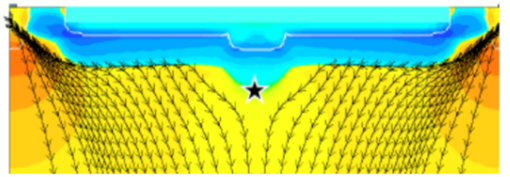
Optimations for Radiation Hardness

1. Structuring underneath dpw

2. Lower thresholds and noise
   -> mods to analog electronics



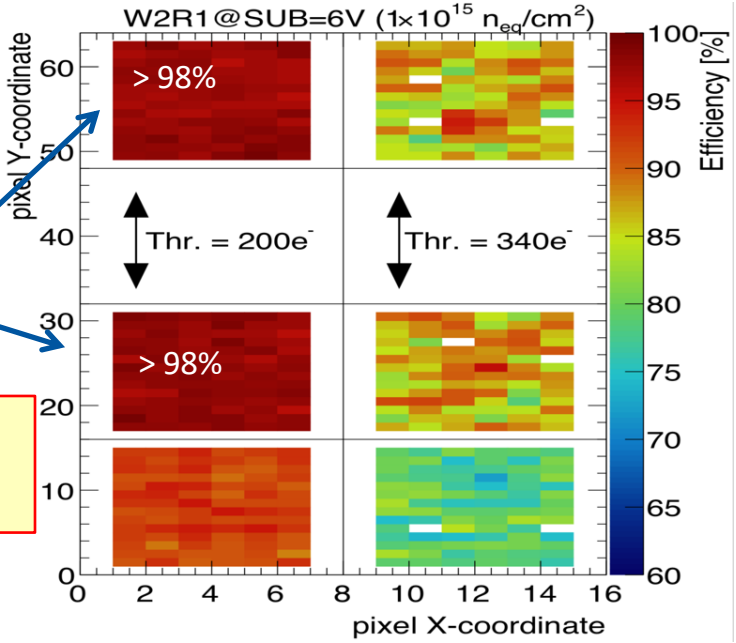




M. Dyndal et al., 2020_JINST_15_P02005

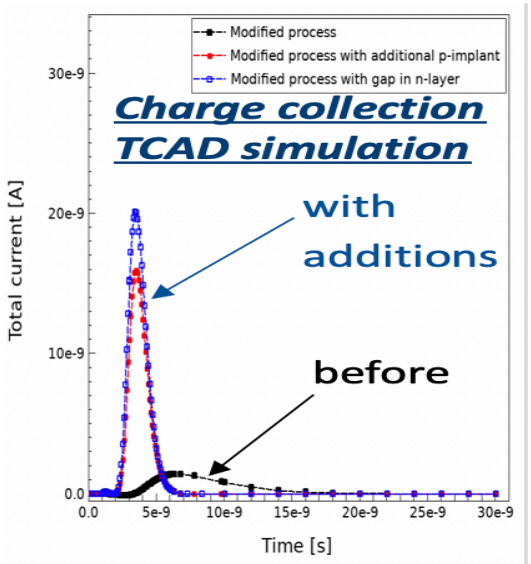
MiniMALTA test chip
36x36µm²
after 10^{15} n_{eq}/cm^2

measures
1 plus 2



3. high resistivity substrate
   (pCz)

M. Munker 10.1088/1748-0221/14/05/C05013



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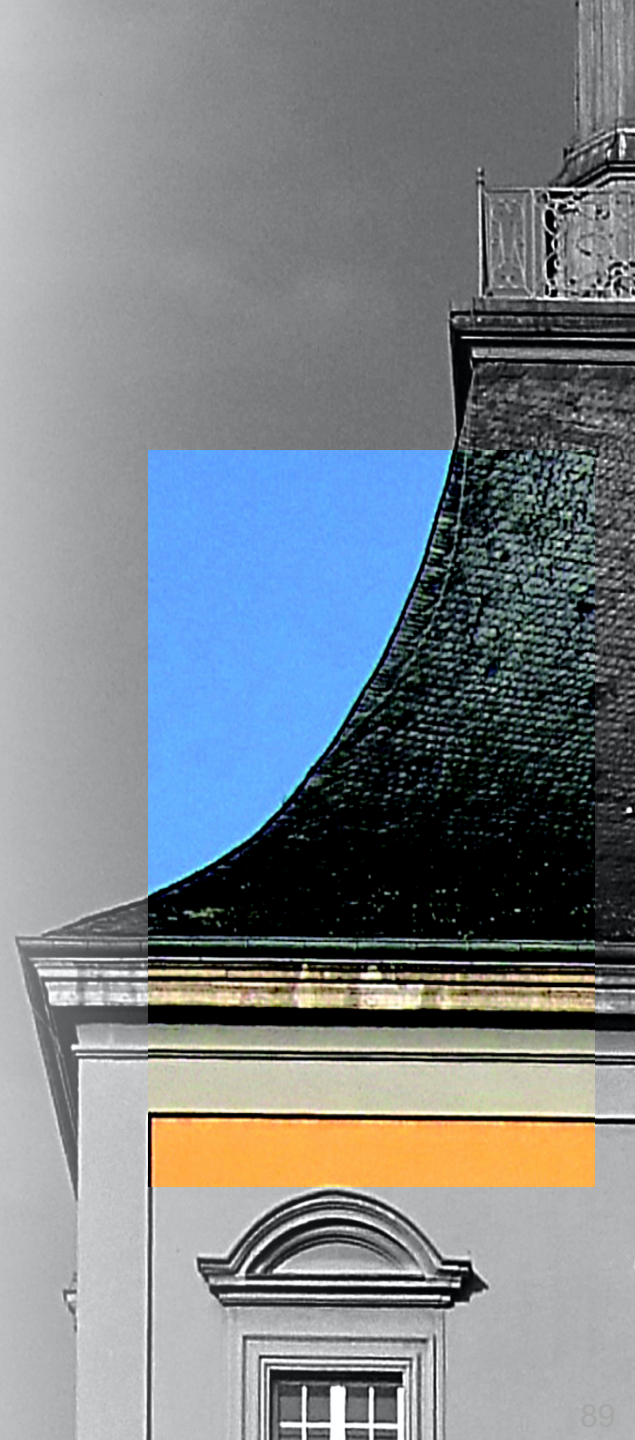
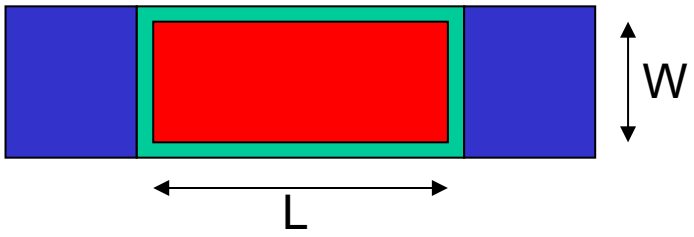
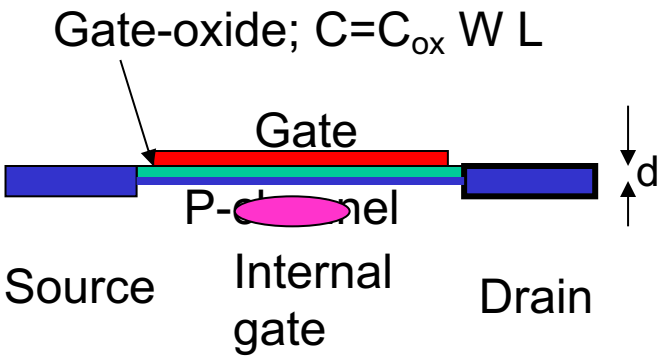
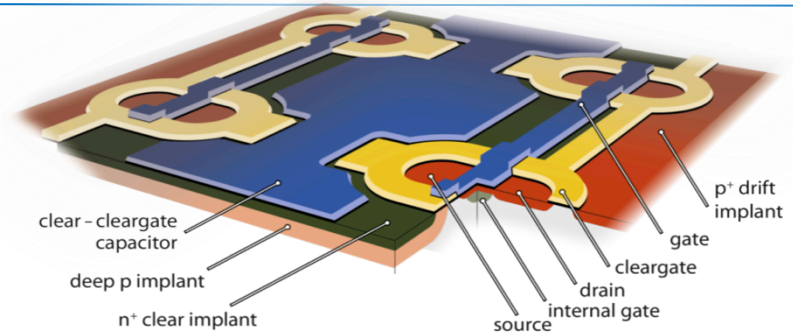
DEPFET Pixels

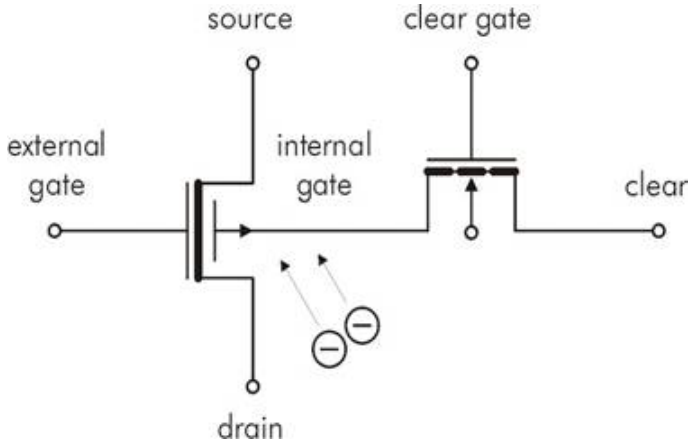


How does a DEPFET work?









A charge **q** in the internal gate is – via the capacitance to the channel – a voltage which "steers" the channel current I_d together with the external gate voltage, which hence effectively changes by: $\Delta V = \alpha\ q / (C_{ox}\ W\ L)$.
$\alpha < 1$ due to stray capacitances

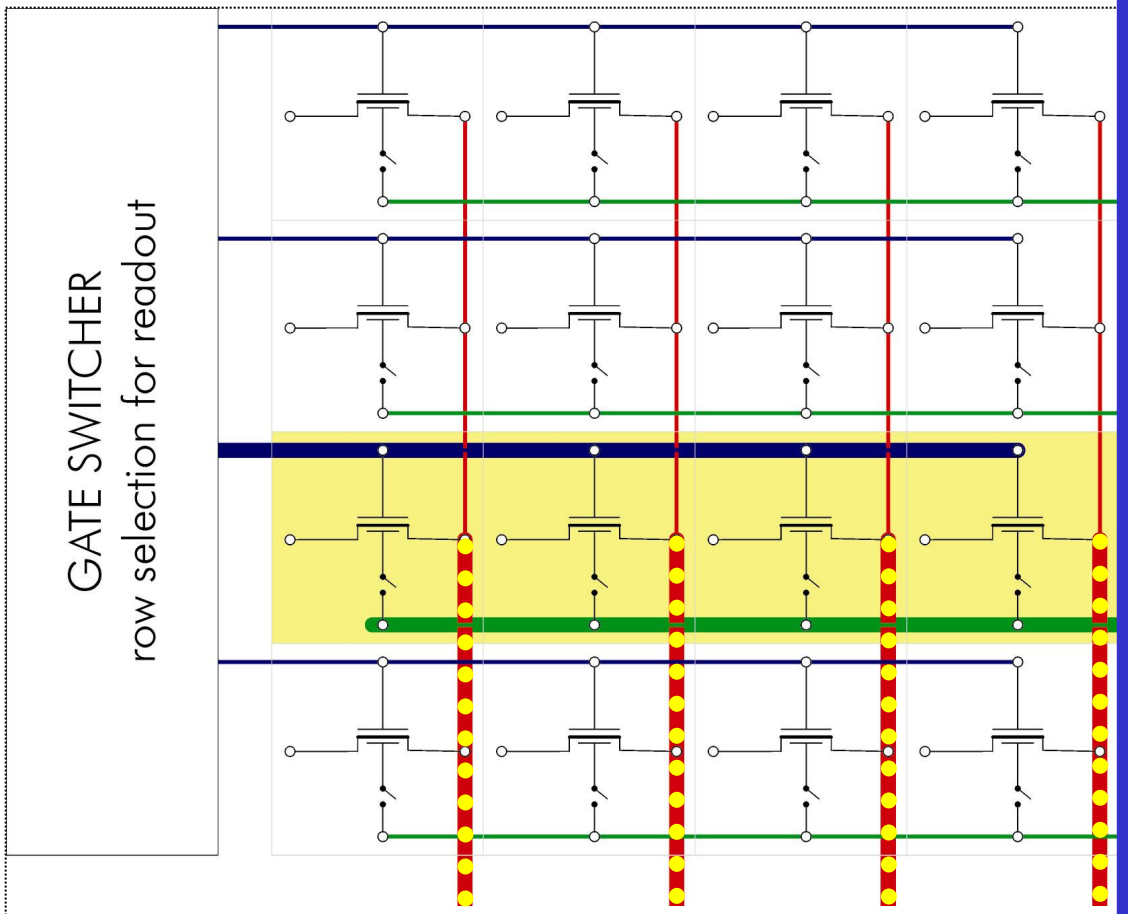
Kemmer, J., G. Lutz et al., Nucl. Inst. and Meth. A 288 (1990) 92

q

features:

- g_q~ 700 pA/e^-
- small intrinsic noise
- sensitive off-state, w/o power used

DEPFET pixels: „rolling shutter“ frame R/O



- 1 row active

  (1) read signal + ped current

  (2) CLEAR

  (3) read pedestal current

  merge currents: (1) – (2)

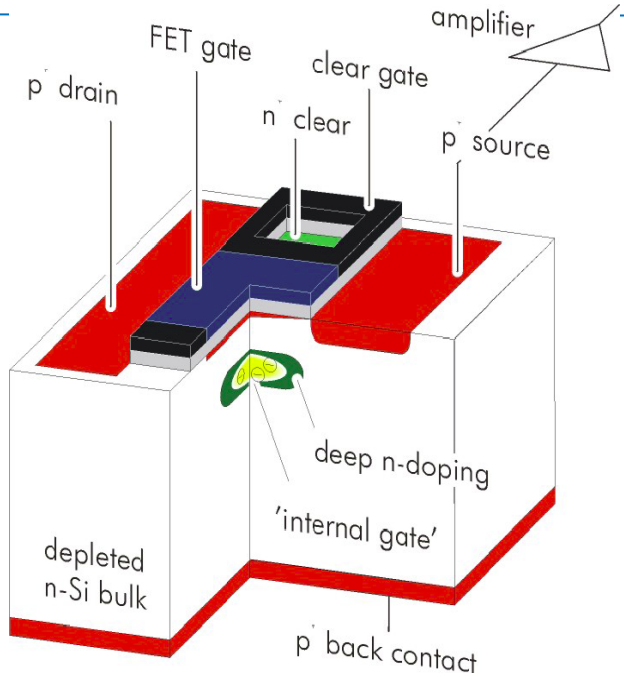
- all other rows OFF

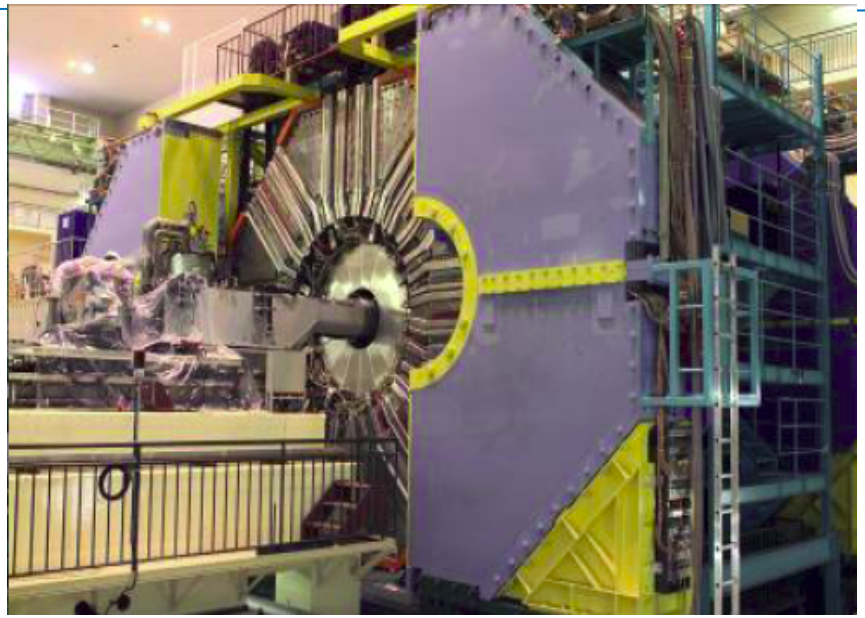
  still active for signals

→ low power !

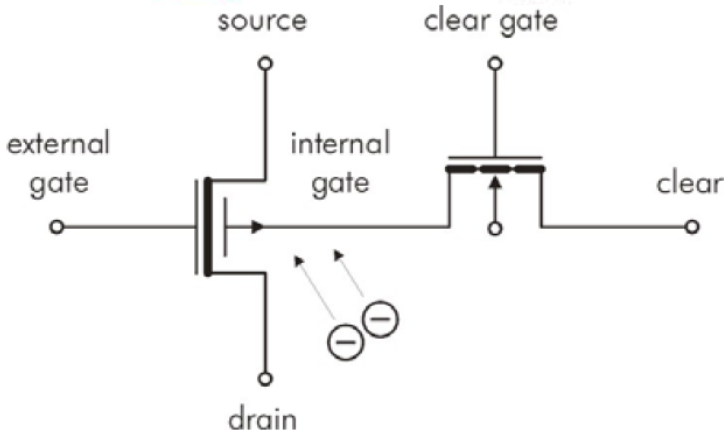
(60 mW/cm^2)

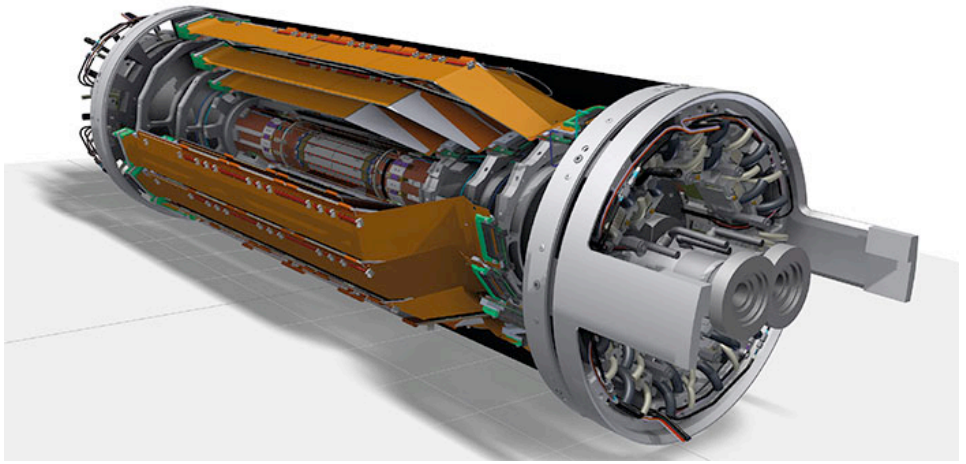
DEPFET pixels





Vertex Detector
for Belle2 (KEK, Japan)
total area: 0.014 m^2



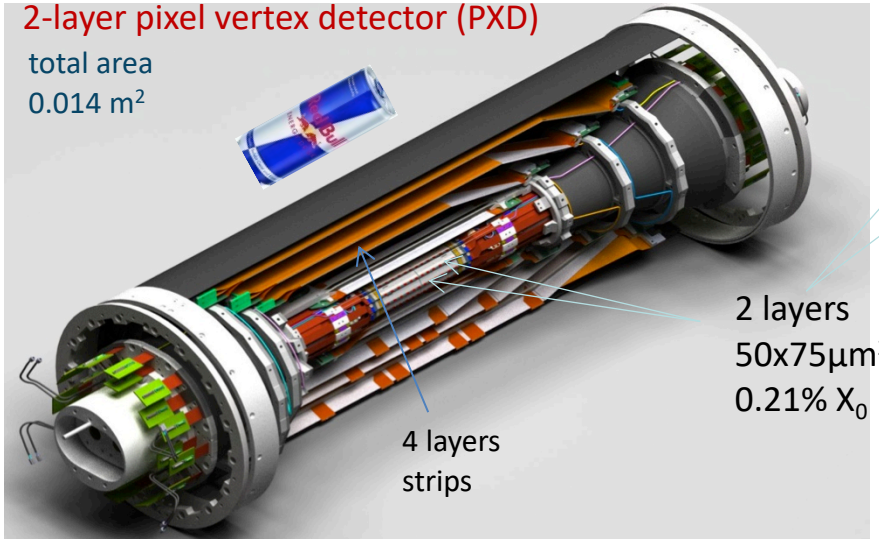


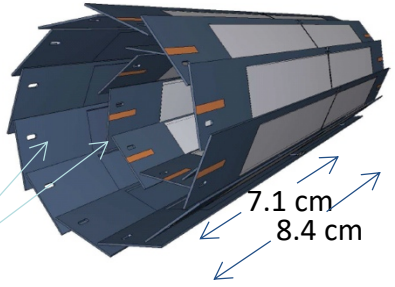
BELLE II DEPFET Pixel Detector

UNIVERSITÄT BONN

2-layer pixel vertex detector (PXD)

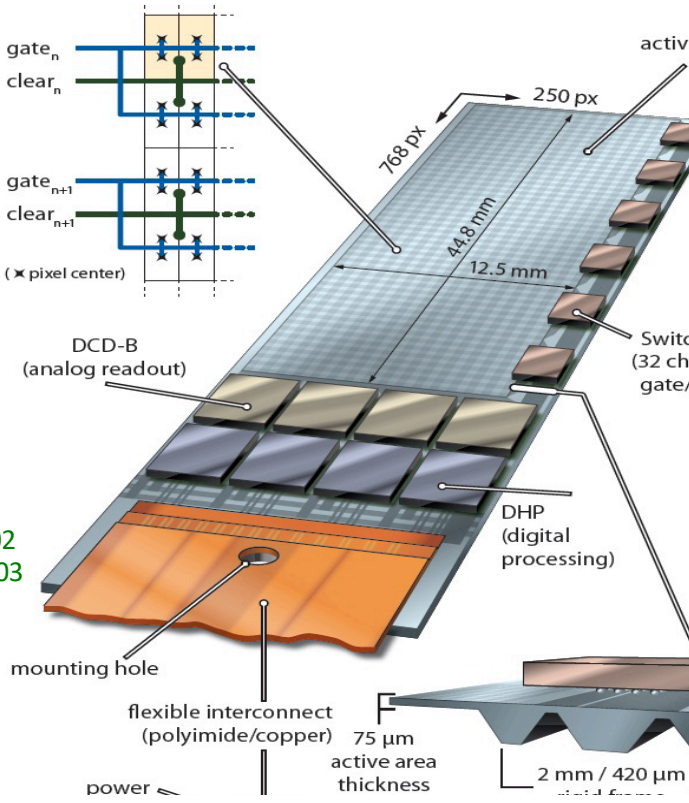
total area
0.014 m^2

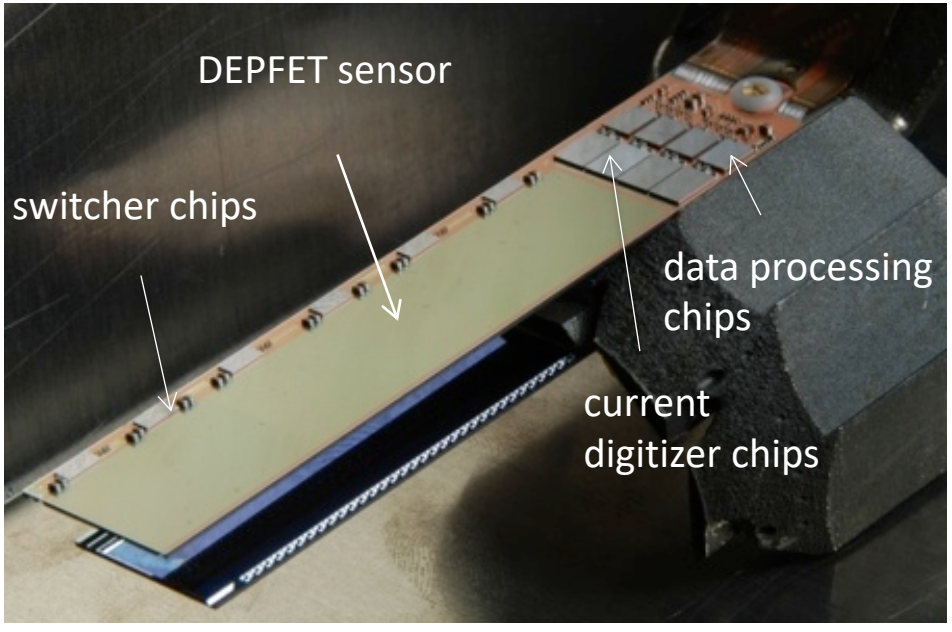


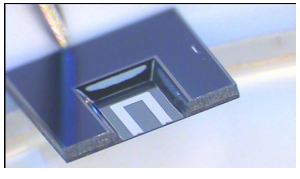


high spatial resolution

C. Marinas et al., JINST 10 (2015) 11, C11002
C. Kiesling et al., PoS EPS-HEP2011 (2011) 203







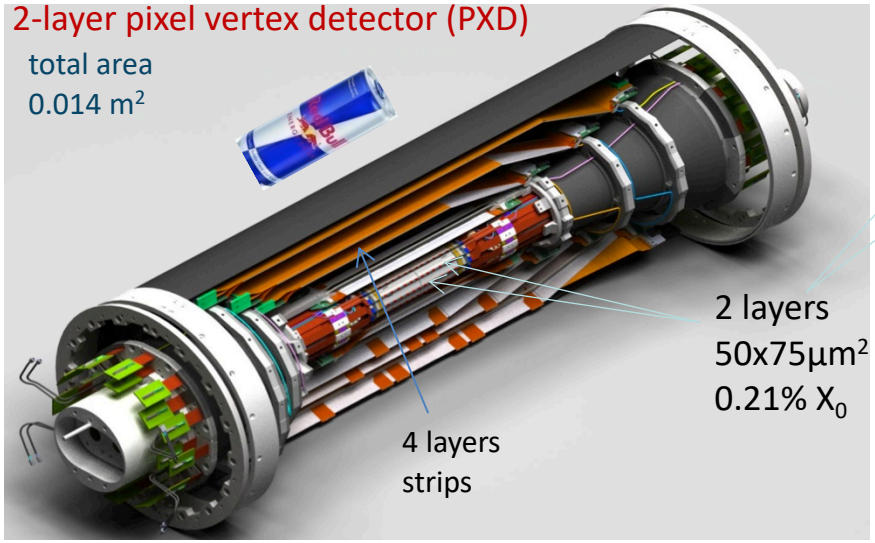
L. Andricek,
IEEE Trans.Nucl.Sci. 51 (2004) 1117-1120

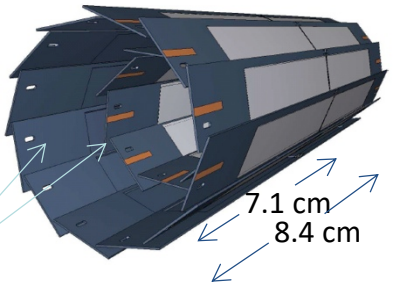
BELLE II DEPFET Pixel Detector

UNIVERSITÄT BONN

2-layer pixel vertex detector (PXD)

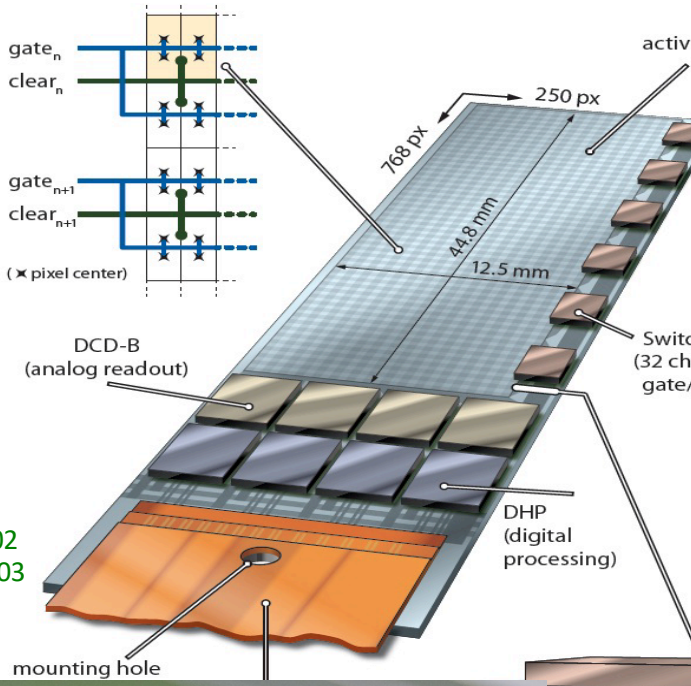
total area
0.014 m^2

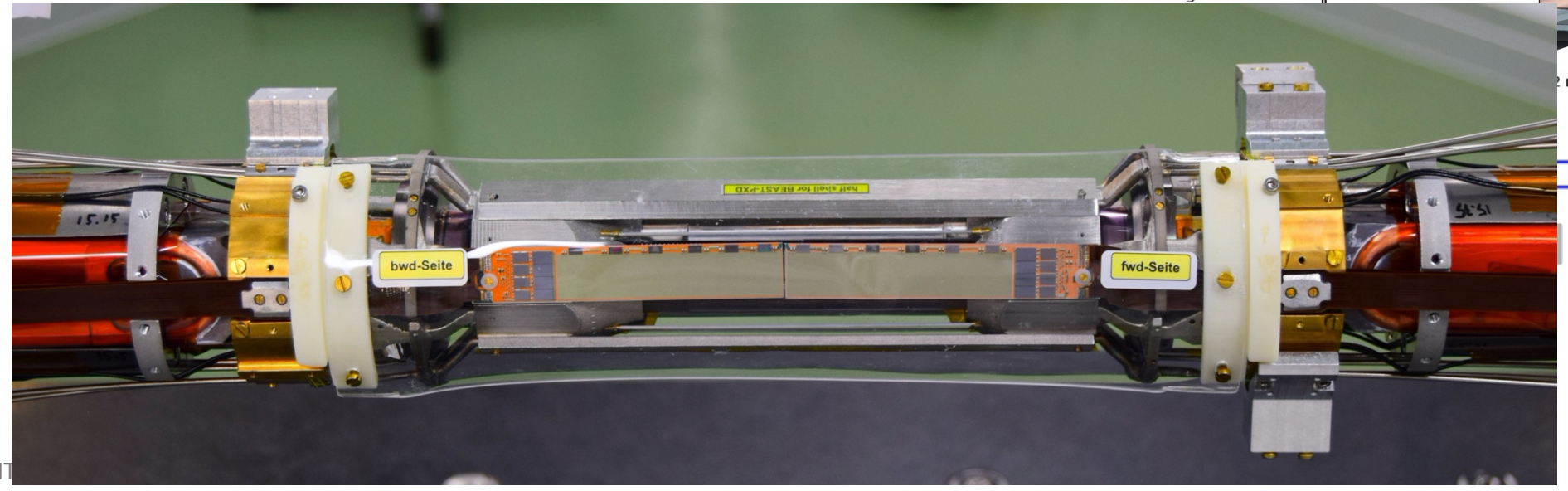


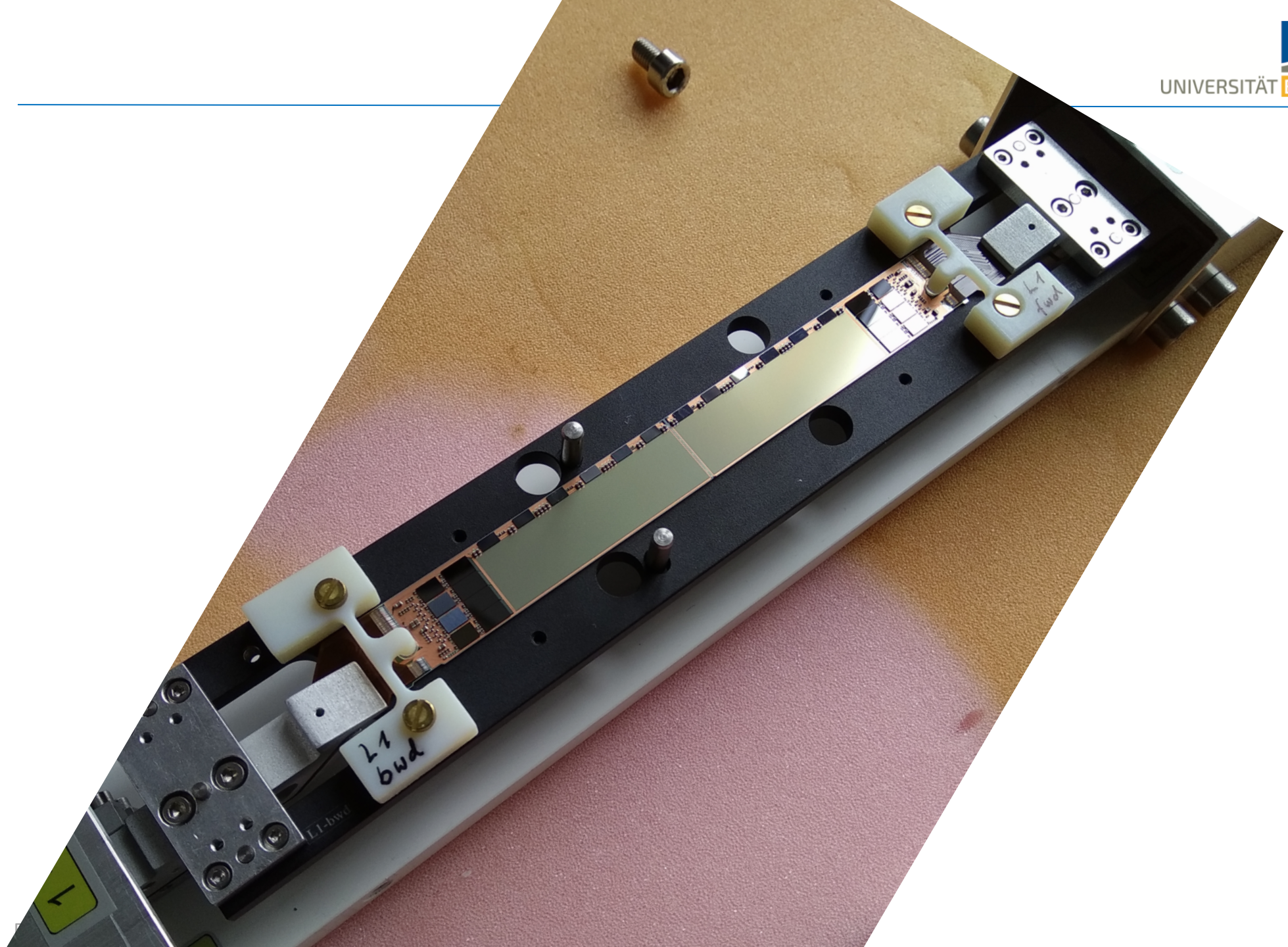


high spatial resolution

C. Marinas et al., JINST 10 (2015) 11, C11002
C. Kiesling et al., PoS EPS-HEP2011 (2011) 203

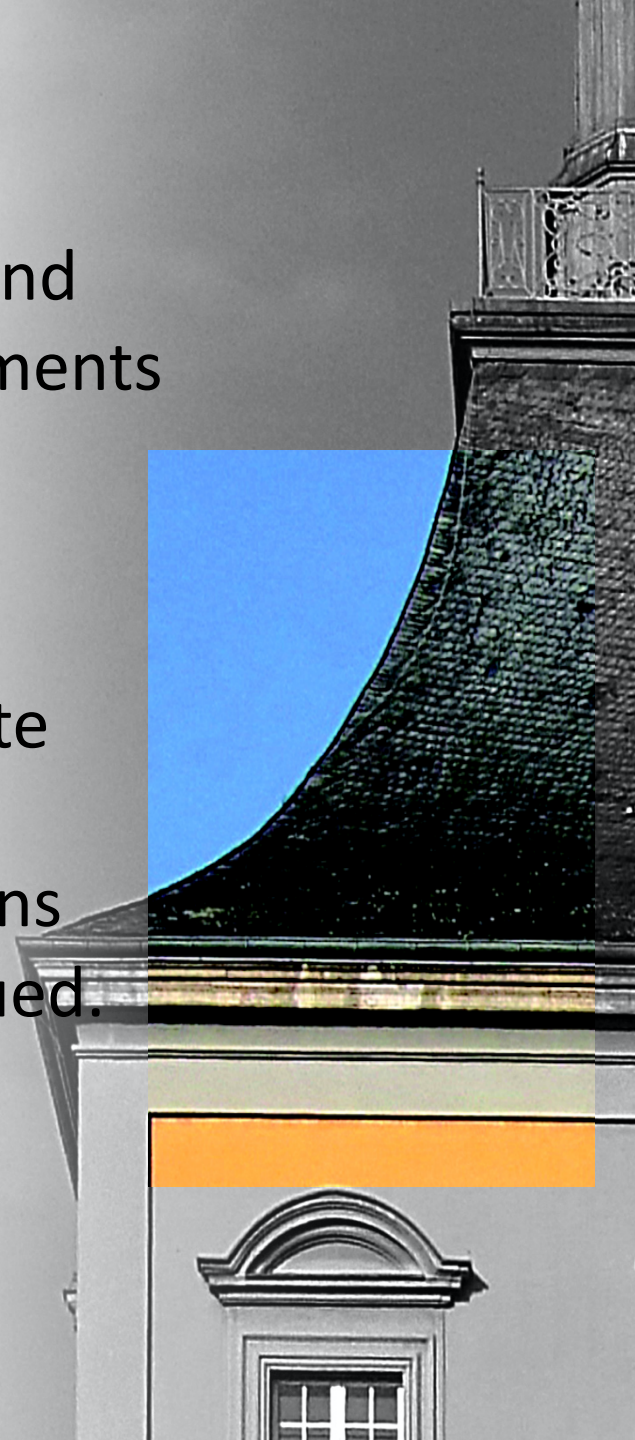




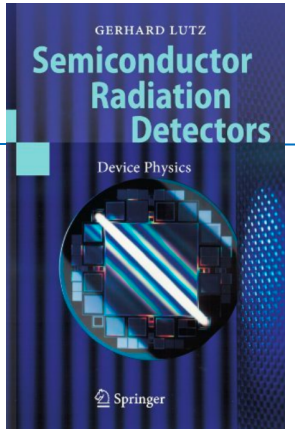

L1 bwd
L1 fwd
L1-bwd

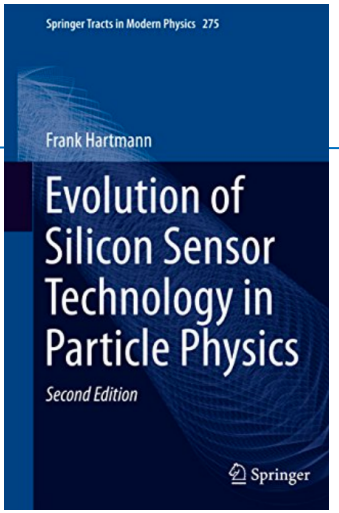
CONCLUSIONS/MESSAGES

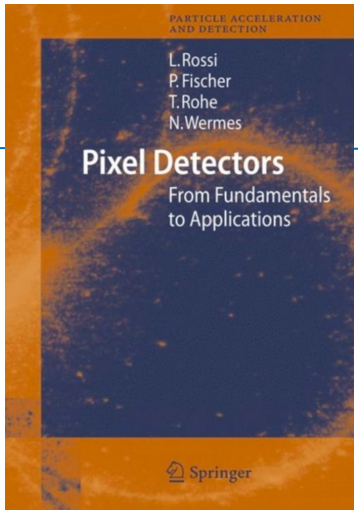
- Pixel detectors are essential for vertexing and tracking in high rate and radiation environments
- Hybrid pixels are meanwhile matured, but have also many disadvantages (…)
- DEPFETs
- MAPS are the choice for low to medium rate and radiation experiments and DMAPS point to the future also in harsher conditions
- Large & small electrode concepts are pursued.



Further Reading







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- Rossi, Fischer, Rohe, Wermes, "Pixel Detectors: From Fundamentals to Applications", Springer Berlin-Heidelberg-New York, 2006, (ISBN 3-540-283324)

- F. Hartmann, "Evolution of Silicon Sensor Technology in Particle Physics", Springer 2017

- M. Garcia-Sciveres and N. Wermes, "Review of advances in pixel detectors for experiments with high rate and radiation" Rept.Prog.Phys. 81 (2018) no.6, 066101 DOI: 10.1088/1361-6633/aab064

- Kolanoski, H. und Wermes, N. Teilchendetektoren – Grundlagen und Anwendungen (Springer/Spektrum 2016)

- **Kolanoski, H. and Wermes, N. (new edition) Particle Detectors – fundamentals and applications (Oxford University Press 2020, in print)**