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IRIO-OpenCL: Simplified development and integration of DAQ and processing systems using OpenCL for IntelFPGA devices

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Many frameworks exist to ease the integration of FPGA based systems into the Instrumentation & Control systems that are required on Big Science facilities. We present a new approach, using the heterogeneous programming language OpenCL to design and develop acquisition and processing applications. This approach reduces the usage of HDL languages significantly to describe the hardware on the FPGA, shortens the development cycle for compliant COTS solutions, and is well suited for the heterogeneous environment that is often found on Big Science experiments.

The work presented here is a set of methods and tools that allow developing applications for FPGA-based instruments in a standardised way. The framework comprises elements such as: an OpenCL compliant Board Support Package with a PCIe interface; an OpenCL IO channel to communicate with high-speed AD/DA converters using the JESD204B standard; a set of OpenCL Kernels to support common DAQ functionality, capable of acquiring and processing at high sampling rates; and a standardized software interface, including the ITER Nominal device Support (NDSv3) software layer that integrates the whole solution with EPICS.

On the hardware side, the system has been implemented in an MTCA chassis with a carrier hub, which provides an optical PCIe (gen3) interface, connected to the host computer. The Advanced Mezzanine Card (AMC) module is the N.A.T Advanced Mezzanine Card NAMC-Arria10-FMC . This board mounts an IntelFPGA ARRIA10-SoC and includes an FMC (FPGA Mezzanine Card) connector where the Analog Devices AD-DAQ2FMC-EBZ module providing two 1GS/s ADC channels together with two 1GS/s DAC channels.

An example use case for data acquisition and processing system was implemented to estimate the e the average neutron flux emitted by the plasma in a fusion experiment. The DAQ system digitises the pulses produced by the neutrons in the fission chamber and, applies hardware signal processing algorithms to estimate the neutron flux: Pulse Counting, Campbelling, and Current counting. All the high-performance tasks of acquiring and processing involved in the algorithms are carried out by OpenCL Kernels, which, as a result of the compilation process, are implemented in hardware that is deployed in the FPGA.

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