(physics) e^+e^- tracking system

LUXE workshop, April 2019 @ DESY

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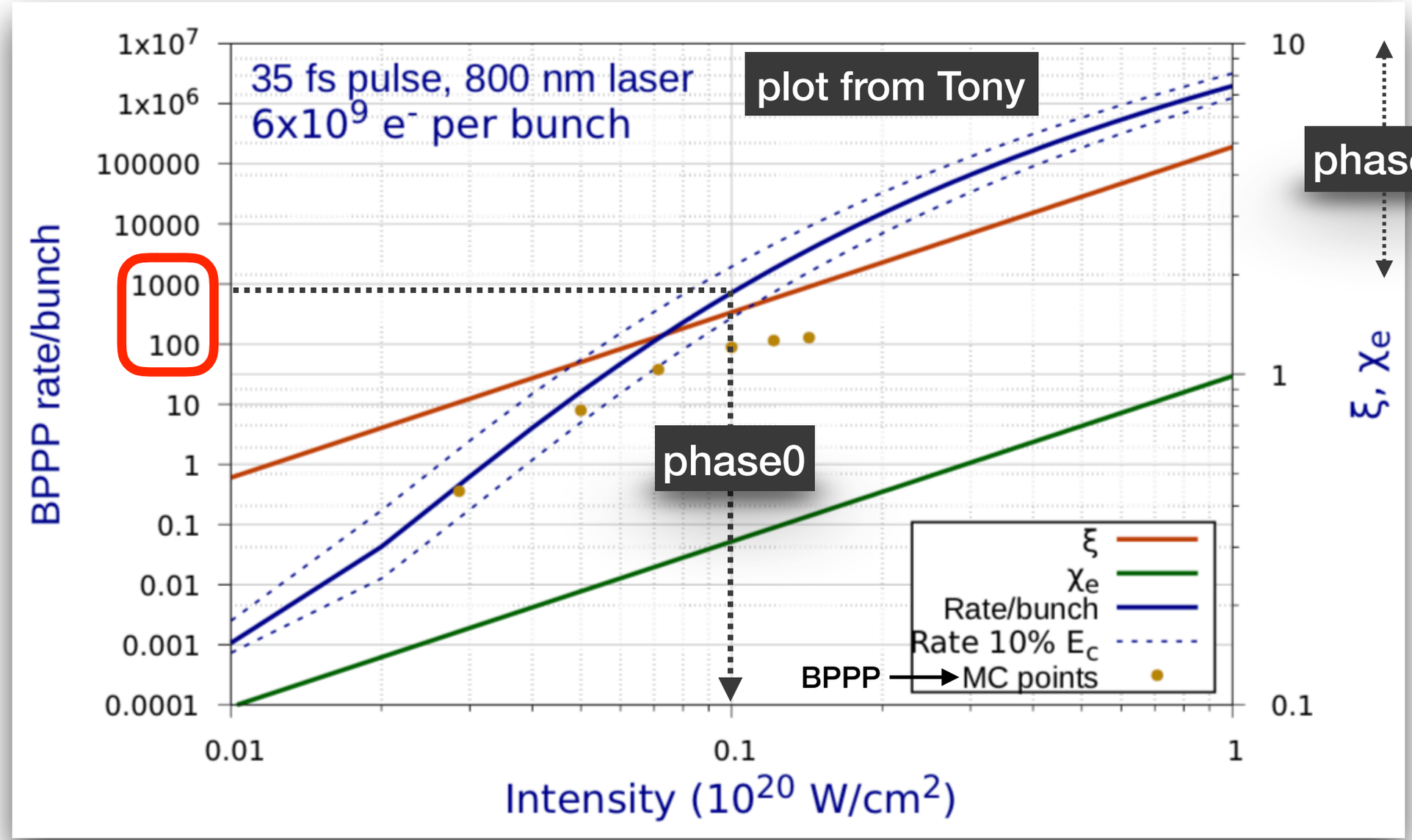
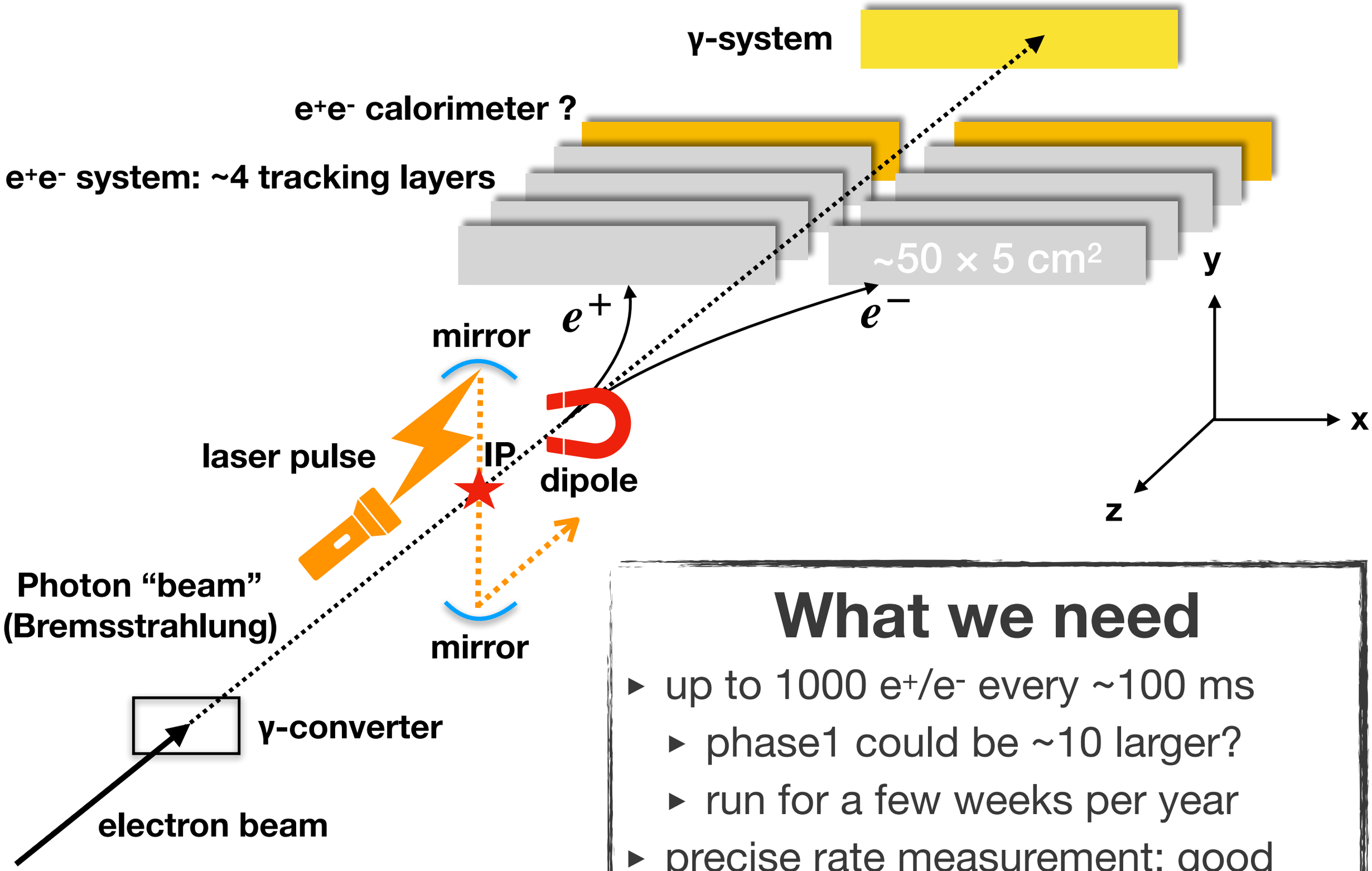
WEIZMANN INSTITUTE OF SCIENCE

BPPP @ LUXE



- Phase0: 100-1000* e^+e^- pairs/pulse/bunch (BPPP, more in phase1)
- Use only 1 bunch out of 2700 bunches from the train
- Laser pulse frequency is 1-10 Hz ⟶ ~100 ms “window” to recover



What we need

- up to 1000 e^+/e^- every ~100 ms
  - phase1 could be ~10 larger?
  - run for a few weeks per year
- precise rate measurement: good position and timing resolution
- rad-hardness isn't a limiting factor

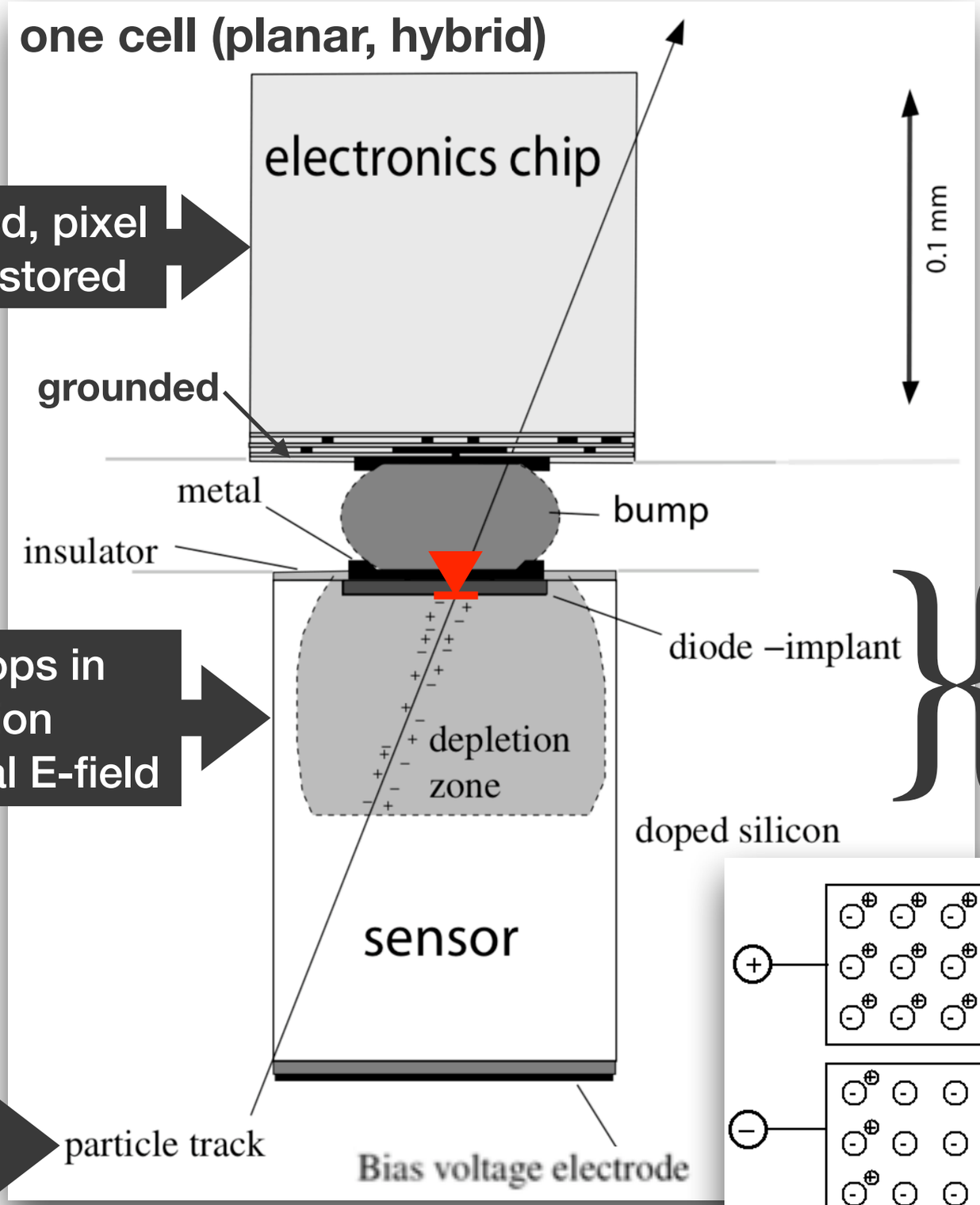
Main questions

- Resolutions?
  - space (electrode size & pitch)
  - timing (charge collection)
  - energy (from track angle and *B*-field)
- Vertex reconstruction?
  - e^+e^- correlation in OPPP?
- Trigger? (synced with beam & laser)
- Area to cover? …#channels
- Material budget?
- Which technology?
  - also dictate DAQ

- I will talk about pixels
  - a bit about technologies
  - some recent examples
- cannot possibly cover everything

Pixels

Pixel in a nutshell

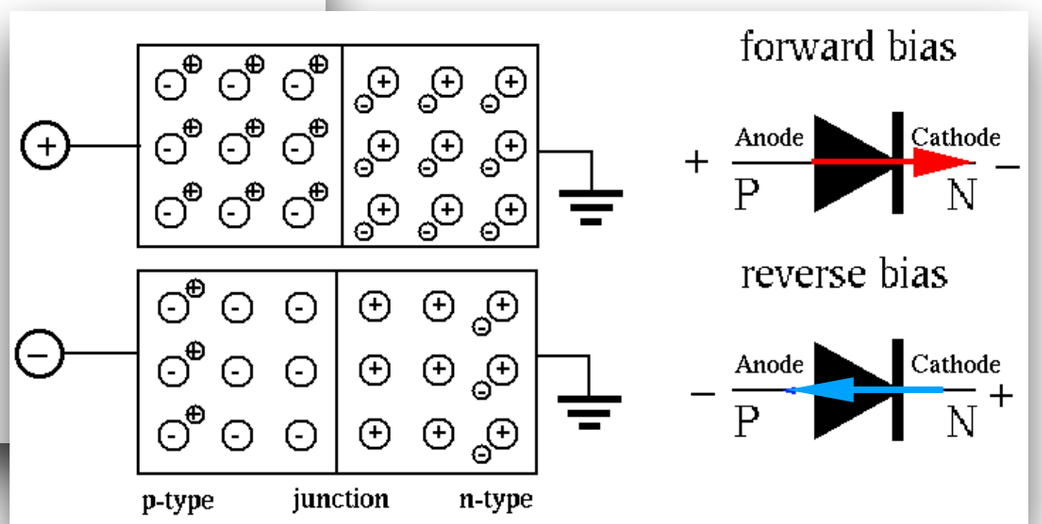


3 signal is amplified, pixel is identified and stored

2 drift signal develops in the depletion region under the external E-field

Thickness of sensitive part depends on the bias voltage and on the sensor parameters

1 ionising particle traversing



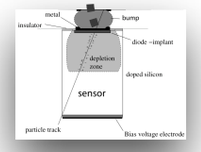
Analog FE in a nutshell

Low bandwidth feedback:
compensate for sensor DC leakage current
which can be significant after irradiation

Continuous reset

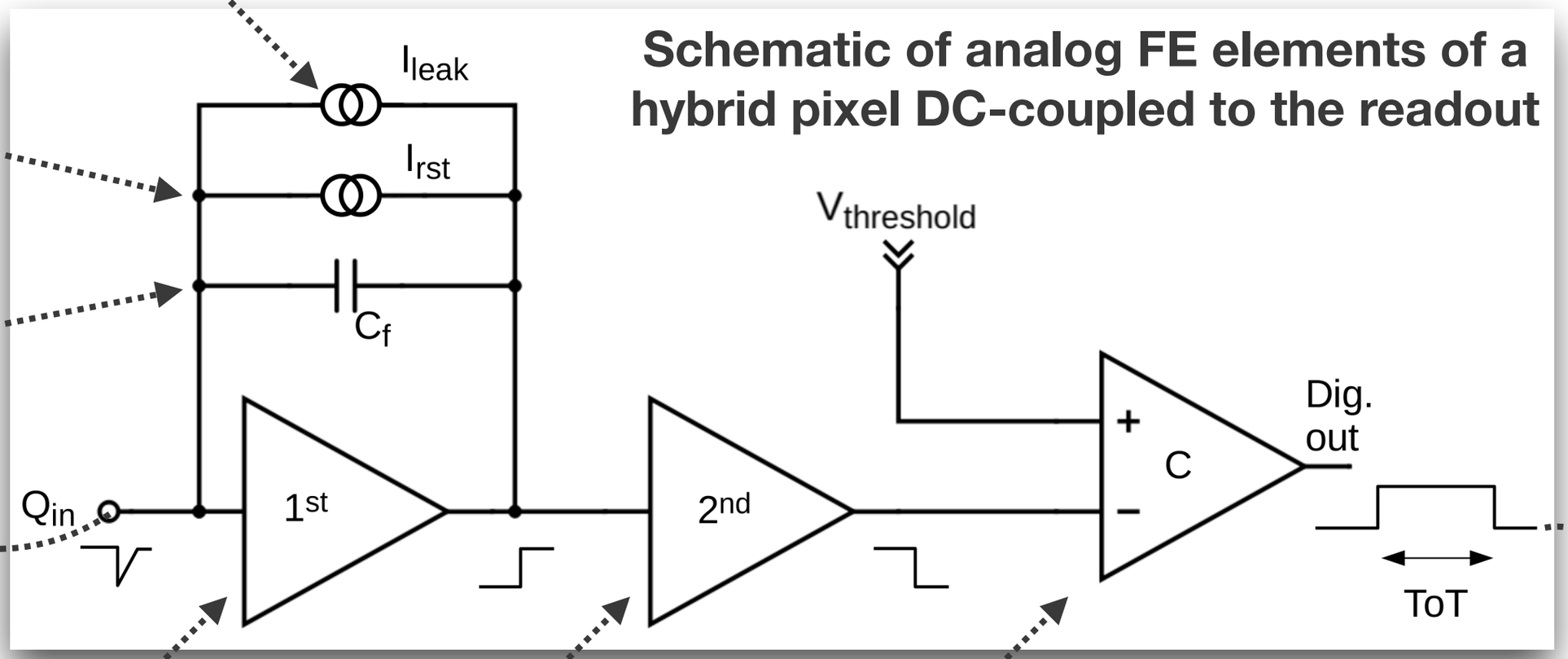
Capacitive feedback
(high gain = small C_f)

signal



pixel
sensor only

Schematic of analog FE elements of a hybrid pixel DC-coupled to the readout



Charge Sensitive Amplifier (CSA)

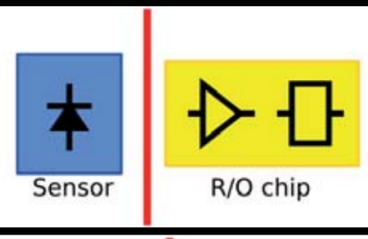
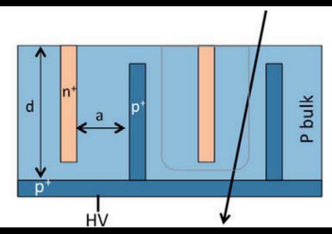
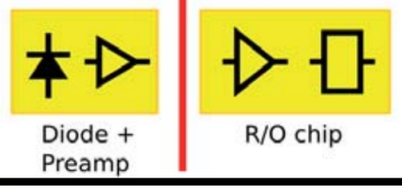
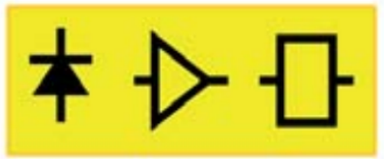
Voltage gain

Comparator (C): pulse height discrimination

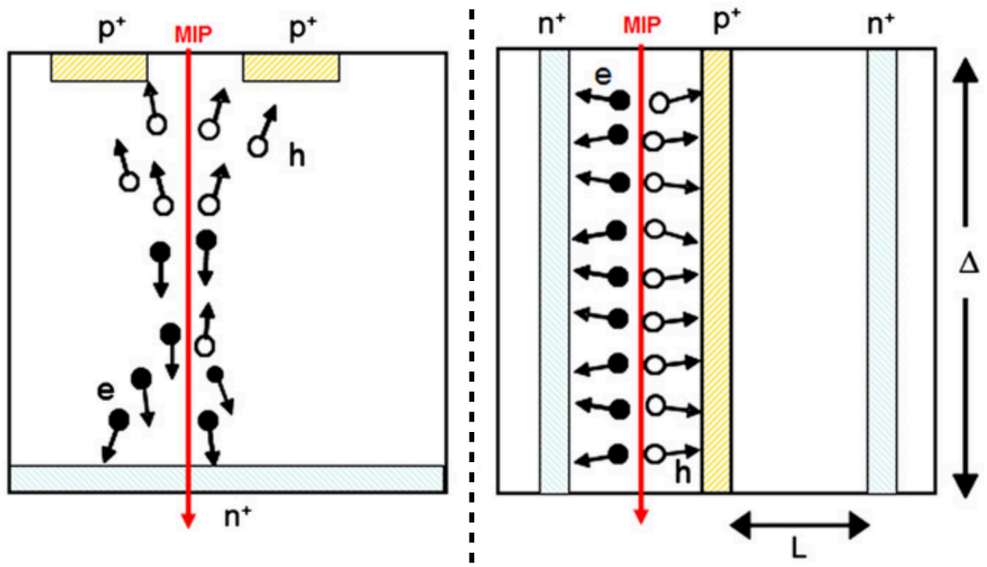
ToT digitisation:
count clock cycles
while the **comparator**
is above threshold

Technologies

- Sensitive for relativistic charged particles and keV-MeV photons (converted in the medium)
- Excellent spacetime resolution
- Vastly used by HEP experiments

	Planar	3D
Passive Hybrid		
Active Hybrid		?
Monolithic Active		Not yet

- n-in-p type (n-type pixel) cost-efficient 6” and 8” wafer single sided processing technologies
- CMOS vendors more open to small markets

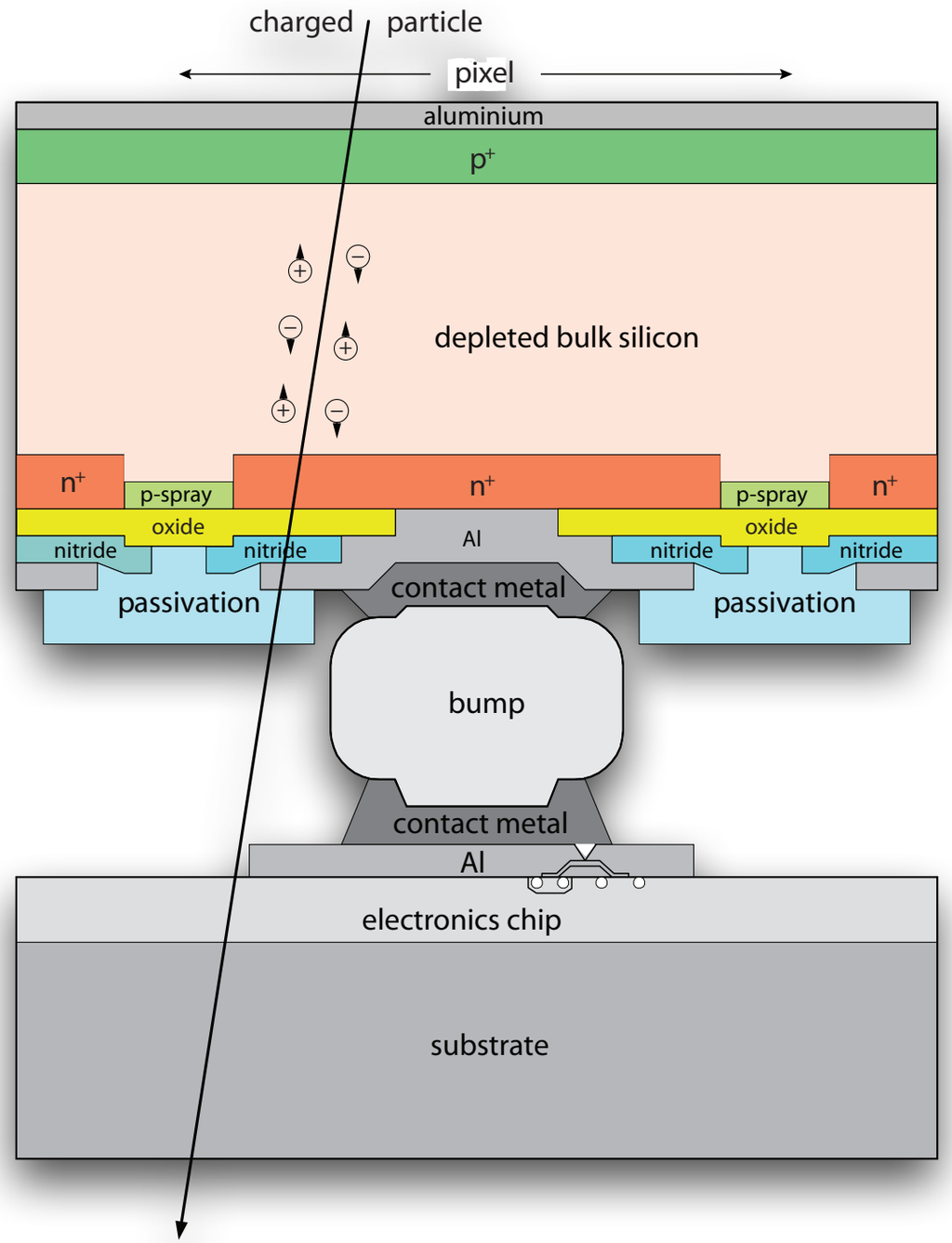


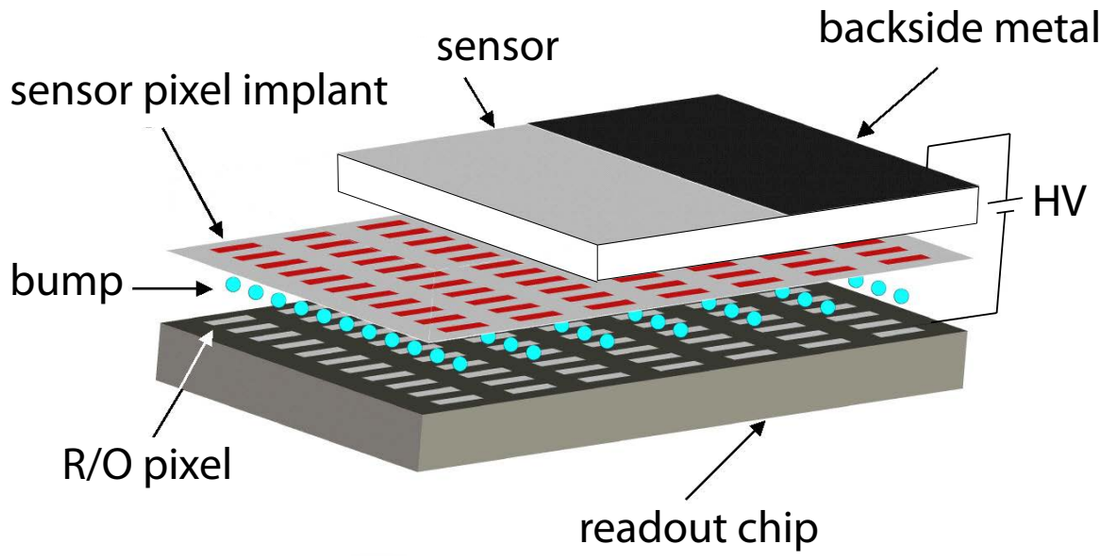
Collection path	200–300 μm	~50 μm
Depletion voltage	30–100 V	< 10 V
Charge collection time	Tens of ns	~ns

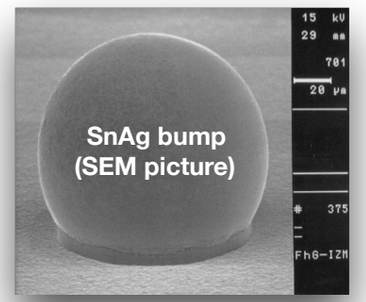
Planar/3D

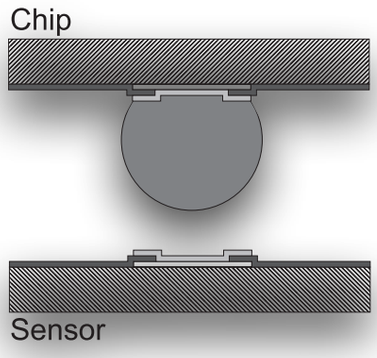
Hybrid

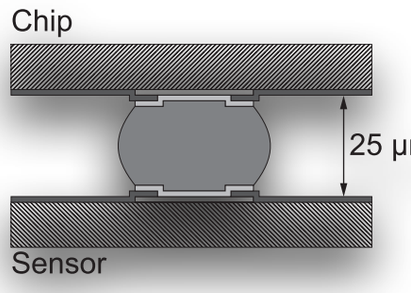
Planar Hybrid Pixels











- Common SS technology for HEP experiments
- Rad-hardness: silicon with increased oxygen content + operation at low temperatures
- Relatively large material budget, typically >1.5%X_0 per layer (with cooling, support, etc)
- Bump-bonding and flip-chipping is complex

"…the trend in hybrid pixel module development goes to large readout chips and thin sensors, preferentially using p-type bulk material, all being beneficial for cost, radiation tolerance, and detector mass, while the handling and hybridisation demands increase." [Rept. Prog. Phys. 81 (2018) no.6, 066101]

Radiation impact

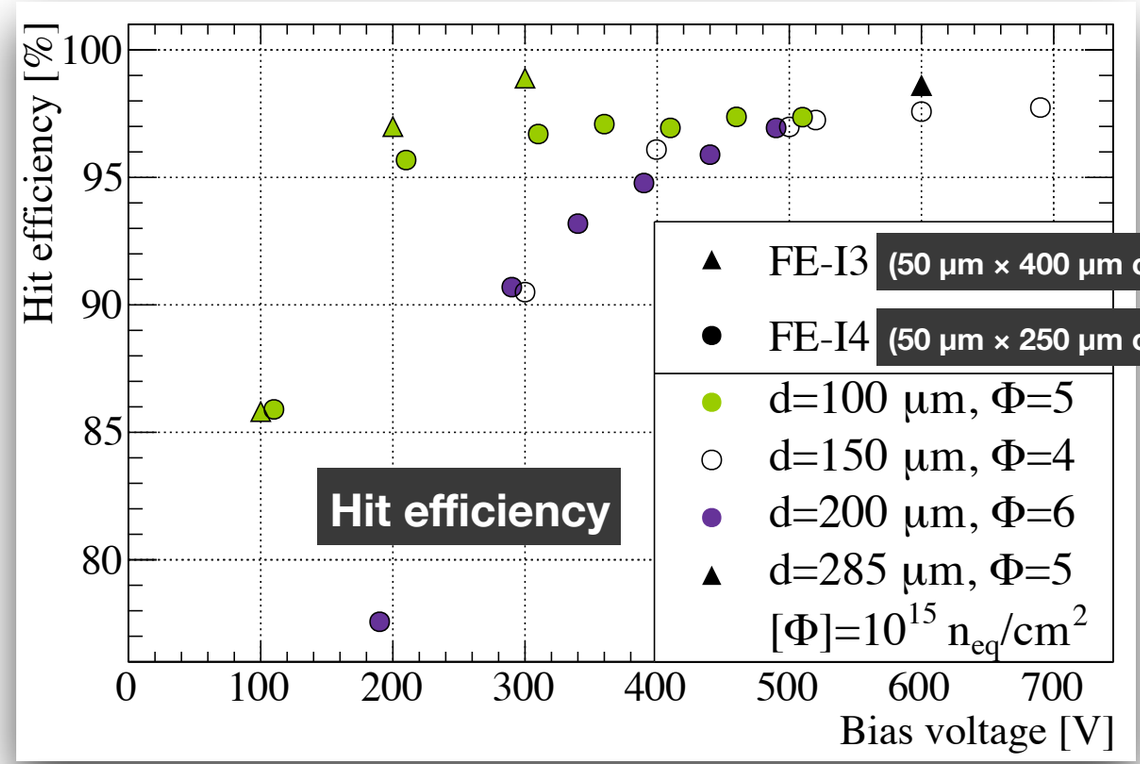
For planar hybrid pixels

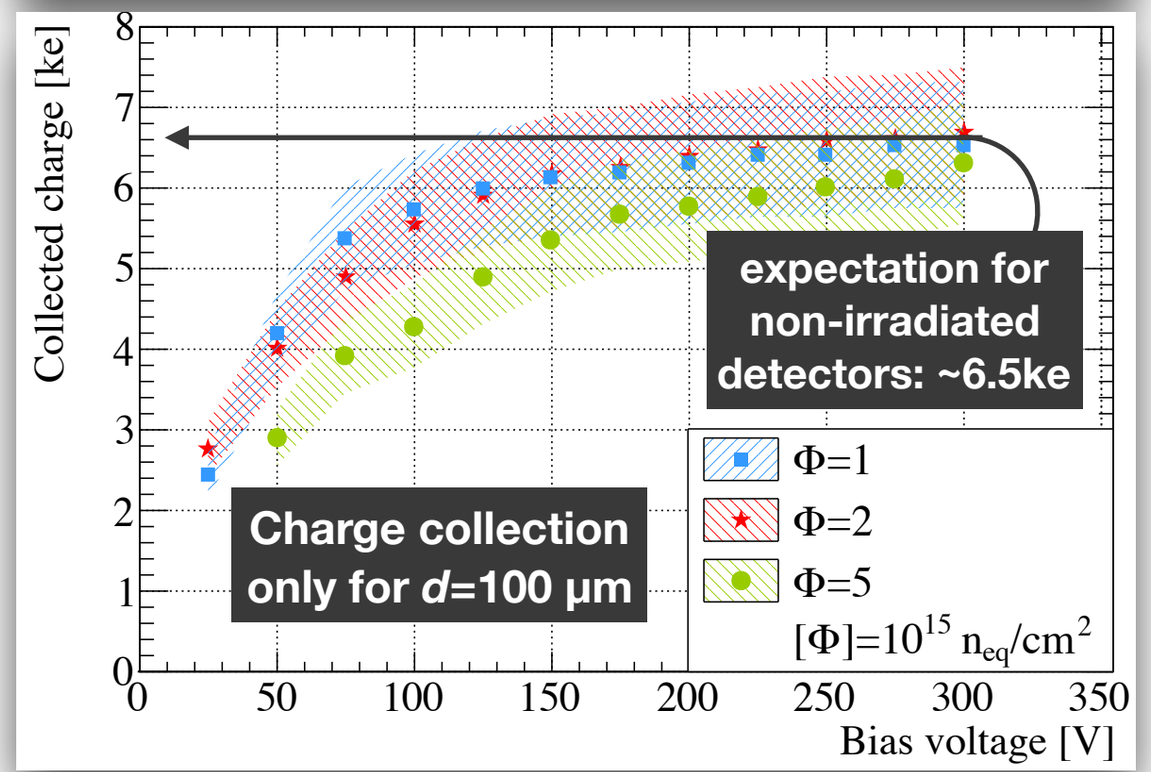
- Dose measured in neutron-equivalent exposure per unit area: n_{eq}/cm^2

- High hit efficiencies after irradiation
  - for thinner sensors and/or
  - for higher bias voltages (>500 V)

- Charge collection saturates with voltage only for thin sensors (100 μm)
  - expect ~6500 e for non-irradiated
  - no saturation for thicker sensors

- FE-I4 chip developed for the ATLAS IBL
- Modules tested with 4 GeV electrons (DESY) and 120 GeV pions (SPS)





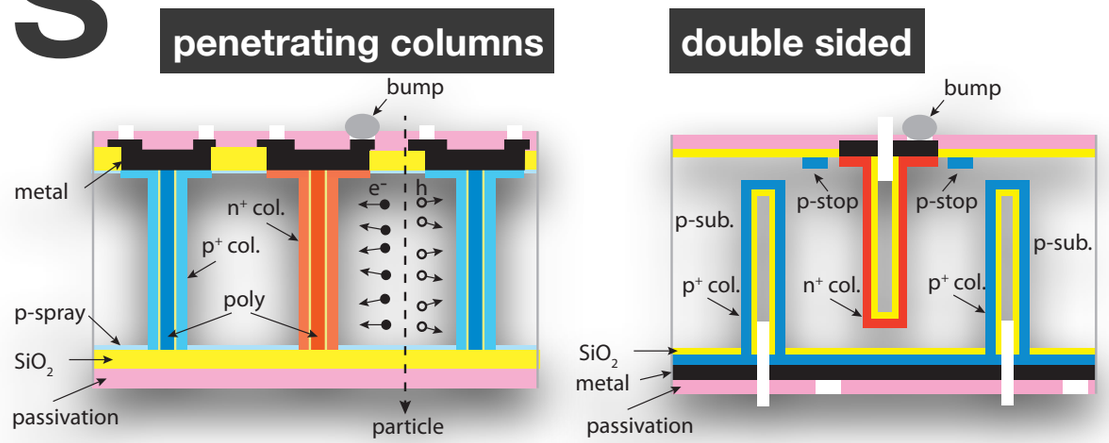
Nucl. Instrum. Meth. A831 (2016) 111-115

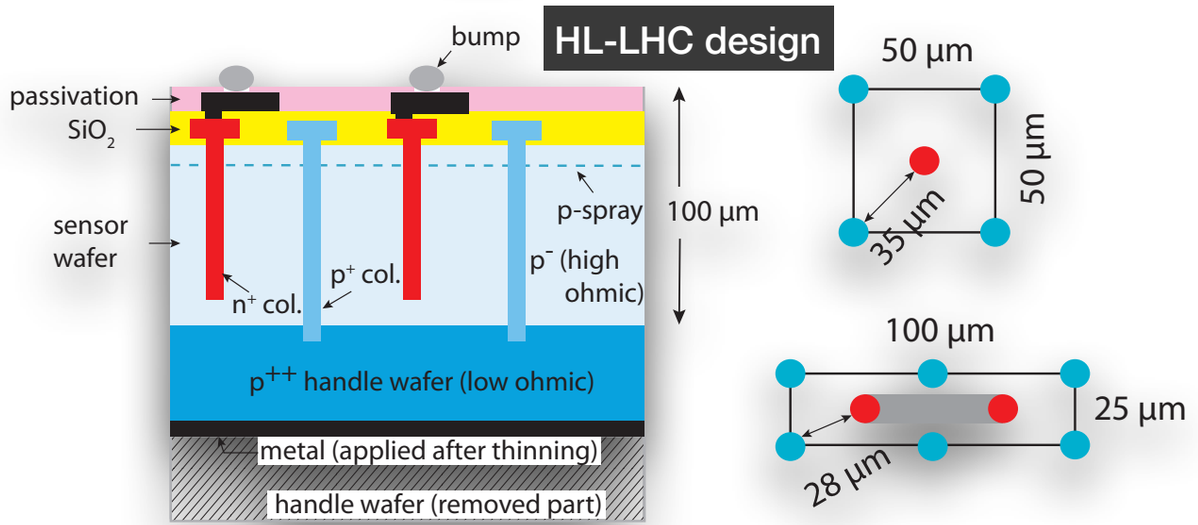
3D Hybrid Pixels

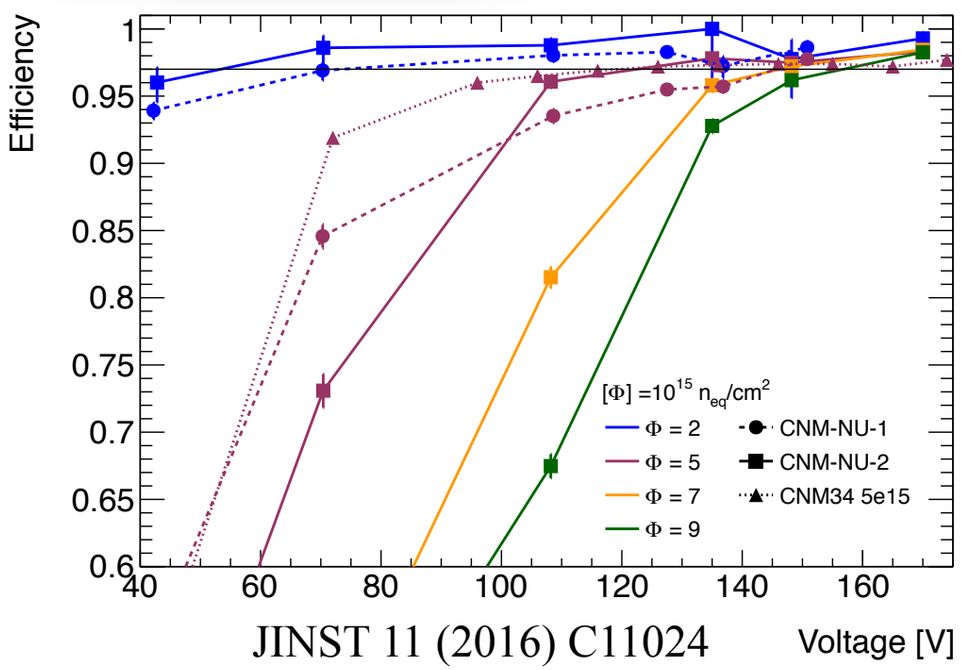
- Electrode distance smaller than the typical sensor thickness (~50 μm)
  - high drift fields for moderate voltages
  - requires less cooling
  - reduced trapping probability
    - increased radiation tolerance
  - higher capacitance (more noise)

- Small thickness (~100 μm)
  - difficult handling/hybridisation (low yield)

- ATLAS IBL pixels proven to operate well!
- HL-LHC design (~5 nm implants):
  - ~100 μm thick sensors on 6” wafers
  - very slim ~50 μm or fully active edges







JINST 11 (2016) C11024

ROICs for Hybrid Pixels

- Hybrid approach: independent optimisation of ROIC and sensor
- The defining ROIC characteristics are
  - dedicated amplification and discrimination channel per pixel (FE)
  - all the FEs should be able to operate in parallel

- Output of the FE is digitised on the pixel (on-chip digitisation)
  - allows for higher readout bandwidth
  - can also be sampled on an analog memory for later readout
  - preferred digitisation method has so far been ToT

	1^{st} **gen.**	2^{nd} **gen.**	3^{nd} **gen.**
Hit data storage density	< 1 Gb/s/cm^2	5 Gbps	40 Gb/s/cm^2
Chip output bandwidth	40-160 Mb/s	0.3-1.2 Gbps	2-20 Gb/s

mainly analog matrix, with digital operations implemented using full custom circuits. Digital processing & data buffering done in the periphery. Results in a relatively large periphery area and the need for high bandwidth data transfer from pixels to periphery

synthesised logic within the pixel matrix, enabled by higher logic density. Matrix became a mix of analog columns and digital columns synthesised with digital design tools. Digital processing and storage in the columns meant the periphery area could shrink and the hit rate capability increased

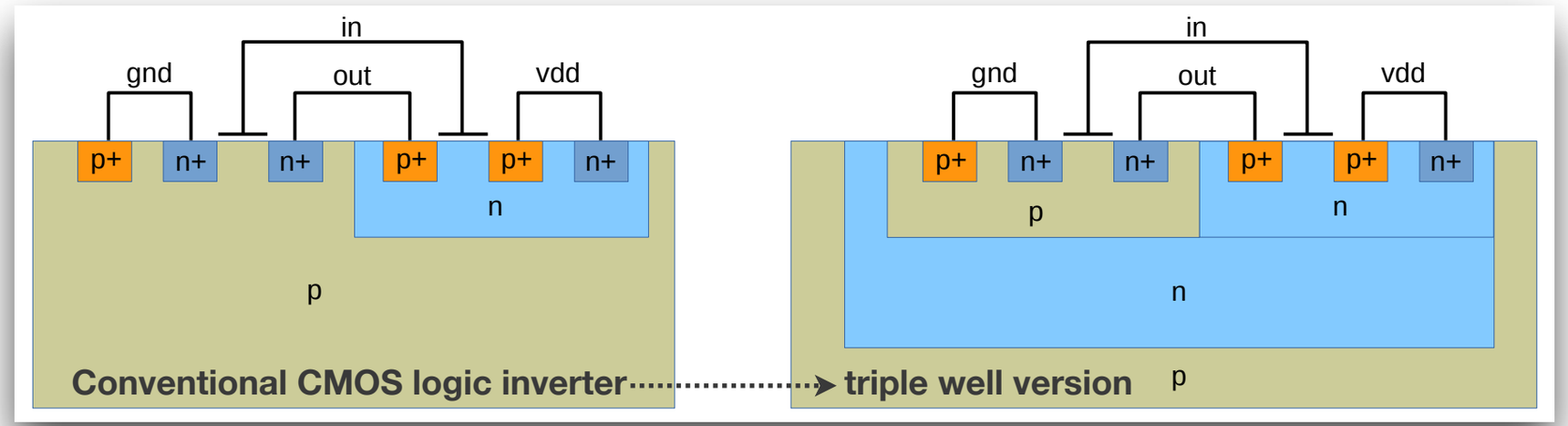
essentially digital, with embedded analog amplifiers kept to a minimum and logic complexity rivalling commercial microprocessors

ROICs isolation

- Key element of fully digital chips is isolation of circuits within the same chip
  - digital switching produces current spikes
  - currents induced in the Si inject parasitic signals into the analog circuits
  - even if analog and digital circuits use different power supplies/grounds

- Mitigated by isolating circuits from the bulk substrate
  - strongly attenuates noise coupling but does not eliminate it completely
- Designs vary between isolating only analog circuits, only digital circuits, or both from the true bulk substrate

The CMOS ROIC alone

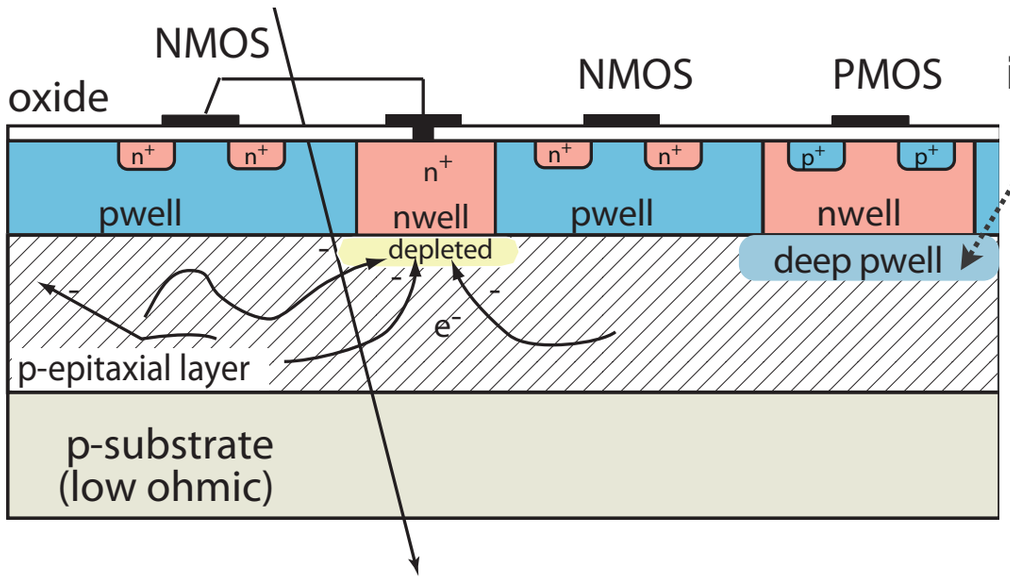


NMOS device and the local gnd are isolated from the substrate

Monolithic

Active

Monolithic Active Pixel Sensors



Conventional MAPS

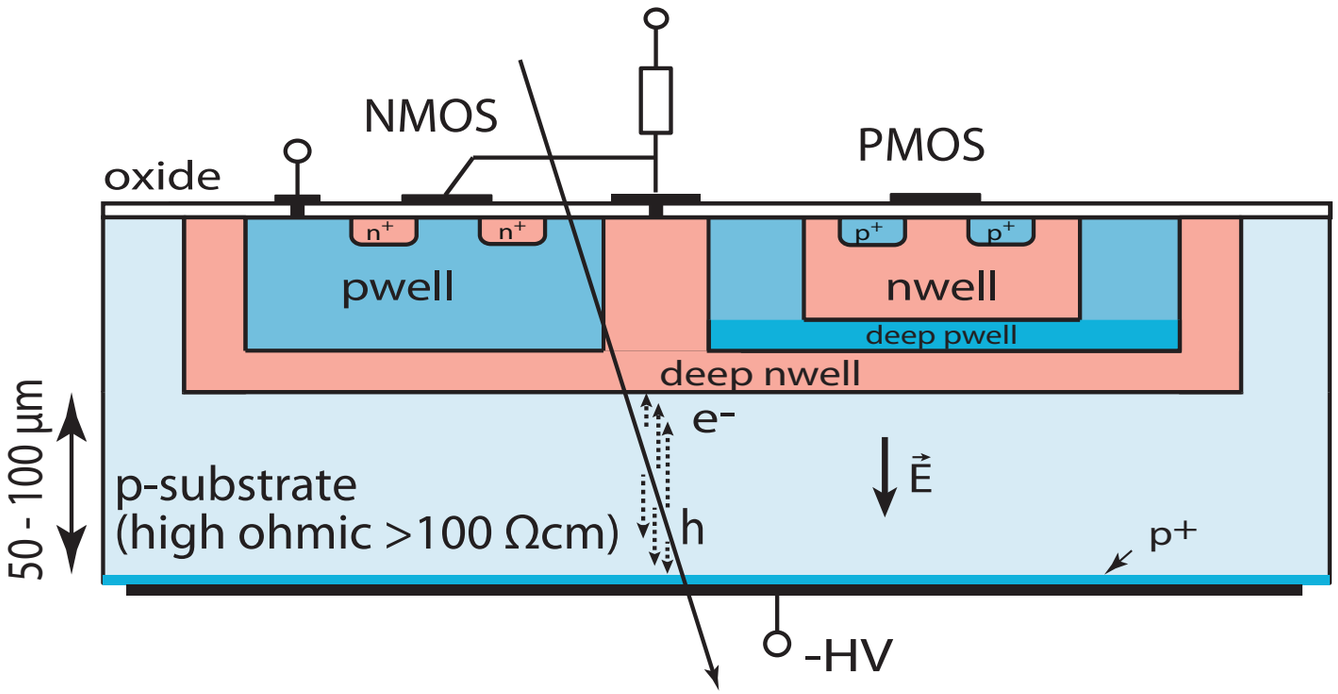
- Conventional Si+CMOS readout pixel
- Requirement from particle physics, but…
- Smartphone image sensors independently evolved in this direction

- Sensing volume is a 1-20 μm **epitaxial** layer grown on a lower quality wafer hosting the CMOS circuitry
  - Charge deposited in the epilayer can reach 4000 e^- for 15 μm thickness

- Epilayer is depleted only very locally around the charge collection node
  - deposited charge is mostly collected by diffusion rather than by drift
  - signal generation slow and incomplete (not all charges arrive at the node)

- MAPS successfully implemented in “lower-than-LHC-pp” rate and low-radiation experiments, e.g. **STAR** and **ALICE inner tracking system (ITS) Upgrade**
  - **ALPIDE** (ITS) is a 1.5×3 cm^2 large MAPS with 512×1024 (row×column) 28×28 μm^2 pixels binary read out, with a resolution and a peaking time of ~5 μm ~2 μs
  - continuously active discriminating amplifier and a multiple-event memory

Monolithic Active Pixel Sensors



Depleted MAPS structure (DMAPS)

- mid to high resistivity (≲1 kΩcm)
- need sufficient bias (≳150 V)
- commercial CMOS technology with some modifications

- Charge collection via drifting rather than diffusion
- DMAPS are more rad-hard than MAPS by construction
  - avoid long collection paths (charges can be trapped after irradiation)
- R&D goal is to achieve some (50-100 µm) depletion depth ($d \sim \sqrt{\rho V}$)
  - reasonably large signal (~4000 e^-)
  - fast and in-time efficient charge collection
  - maintain full functionality: minimum interference of elx/detector signals

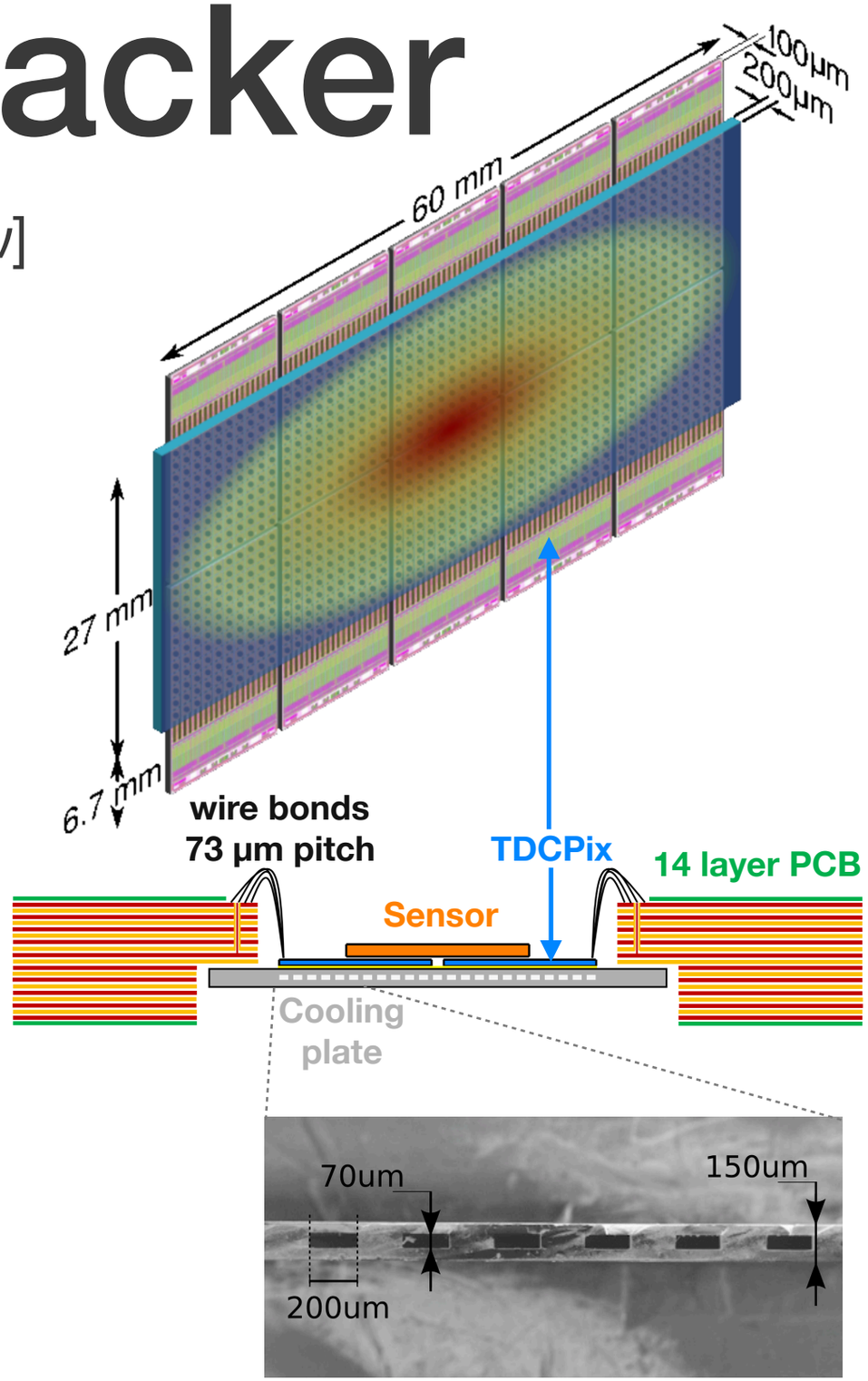
Recent Real Life Examples

NA62 Gigatracker

- Experiment set to measure the ultra rare Br[$K^+ \longrightarrow \pi^+ \nu\nu$]

- Detector has to track particles in a beam
  - with a flux reaching 1.3 MHz/mm^2
  - single-hit timing with 200 ps RMS resolution
  - for a total material budget of less than 1.5X_0

- Detector has 3 stations
  - 200 μm thick sensor, of 300×300 μm^2 pixels
  - bump bonded to a 2×5 100 μm thick ASIC (IBM)
    - read out 40×45 asynchronous pixels per chip
  - junction is fully depleted with a bias of ~60 V
  - but sensor is operated at bias voltage up to 450 V
    - charges can drift through the junction in <10 ns
  - first detector cooled with **micro-channels**

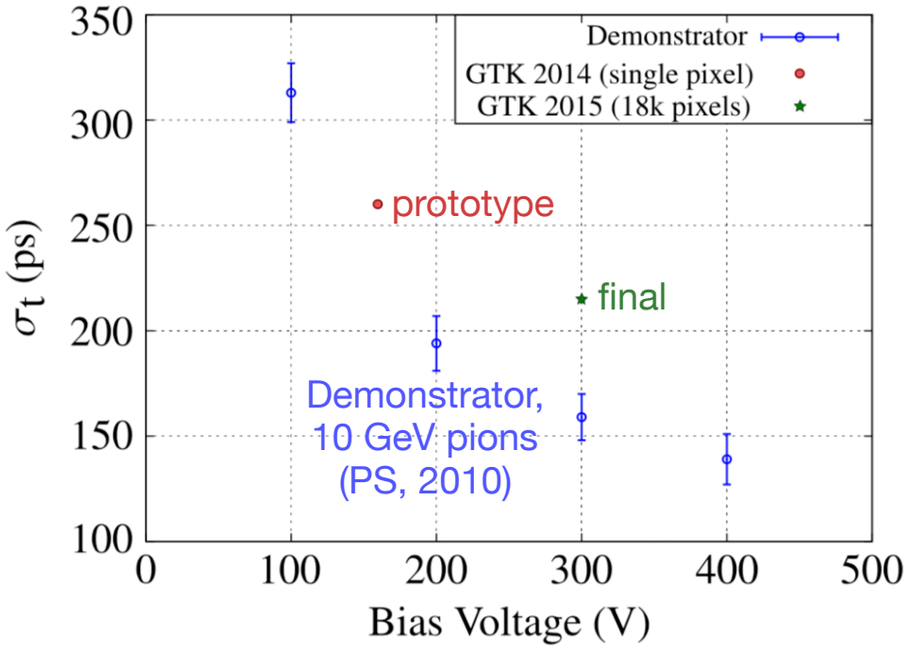


PoS (VERTEX2015) 016
Nucl. Instrum. Meth. A 845 (2017) 147-149

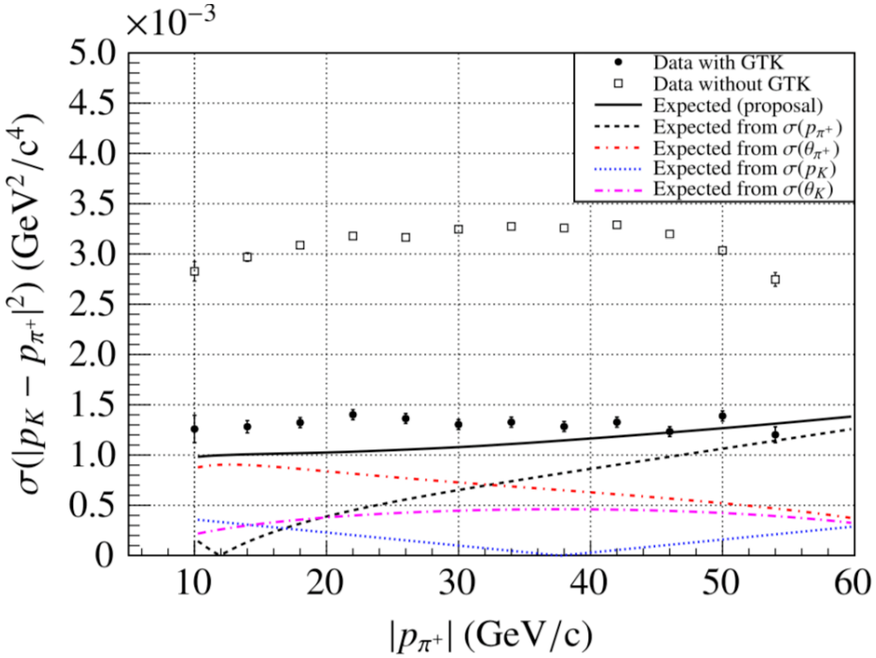
- ASIC (TDCPix) accepts both bias polarities: p-in-n, n-in-p
  - analog logic of the pixel array is separated from the digital & time-to-digital conversion (TDC) logic, sitting outside the array

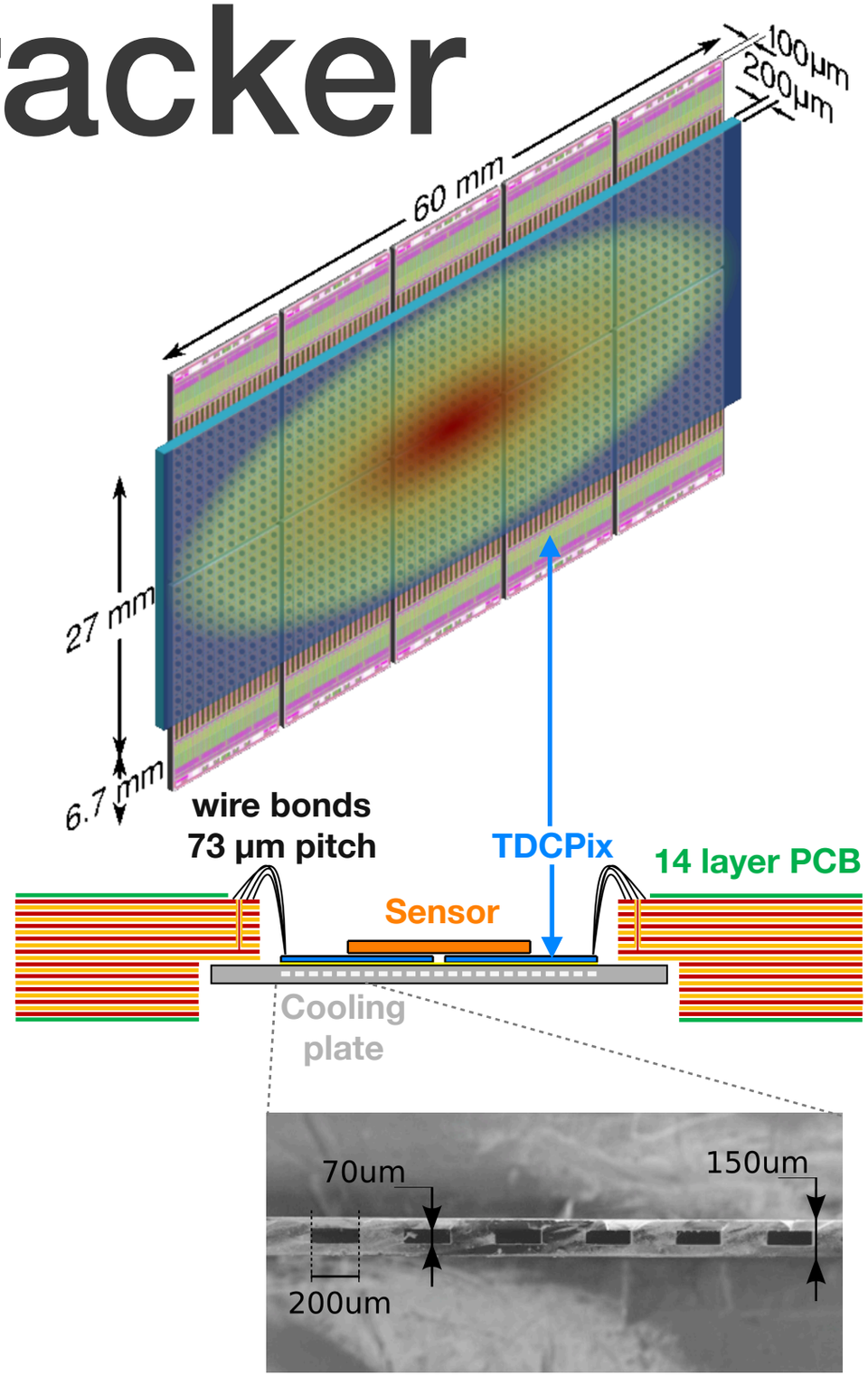
NA62 Gigatracker

Hit arrival time resolution vs the bias voltage



squared missing mass resolution vs π^+ momentum

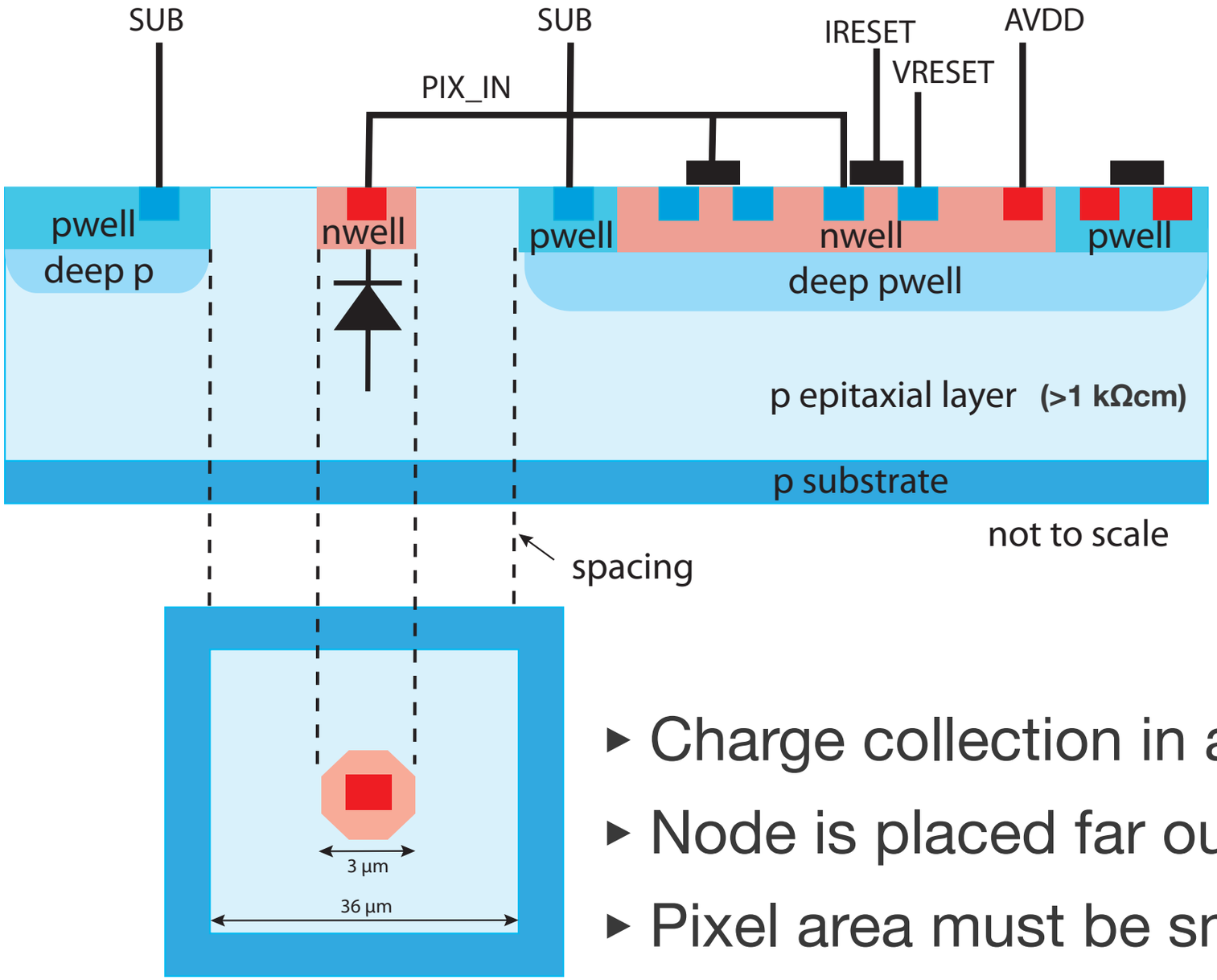




PoS (VERTEX2015) 016
Nucl. Instrum. Meth. A 845 (2017) 147-149

- Time resolution as good as 200 ps can be achieved
- First time in HEP: micro-channel cooling (material budget <0.5X_0/station)
- Measure momentum and arrival time of particles in a beam with a flux as high as 1.3 MHz/mm^2

Small fill-factor DMAPS



not to scale

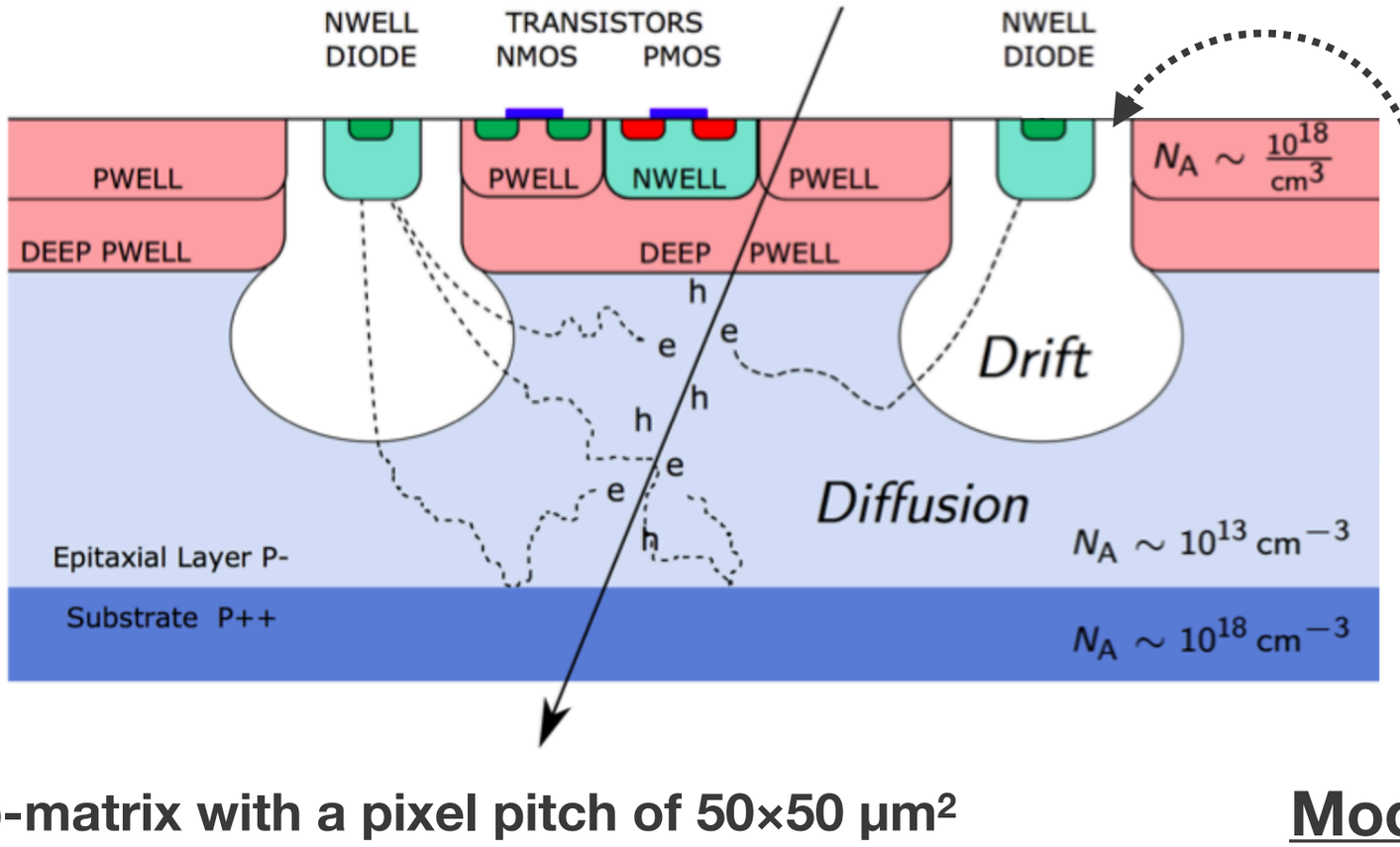
Pixel cell in a 180 nm quadruple well technology by TowerJazz:

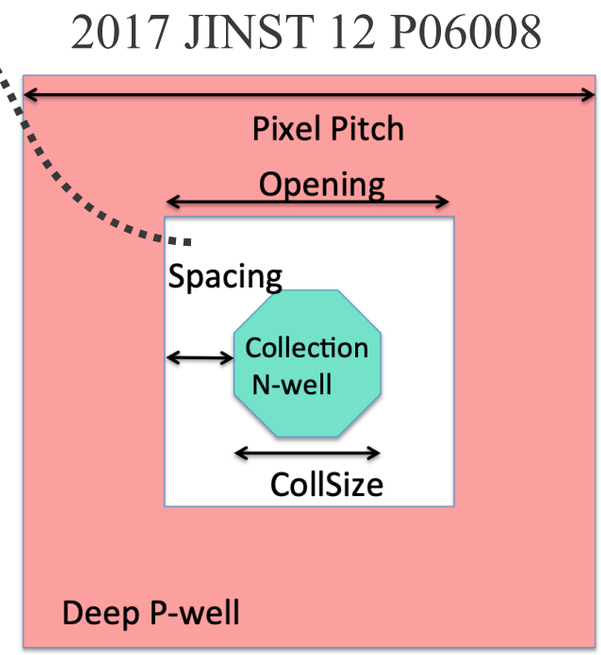
- elx is enclosed in a deep p-well
- charge is collected by a small n-well collection node

- Charge collection in a high ohmic p-epitaxial layer
- Node is placed far outside the elx area
- Pixel area must be smaller than ~40 µm
  - to limit the charge collection max path
- Capacitance is very low: 3-10 fF ⟶ low noise

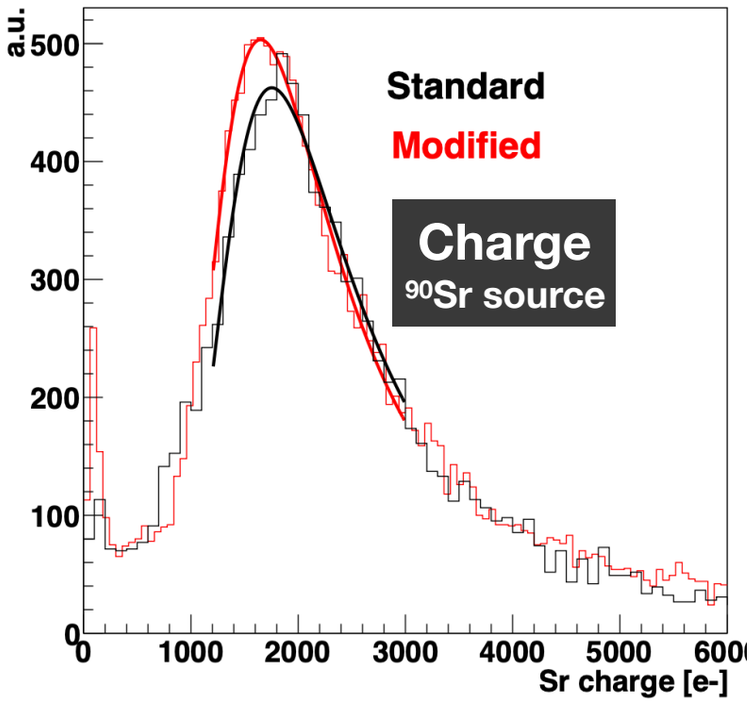
Small fill-factor DMAPS

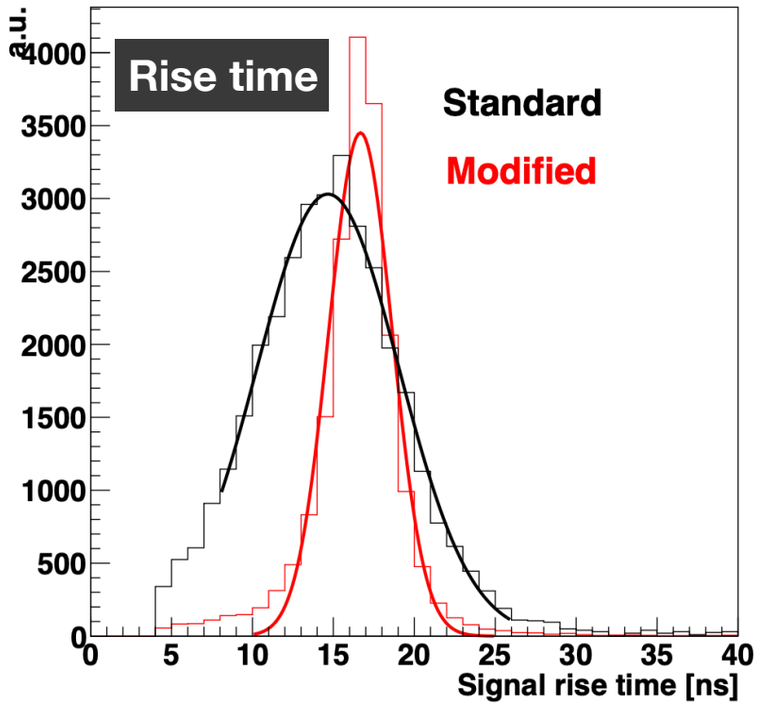
TowerJazz 180nm **standard** p-type epi Si & substrate, and n-type collection diode



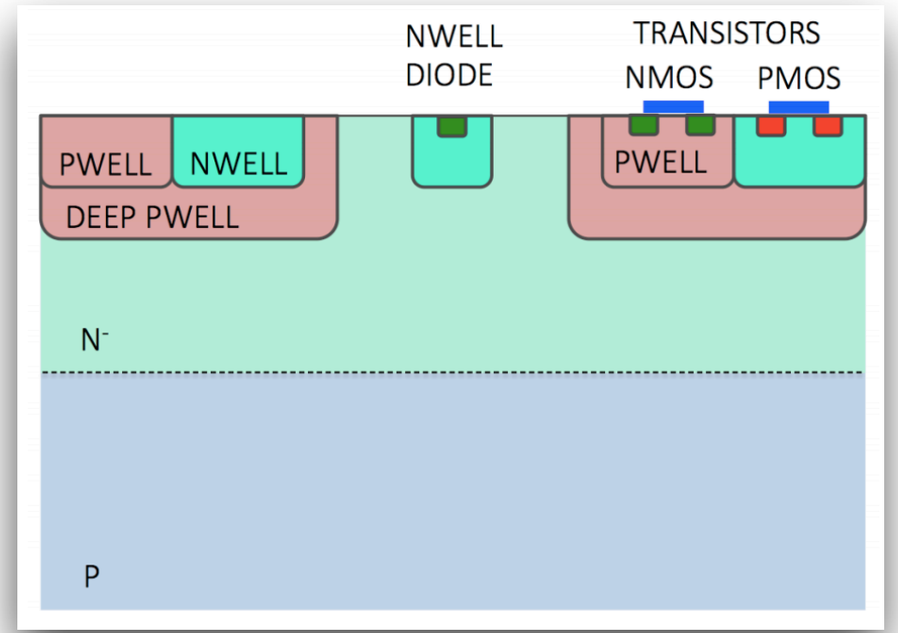


signals of the sub-matrix with a pixel pitch of 50×50 μm²





Modified TJ180 (enhanced depletion)

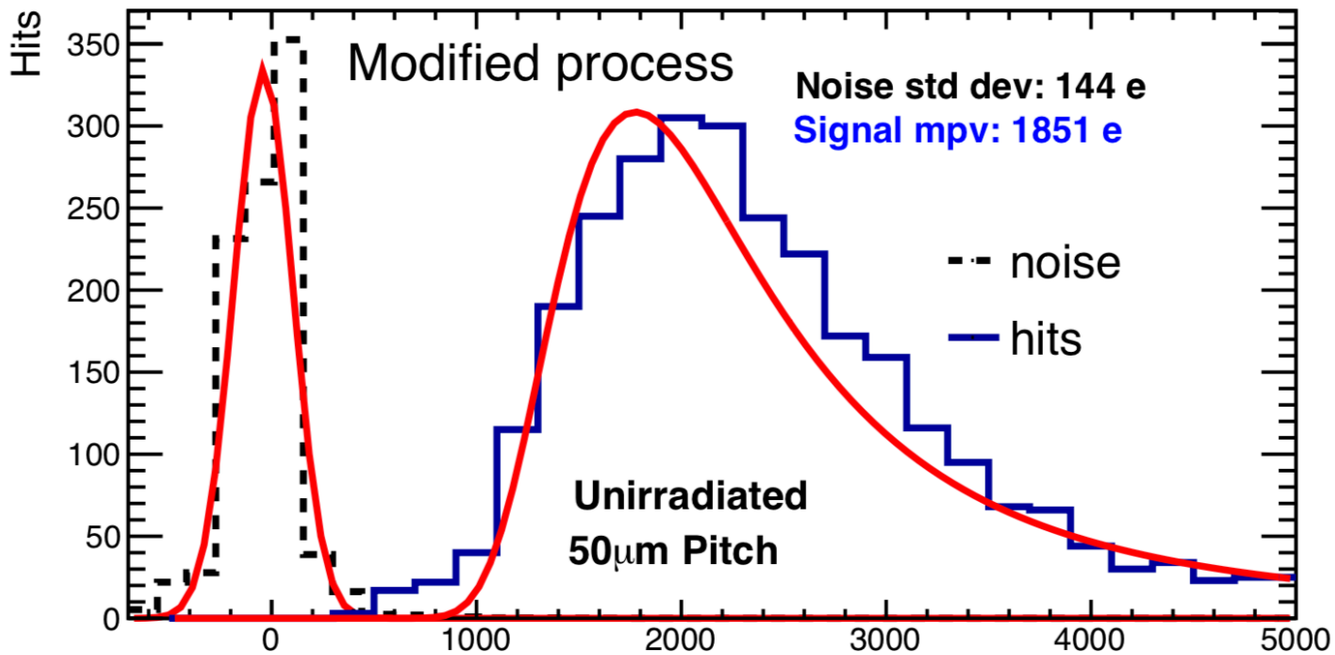


Small fill-factor DMAPS

2017 JINST 12 P06008

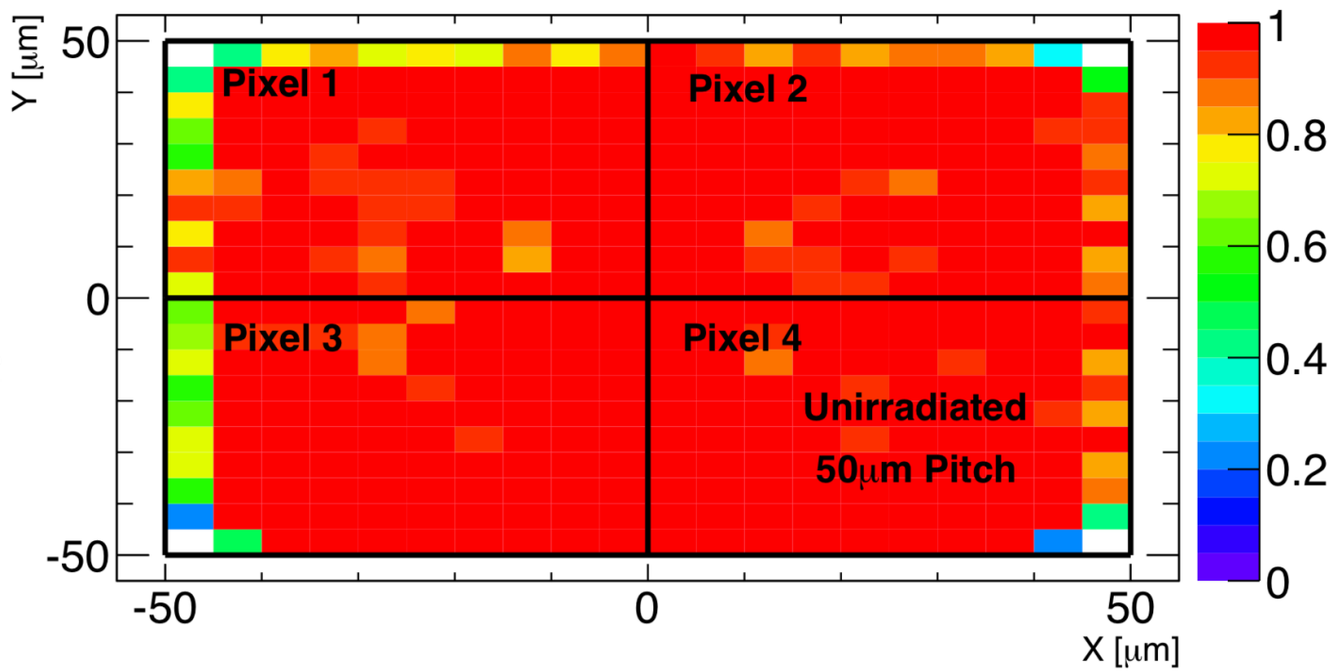
Signal & Noise:

- SPS testbeam with 180 GeV pions
- using independent pixel telescope
  - with a spatial resolution of 9 μm



Efficiency:

- readout a 2×2-pixel subset from the sensor matrix in its centre
- efficiency as function of the hit position for an unirradiated modified 50×50 μm² pixel sensor with 3 μm electrode and 18.5 μm spacing



Summary

- Time to define the requirements
  - expected rate has the biggest impact
  - expected coverage
  - desired spacetime resolutions come next
  - mechanics to follow

- Translated to technologies, what we can estimate now looks like
  - 4-5 stations or 8-10 in total (2 sides) of ~50×5 cm^2 area each
  - pixel size of 50 μm (or <100 μm) for good resolutions

- Many tech options on the table
  - Extensive R&D + testing programs driven by the LHC upgrades
  - MAPS/DMAPS seem appealing as a complete solution
    - though quite new (not a lot of experience)
  - Plenty of hybrid designs with existing electronics solutions
    - though hybridisation is getting more complicated

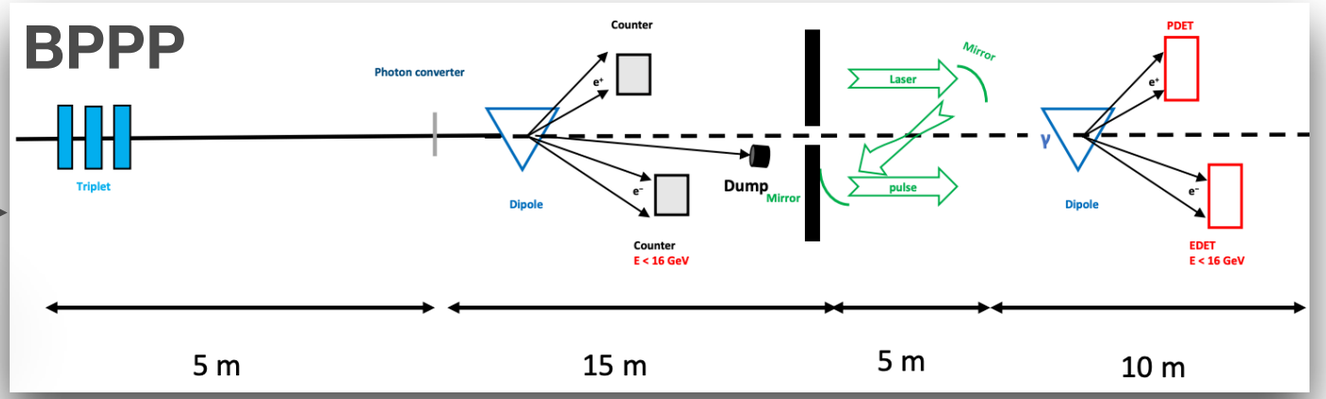

THANK YOU
THANK YOU
THANK YOU
THANK YOU

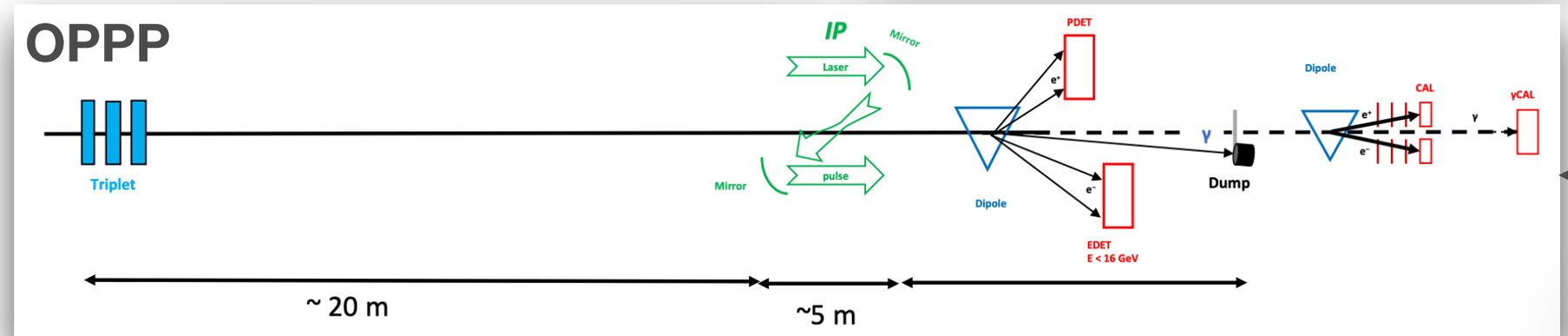
BACKUP

OPPP/BPPP @ LUXE

Bremsstrahlung

$\gamma_B + n\omega \rightarrow e^+e^-$





Compton

$e + n\omega \rightarrow e' + \gamma$

$\gamma + n\omega \rightarrow e^+e^-$

- XFEL electrons
  energy: 17.5 GeV, N_e per Bunch: 6×10^9, using only 1 bunch out of 2700 in the train, bunch length: 25 μm & emittance ~1.4 mrad×mm (beam-spot is $\sigma_{xyz}=5\times5\times24$ μm^3)
- Conversion target (BPPP only): Tungsten with thickness $X/X_0=1\%$, Emitted photon's energy distribution according to equation 13 in theory paper (also in PDG)
- Laser: Ti-Sapphire, energy: 0.35-7 J, shot duration: 35 fs, spot size: 10 μm, ω=1.55 eV (800 nm), I=0.1-2×10^{20} W/cm^2, pulse frequency: up to 10 Hz
- Collision angle (e/γ & ω): θ=π/12

Pixels, generally

- Pixels are in general high speed, with good time resolution & ability to select hit patterns, also at high rates
- Hybrid pixels: planar integration technology allows to put together those building blocks in a matrix covering few square centimetres
  - Matrices can then be put together to cover larger surfaces

- Particles crossing the silicon detector (or photons absorbed in it) generate charged carriers (on average 1 e-h pair per 3.6eV deposited)
- Carriers generated in the depletion zone lead to a current signal much larger than the thermal background current ⟶ detectable!
- In the undepleted regions
  - too low E-field to collect charges in a short time
  - too many majority carriers allowing charge recombination

- The need for small pitches between bond connections imposed a very high demand on industrial standards when pixel R&D for the LHC started
  - At the time, required pitch of 50 μm was ~15 years ahead of industrial demands
  - This has become a standard and requirements for current hybrid pixel R&D often target pitches less than 50 μm

Detection of particles

- relativistic particle looses energy through many collisions with the electrons of the crystal and generates ~80 e-h pairs per μm of path in a few μm wide cylinder around its trajectory
- these charges drift under the action of the external E-field at a speed which depends on it, but saturates at ~10^7 cm/s for fields close to ~10 kV/cm
- The charges can therefore be collected in less than 10 ns, resulting in a current of about 0.5 μA
- During the drift the charges do not exactly follow the E-field lines:
  - diffusion due to random thermal motion in the crystal lattice
  - the spread of the arrival position is a Gaussian with $\sigma=\sqrt{(2Dt)}$
  - a few μm at the collecting electrode assuming a typical electron diffusion constant of 35 cm^2/s and a transit time of 10 ns
  - the diffusion constant is higher for electrons than for holes, as it scales with the mobility

Pixel size impact

- Each pixel covers a very small area over a thin layer of silicon
- Individual pixel has a very low capacitance ~O(0.1 pF) dominated by coupling to the neighbouring pixels rather than to the backside plane
- The direct inter-pixel coupling has to be kept to a minimum with proper sensor design to avoid cross talk between pixels.

- The low capacitance allows fast signal shaping with very low noise
- common to obtain noise of ~200e^- for electronics operating at 40 MHz
  - e.g. a S/N>100 for fully depleted 300 μm thick sensors.
  - this allows operation in absence of spurious noise hits.
  - A detection threshold set at, e.g., $10\sigma_{noise}$ gives full efficiency and very low probability that a noise fluctuation exceeds the threshold
  - backgrounds e.g. elx pickup, cross talk, low-energy photons exist, but a spurious hit probability of $<10^{-8}$ per pixel can be reached

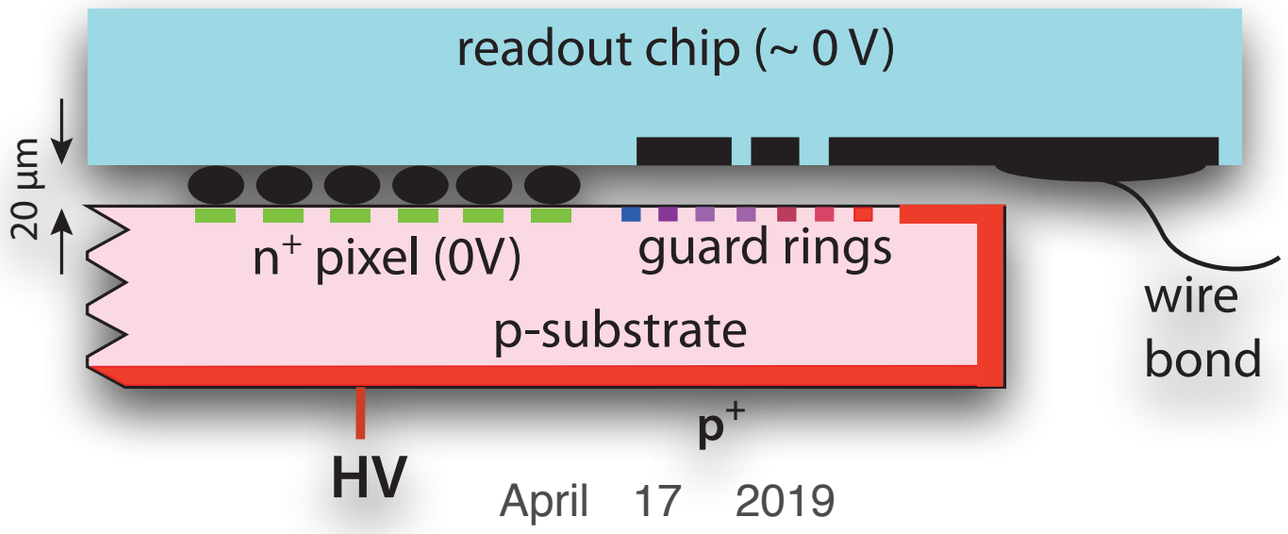
Sensor thickness impact

- While providing smaller signals per MIP, benefits of thin sensors are
  - **higher electric fields** as well as
  - **shorter and faster electron collection** for a given bias voltage
    - and hence **better radiation tolerance**.
- Thin 6” or even 8” sensor wafer production is enabled by techniques employing SOI or Si-Si handling wafers, or by thinning (e.g. by cavity etching) and forming a back side ohmic contact at low temperature after the front side processing is complete.
- Currently the limit in thickness is considered to be around 50 μm

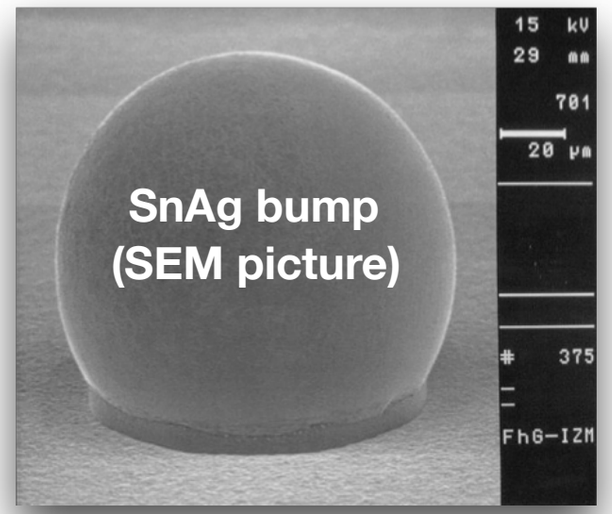
Guard rings design

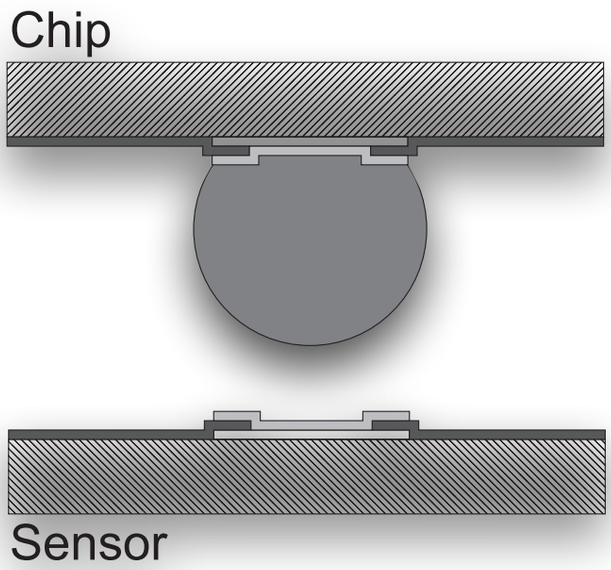
- bringing down the potential from the bias implants (HV) to the pixel implants (0V), play an important role in optimising the breakdown behaviour of sensors after irradiation
- The number of rings, implant distance and size, as well as metal overhangs for vertical field suppression are the parameters to optimise.
- Optimal performance rad-tolerant has been obtained with 10–11 rings with metal overhangs on both sides of the implant over a total length of 350 μm
- The distance from the edge to the active part of the sensor is ≳400 μm
- Other designs trying to minimise this distance 20 μm make use of etched and doped edges, called active edges, reaching values down to about 50 μm
- if cost saving single sided processing is to be used, the guard ring structure needs to be placed on the electrode side and is thus in very close proximity (~<20 μm) to the readout chip, a challenge for the design

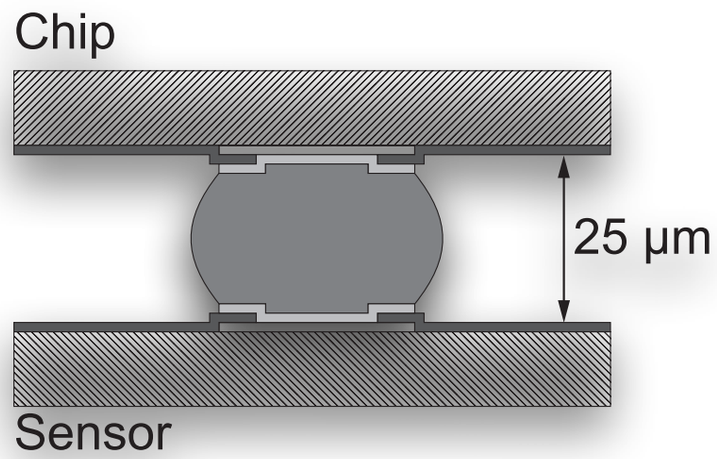
1-sided n⁺-in-p design



Bonding







Eutectic solder bumps and the flip-chipping process:

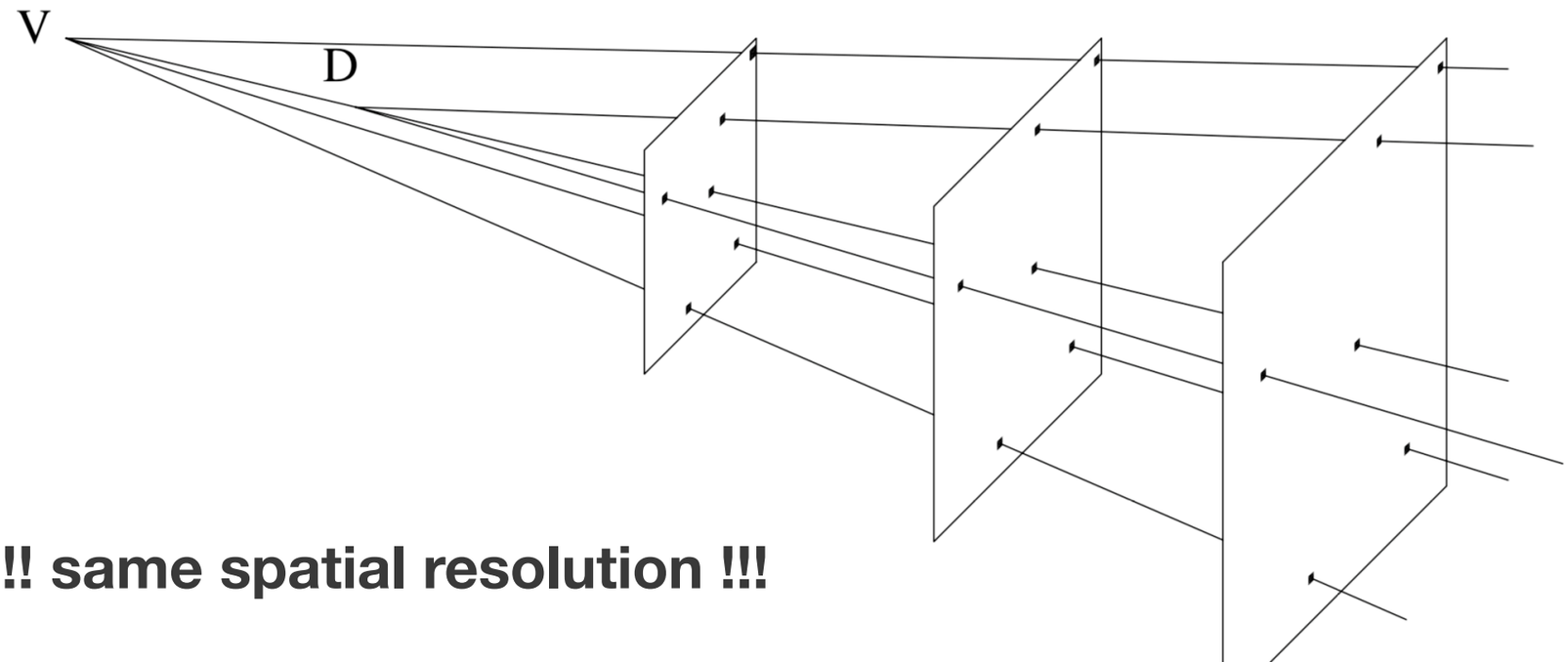
Solder bump attached to a readout chip is bonded to the Under Bump Metalization (UMB) of the sensor, reaching high connection density down to pitches of 25 µm & bump dimensions of (15 µm)[3]

- Demands the bond connection:
  - small capacitance additions to the preamplifier
  - good yield with $<10^{-4}$ defect rate (open or short) and good contacts (<100 mΩ)
  - robustness against temperature cycling (–40°C to +60°C)
- Bonding types
  - Integrated circuits are usually bonded to sensor wafers (chip-to-wafer, C2W).
  - Wafer-to-wafer bonding (W2W) is a cost attractive
- Bonding procedures:
  - intermediate media: e.g. by means of solder or adhesive-bonding using glue layers
  - direct bonding: either metal-to-metal or silicon oxide-to-oxide

Microstrip testcase

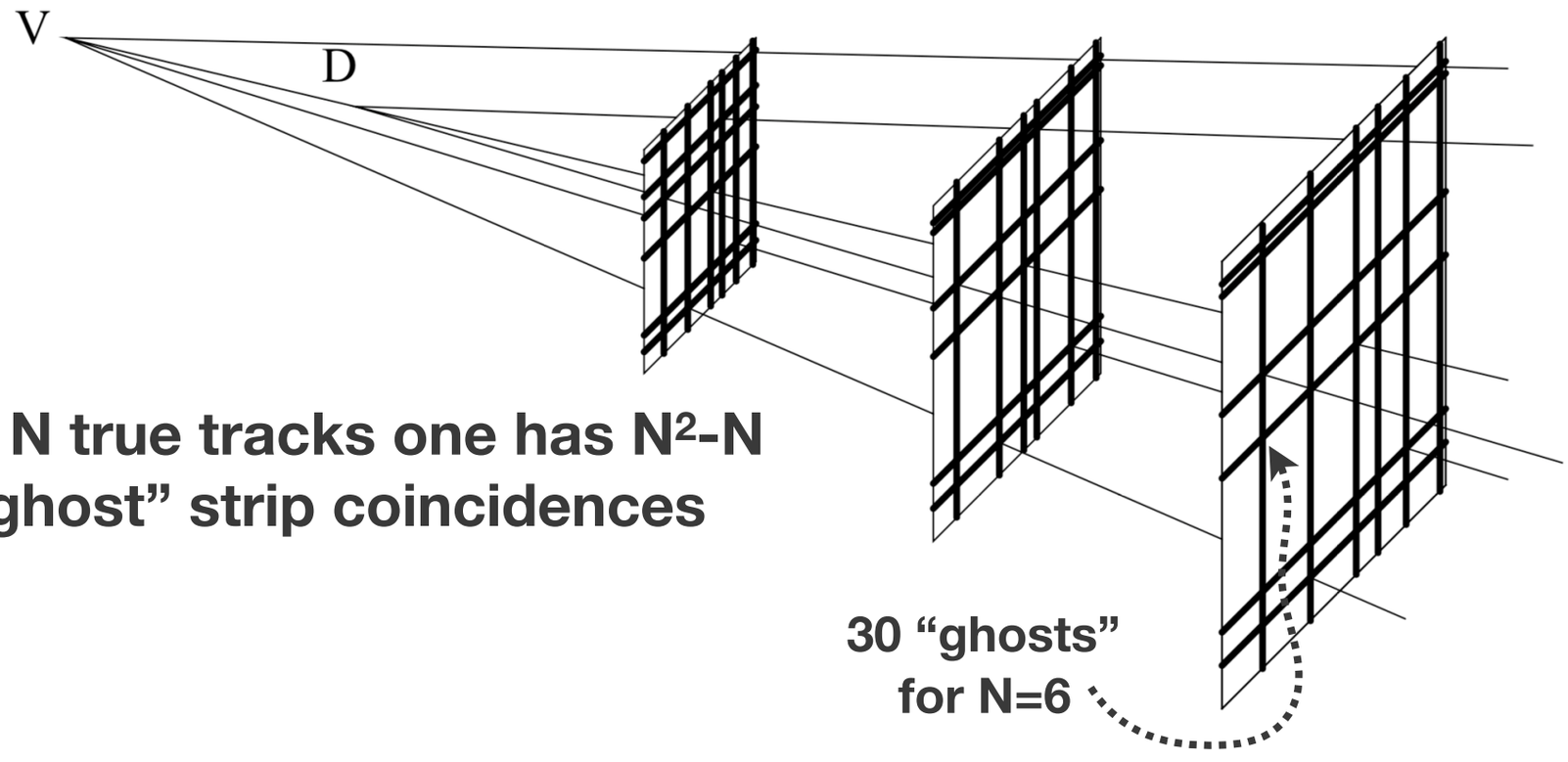
Tracking: Pixels vs Strips

three pixel layers with
100-μm pixel pitch



!!! same spatial resolution !!!

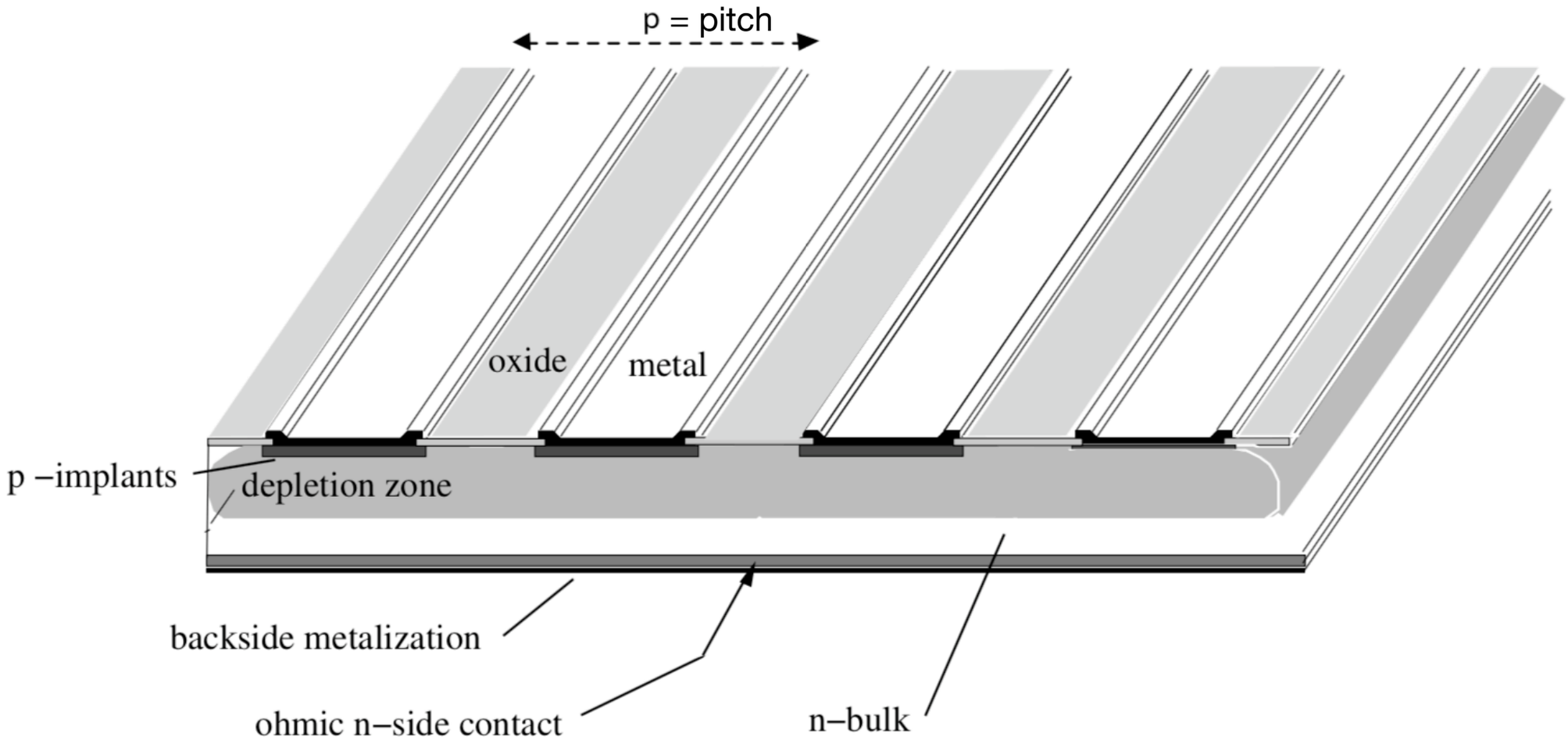
three double-sided microstrip
layers with 100-μm strip pitch



For N true tracks one has N^2-N "ghost" strip coincidences

30 "ghosts" for N=6

Microstrip simple layout



- consider a 300-μm-thick n-doped silicon wafer (i.e. silicon doped with the addition of a pentavalent impurity, like phosphorus)
- Assume that each strip is a p-implant (i.e. doped with a trivalent impurity, like boron)
- The doping must be such as to largely overcome the intrinsic carrier densities in silicon at room temperature (~$10^{-10}/cm^3$) and will therefore determine the abundance of free electrons (holes) in the n-zone (p-zone)

Operation principle

- The resistivity of doped silicon depends only on the dopant density N and on the majority carrier mobility μ: ρ=1/(eNμ)
- The interface region between the n-doped and the p-doped regions will be emptied of free charges:
  - majority of carriers in each region diffuse through the junction and recombine with the opposite sign charge carriers
  - *E*-field is generated due to the excess charge from the immobile doping atoms
  - *E*-field balances the diffusion and establishes an equilibrium
    - equilibrium is characterised by the absence of free charges in a region which extends to thickness *W* ⟶ this is called the "depletion zone"
- *W* depends on the dopant concentration N of the lower doped bulk material and on the reverse bias voltage *V* across the junction
- Depletion zone can be seen as a charged capacitor *C* per unit area
- Increasing *V* increases *W* (depletion zone thickness) and reduces *C* (capacitance)
  - both these effects increase the signal-to-noise ratio, S/N
  - the best S/N is achieved for fully depleted sensors: *W* = thickness of silicon layer

$$W = \sqrt{2\varepsilon_0\varepsilon_{\mathrm{Si}}(V/eN)} = \sqrt{2\varepsilon_0\varepsilon_{\mathrm{Si}}(V\mu\rho)}$$

$$C = \varepsilon_0\varepsilon_{\mathrm{Si}}/W = \sqrt{e\varepsilon_0\varepsilon_{\mathrm{Si}}N/2V}$$

Operation diagram

Resistivity

$$\rho = \frac{1}{eN\mu}$$

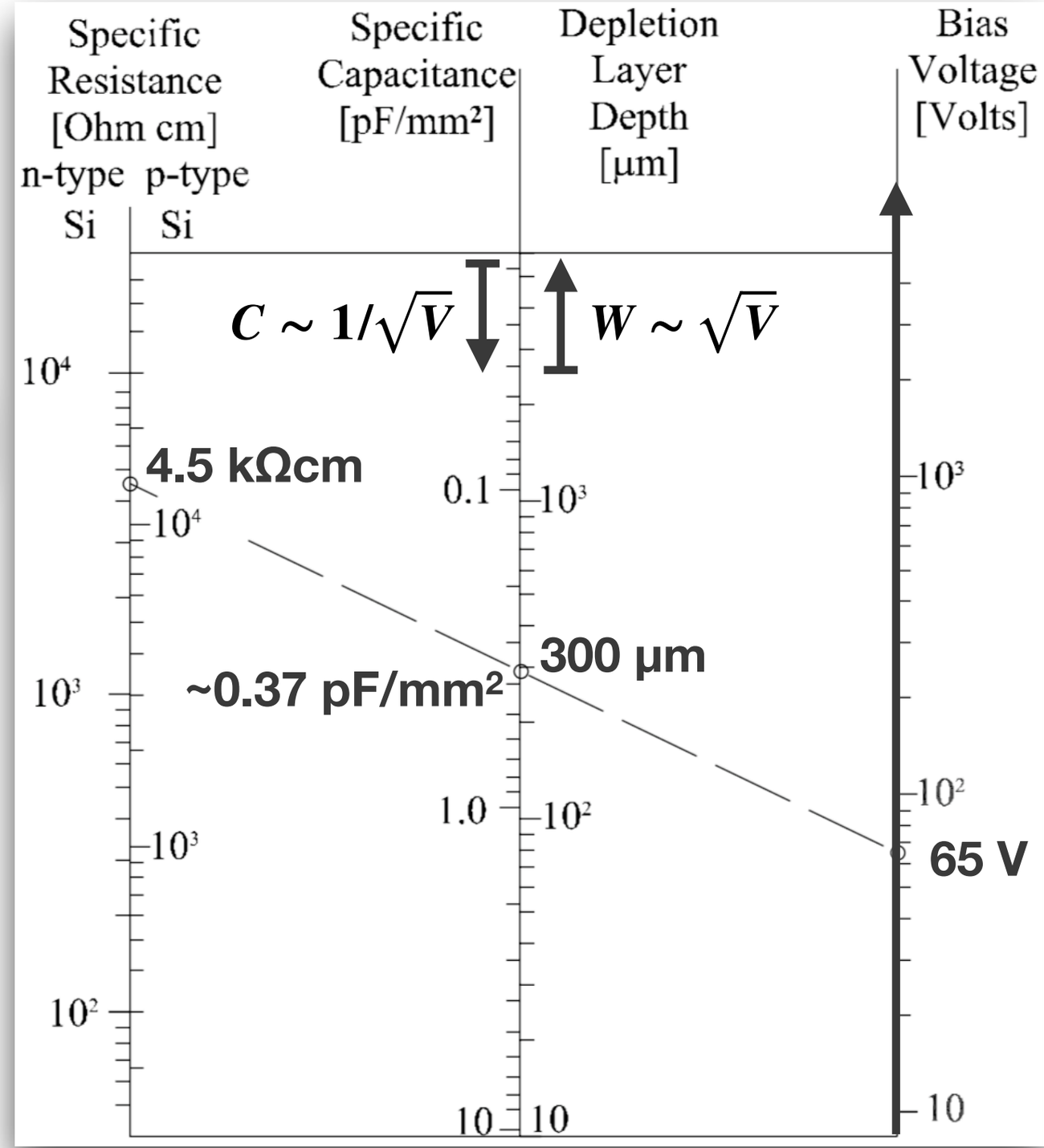
Depletion zone thickness

$$W = \sqrt{2\varepsilon_0\varepsilon_{\mathrm{Si}}(V/eN)} = \sqrt{2\varepsilon_0\varepsilon_{\mathrm{Si}}(V\mu\rho)}$$

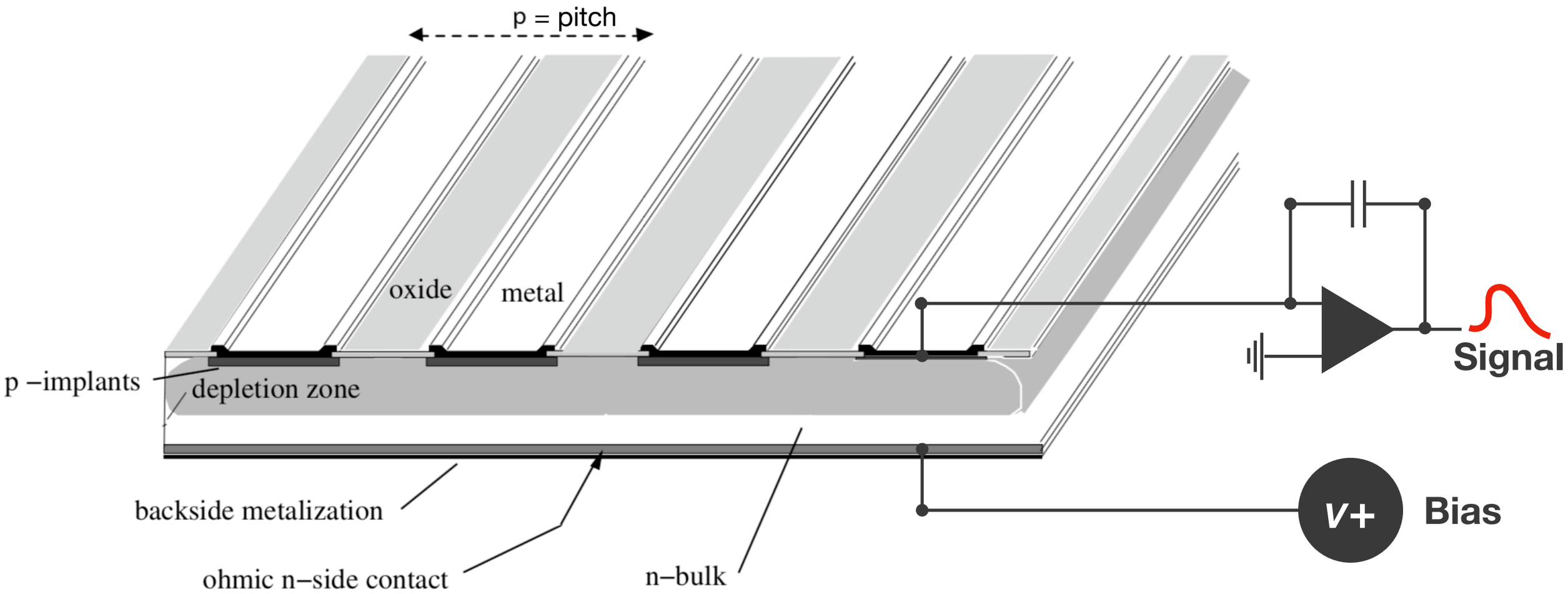
Device's capacitance

$$C = \varepsilon_0\varepsilon_{\mathrm{Si}}/W = \sqrt{e\varepsilon_0\varepsilon_{\mathrm{Si}}N/2V}$$

Assuming a silicon resistivity of 4.5 kΩcm, a 300 μm thick n-type silicon detector fully depletes at 65 V bias voltage

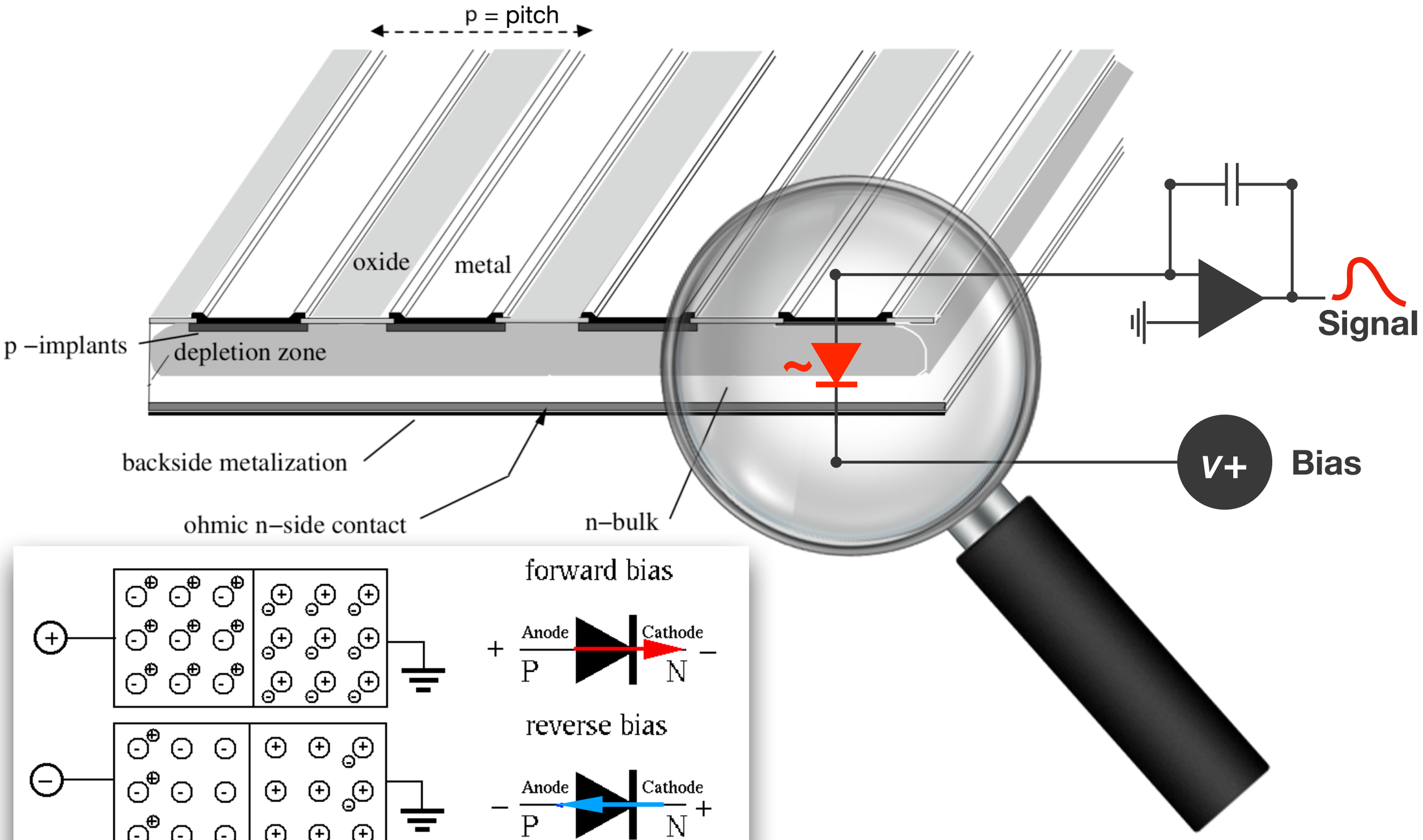


Bias & Readout circuit



- n-type silicon substrate with p-implants is a set of pn-junctions (microstrips) acting as independent diodes
- If these “diodes” are reversely polarised, e.g. applying a positive voltage on the n-side and connecting each p-implant to ground through its readout amplifier, very little current flows through them
- The majority carriers experience a barrier due to the voltage applied externally
- The minority carriers (holes in this example) are constantly removed out of the depleted region by the field in the junction, generating a small current: “dark current”
- As the carriers are thermally generated, this current depends on temperature and is also known as thermal background current

Bias & Readout circuit

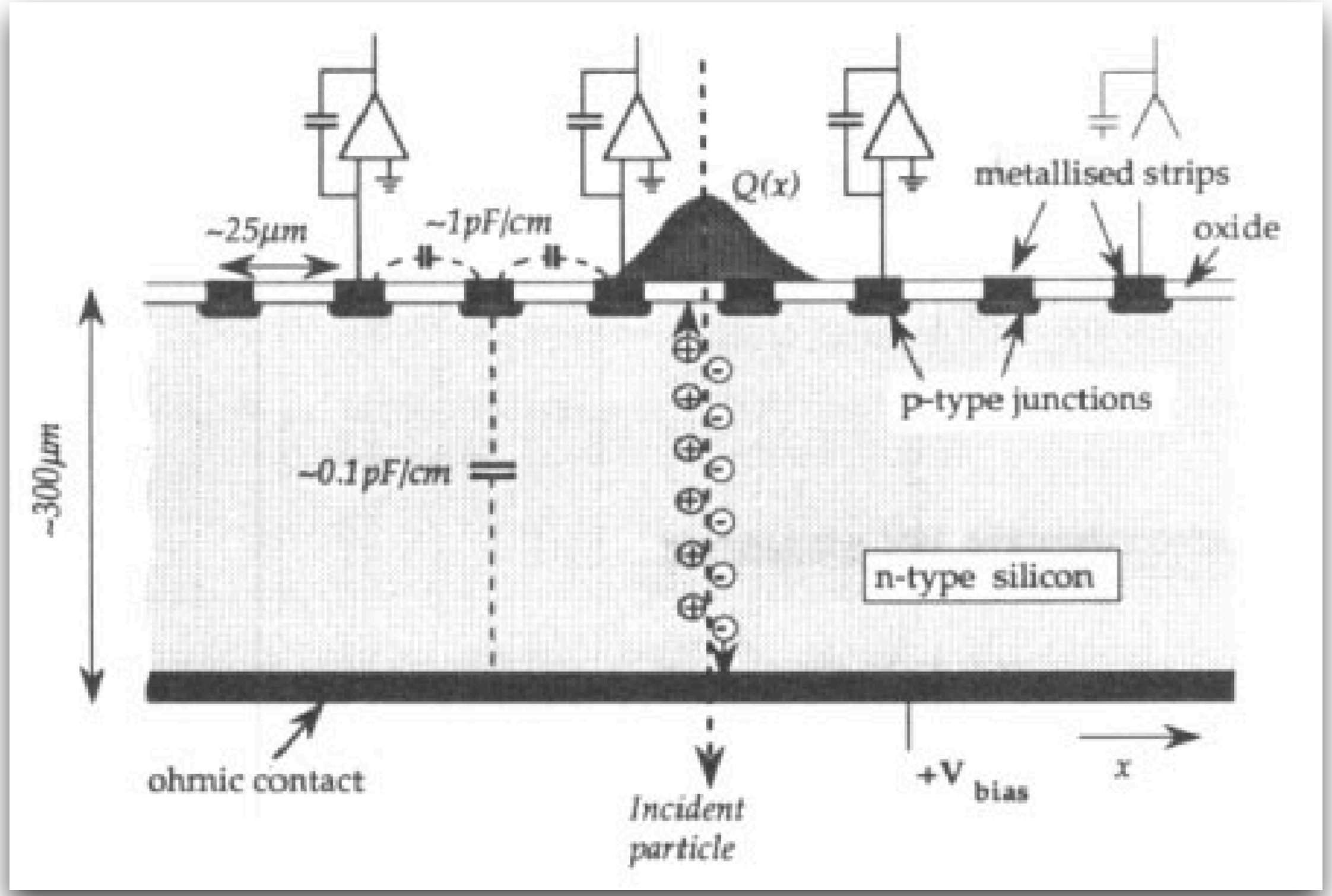


Misc

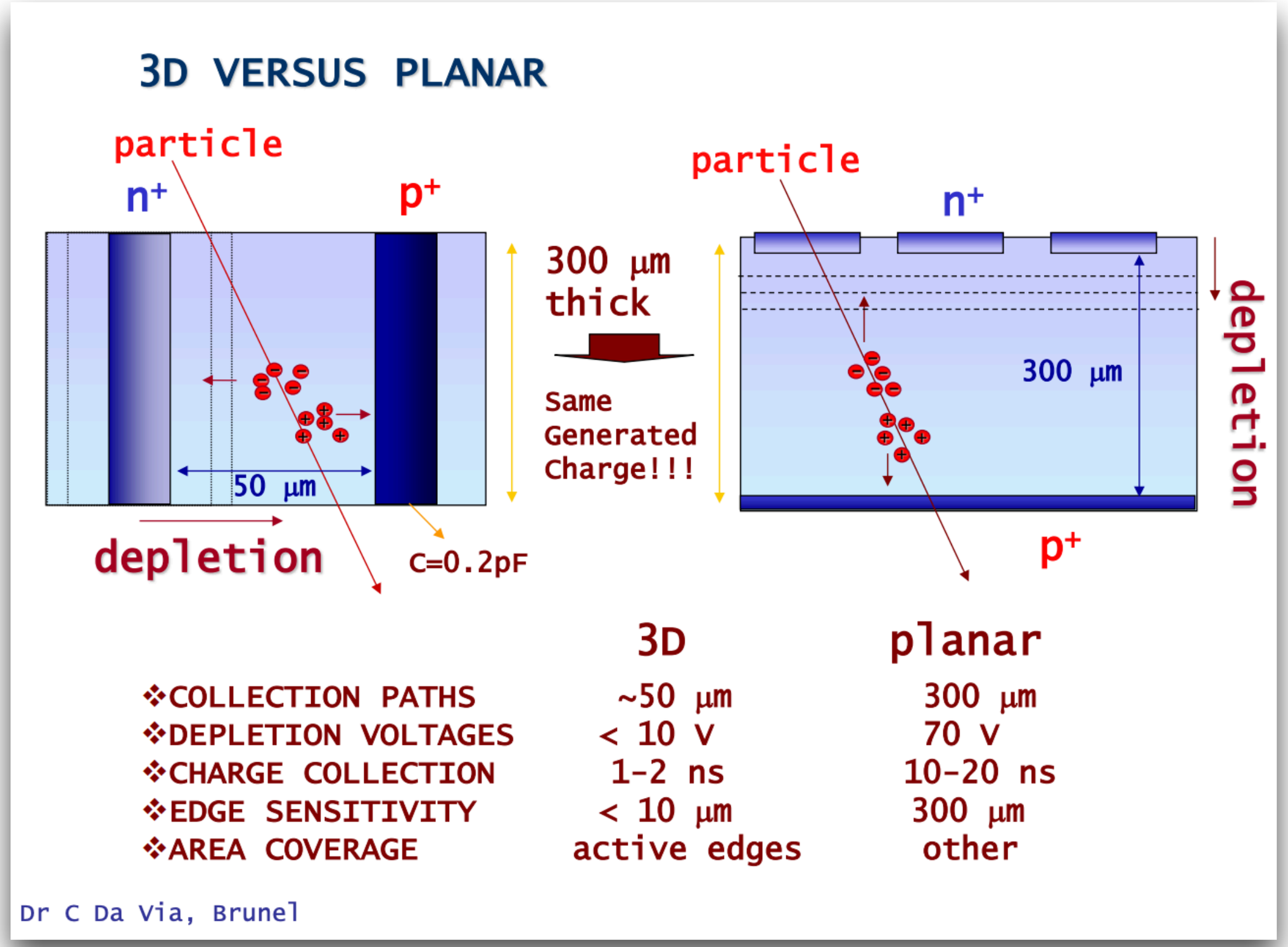
Analog FE

- Function: Discriminate true hits from noise with the correct timing
- Requires fast leading edge response (high slew rate)
  - can be achieved with high input gain
- Input charge to output voltage gain is $1/C_f$ and the characteristics of the 1st stage amplifier
- Charge transfer efficiency (sensor⟶integrator) is: $(C_{det} + G \times C_f)/C_{det}$
  - C_{det} = detector load capacitance and G is the 1^{st} stage open loop gain
    - G~10 for 1 μA current and 1 V power supply
- high open loop gain is needed in order to have both high gain (small C_f) and good charge transfer efficiency
- ROICs' minimum stable threshold, imposed by decreasing input signals:
  - ~2500 electrons in 1^{st} generation
  - ~500 electrons for the 3^{rd} generation
- Figure of merit is not S/N, but rather signal to threshold ratio!
  - ENC = equivalent input charge noise

Rep. Prog. Phys. 57 (1994) 481-531

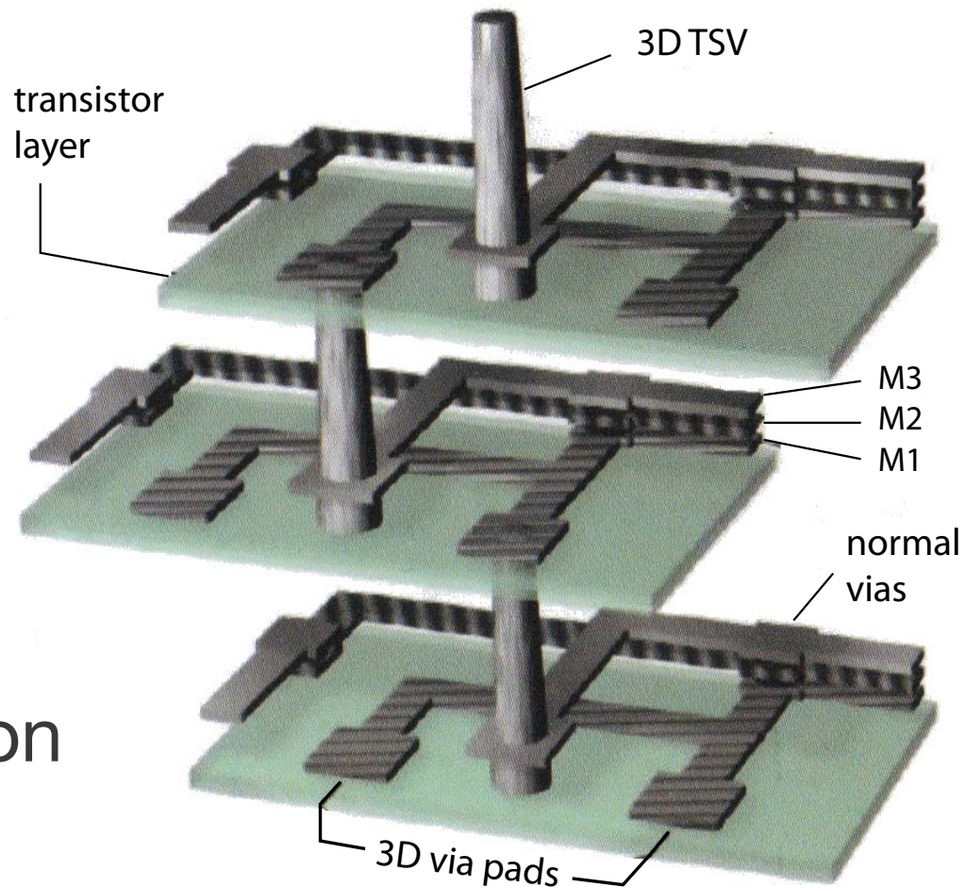


http://people.brunel.ac.uk/~eestprh/pghep/Silicon1.pdf



3D-integration and TSV

- Extending electronics integration into the 3rd dimension is regarded as the second route to ever increasing circuit density (apart from feature size shrinking)
- 3D-stacking of several electronic device layers (tiers) is thus an eminent field of industrial research
  - reduced power consumption
  - smaller involved capacitances
  - larger I/O bandwidth
  - more functionality at lower cost
- Vertical vias running through layers of silicon (TSVs) are a key ingredient for 3D-stacking



- Tiers can be different CMOS layers but also electronics and sensor layers or layers interfacing to an optical signal transport