# Update on GigE Vision implementation in FPGA.

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## Abstract

Presented here are the latest updates from the development of the GigE Vision in MicroTCA.

First we present the results of the certification process at AIA plug-fest, where our implementation had to interface with cameras from several vendors.

A new hardware platform (Struck SIS8160 - an Advanced Mezzanine Card for MicroTCA platform) was also added to the list of supported hardware. With two 64-bit wide DDR4 memories this board offers a good platform for data intensive application, and with the support for White Rabbit is also allows timestamping of the captured frames.

Lastly we present the steps needed to extend the support for 10 GigE Vision, based on 10 Gigabit Ethernet.

## Introduction

DIPC-7050 GigE Vision stack[1,2,3] is an implementation of GigE Vision protocol in FPGA. Because of highly-parallel nature of FPGAs, such an implementation can achieve very high througput and deterministic latency.

## Certification process

GigE Vision standard is maintained by **Automated Imaging Association (AIA)** trade group. To improve interoperability between products, plugfests are hosted regularly (twice per year) where devices from different vendors are tested together.

We have attended a plugfest on October 9th, 2019 at Lago Maggiore, Italy. Our implementation of the standard successfully inter-operated with cameras from **Allied Vision**, **Basler**, **JAI**, **Hamamatsu** and **Teledyne**. This makes our implementation compliant with the GigE Vision standard.

We have also identified some cameras which had interoperability issues with our implementation. One of the camera was (incorrectly) checking the Ethernet frame length. Cameras from three other vendors do not support *Manifest Table* which we relied upon for obtaining the camera information. We are mitigating the issues on our side, and we expect to increase the number of compatible cameras on future plugfests.

## Support for 10 GigE Vision

With ever increasing needs for higher frame rates and larger image sizes is the 1 Gigabit Ethernet interface specified in GigE Vision standard becoming a limitation. To illustrate the throughput needed we here present two examples.

| | FLIR Oryx 10GigE[4] | JAI SW-4000T-10GE[5] |
|---|---|---|
| Frame rate [FPS] | 162 | 97000 |
| Resolution [px] | 2448 x 2048 | 4096 x 1 |
| Bit depth [bit] | 12 | 10 |
| Total througput [Mbit] | 9746* | 9535** |

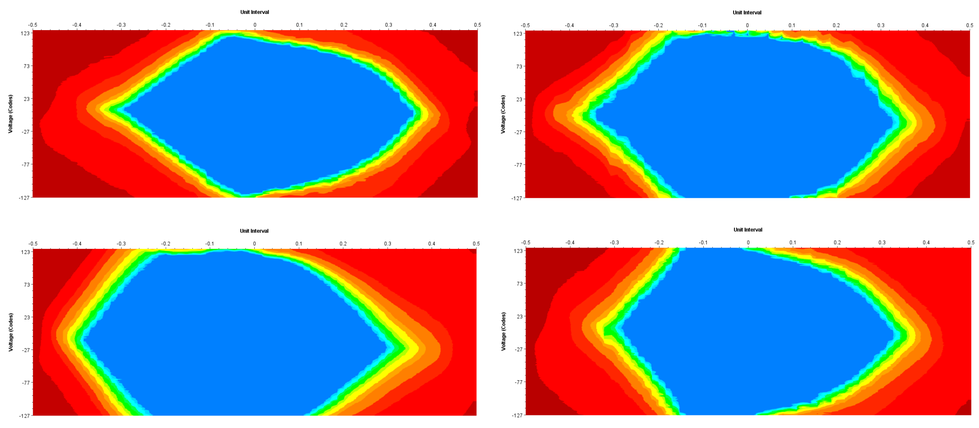
* when using Mono8
** when using RGB8

To resolve the issue of the throughput was the standard extended to support **10 Gigabit Ethernet** (as specified in IEEE 802.3 Ethernet).

Although it was already demonstrated that the image processing can run at 312.5 MHz with 32-bit wide interface[6] is this frequency usually too high for more complex logic chains. We have decided to also provide an implementation running at **156.25 MHz** with **64-bit** wide interface. We are currently working on the implementation of the wider data path.

10GBASE-T compliant SFP module

### Test on SIS8160 with DFMC-4SFP+ at 10.3125 Gbps

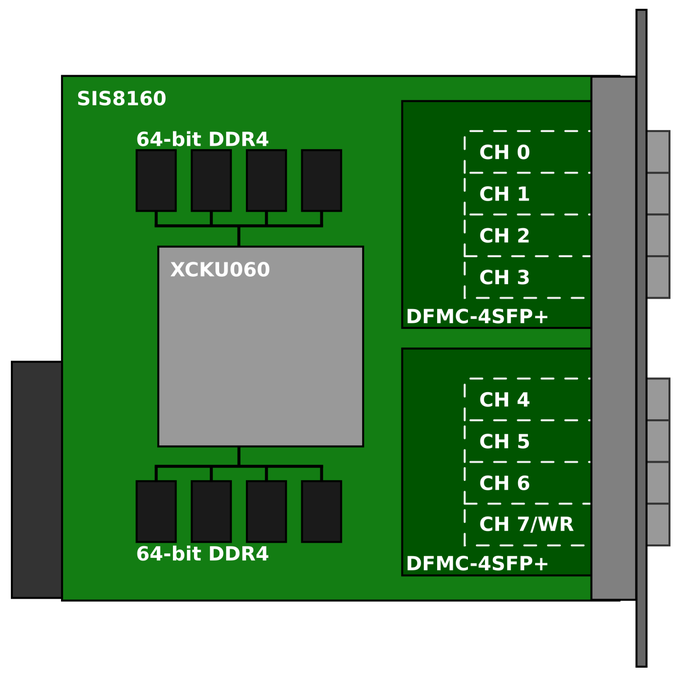



## New hardware platform

In the past we have made our implementation work on:

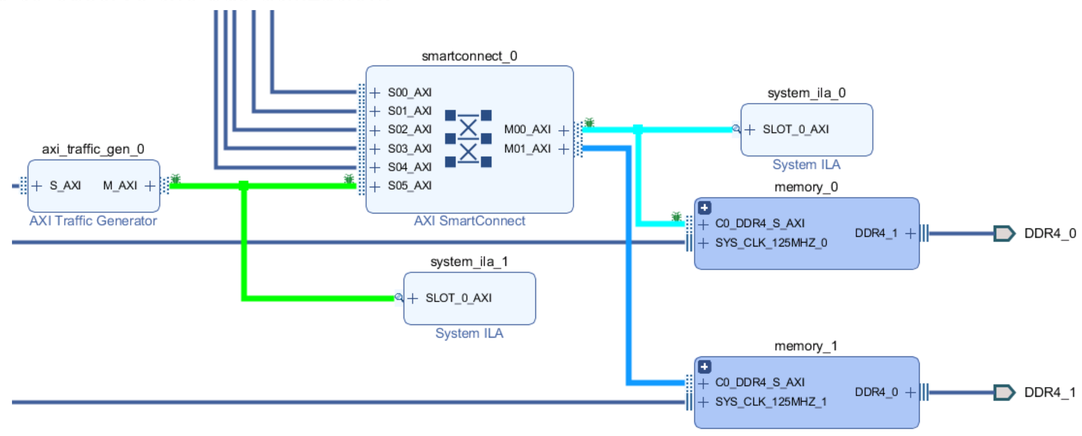
- DAMC-TCK7 with Kintex 7 FPGA
- Xilinx KCU105 evaluation kit with Kintex UltraScale FPGA
- NAMC-ZYNQ-FMC with Zynq 7000 programmable device

In the last months we have extended the support to **Struck SIS8160** Advanced Mezzanine Card. The main differences between already supported boards are two: the board contains **two 64-bit DDR4** memories (providing very high throughput for data), and **White Rabbit** endpoint could be implemented for time-stamping of the frames.

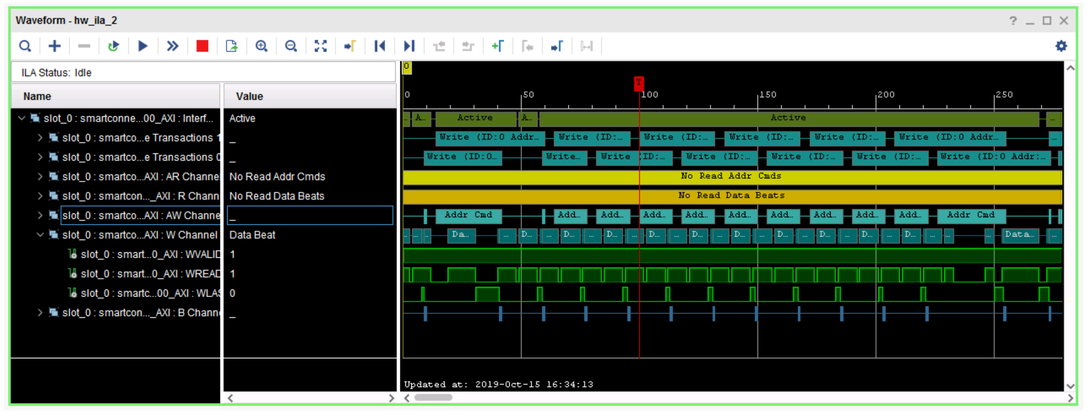



### DDR4 performance measurement on SIS8160

Xilinx AXI Traffic Generator was used to write data into DDR4 memory, and System ILA was used to observe the bus utilization.




Observation of the AXI4 interface during the write transfer (highlighted in cyan above):




**Interface width = 512 bit**
**Interface frequency = 250 MHz**
**Measured efficiency = 80.2 %**
**Number of DDR4 controllers = 2**
**Achieved throughput = 205.3 Gb/s = 25.6 GB/s**

## Conclusion and outlook

Several new features were presented. Most importantly, our implementation of the GigE Vision protocol is now certified with the certification body (AIA) and the interoperability was recently demonstrated on a plugfest. A new hardware platform, Struck SIS8160, was added to the list of supported and tested hardware platforms, providing a wider datapath for image data. Finally, an increasingly popular 10 GigE Vision was discussed, and the changes needed to be implemented to support the higher data rate.

## References

[1] S. Stubbe, J. Marjanovic, A. Gornott: Implementation of GigE Vision standard and applications in MicroTCA, MTCAWS 2018
[2] S. Stubbe, J. Marjanovic: GigE Vision high-speed image processing on FPGAs for science and industry, ARD MT 2019
[3] https://techlab.desy.de/products/gige_vision_solutions/dipc_7050_gige_vision_stack/
[4] https://www.flir.com/products/oryx-10gige/
[5] https://www.jai.com/products/sw-4000t-10ge
[6] J. Marjanovic: Low vs High Level Programming for FPGA, IBIC201