Development of an FMC+ carrier in MicroTCA.

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2019-10-17

ARD ST3 2019

DESY.

MICROTCA TECHNOLOGY LAB
HELMHOLTZ INNOVATION LAB

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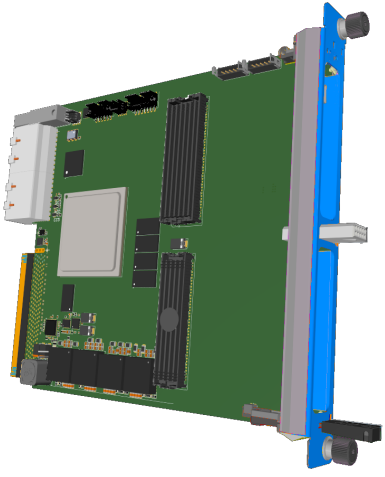
RESEARCH FOR GRAND CHALLENGES

MTCA ARD

An FMC+ carrier in MicroTCA

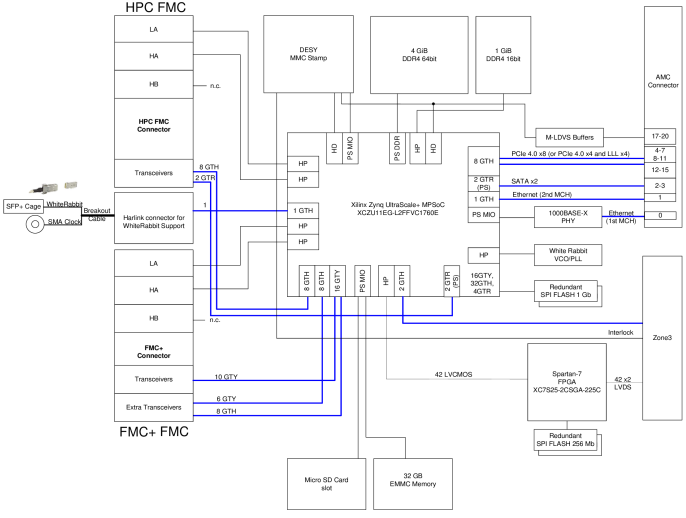
Standards:

- MicroTCA
- MicroTCA.4 (Zone 3)
- FMC
- FMC+
- Communication protocols
  (PCIe, 10/40G Eth)



Block diagram

The board is based around Xilinx Zynq UltraScale+ MPSoC



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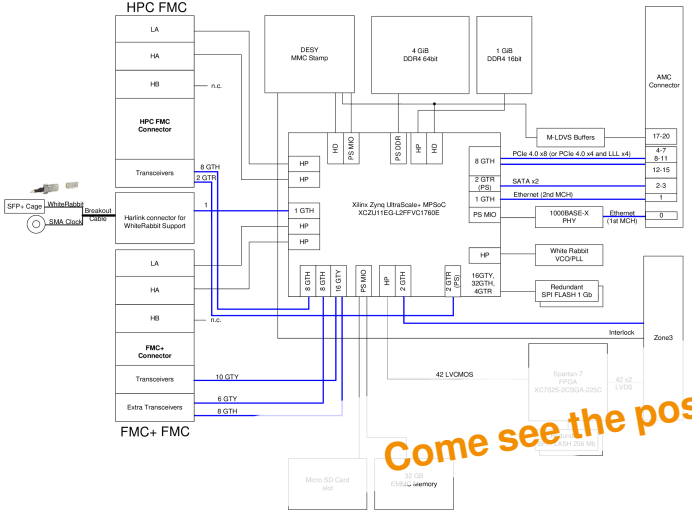
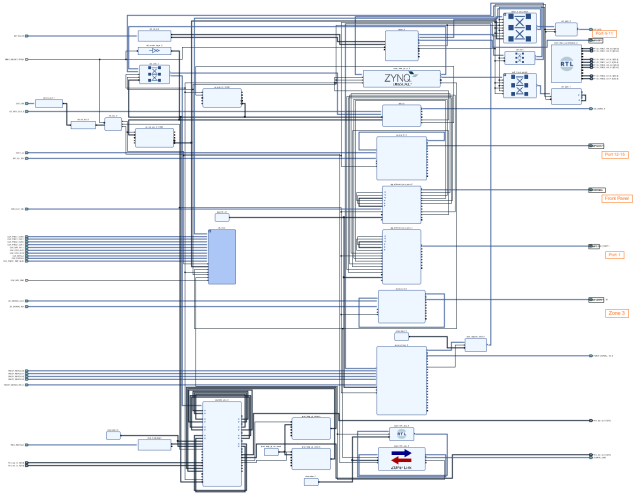


Come see the poster!

Reference Design

Contains support for all peripheral components (PCIe, DDR4, ...)



two DFMC-DSx00 mezzanines

Two IP cores to communicate with ADCs and other peripherals, DMA system