Development of an FMC+ carrier in MicroTCA.

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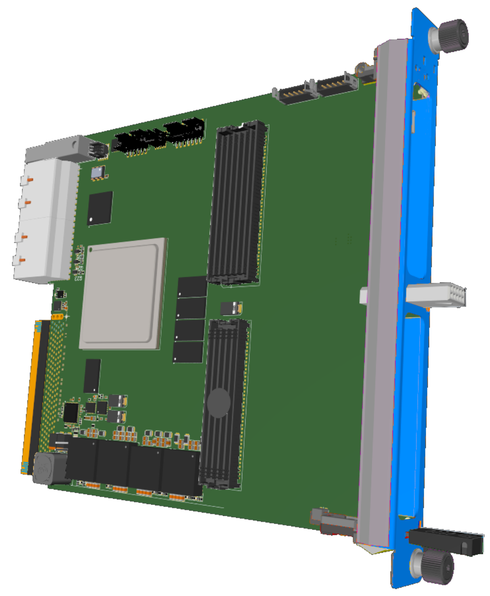
Abstract

The ecosystem of FMC/FMC+ carriers in MicroTCA (Advanced Mezzanine Card form factor) is very diverse. The requirements for such a board are very demanding, and sometimes even opposing to each other. The definition of a set of requirements that will satisfy most of the use cases is a challenging task. Presented here is the DAMC-FMC2ZUP, a modern and high-performance FMC+ carrier in AMC form factor, hosting a Xilinx Zynq UltraScale+ MPSoC. The FPGA has a total of 52 transceivers (32 GTH, 16 GTY, 4 GTR) providing support to the diverse communication interfaces towards the FMC slots, backplane and RTM. The four cores ARM processor with Mali graphics, and the availability of DisplayPort and USB interfaces over USB Type-C allow to use the board in stand-alone mode.

The board is fully backward compatible with DAMC-FMC25, an FMC carrier based on two-FPGA solution, with Virtex-5 and Spartan-6.

There are two firmware projects already available for the board. The first one contains support for all peripheral components and can serve as a reference design for custom projects. The second one contains the Intellectual Property (IP) cores to support two DFMC-DS500/800 FMC mezzanines, providing a digitizer solution with 4 channels, 12 bits and up to 800 MSPS. Mounting two DFMC-4SFP+ creates a solution with 8 SFP+ connections on the front panel, each one able to communicate at data rates of 10 Gbit/s and higher.

DAMC-FMC2ZUP is a versatile platform ideal to perform control tasks around a particle accelerator. Combined with the modularity of the MicroTCA platform it can be a building block for a larger system.



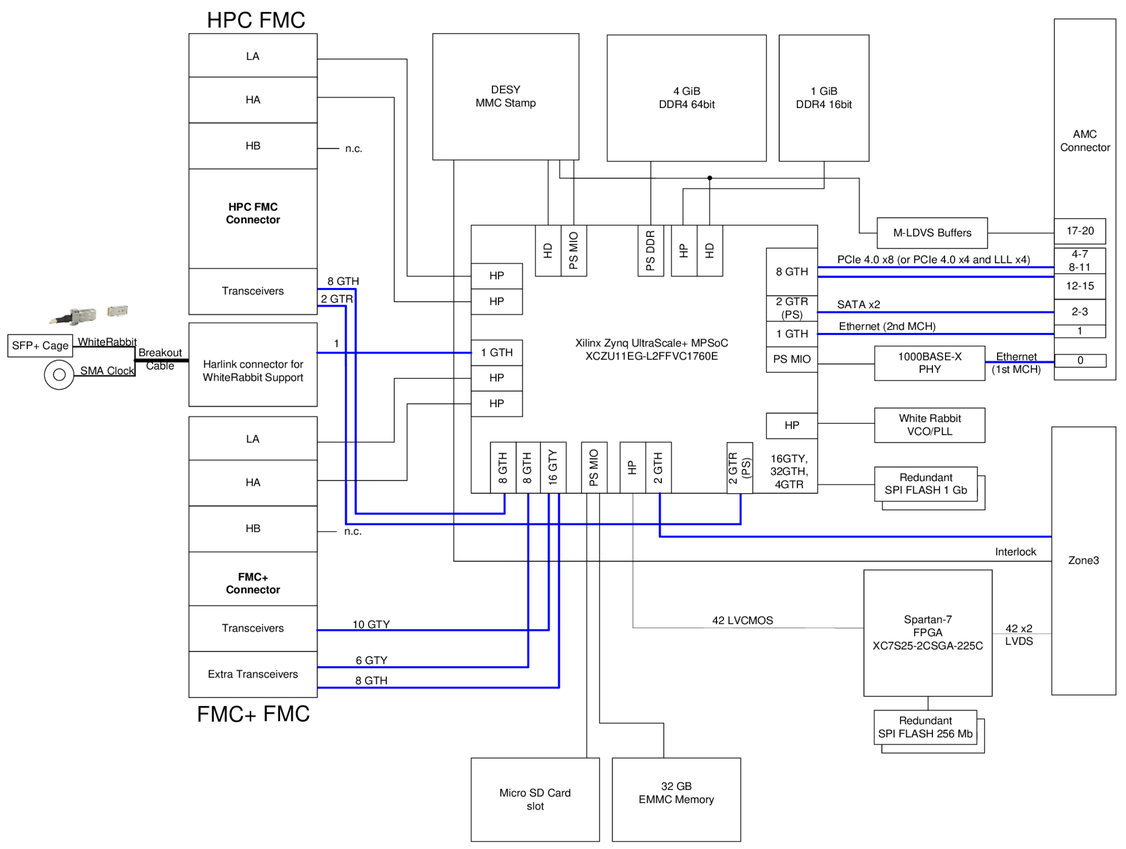
Standards involved

- MicroTCA/AMC
- MicroTCA.4 (Zone 3)
- FMC
- FMC+
- Communication protocols

MicroTCA.0 standard refers to **Advanced Mezzanine Card** as a basic building block of such a platform. Advanced Mezzanine Card (AMC) defines mechanical form factor, electrical and management interface.
MicroTCA.4 further extends MicroTCA.0 standard with additions important for experimental physics. A large area for I/O from the rear and facilities for precise clocks are forseen and specified.
FMC (FPGA Mezzanine Card) provides a compact method for the functionality of the FPGA boards with custom analog or digital I/O.
FMC+ recognizes the migration to fast serial interfaces for ADCs and DACs (e.g. JESD204B and JESD204C) and extends the basic FMC connector with additional lanes for Multi-Gigabit transceivers.
Several **communication protocols** are specified in AMC Family of Specification. AMC.1 defines requirements for PCI Express, AMC.2 defines requirements for 10G and 40G Ethernet, AMC.3 defines requirements for storage and AMC.4 defines requirements for Serial Rapid I/O.

Block diagram

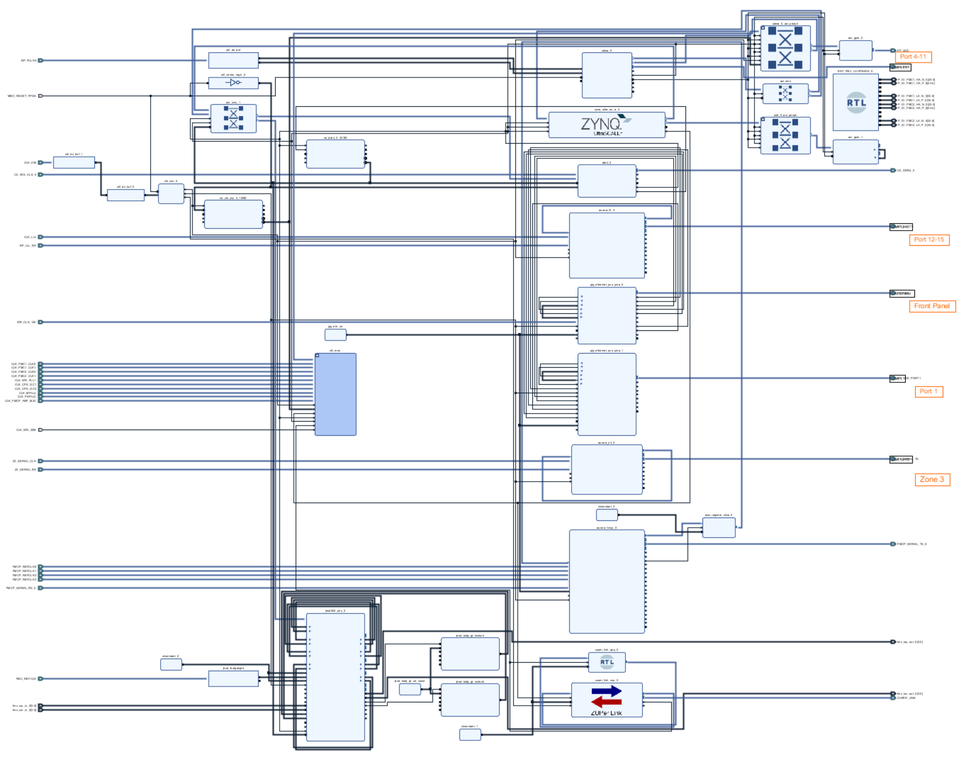
Shown on the figure below is the block diagram of *DAMC-FMC2ZUP*.



FPGA projects

Allocation of critical resources (MGTs, High-Performance memory banks, PCIe hard IP, clock routing) is an important step when designing a new board. This is why we have chosen an *iterative approach*, where the reference design for FPGA and schematics were updated in sync.

Project 1: Reference Design



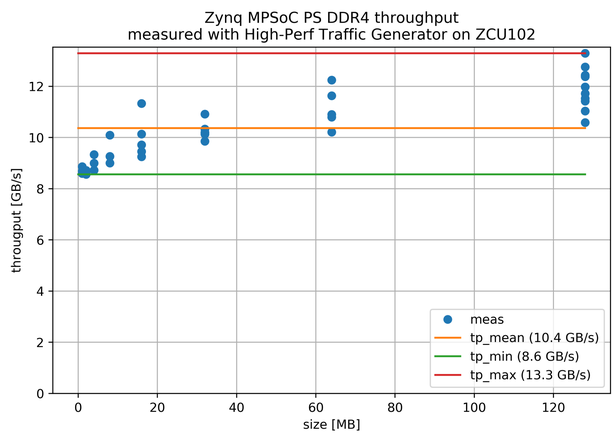
Project 2: two DFMC-DS800

As a typical but relatively demeaning use case, an application with two DFMC-DS800[1]was selected. Each DFMC-DS800 hosts an ADC12D800RF with 2 channels, producing 12-bit samples at 800 MSPS.

The fast LVDS interface between ADC and FPGA requires fast de-serializers, precise delay control and low-skew clocks. We have confirmed that in the current design all timing constraints are met.

On the other side a fast digitizer might require fast interface to on-board memory in order to store the sampling data. When the ADC data is not-padded to 8-bit boundary, the two ADCs will produce $800MHz * 12b * 4ch = 38.4Gbps = 4.8GBps$. When the ADC data is padded to 8-bit boundary (making each sample 16b wide), the two ADCs will produce $800MHz * 16b * 4ch = 51.2Gbps = 6.4GBps$. Those are quite demanding requirements.

To evaluate the proposed memory architecture we have used Xilinx ZCU102 evaluation kit: a High-Performance Traffic Generator is connected to 4 Xilinx DMAs, all connected to High-Performance PL-PS bridges. Results of the throughput measurements are shown on the figure below. It can be seen that memory architecture can support even very demanding applications.



Summary

DAMC-FMC2ZUP is a modern and high-performance AMC board, and with combination of firmware and software is a versatile platform for accelerator controls and diagnostics.

References

[1] J. Zink: High-Speed Direct Sampling FMC for accelerator diagnostics, MTCAWS 2017