LUXE (e^+e^-) detector

Noam Tal Hod

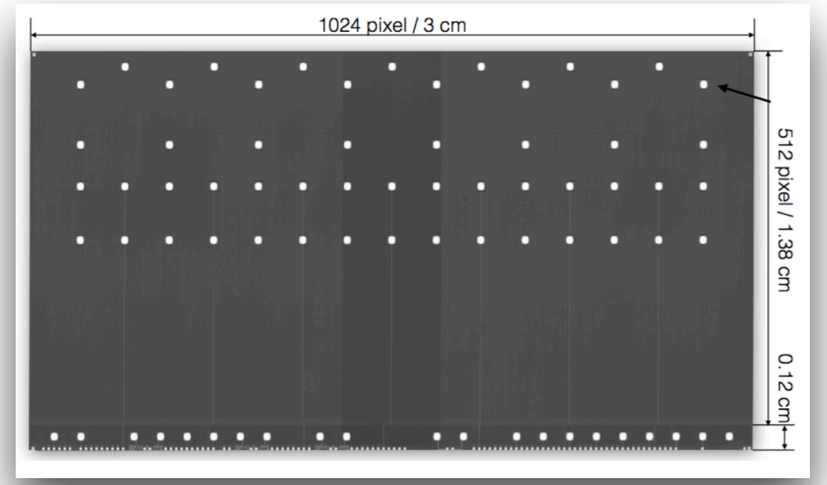
May 7 2019

Recap

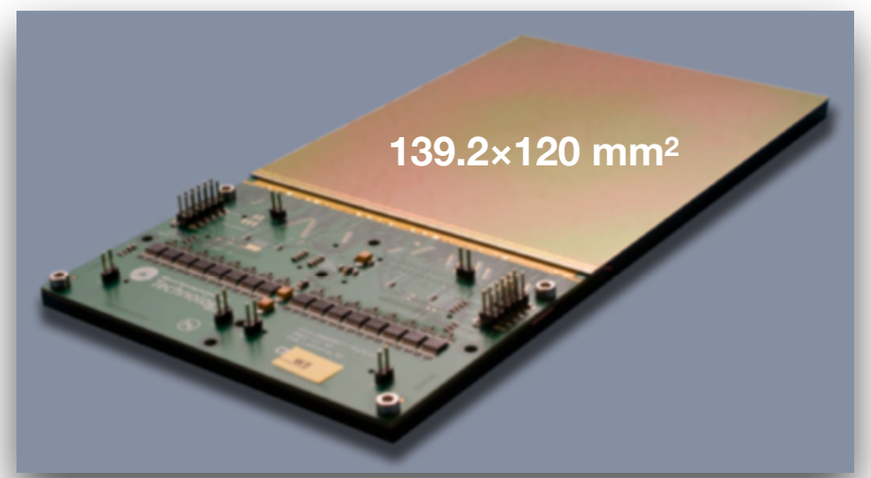
- Review of pixel technologies in the workshop
  - https://indico.desy.de/indico/event/22605/session/4/contribution/7
  - consensus towards ALPIDE/Malta technologies or similar (D)MAPS
- After the workshop:
  - been in touch with Luciano Musa and Heinz Pernegger
  - I presented LUXE in general and the detector plan particularly
  - both are very enthusiastic about the experiment and about the possibility of us using their technologies
  - TowerJazz link: both happy to share the technology
  - discussed several options to move forward including costs (today)

ALPIDE

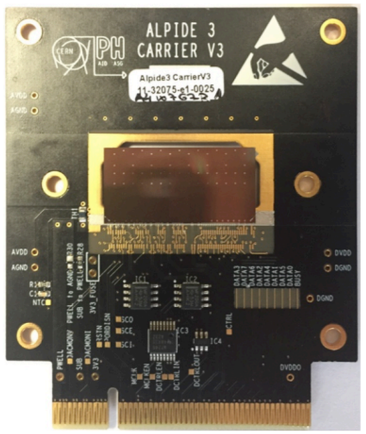
- Really a production module (Chip+DAQ board / HIC)
  - used by ALICE, explored by CLiC
  - proton CT / hadron therapy (several places)
  - sPHENIX (RHIC facility at BNL), NICA (Dubna),
  - few applications for space (on satellites)
- Feature size 27×29 μm^2⟶ resolution of σ~5 μm

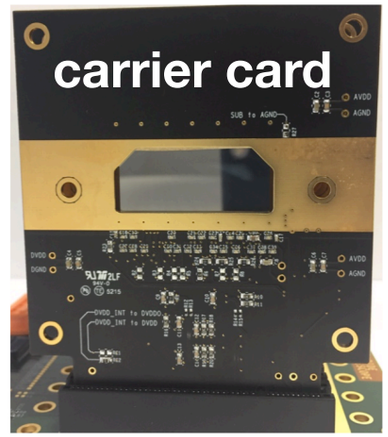


- Time resolution of a few μs
- Probability that a random pixel fires (dark current rate) is very low: ~10^{-5}
  - orders of magnitude lower than hybrid pixels
- Using standard 180 nm TowerJazz technology
  - already modified for HEP (“CERN option”)
  - Stitching: sensor can be as large as the wafer e.g. ~14×14 cm^2 w/o support structures and electrical substrates



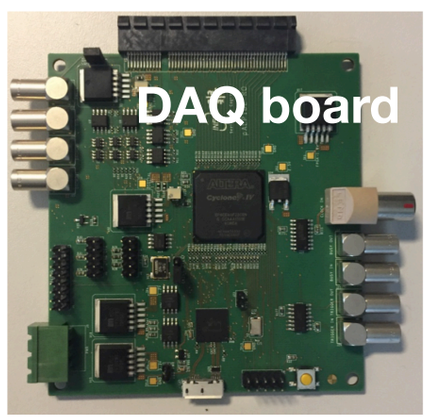
ALPIDE





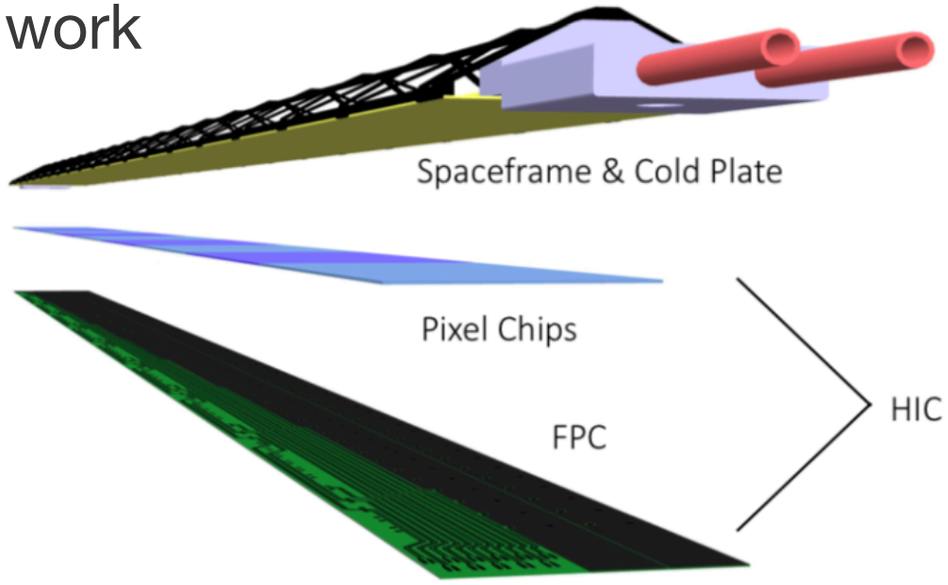
Individual sensors, e.g. for a telescope

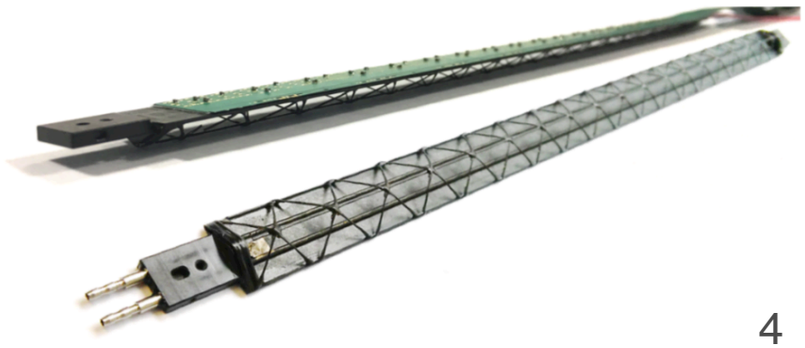
- chip ~3×1.5 cm² + DAQ board (USB interface): >1500 CHF



HIC 27×0.15 cm² (Hybrid Integrated Circuits) modules (staves)

- sensors and board glued on a carbon fibre support structure
- ~13k CHF (“gold category”: >50/500k dead pixels/sensor)
- possible to go longer but requires some engineering work
- each sensor has its own readout line (2 Gb/s)
- standard Samtec cables transmit the signal
- MOSAIC readout system developed in Bari (Italy)
  - can read a few staves simultaneously
- ALICE readout unit (one per stave)
  - GBT link / PCI express ⟶ one PC can in principle handle 24 staves. Given our 10 Hz pulse rate this looks reasonable





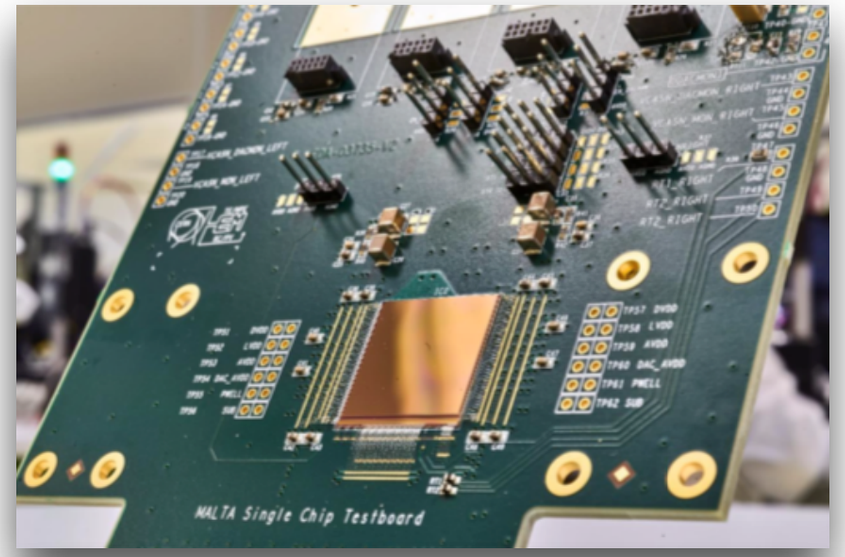
ALPIDE

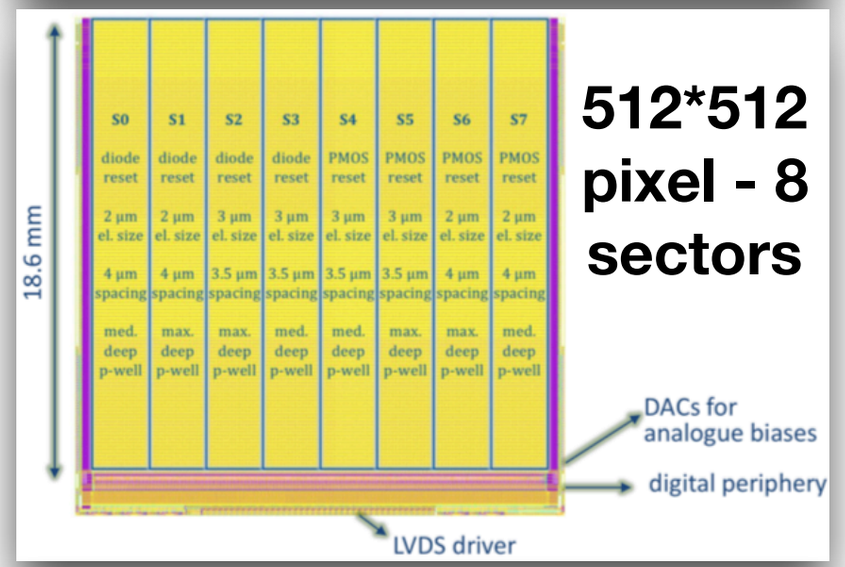
- HICs production flow (approximately):
  1. fabricate sensors at TowerJazz
  2. thinning and dicing in S. Korea / Germany
  3. testing in S. Korea
  4. bonding to PCB, gluing, assembly at CERN
  5. mount on the carbon fibre frame at CERN

- For our needs, the staves solution seems very appealing
  - 4 layers × 2 sides × 2 to cover 50 cm (27×0.15 cm^2 staves):
    - 16 staves + 2 spares… **~234k CHF (could be lower)**
  - computing costs should be small
  - services & patch panels, mechanics & cooling, readout electronics & power supplies, (motorised) alignment system
    - **TBD (probably not below 100k CHF)**

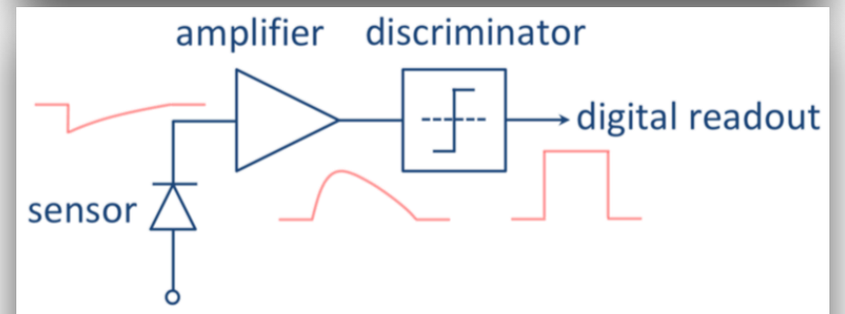
MALTA

- Not yet a production module
  - at least not a large-scale prototype yet
  - R&D target rad-hardness (10^{15} n_{eq}/cm^2) and timing (peaking time<25 ns)
  - Feature size 36.4×36.4 μm^2
    - full matrix has 512x512 pixels
    - active area of ~2x2 cm^2
    - asynchronous readout (reduce digital power consumption, increase hit rate capability, i.e. >100MHz/cm^2)
- A few users already (PSI, high rate proton experiment in Vienna)
- Recent micro-cooling tests are successful
- Can get a test chip from Hienz for free
  - xilinx evaluation board for one sensor at ~2000-3000
- can also buy a full “testbeam setup” (TBC)





512*512 pixel - 8 sectors



- 2-3 um collection electrode → small input capacitance
- 3.4 – 4 um separation between electrode and electronics → low cross talk
- 1 uW/pixel analog power (75 mW/cm²)
- 10 mW/cm² digital power @ layer4

Sensor and analogue front-end (shaper-amplifier and discriminator) shielded from digital part to **minimise crosstalk**

Time walk information preserved

Summary

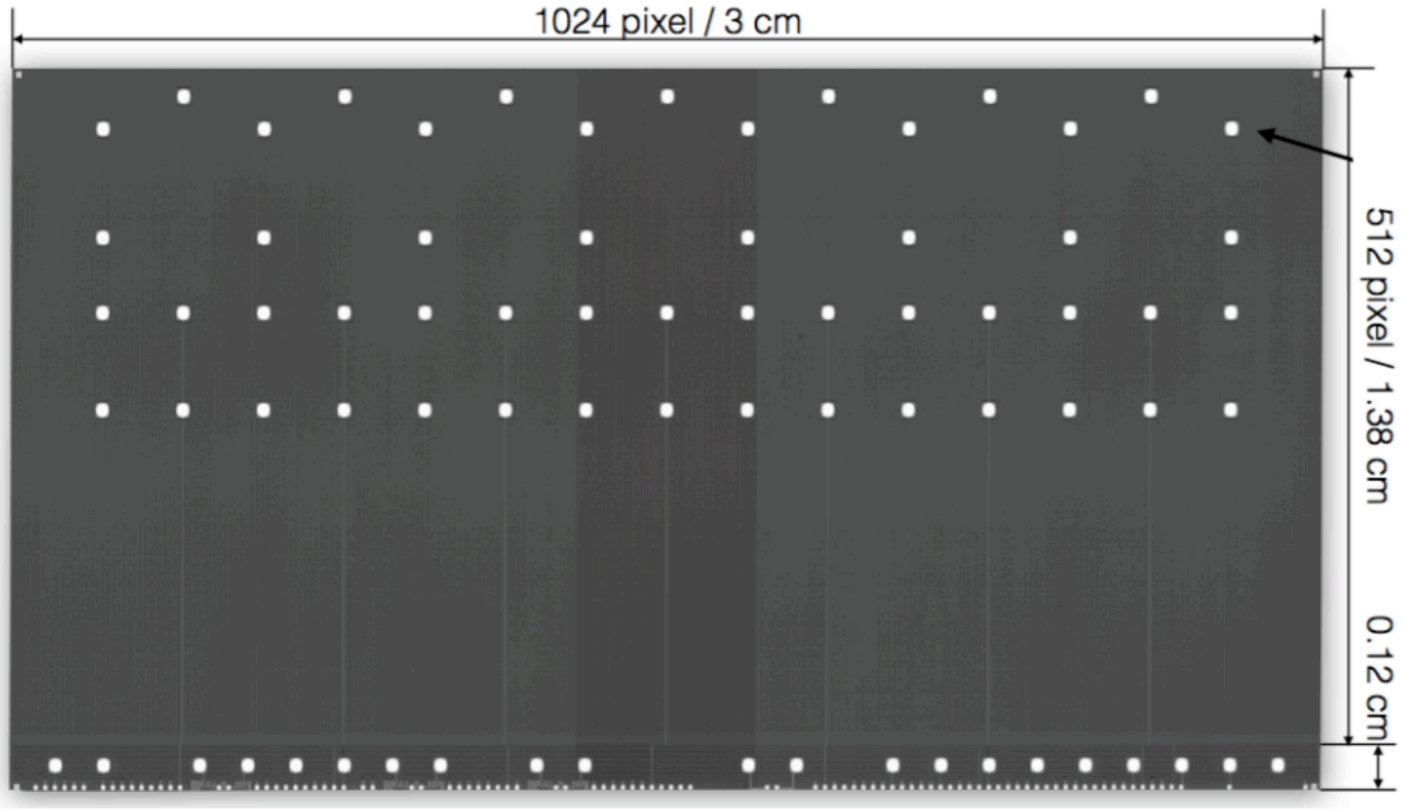
- ALPIDE
  - seems to match our needs, although the timing isn't the best
  - off the shelf, can be ready in a short time, already quite integrated
    - effectively no further design needed ⟶ only some adaptations
  - I will get from Luciano a detailed list of specifications
  - I will get in touch with the ALPIDE simulation people
    - study the detector response, efficiency, etc.
  - New developments target smaller features 10×10 μm^2⟶σ~1 μm, lower power consumption and ~100 ns integration time

- MALTA:
  - very promising and more cutting-edge, but not yet ready
  - will require some non-negligible design/engineering work

- Recommendation:
  - go with ALPIDE in phase0 while checking the developments on the MALTA front for phase1 possibly
  - very preliminary & rough cost: ~350 CHF (with a grain of salt now…)

BACKUP

ALPIDE



- Produced in the TowerJazz 180nm CMOS Imaging Sensor (CIS) process
- Full CMOS within pixel matrix

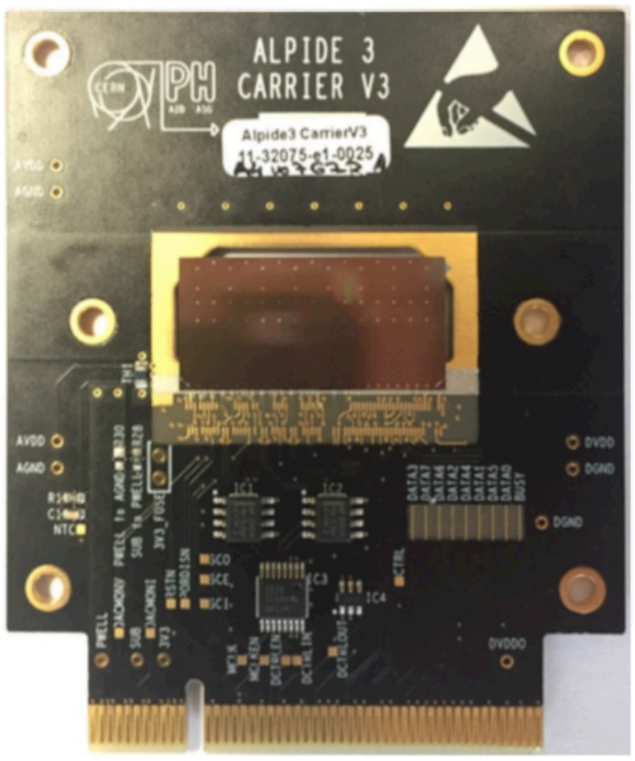
Key concepts:

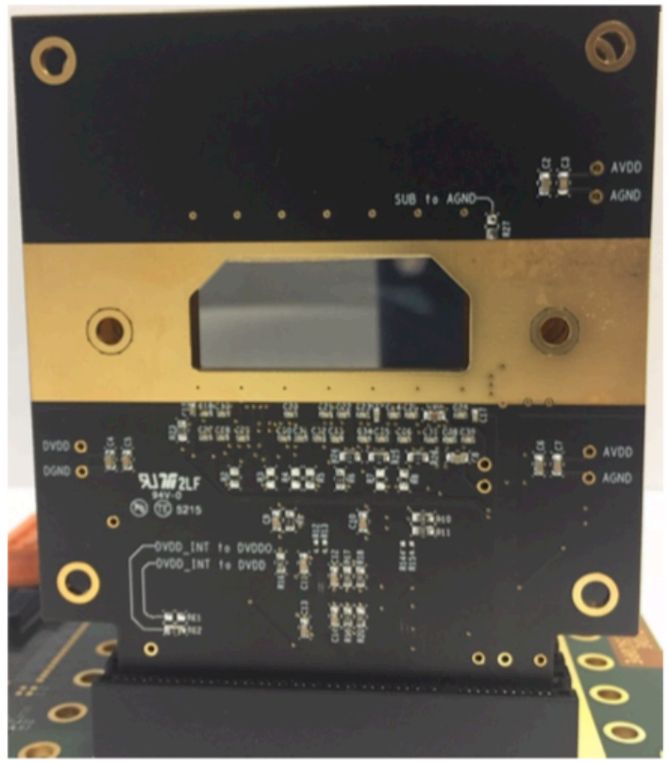
- In-pixel amplification
- In-pixel hit discrimination
- In-pixel 3-level event memory
- In-matrix zero-suppression

Features:

- Dimension: 30mm x 15mm (1024 x 512 pixels)
- Thinned to 50µm (0.05% x/X_0) or 100µm
- Pixel pitch: 29µm x 27µm
- Possibility to apply reverse substrate bias
- Event-time resolution 2-4 µs (charge collection time only 1-30ns, but not exploited)
- Very low power consumption (40mW/cm^2) -> no cooling needed in test beam setup
- Global shutter: triggered acquisition (up to 200 kHz Pb-Pb, 1MHz pp) or continuous (progr. integration time: 1µs - ∞)
- Binary readout
- 1.2 Gbit/s high-speed link, can drive up to 5m of cable
- Two possible connection schemes: pads over the matrix and pads at the periphery

ALPIDE



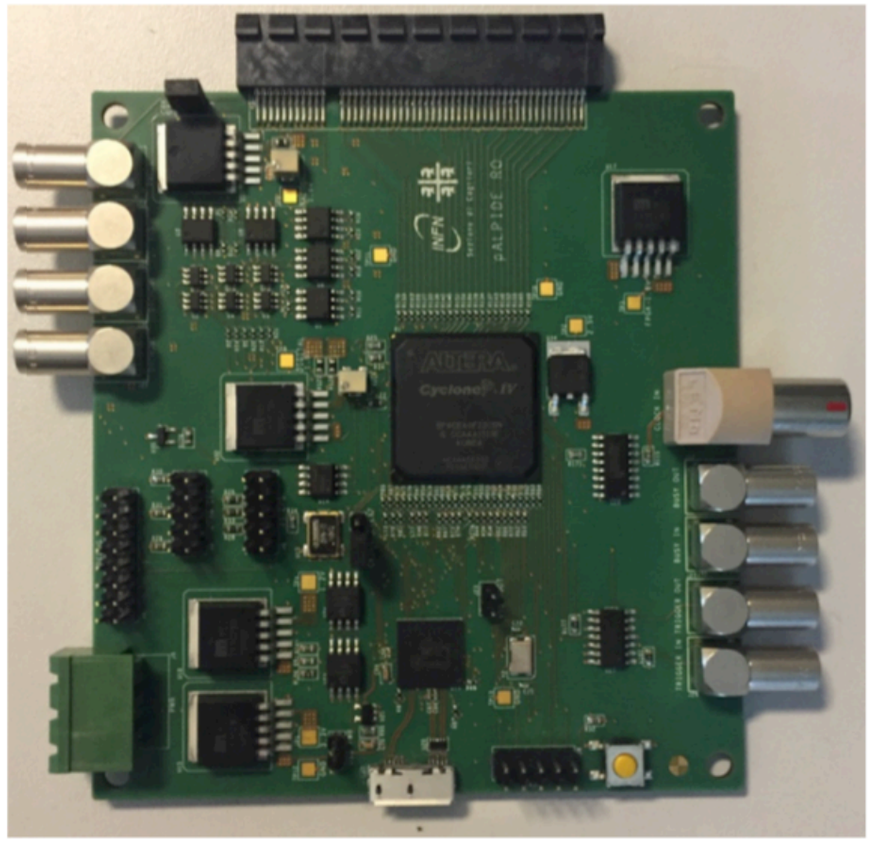


ALPIDE carrier card:

- Large opening underneath ALPIDE to reduce material budget
- PCIe connector used as mechanical and electrical interface (with custom electrical protocol)
- Small pads at periphery used for bonding

DAQ board:

- USB-3.0 for connection to PC
- PCIe connector for carrier card
- Various GPIO connectors



- ALPIDE telescopes typically consist of 7 planes, plane distance ~2cm
- Central chip is typically treated as Device Under Test (DUT)

MALTA asynchronous readout