LUXE pixel tracker

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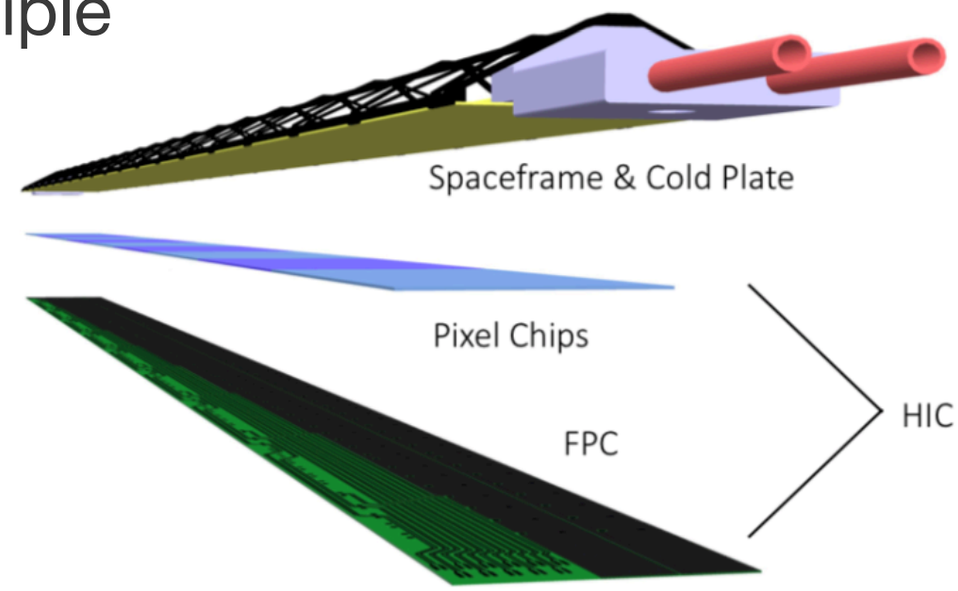
Recap

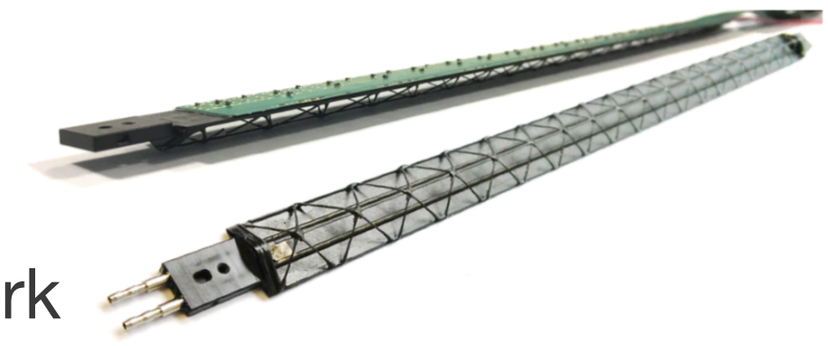
- Review of pixel technologies in the workshop
  - https://indico.desy.de/indico/event/22605/session/4/contribution/7
  - consensus towards ALPIDE/Malta technologies or similar (D)MAPS
- After the workshop:
  - presented realistic (D)MAPS options for LUXE's phase0:
    - https://indico.desy.de/indico/event/23172/
  - proceed with the integrated ALPIDE solution (ALICE ITS)
    - off the shelf, ready in a short time, already integrated
    - effectively no further design needed ⟶ only some adaptations
    - very preliminary cost: ~350 CHF (TBC by early July)
- Today: discussion about agreements and simulation

ALPIDE Simulation

Jouri A. Belikov

- Framework: https://github.com/AliceO2Group/AliceO2
- Based on GEANT3
  - much faster than GEANT4 (problem for the HL-LHC)
  - but, compatible also with GEANT4 in principle
- Not simulating the electronics response
- LHC standard simulation flow concept
  - particles ⟶ hits ⟶ clusters ⟶ tracks
  - particles: physics part (e.g. “particle gun”)
  - hits part is the digitised detector response
  - clustering and tracking is reconstruction
- Stave geometry already implemented
  - carbon fibre support, flex cables etc.
  - can be configured from a file ⟶ most of our work
- Sensors' response already integrated
- Input: basically TParticle ROOT object
- Output: {x,y,z} position and energy deposition





Some formalities

- Discussing with Luciano Musa (CERN), there's a mutuel will to try to keep the procedure as simple as possible
- The ALPIDE circuit is a rad-hard component and therefore it is subject to restrictions of its export license, which are set by the Israeli authorities
- For a few samples distributed in Europe, the signature of a compliance letter is sufficient
  - stating that the sensors will be used for a scientific research in particle physics and in no case the circuits will be used for other applications or exported to another country
- If we decide to build the entire tracker using the ALPIDE sensors or the ALICE ITS staves, including the readout electronics, it would be better to have an MoU between CERN and DESY, defining the scope and terms of the agreement
  - since in this case DESY would become the end-user of the sensors, we will also need to sign the "End User Statement" to obtain a license from the Israeli export control office (it belongs to the ministry of commerce)
  - in practise, TowerJazz takes care of that and the procedure, which is rather straightforward, takes a couple of weeks
- Payment: CERN can either issue an invoice to DESY, in the framework of a scientific collaboration, or DESY can do the payment via a CERN team account

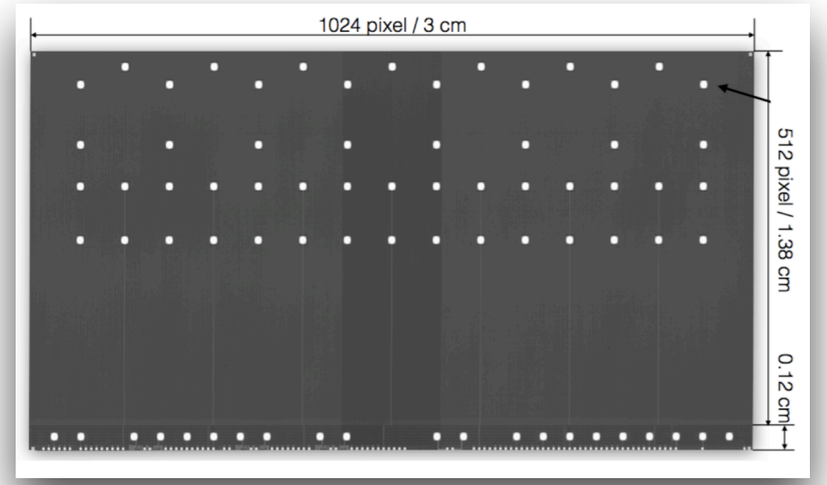
Summary

- ALPIDE samples
  - Beate, Matt and me (at least) are interested in a few samples
  - Matt is interested to build Jena a smaller replica of what we will eventually do in LUXE and that is could be a good experience
- ALICE ITS staves
  - agreements should be written (easy)
    - I will ask Luciano for templates of these
- Tracker services costs: I will meet with Luciano at CERN in early July
- Simulation: I'm starting to test it locally (after writing my LoI part)
- Design issues:
  - start thinking about the motorised stages (space drawings?)
  - start thinking about the trigger (laser?)
  - start thinking about the tracker+calorimeter integration

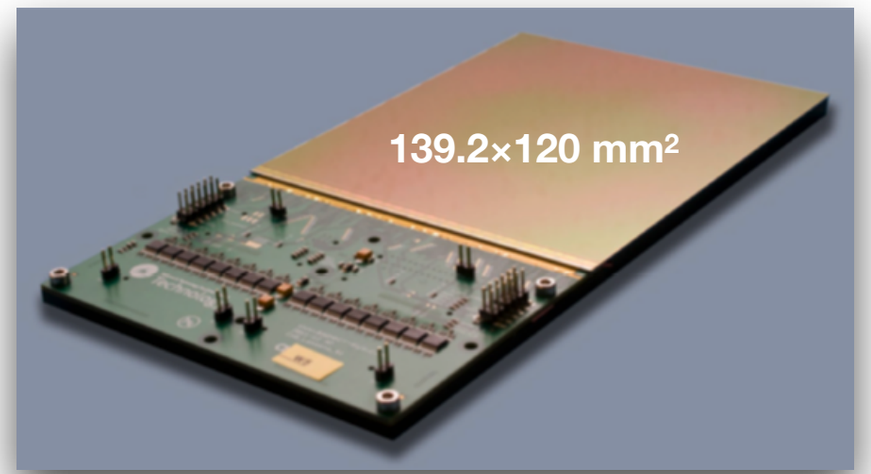
BACKUP

ALPIDE

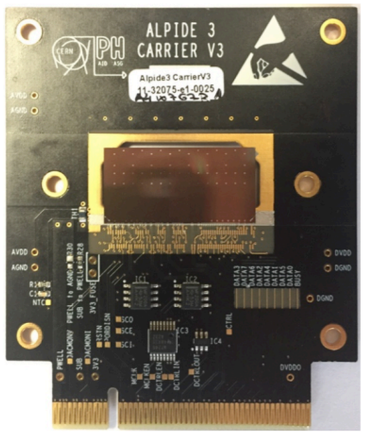
- Production module (Chip+DAQ board / HIC)
  - used by ALICE, explored by CLiC
  - proton CT / hadron therapy (several places)
  - sPHENIX (RHIC facility at BNL), NICA (Dubna),
  - few applications for space (on satellites)
- Feature size 27×29 μm^2⟶ resolution of σ~5 μm

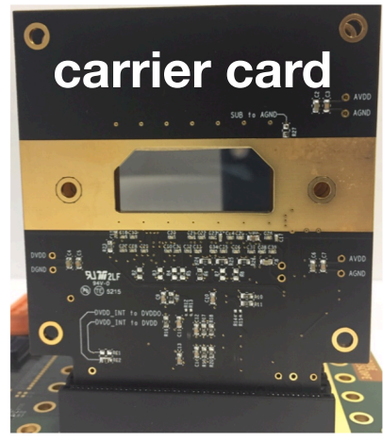


- Time resolution of a few μs
- Probability that a random pixel fires (dark current rate) is very low: ~10^{-5}
  - orders of magnitude lower than hybrid pixels
- Using standard 180 nm TowerJazz technology
  - already modified for HEP (“CERN option”)
  - Stitching: sensor can be as large as the wafer e.g. ~14×14 cm^2 w/o support structures and electrical substrates



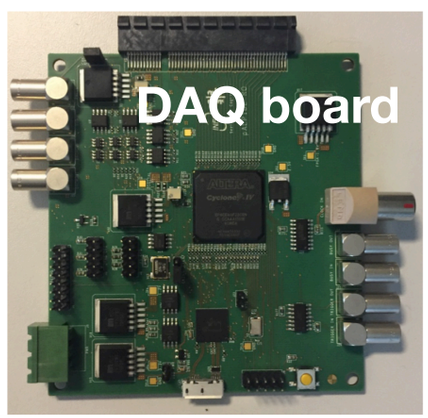
ALPIDE





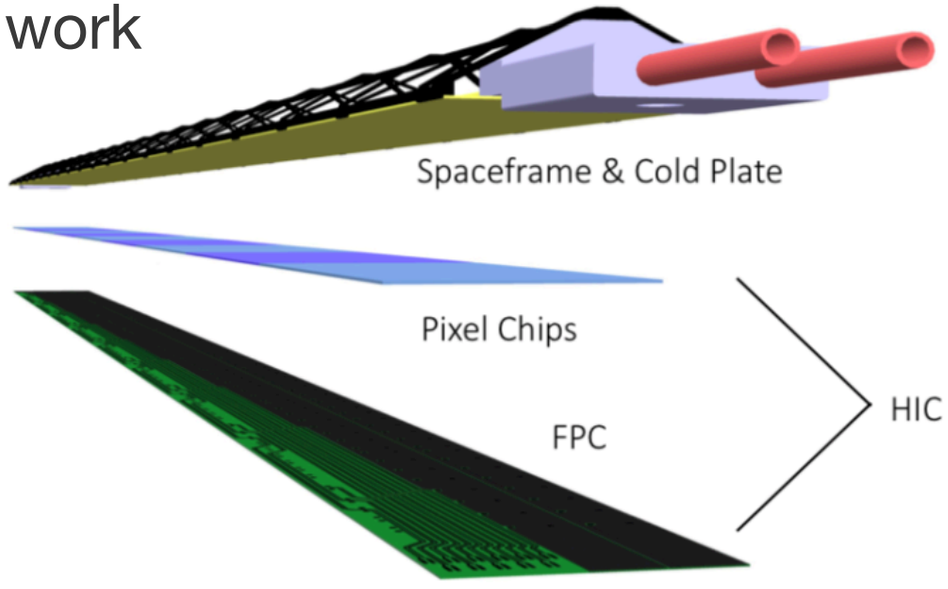
Individual sensors, e.g. for a telescope

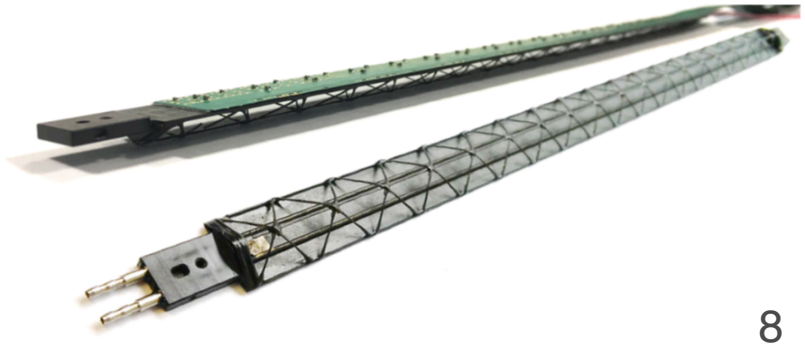
- chip ~3×1.5 cm² + DAQ board (USB interface): >1500 CHF



HIC 27×0.15 cm² (Hybrid Integrated Circuits) modules (staves)

- sensors and board glued on a carbon fibre support structure
- ~13k CHF (“gold category”: >50/500k dead pixels/sensor)
- possible to go longer but requires some engineering work
- each sensor has its own readout line (2 Gb/s)
- standard Samtec cables transmit the signal
- MOSAIC readout system developed in Bari (Italy)
  - can read a few staves simultaneously
- ALICE readout unit (one per stave)
  - GBT link / PCI express ⟶ one PC can in principle handle 24 staves. Given our 10 Hz pulse rate this looks reasonable



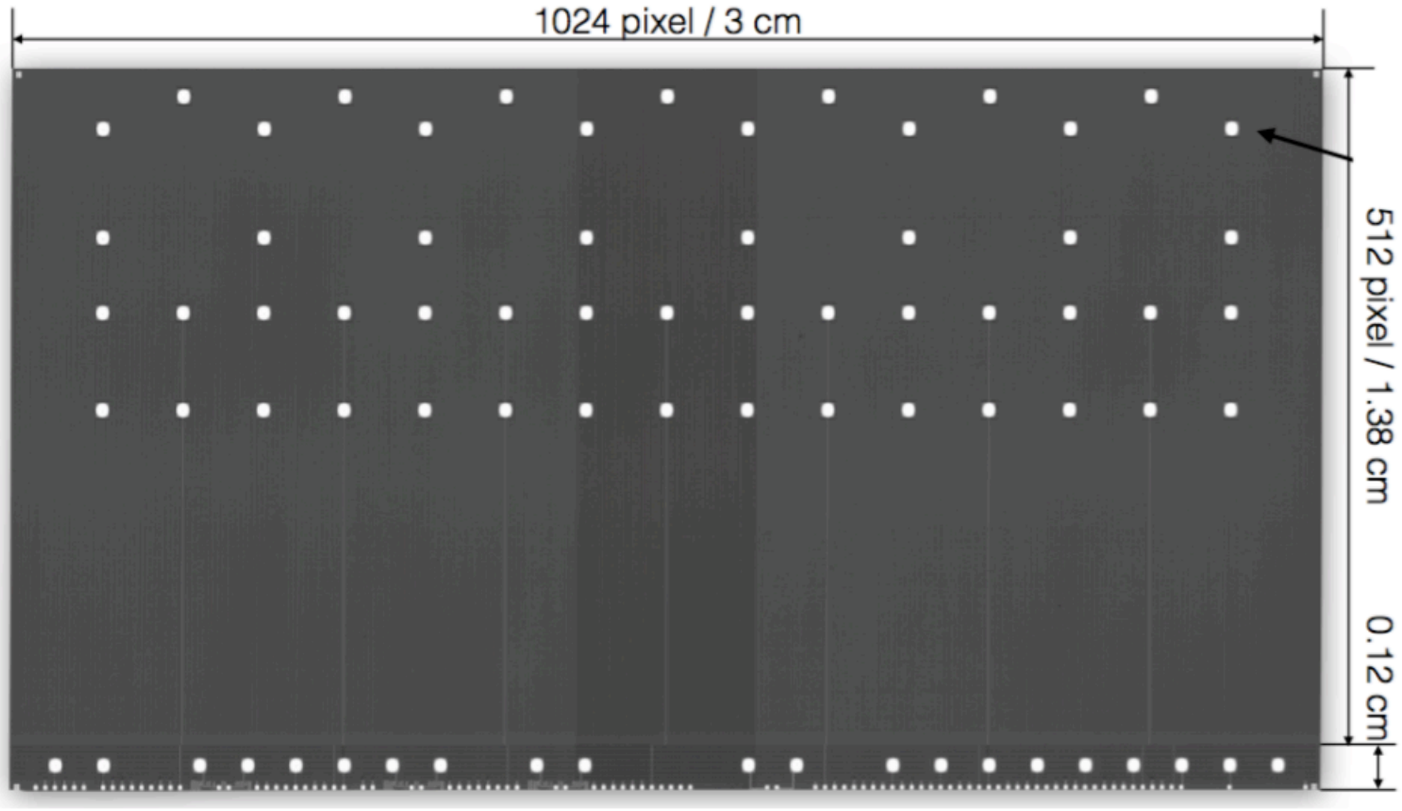


ALPIDE

- HICs production flow (approximately):
  1. fabricate sensors at TowerJazz
  2. thinning and dicing in S. Korea / Germany
  3. testing in S. Korea
  4. bonding to PCB, gluing, assembly at CERN
  5. mount on the carbon fibre frame at CERN

- For our needs, the staves solution seems very appealing
  - 4 layers × 2 sides × 2 to cover 50 cm (27×0.15 cm^2 staves):
    - 16 staves + 2 spares… **~234k CHF (could be lower)**
  - computing costs should be small
  - services & patch panels, mechanics & cooling, readout electronics & power supplies, (motorised) alignment system
    - **TBD (probably not below 100k CHF)**

ALPIDE



- Produced in the TowerJazz 180nm CMOS Imaging Sensor (CIS) process
- Full CMOS within pixel matrix

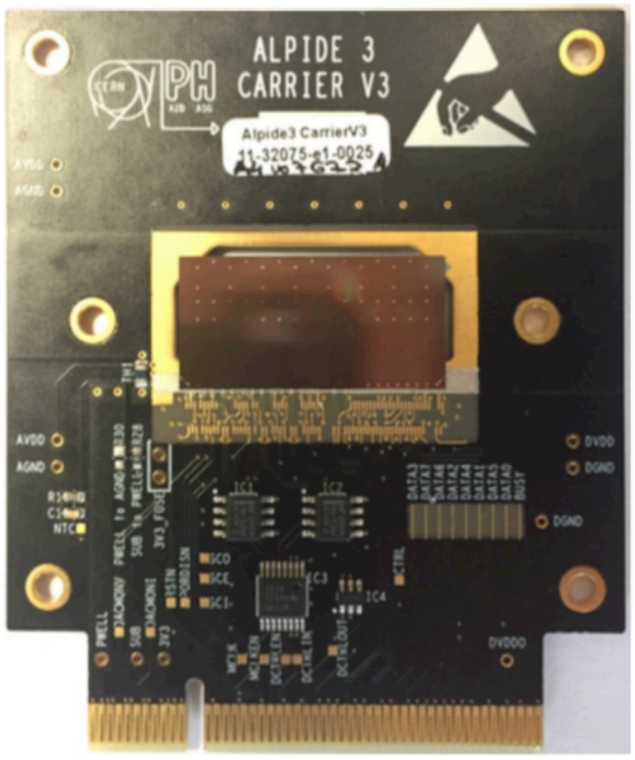
Key concepts:

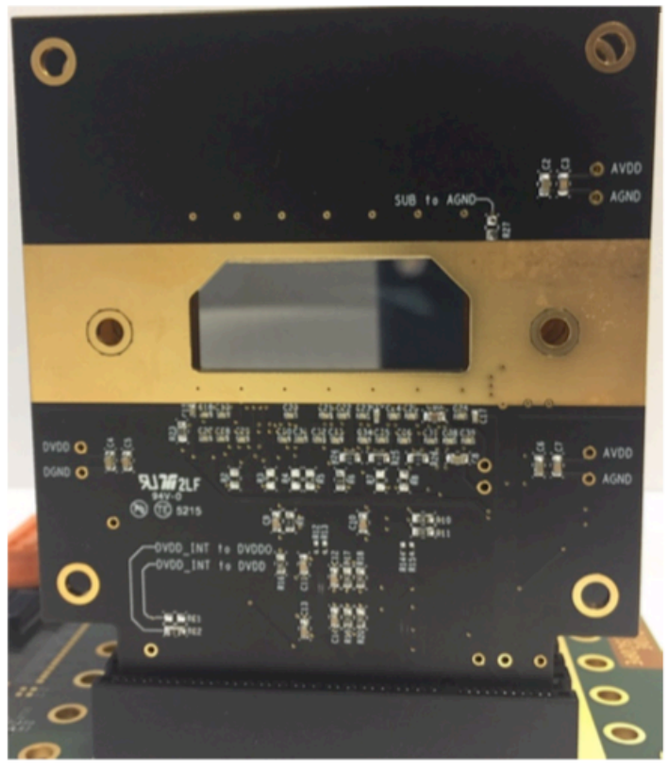
- In-pixel amplification
- In-pixel hit discrimination
- In-pixel 3-level event memory
- In-matrix zero-suppression

Features:

- Dimension: 30mm x 15mm (1024 x 512 pixels)
- Thinned to 50µm (0.05% x/X_0) or 100µm
- Pixel pitch: 29µm x 27µm
- Possibility to apply reverse substrate bias
- Event-time resolution 2-4 µs (charge collection time only 1-30ns, but not exploited)
- Very low power consumption (40mW/cm^2) -> no cooling needed in test beam setup
- Global shutter: triggered acquisition (up to 200 kHz Pb-Pb, 1MHz pp) or continuous (progr. integration time: 1µs - ∞)
- Binary readout
- 1.2 Gbit/s high-speed link, can drive up to 5m of cable
- Two possible connection schemes: pads over the matrix and pads at the periphery

ALPIDE



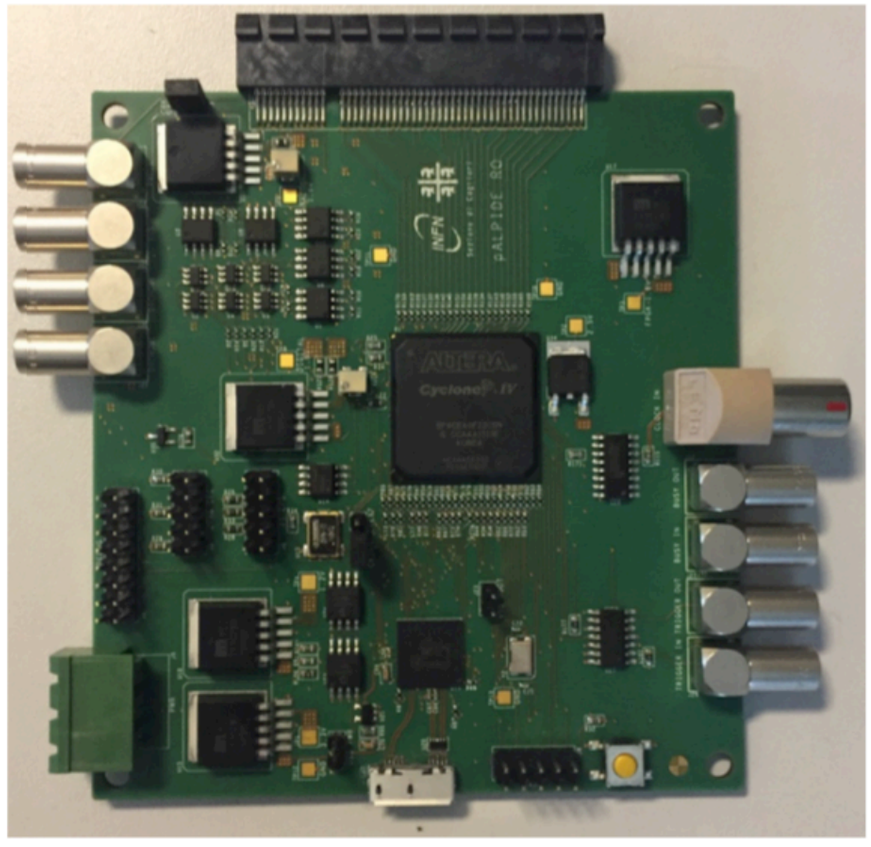


ALPIDE carrier card:

- Large opening underneath ALPIDE to reduce material budget
- PCIe connector used as mechanical and electrical interface (with custom electrical protocol)
- Small pads at periphery used for bonding

DAQ board:

- USB-3.0 for connection to PC
- PCIe connector for carrier card
- Various GPIO connectors



- ALPIDE telescopes typically consist of 7 planes, plane distance ~2cm
- Central chip is typically treated as Device Under Test (DUT)