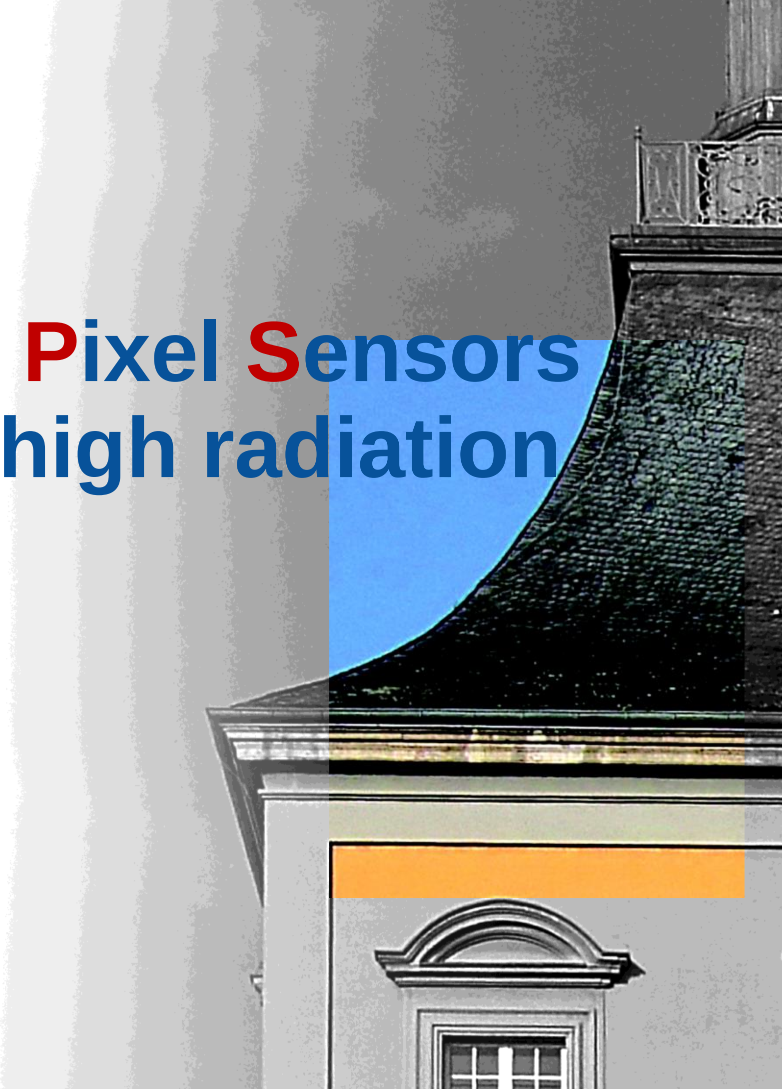
Depleted Monolithic Active Pixel Sensors (DMAPS) for high rate and high radiation experiments at HL-LHC

and other works

Toko Hirono (University of Bonn)



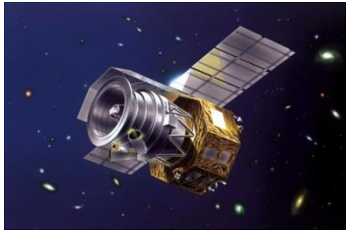
Outline

- Introduction
- Development of depleted monolithic active pixel sensors
  - Motivation
  - Design concepts
  - Results of characterization
  - Conclusion
- Overview of other works
- Summary

Reference = Author

Intorduction

- Toko Hirono
  - 2000: Master‘s degree in astrophysics (Nagoya Uni., Japan)
    - Development of far-infrared detector for Japan’s astronomical satellite

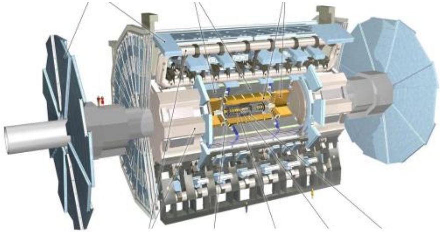


https://global.jaxa.jp/projects/sas/astro_f/

  - 2000-2014: “Research scientist“ (permanent position) in a synchrotron radiation facility (SPring-8, Japan)
    - Upgrade and development of control and data acquisition system for accelerators and beamlines
    - Development of detector for high energy X-ray

http://xfel.riken.jp/eng/gallery/index.htm

  - 2014-4/2019: PhD in high energy particle physics (Uni. Bonn, Germany)
    - Characterization of pixel detector for high energy particle physics experiments

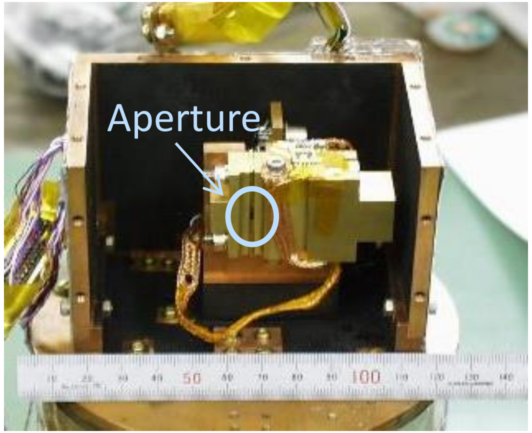


https://atlas.cern/discover/detector

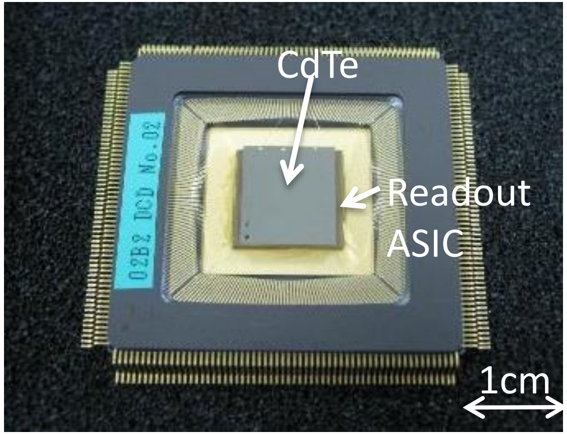
Works in many different fields of physics

Common in my works

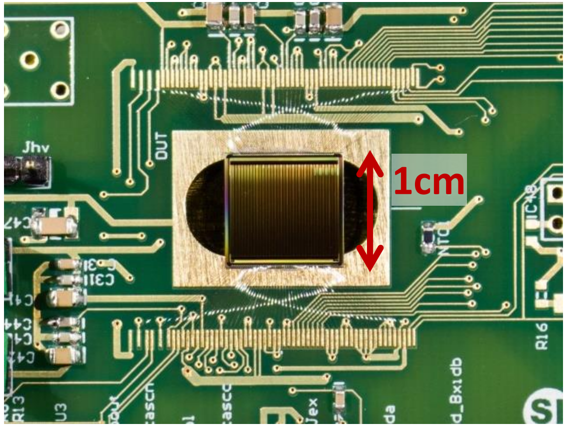
❑ Master thesis
Ge:Ga 2D array detector



❑ SPring-8
CdTe hybrid pixel detector



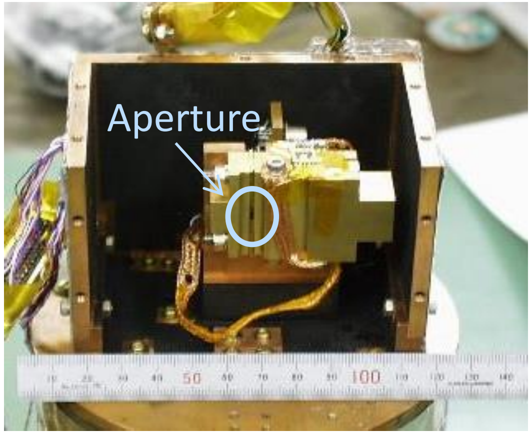
❑ PhD. thesis
Monolithic active pixel sensor



➡ Study on semiconductor detectors

Common in my works

☐ Master thesis
Ge:Ga 2D array detector



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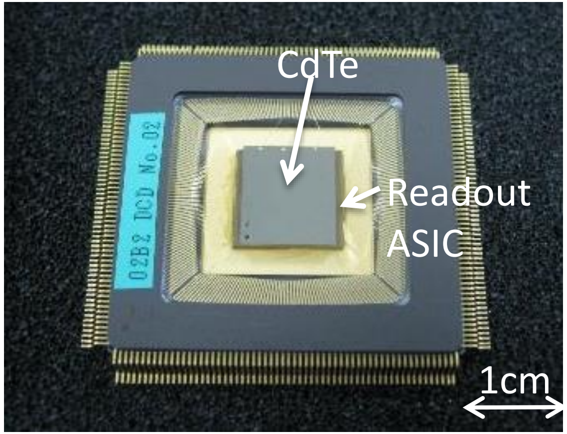
CdTe hybrid pixel detector



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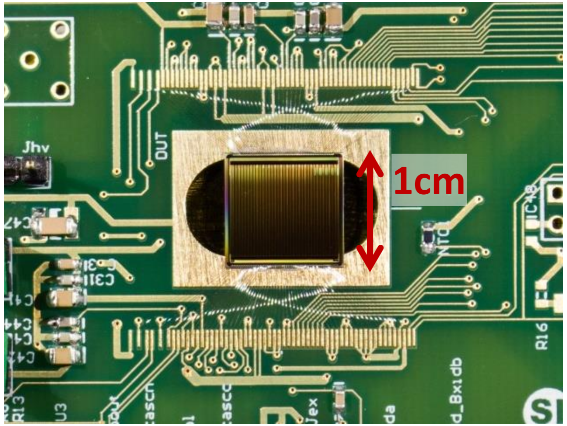
Monolithic active pixel sensor

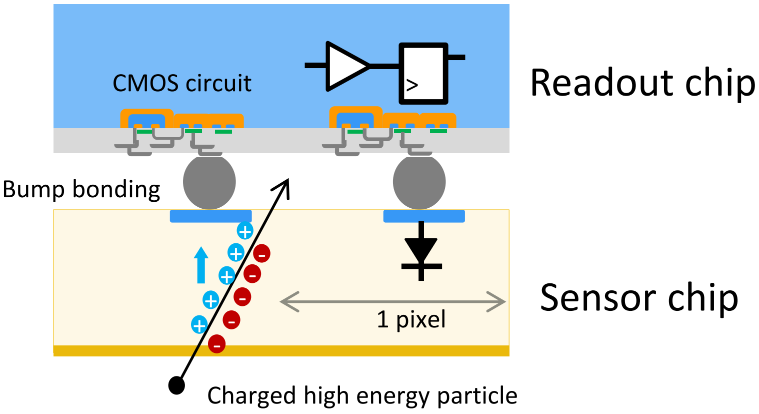


➡ Study on semiconductor detectors

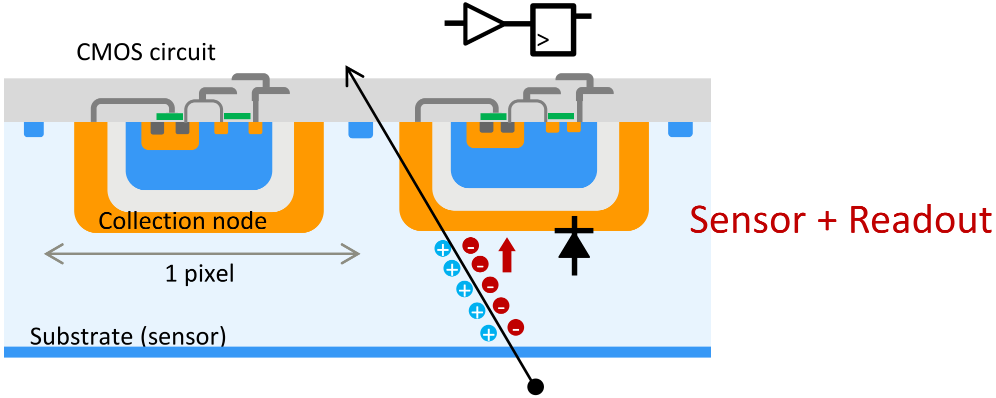
Deplete Monolithic Active Pixel Sensors (DMAPS)
for high rate and high radiation experiments at HL-LHC

What is
(Delpeted) Monolithic Active Pixel Sensors

❑ Hybrid Pixel Detector



❑ Monolithic Active Pixel Sensor (MAPS)



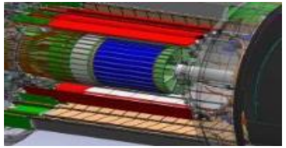
MAPS has the sensing part and the readout electronics in one chip

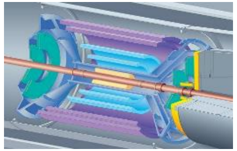
→ No fine pitch bump bonding between sensor and readout circuitry

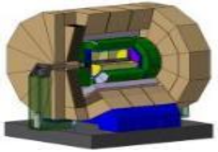
- Less material
- Cost saving, high wafer throughput, schedule saving

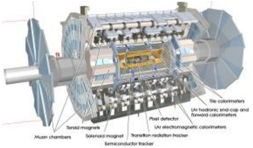
UNIVERSITÄT BONN

Requirements for pixel detector layers in high energy particle physics


STAR


ALICE-LHC


ILC


ATLAS

	STAR	**ALICE-LHC**	**ILC**	**ATLAS-LHC**	**ATLAS-HL-LHC**	
					Outer	Inner
Timing [ns]	110	20 000	350	25	**25**	25
Particle Rate [kHz/mm^2]	3.8	10	250	1000	1000	10000
Fluence [n$_{eq}$/cm^2]	> 10^{12}	> 10^{13}	10^{12}	2x10^{15}	**1-2x10^{15}**	2x10^{16}
Ion. Dose [Mrad]	0.09/year	0.7	0.4	80	**50-80**	>500

MAPS

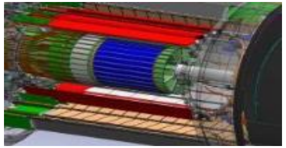
- High spatial resolution
- Low hit-rate
- High radiation tolerance

Hybrid detector

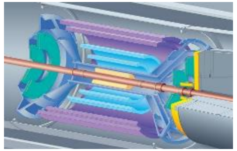
- Fast response
- High hit-rate
- High radiation tolerance

Requirements for pixel detector layers in high energy particle physics

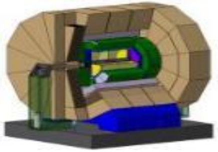
STAR



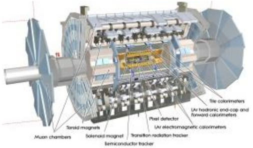
ALICE-LHC



ILC



ATLAS



	STAR	ALICE-LHC	ILC	ATLAS-LHC	ATLAS-HL-LHC	
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Ion. Dose [Mrad]	0.09/year	0.7	0.4	80	**50-80**	>500

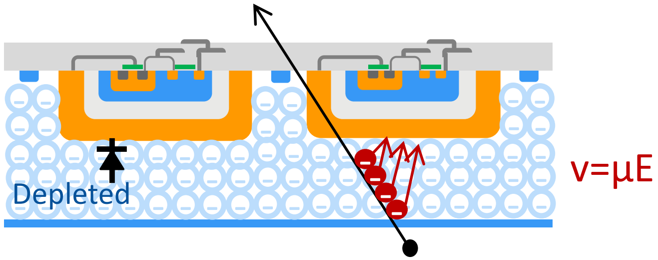
?

In my PhD dissertation,

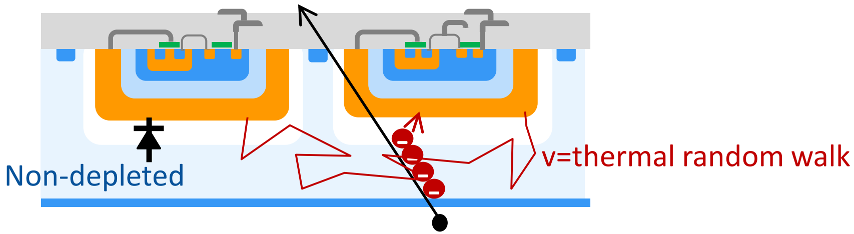
suitability of DMAPS for outer layers of future ATLAS Pixel Detectors has been investigated

Why Depleted Monolithic Active Pixel Sensor?

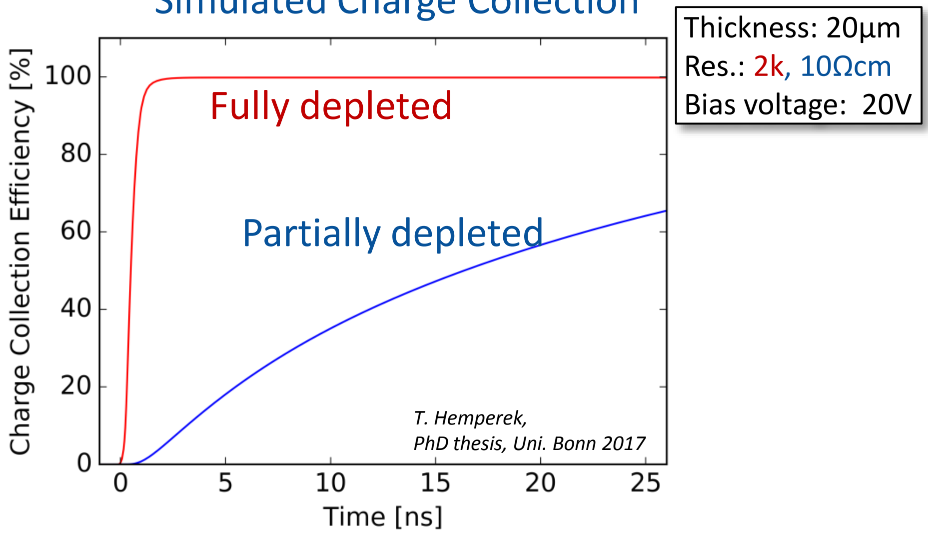
☐ Charge collection mainly by drift



☐ Charge collection mainly by diffusion



Simulated Charge Collection



T. Hemperek,
PhD thesis, Uni. Bonn 2017

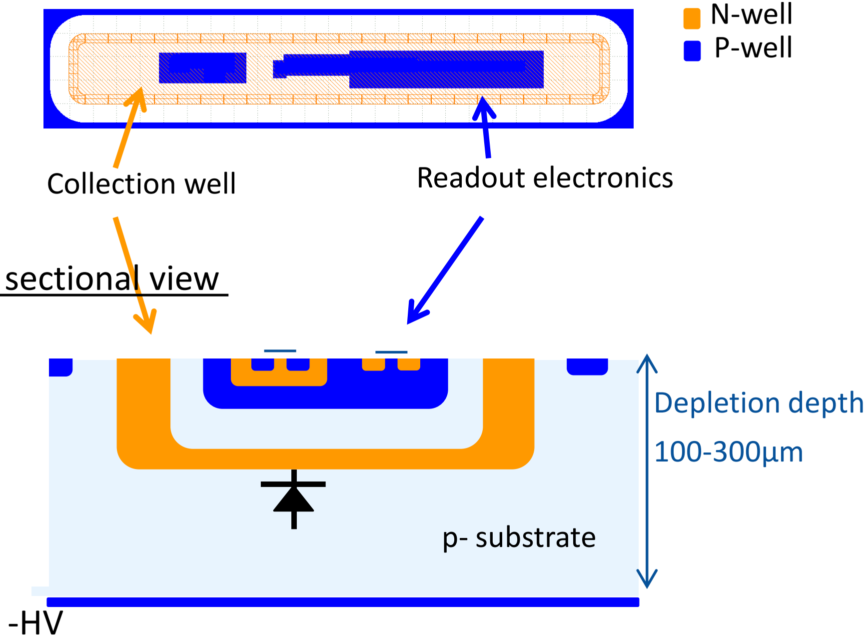
Charge collection by drift is mandatory ➡ Depleted Monolithic Active Pixel Sensor (**DMAPS**)

Two DMAPS designs

❑ **Large** collection electrode design

Top view

Cross sectional view



▰ N-well
▰ P-well

Collection well

Readout electronics

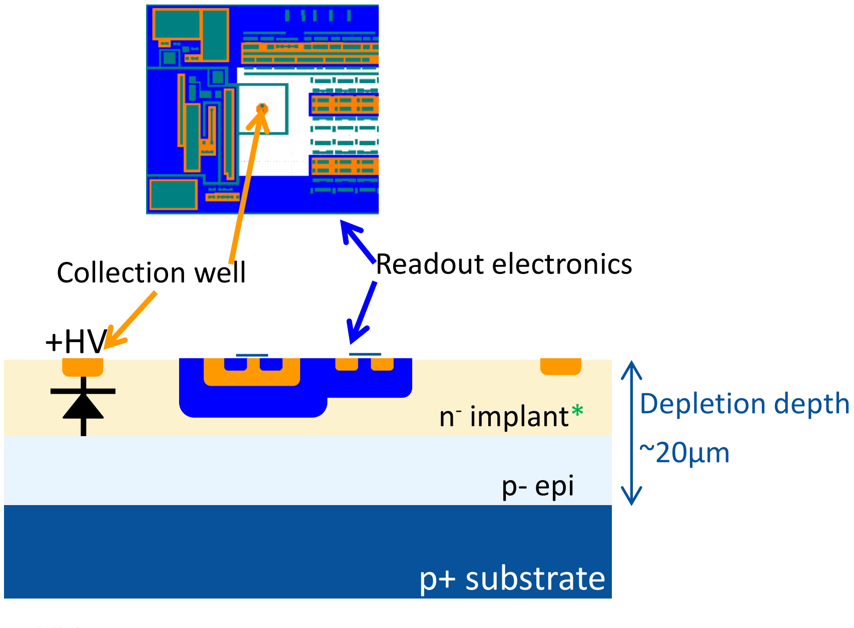
Depletion depth

100-300µm

p- substrate

-HV

❑ **Small** collection electrode design



Collection well

Readout electronics

+HV

n$^-$ implant*

p- epi

p+ substrate

Depletion depth

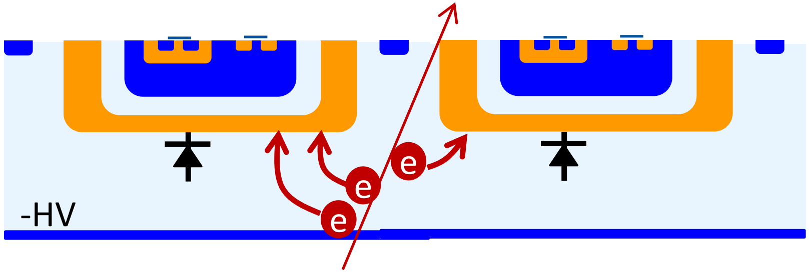
~20µm

-HV

*W. Snoeys et al, 2017 NIMA **871** 90*

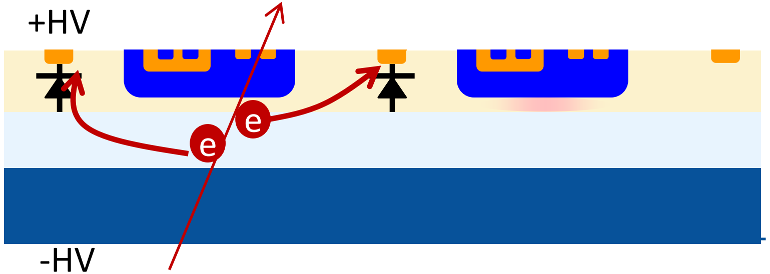
Two DMAPS designs: Radiation hardness

- ☐ **Large** electrode design
  = Small gap between electrode
  = Readout electronics is isolated from substrate



- – Short charge drift path ☺
  → High radiation hardness
- – High bias voltatge + highly resistive wafer ☺
  → Large depletion area
  → Large signal

- ☐ **Small** electrode design
  = Large gap (~pixel size) between electrodes



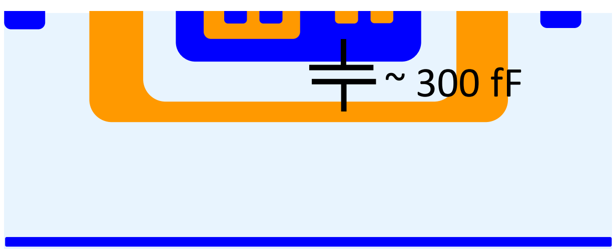
- – Long charge drift path ☹
- – The electric field directing the collection electrode is weak at the pixel edge ☹

Two designs: Power consumption

- ☐ **Large** electrode design = Large C_{det}

Response time of amplifier: $\tau_{CSA} \approx \frac{1}{g_m}\frac{C_{det}}{C_f}$

Noise: $ENC^2_{thermal} \approx \frac{4}{3}\frac{kT}{g_m}\frac{C}{\tau_f}$



→ High power consumption ☹

→ Delicate electronics design to aviod signal cross coupling between the colleciton node and readout electronics ☹

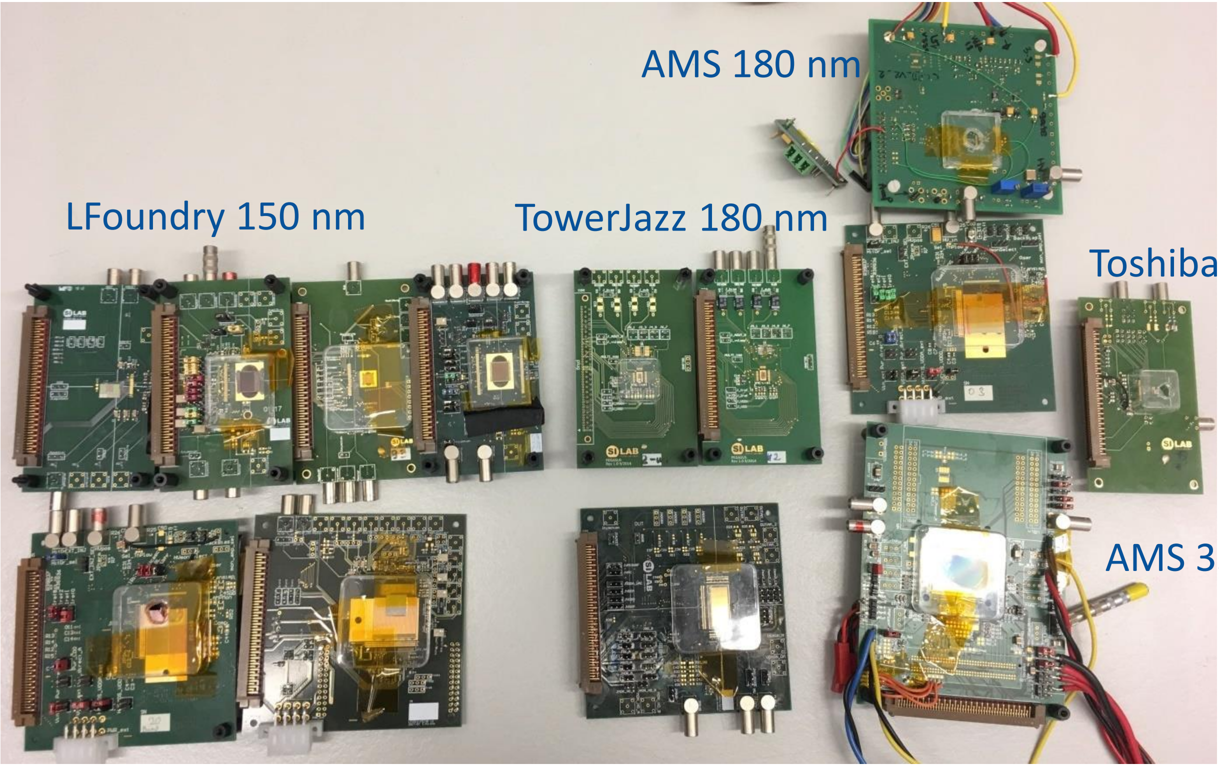
- ☐ **Small** electrode design = Small C_{det}

Signal to noise: $\frac{S}{N} \approx \frac{Q/C_{det}}{\sqrt{g_m}} \sim \frac{Q/C_{det}}{\sqrt[m]{P}}, \quad P \sim \left(\frac{Q}{C_{det}}\right)^{-m}$

→ Low power consumption ☺

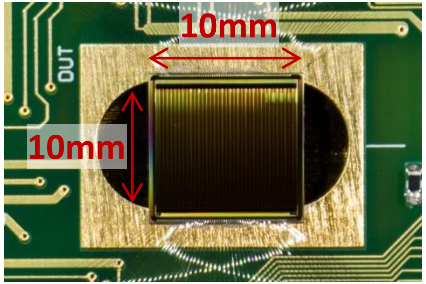
→ Less sensitive to cross coupling ☺

Prototypes I worked with



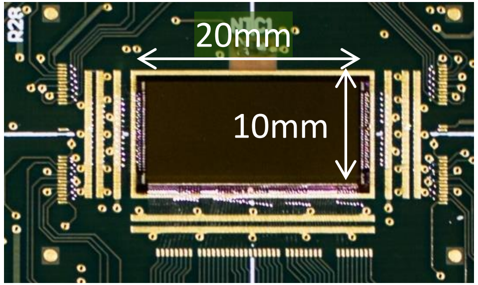
Fully-monolithic large-scale prototypes

❑ **Large** electrode design: LF-Monopix



- Fully monolithic
- LFoundry 150nm CMOS process
- Sensitive volume: >2kΩcm highly resistive substrate
  Thickness = 100µm, 200µm (725µm)
- Pixel size: 250µm × 50µm
- Bonn/CPPM/IRFU

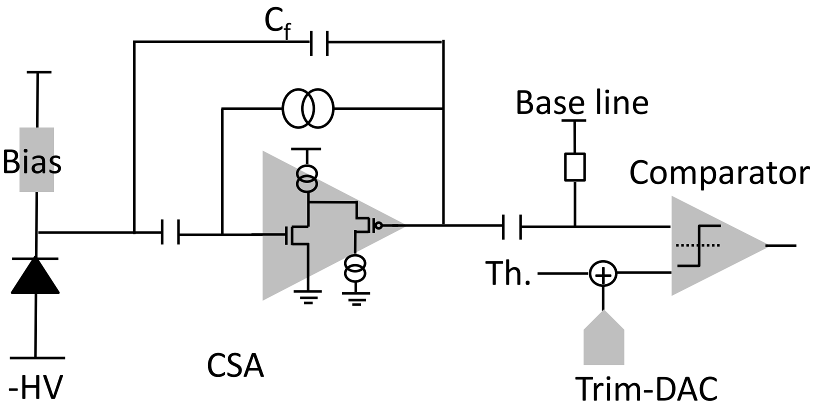
❑ **Small** electrode design: TJ-Monopix



- Fully monolithic
- TowerJazz 180nm CMOS process w/ n^- implant
- Sensitive volume: n^- implant + 1kΩcm epi-layer
  Thickness = ~20µm
- Pixel size: 40µm × 36µm
- Bonn/CERN

In-Pixel electronics (Analog frontend)

- **Large** electrode design: LF-Monopix



- **Small** electrode design: TJ-Monopix

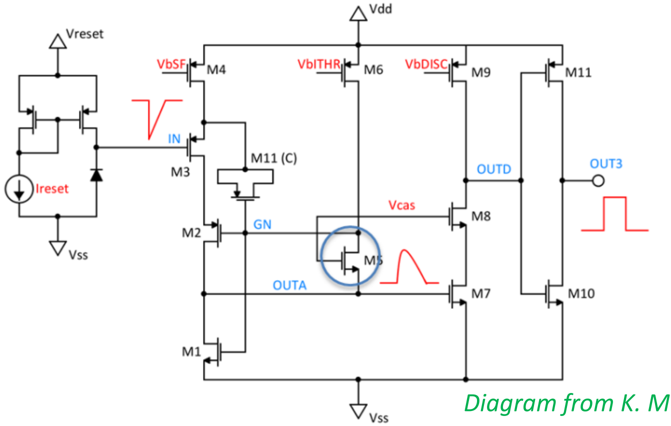


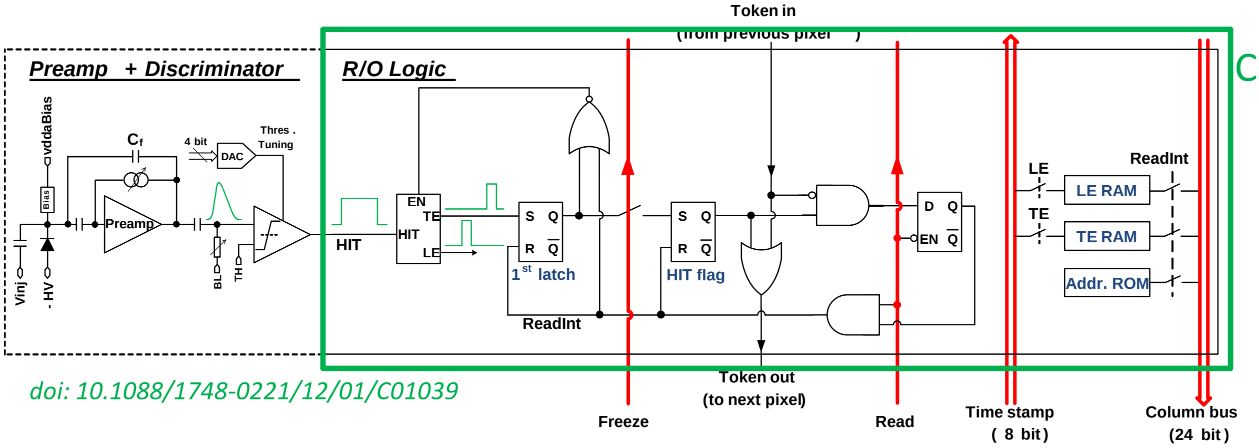
Diagram from K. Moustakas et al, IEEE NSS2017

- Power-saving analog frontend
  - CSA
  - Discriminator + w/ 4-bit trim DAC

- Space-saving, high-gain-low-noise analog frontend
  - Novel preamp and discriminator drive from ALPIDE
  - w/o trim DAC

In-Pixel electronics (Digital R/O logics)

Fully synchronous column drain architecture



Common in both prototypes

doi: 10.1088/1748-0221/12/01/C01039

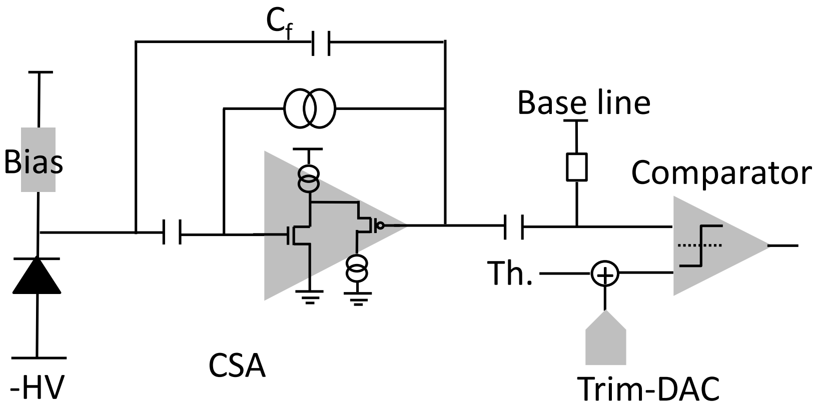
❑ **Large** electrode design: LF-Monopix
- R/O logic: 8-bit ToA and ToT (40MHz)

❑ **Small** electrode design: TJ-Monopix
- R/O logic: 6-bit ToA and ToT (40MHz)

Column drain architecture has been used in current ATLAS pixel readout chip (FE-I3)
Hit-rate: Outer layers of ATLAS ITk pixel detectors ≈ Current ATLAS ID pixel detectors

In-Pixel electronics (Analog frontend)

❑ **Large** electrode design: LF-Monopix



- Power-saving analog frontend
  - CSA
  - Discriminator + w/ 4-bit trim DAC

❑ **Small** electrode design: TJ-Monopix

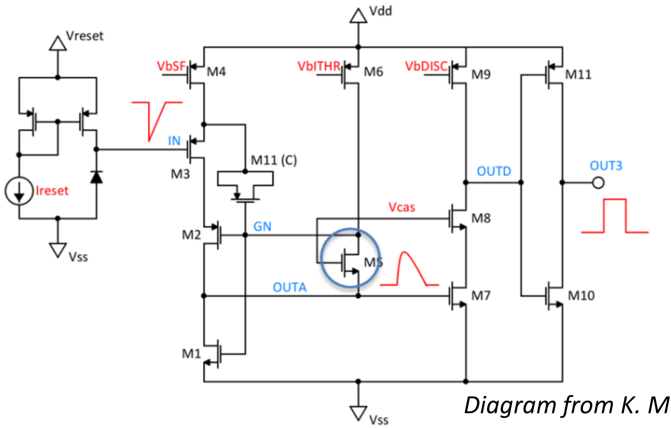
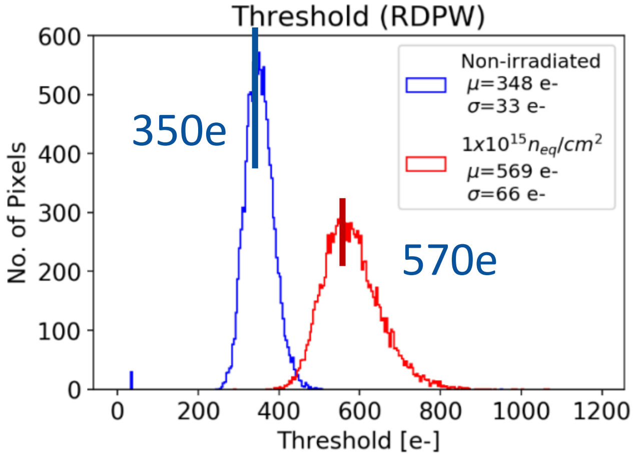


Diagram from K. Moustakas et al, IEEE NSS2017

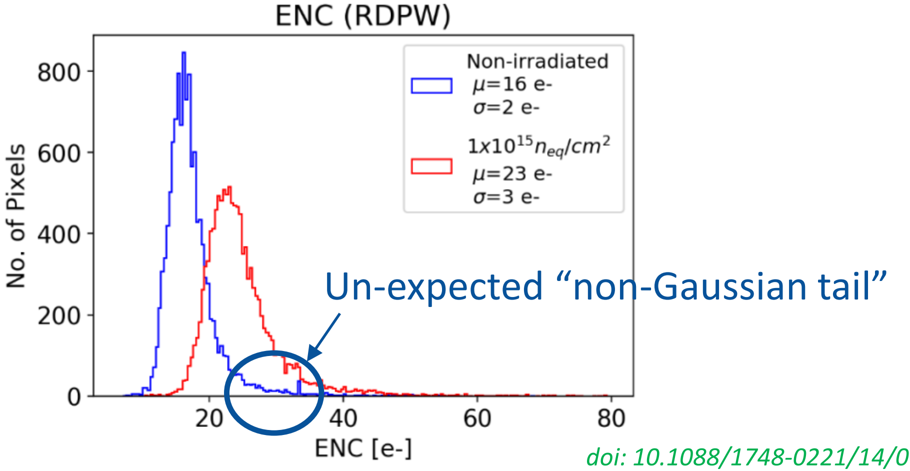
- Space-saving, high-gain-low-noise analog frontend
  - Novel preamp and discriminator drive from ALPIDE
  - w/o trim DAC

ANALOG frontend for Small electrode design



350e

570e



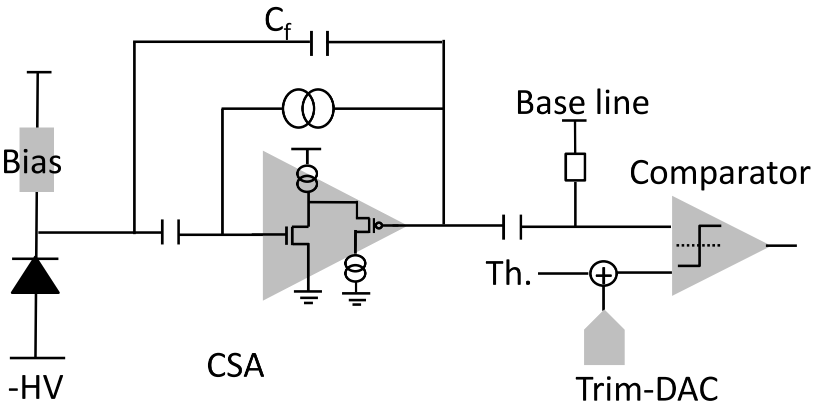
Un-expected “non-Gaussian tail”

doi: 10.1088/1748-0221/14/06/C06006

- The analog frontend functioned even though the leakage current from the sensor is increased by NIEL irradiation
- Lowest threshold=350e (570e)
- Improvement in lowering threshold dispersion by eliminating the “non-Gaussian tail” of ENC distribution will be done in next prototype

In-Pixel electronics (Analog frontend)

- ❑ **Large** electrode design: LF-Monopix



- Power-saving analog frontend
  - CSA
  - Discriminator + w/ 4-bit trim DAC

- ❑ **Small** electrode design: TJ-Monopix

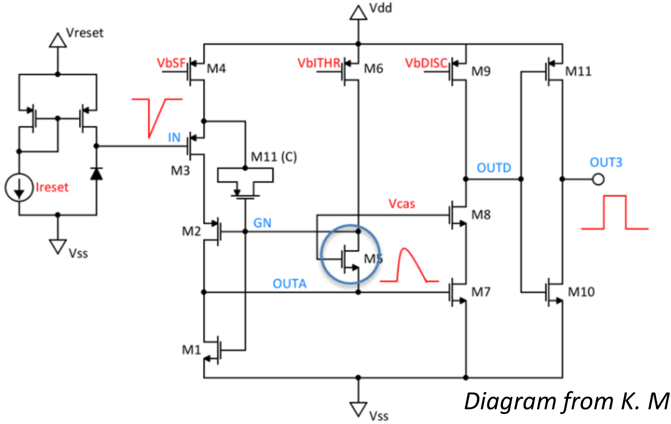


Diagram from K. Moustakas et al, IEEE NSS2017

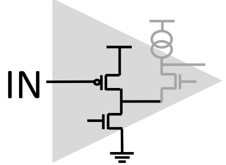
- Space-saving, high-gain-low-noise analog frontend
  - Novel preamp and discriminator drive from ALPIDE
  - w/o trim DAC

TID Radiation Hardness of Large electrode design (Gain & ENC)

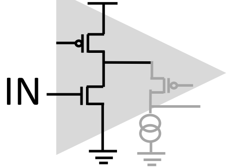
X-ray irradiation up to 50Mrad

- Input transistor of CSA

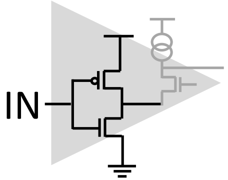
☐ PMOS-CSA ☐ NMOS-CSA ☐ CMOS-CSA



Well-tested



Power-saving

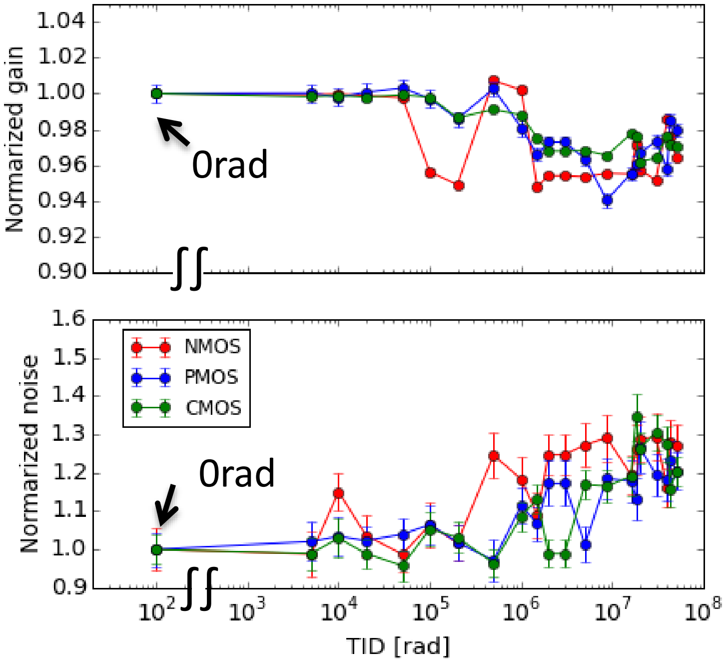


Power-saving

- Irradiated and measured in room temperature
- Gain degradation: <5%
- Noise increase: ~25%
  (due to the increase of the leakage current)

→ No significant degradation in power-saving CSAs

Normalized gain and ENC

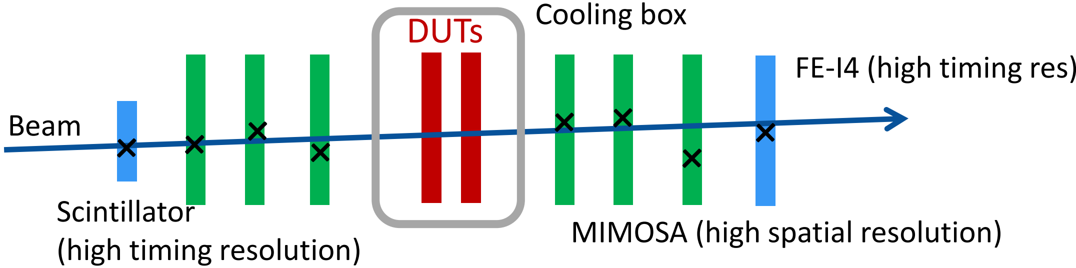


doi: 10.1016/j.nima.2018.10.059

Hit efficiency measurement

$$\text{Hit efficiency} = \frac{\textit{Number of hits detected by DUT}}{\textit{Number of particles passed DUT}}$$

Time and position of each particle
can be obtained by a beam telescope



DUTs

Cooling box

FE-I4 (high timing res)

Beam

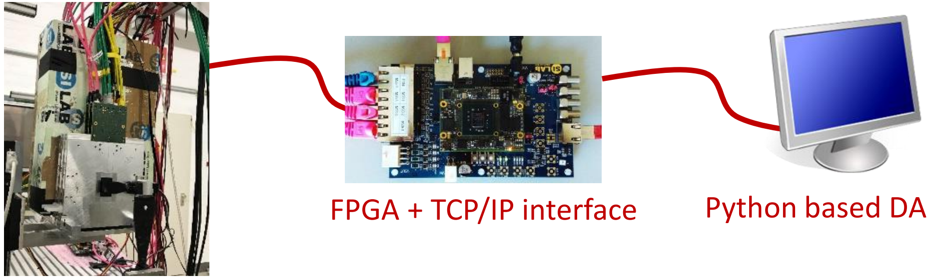
Scintillator
(high timing resolution)

MIMOSA (high spatial resolution)

ELSA 2.5GeV electron beam + EUDET type beam telescope (DESY) + newly developed DAQ

- Suited for ELSA’s beam intensity (~500 kHz, *P. Wolf Bachelor thesis, Uni Bonn*)
- Synchronizing MIMOSA readout for chips with a slow readout

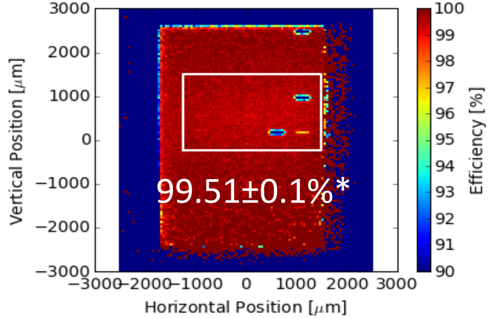
Beam telescope



FPGA + TCP/IP interface

Python based DAQ software

☐ Hit efficiency of LF-CPIX (slow R/O)



T. Hirono PhD thesis Uni Bonn, 2019

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

Hit efficiency

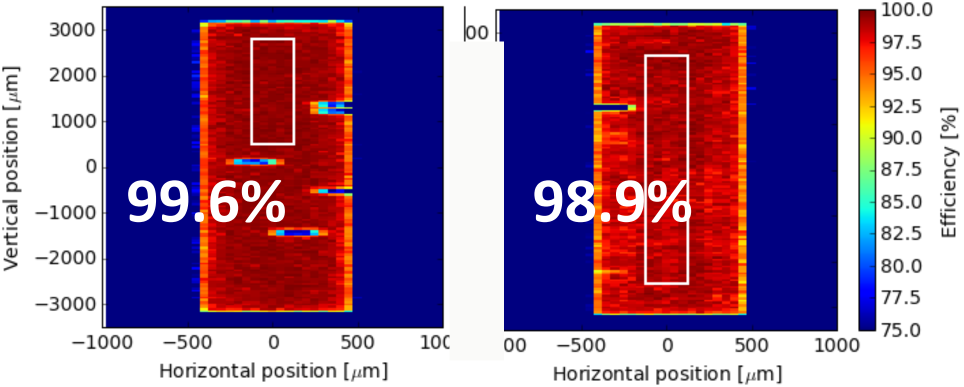
❑ **Large** electrode design: LF-Monopix (750µm)

Un-irradiated

- Noise < 1.2 Hz/pix

Neutron irradiated

- Noise < 0.1Hz/pix



doi: 10.1016/j.nima.2018.10.059

Hit efficiency is as high as 98.9% after the NIEL irradiation ($10^{15}n_{eq}/cm^2$)

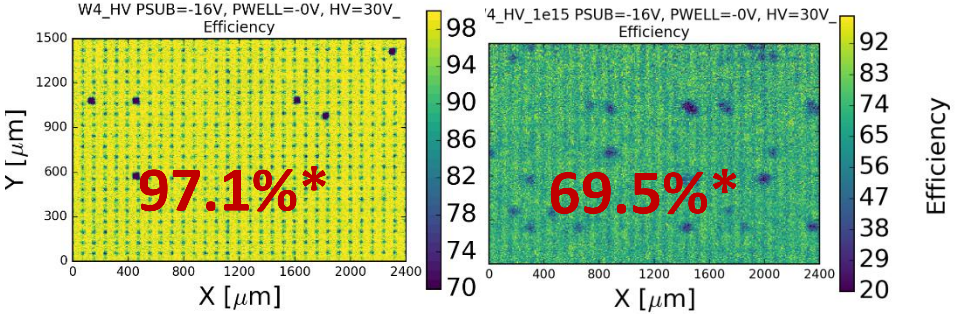
❑ **Small** electrode design: TJ-Monopix

Un-irradiated

- Noise < 10 Hz/pix

Neutron irradiated

- Noise < 10 Hz/pix



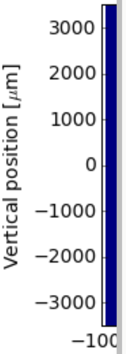
doi: 10.1088/1748-0221/14/06/C06006

Inefficiency was observed even before irradiation

This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

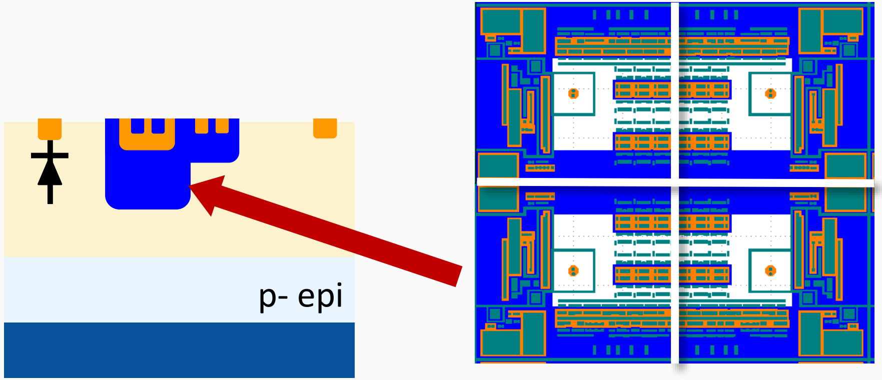
hit efficiency

❑ I

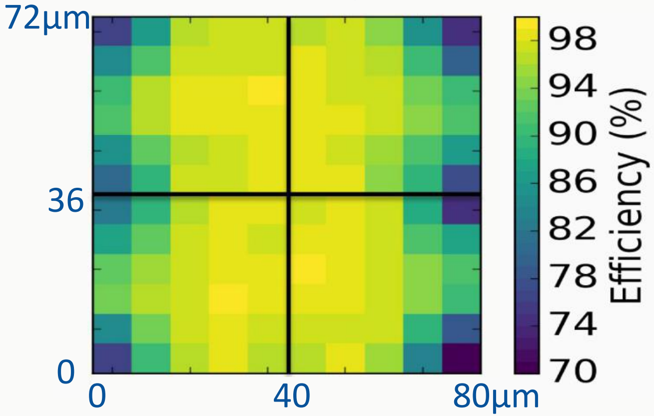


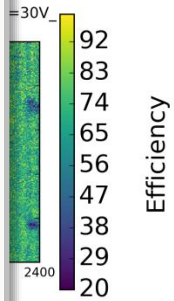
In-pixel hit efficiency of un-irradiated **small** electrode prototype (4 pixels)

❑ Layout



❑ Hit efficiency





o, *PIXEL 2018*

➡ Inefficient regions exist near pixel corner where PWELL are implanted

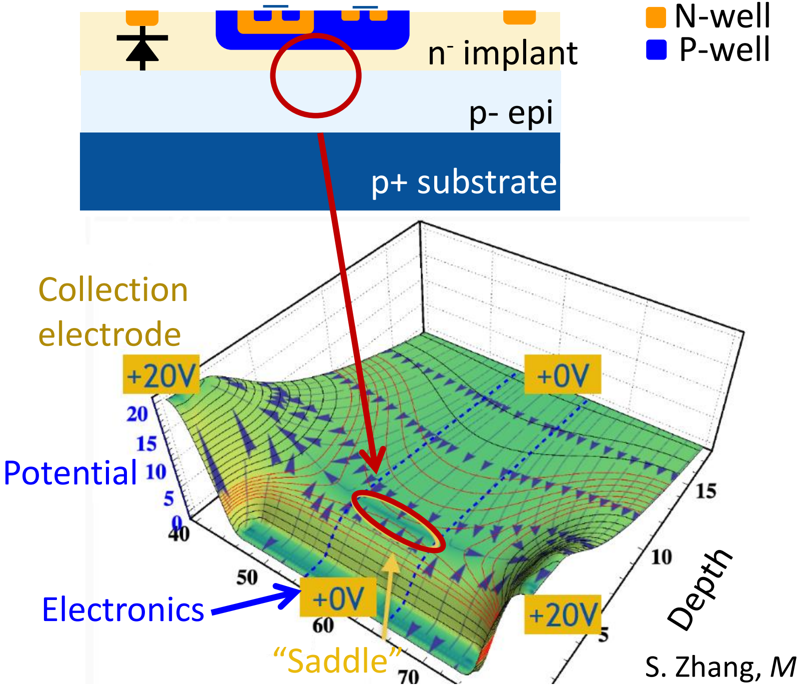
Hit

irradi

tion

Hit Efficiency degradation in Small electrode design

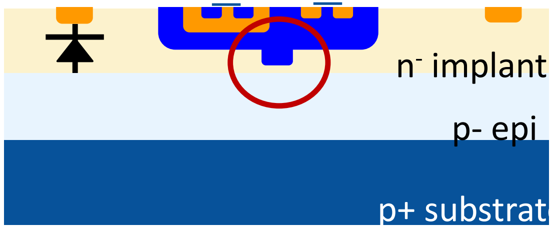
❑ TCAD simulation



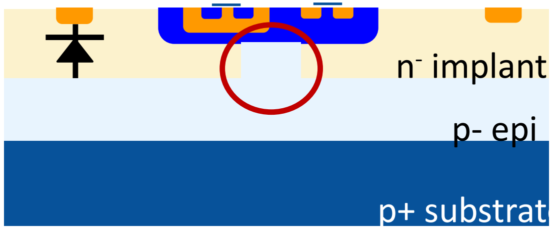
S. Zhang, *Master thesis Uni. Bonn*

Improvements

❑ Modification1: Additional PWELL



❑ Modification2: Gap in n$^-$implant



Conclusion for DMAPS development

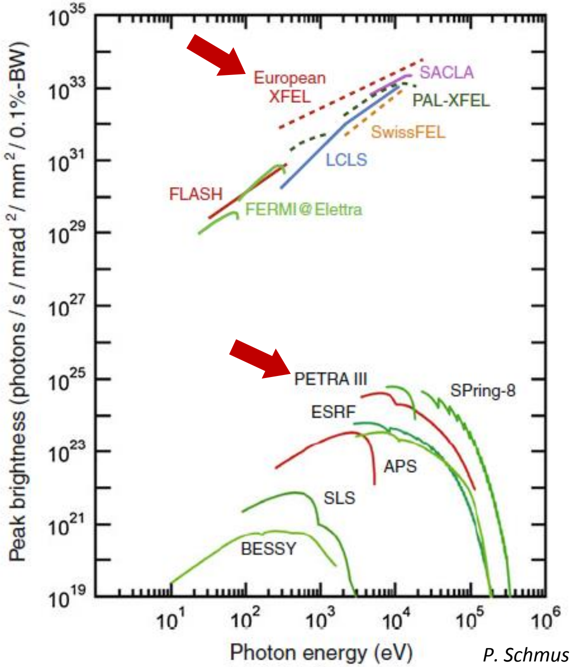
- Two fully-monolithic large-scale matrixes have been tested to discuss the suitability of DMAPS as pixel detector in HL-LHC experiments
  - Large electrode design:
    - No significant degradation due to TID irradiation (50Mrad).
    - Hit efficiency is as high as 98.9% after NIEL irradiation ($10^{15}n_{eq}/cm^2$)
  - Small electrode design:
    - The novel analog frontend and R/O logics functions in the large scale matrix but needs improvement in threshold dispersion and ENC
    - Inefficiency was observed but the improvement is on going

AND…

Other works

- A member of Control and Computing Division in SPring-8
  - Development and maintenance of control and DAQ system for accelerator and beamline
  - Detector development (2009-)

http://xfel.riken.jp/eng/gallery/index.html

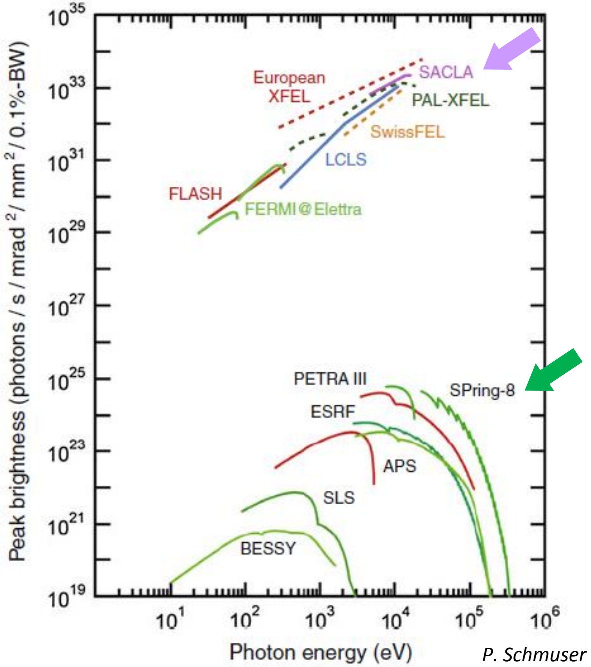


P. Schmuser et al., ISBN 978-319-04080-6 (2014)

Other works

- A member of Control and Computing Division in SPring-8
  - Development and maintenance of control and DAQ system for accelerator and beamline operation
  - Detector development (2009-)

http://xfel.riken.jp/eng/gallery/index.html



High brilliance in high energy (30-100keV) region

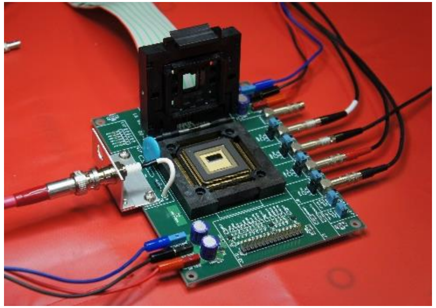
P. Schmuser et al., ISBN 978-319-04080-6 (2014)

Other works (CdTe detectors)

CdTe has high sensitivity in 30-100 keV

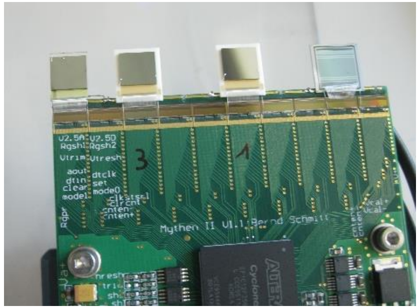
Pixel detector

CdTe + Custom-made ASIC



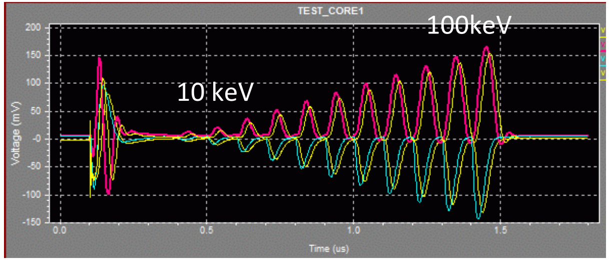
Strip detector

CdTe + Mythen (PSI) readout

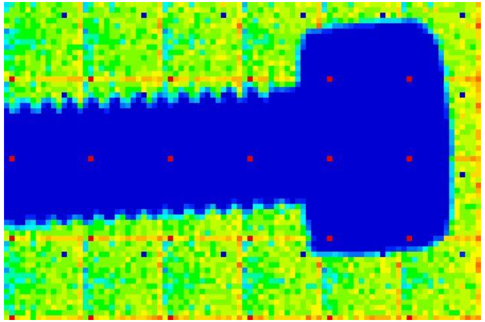


- ASIC simulation

doi: 10.1016/j.nima.2010.12.207



- Characterization of prototypes

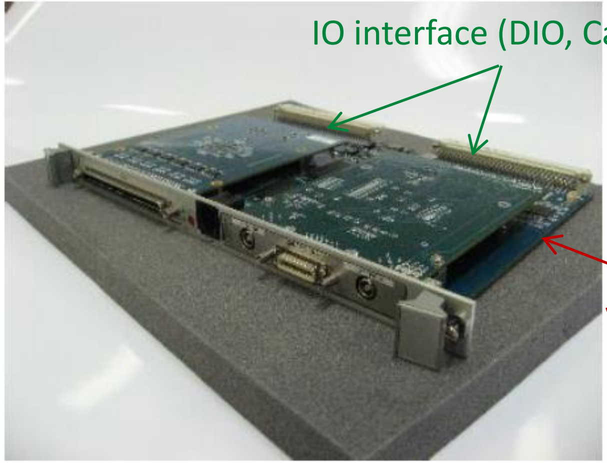


doi:10.1016/j.nima.2013.06.049

Other works (DAQ board)

❑ Upgrade and maintenance of control and DAQ system for beamlines

FPGA board with VME interface



2 mezzanine cards

IO interface (DIO, CameraLink etc)

Base board

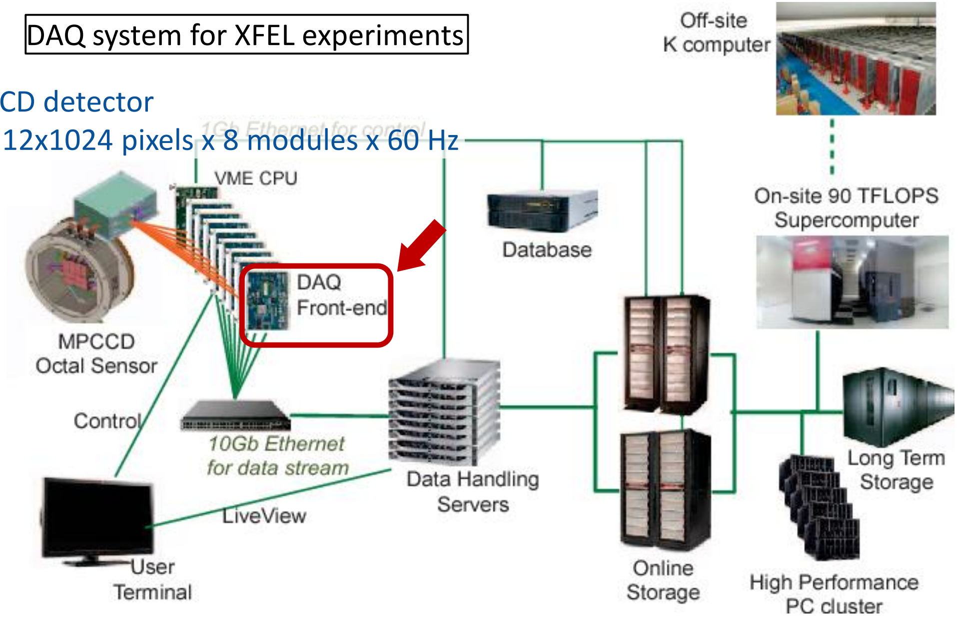
VME interface

FPGA

DAQ system for XFEL experiments

CCD detector

512x1024 pixels x 8 modules x 60 Hz



M. Yamaga et al, 19th IEEE-NPSS Real Time Conference (2014)

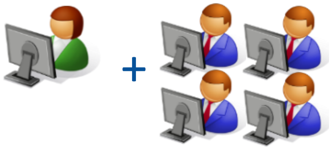
Other works
(Database system administration)

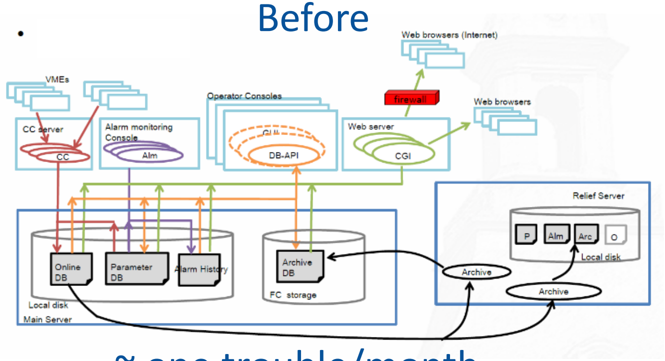
- Control system in SPring8 is “Message And Database Oriented Control Architecture”

Operation of the accelerators relay on the database system
(Troubles in the database system → No beam)

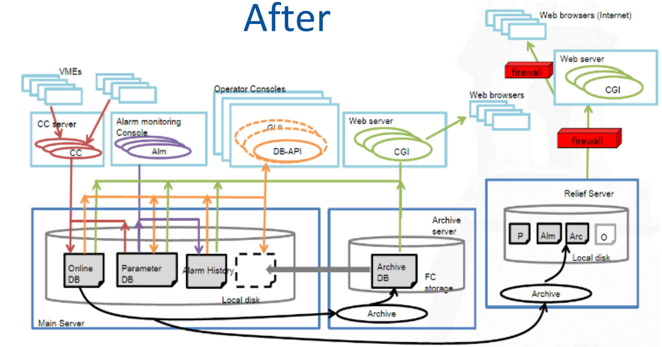
Control system for XFEL was the largest for MADOCA → Upgrade was proposed

T. Hirono et al, Proc of ICALEPCS 2013




Before

~ one trouble/month


After

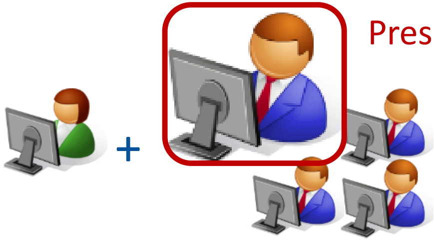
No trouble caused by the database system

Other works
(Database system administration)

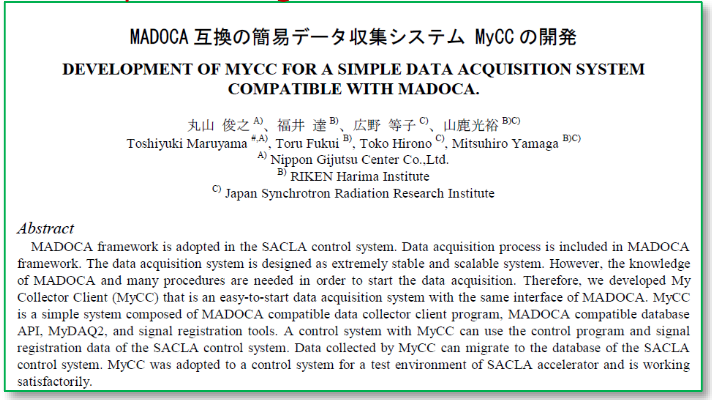
❑ Database system administration

- Control system in SPring8 is “Message And Database Oriented Control Architecture”

→ Operation of the accelerators relay on the database system
(Troubles in the database system → No beam)



Presentation & proceeding in a conference



MADOCA 互換の簡易データ収集システム MyCC の開発

DEVELOPMENT OF MYCC FOR A SIMPLE DATA ACQUISITION SYSTEM COMPATIBLE WITH MADOCA.

丸山 俊之 A)、福井 達 B)、広野 等子 C)、山鹿光裕 B)C)
Toshiyuki Maruyama #,A), Toru Fukui B), Toko Hirono C), Mitsuhiro Yamaga B)C)
A) Nippon Gijutsu Center Co.,Ltd.
B) RIKEN Harima Institute
C) Japan Synchrotron Radiation Research Institute

Abstract

MADOCA framework is adopted in the SACLA control system. Data acquisition process is included in MADOCA framework. The data acquisition system is designed as extremely stable and scalable system. However, the knowledge of MADOCA and many procedures are needed in order to start the data acquisition. Therefore, we developed My Collector Client (MyCC) that is an easy-to-start data acquisition system with the same interface of MADOCA. MyCC is a simple system composed of MADOCA compatible data collector client program, MADOCA compatible database API, MyDAQ2, and signal registration tools. A control system with MyCC can use the control program and signal registration data of the SACLA control system. Data collected by MyCC can migrate to the database of the SACLA control system. MyCC was adopted to a control system for a test environment of SACLA accelerator and is working satisfactorily.

Summary

- In doctoral thesis, depleted monolithic CMOS active pixel sensors (DMAPS) for high energy particle physics has been studied and further developments is on-going.
  - Characterization of silicon detectors
  - Development of hardware, firmware, and software for prototype chips and testing devices including upgrade of the beam telescope DAQ system

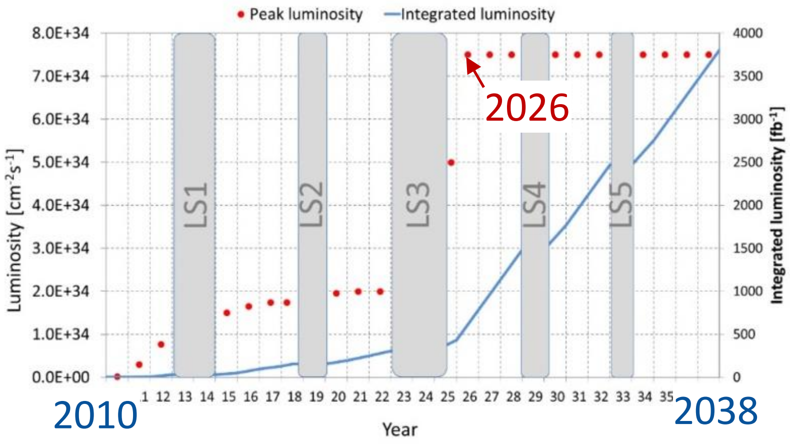
- Working experiences in a large accelerator facility would also helps future works
  - Development of hybrid pixel/strip detectors
  - Leading a project with 4 members

➡ I would like to contribute to projects in DESY's detector group using advantages of my experiences

Backup

High Luminosity-LHC

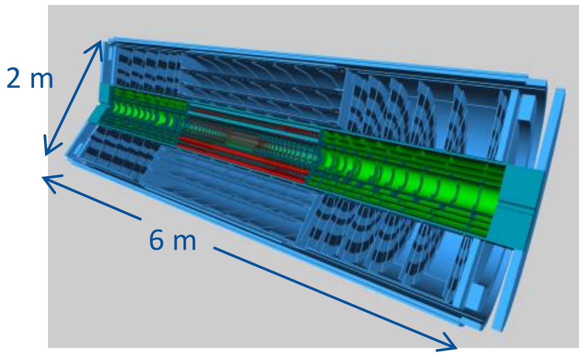
☐ Upgrade of LHC



- Current LHC operation $L = 2 \times 10^{34}$ ➡ HL-LHC operation $L = 7.5 \times 10^{34}$

☐ Upgrade of Detector in LHC (ATLAS Detector)

Large area will be covered by detector with high granularity = pixel detector



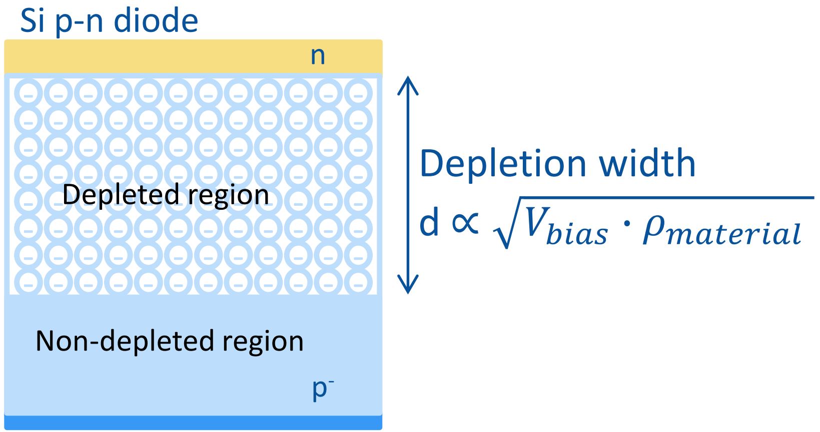
🟥🟩 Pixel detectors

https://twiki.cern.ch/twiki/bin/view/AtlasPublic/HiggsPublicResults

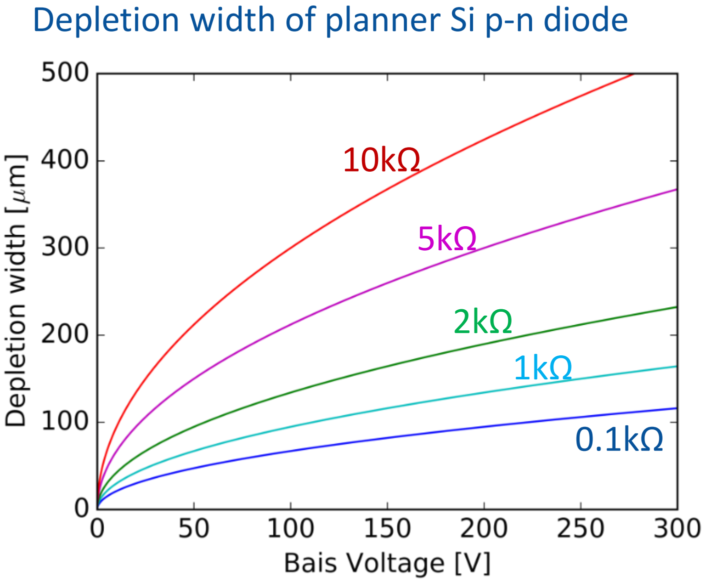
ATLAS ITk Pixel Detector: O ~ 10m^2

Monolithic CMOS active pixel sensors is an attractive option for pixel detector at HL-LHC

Depletion of Si diode



$d \propto \sqrt{V_{bias} \cdot \rho_{material}}$

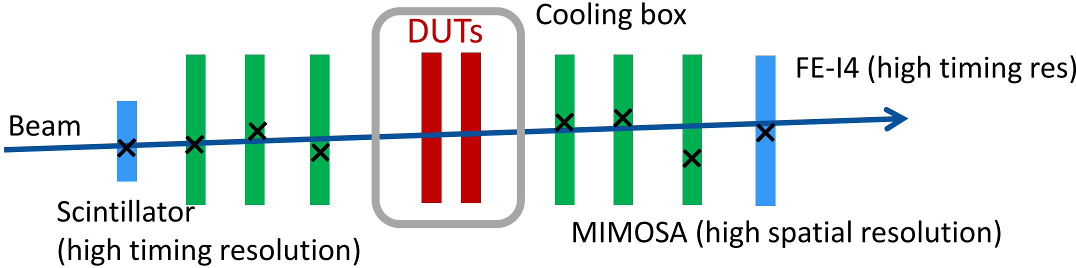


High V + High ρ ➡ Sufficient depleted volume

Hit efficiency measurement

$$\text{Hit efficiency} = \frac{\mathit{Number\ of\ hits\ detected\ by\ DUT}}{\mathit{Number\ of\ particles\ passed\ DUT}}$$

Time and position of each particle can be obtained by a beam telescope


DUTs

Cooling box

FE-I4 (high timing res)

Beam

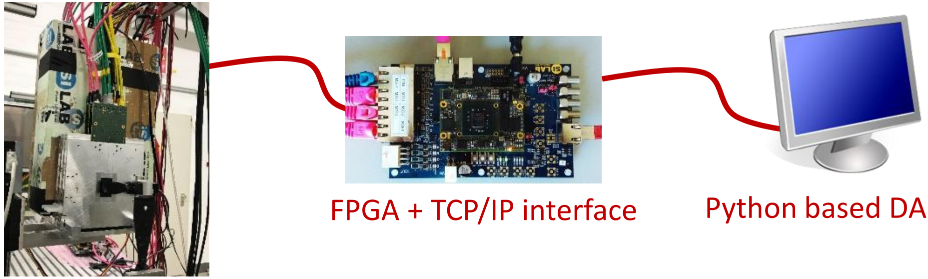
Scintillator
(high timing resolution)

MIMOSA (high spatial resolution)

ELSA 2.5GeV electron beam + EUDET type beam telescope + newly developed DAQ

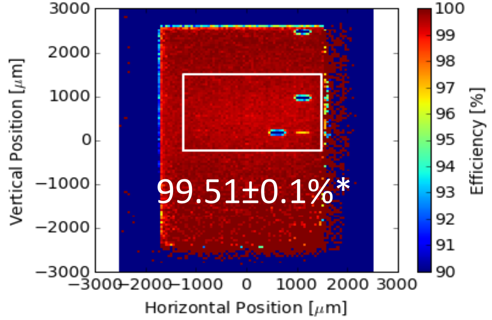
- Suited for ELSA’s beam intensity (~100 kHz)
- Synchronizing MIMOSA readout for chips with a slow readout

EUDET type telescope (DESY)


FPGA + TCP/IP interface

Python based DAQ software

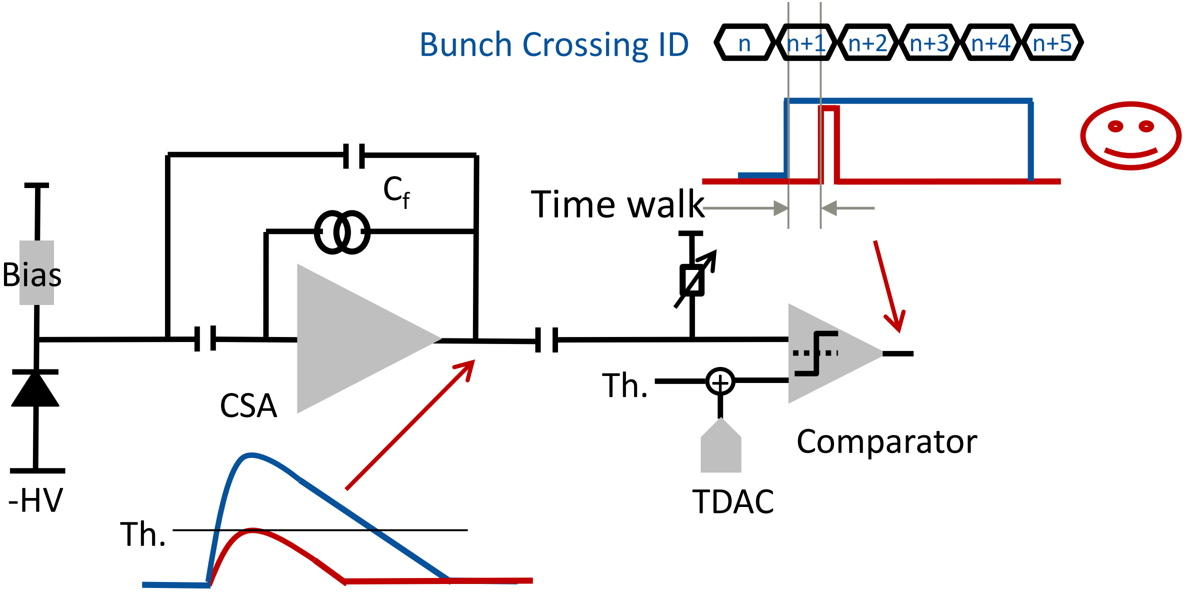
☐ Hit efficiency of LF-CPIX (slow RO)



99.51±0.1%*

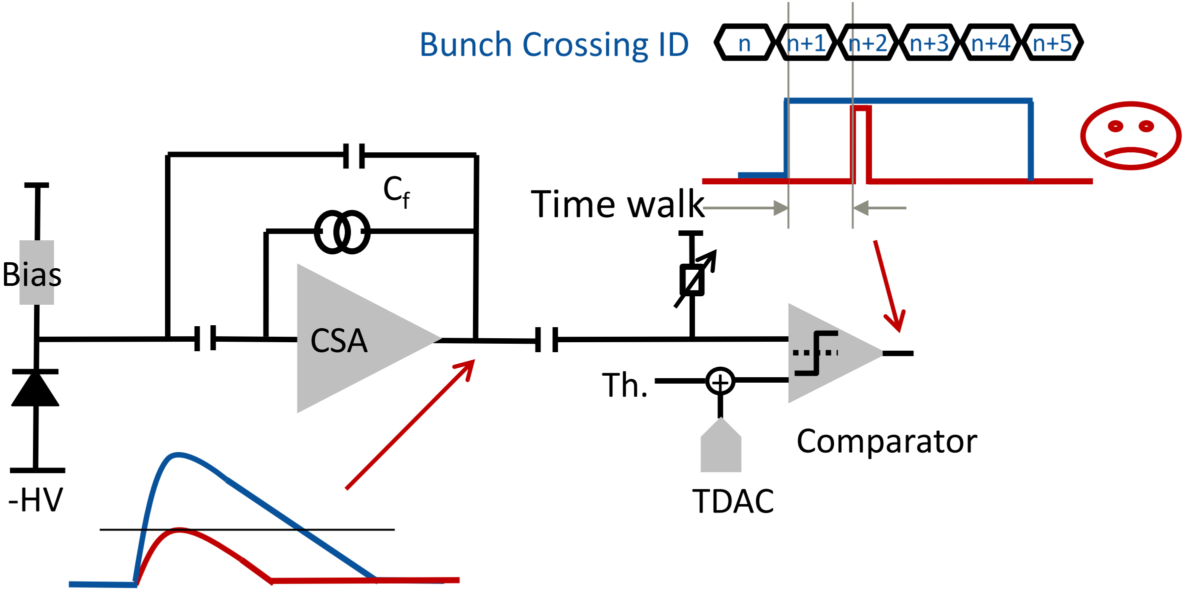
Timing performance required in HL-LHC

Responses in 1 Bunch Crossing (25 ns) will be counted as signal → Smallest signal in 1BCD = In-time threshold



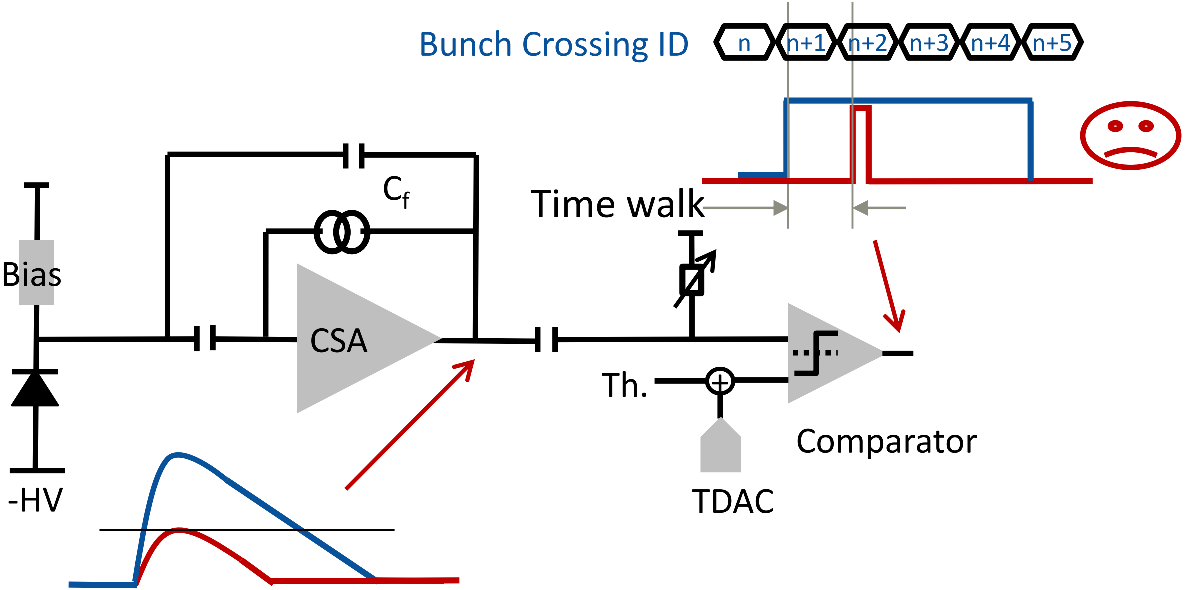
Timing performance required in HL-LHC

Responses in 1 Bunch crossing (25 ns) will be counted as signal → Smallest signal in 1BCD = In-time threshold

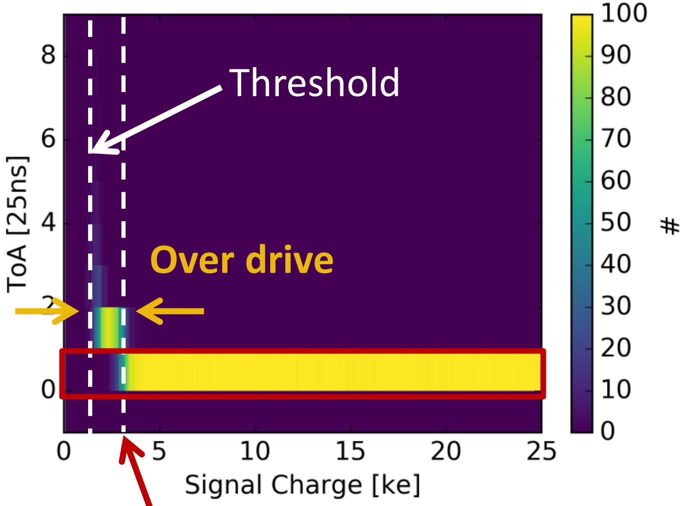


Timing performance required in HL-LHC

Responses in 1 Bunch crossing (25 ns) will be counted as signal → Smallest signal in 1BCID = In-time threshold



☐ In-time threshold and over drive



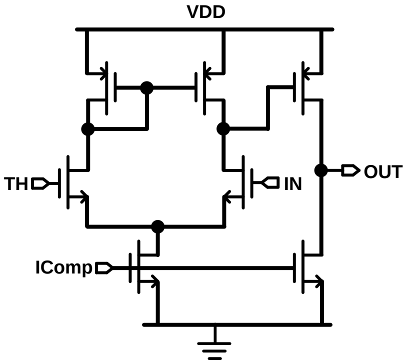
In-time threshold (ToA in 1clk)

ANALOG frontend for Large electrode design

Development of power saving and fast responding discriminator

❑ Conventional type

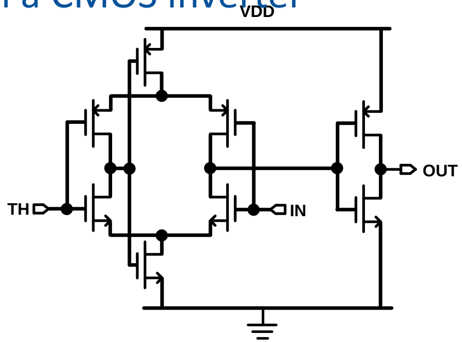
Two-stage open loop structure

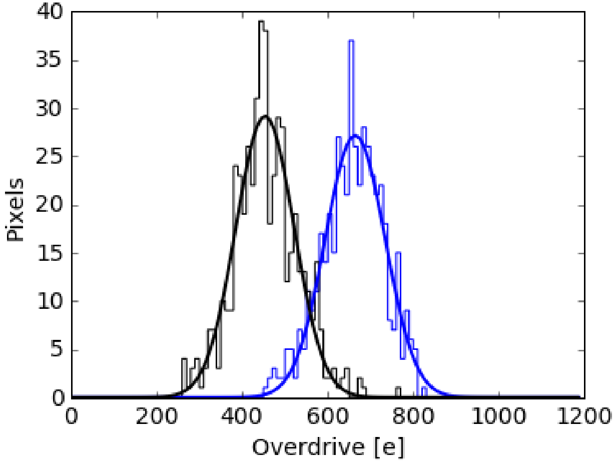


- Bias current: 4.5 µA
- Well tested but slow at threshold edge

❑ New type

Self-biased differential amplifier with a CMOS inverter





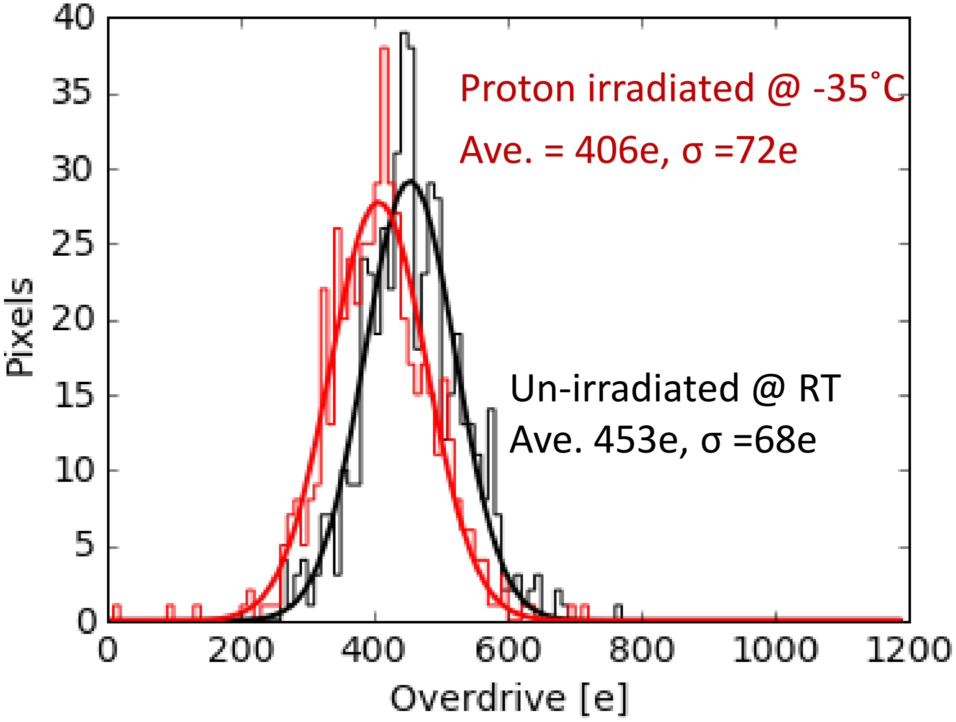
- Self biased: < 4µA
- Faster especially at threshold edge

TID Radiation Hardness of Large electrode design (Over Drive)

- Over drive measurement
  - Threshold: 1500 e

- Difference between irradiated/un-irradiated chip
  - Chip temperature
  - Chip variation
  - Optimization of tunable parameters

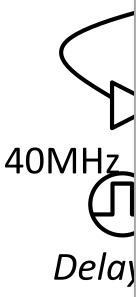
No degradation in timing performance

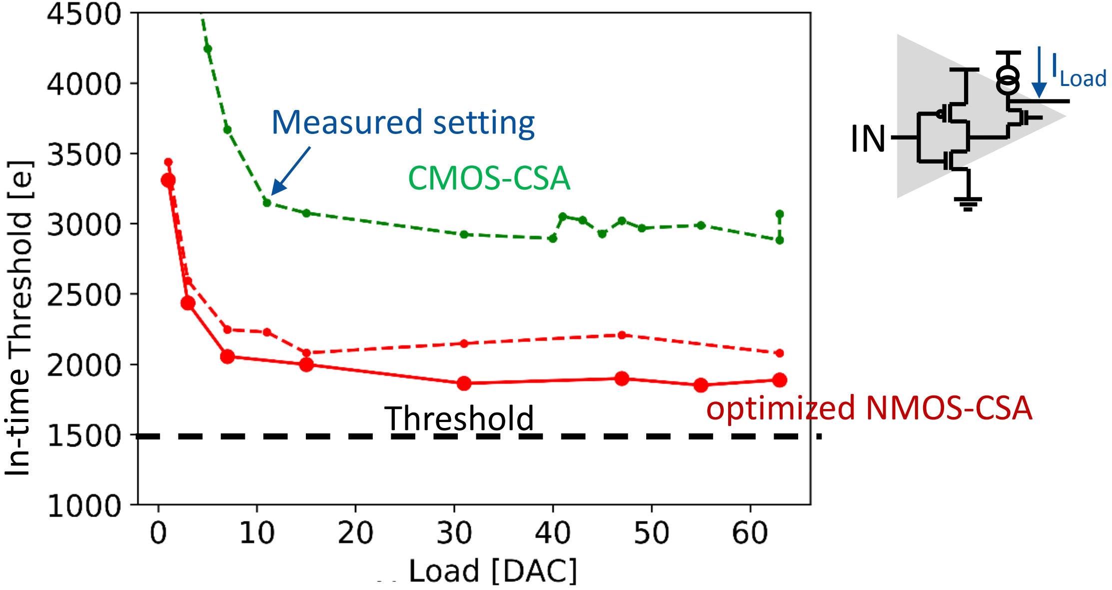


Time walk

Threshold: 1500e
200V/130V
ng: Default
GeV electron

Bea



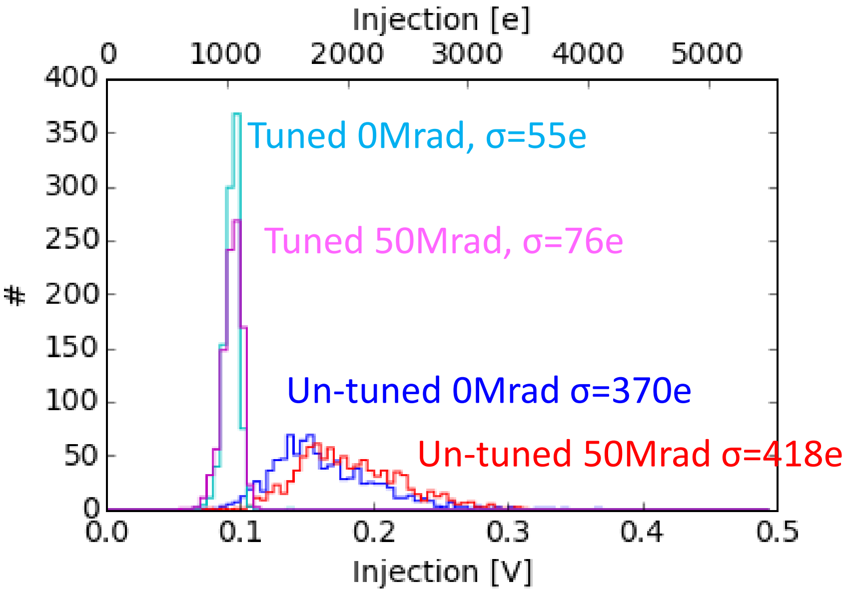


Optimize operation configuration of analog frontend lower in-time threshold

- This
  -
  - High

Radiation hardness (TID)

Un-tuned and tuned threshold dispersions of LF-CPIX (flavor=PMOS)



- The threshold is still tunable after TID=50Mrad (σ<100e *cf. readout noise ≈ 200e*)
- Increase of the tuned threshold dispersion is 20e

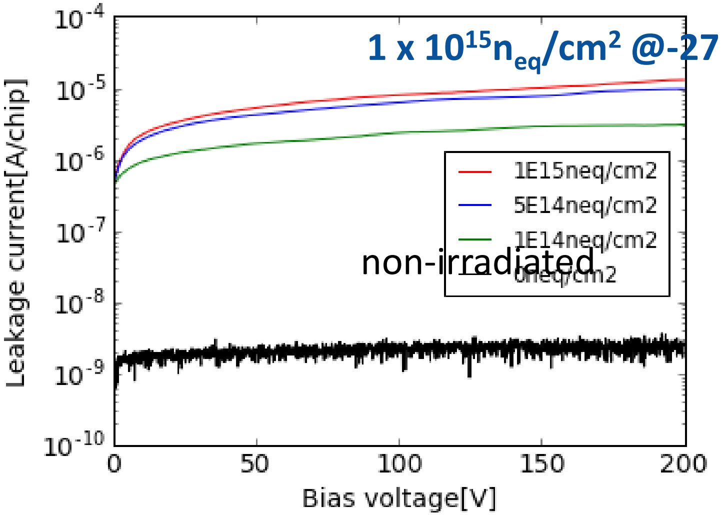
This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

Radiation hardness (NIEL)

- The neutron irradiation test was done in JSI and the MonoPix were annealed 80min @60C

Chip: MONOPIX
DAC setting: Default
Bias voltage: -200V
Temperature: -23C, -27.5C

❑ I-V curve of MonoPix

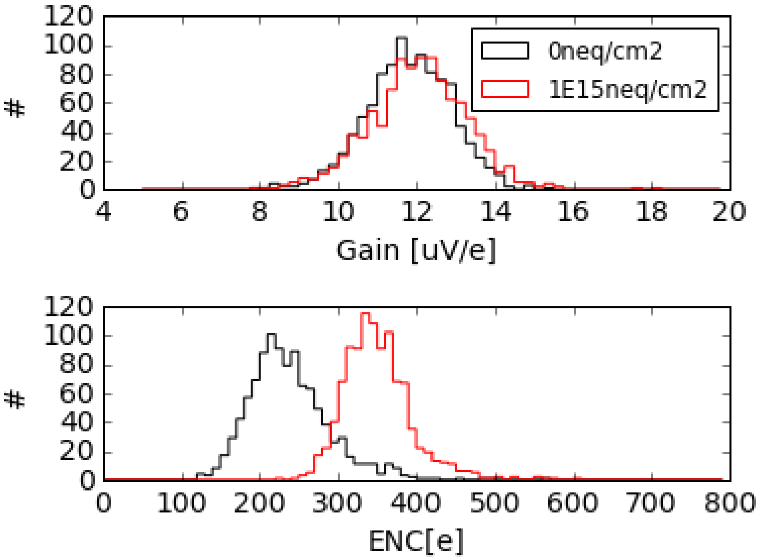


$1 \times 10^{15} n_{eq}/cm^2$ @-27.5 ˚C

non-irradiated

- Breakdown voltage is higher than 200V

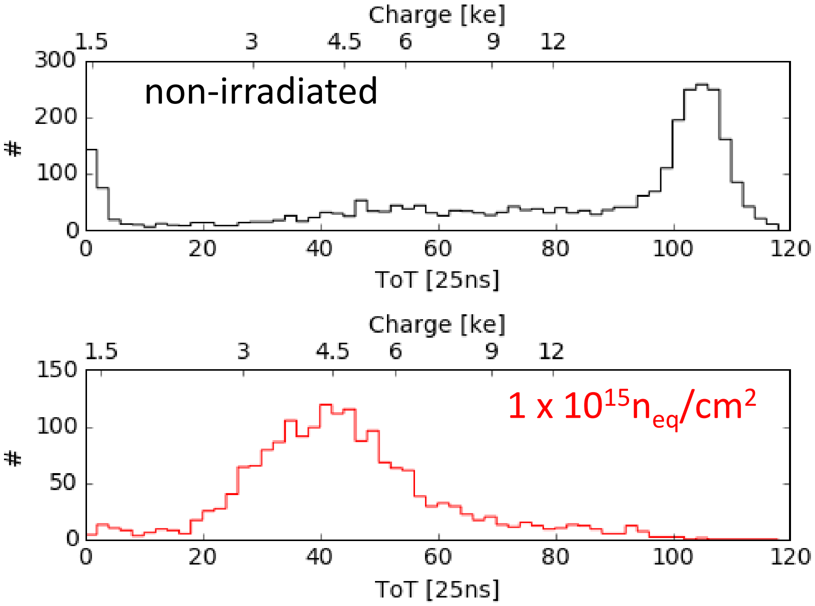
❑ Gain and noise



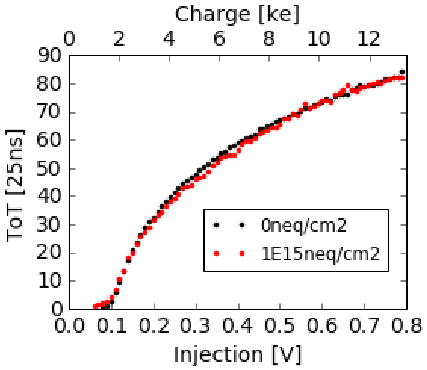
Radiation hardness (NIEL)

Threshold: 1500 e
Bias: -200V (0 n_{eq}/cm^2)
-130V (1 x $10^{15} n_{eq}/cm^2$)
Chip: MONOPIX
DAC setting: Default
Source: 2.5GeV electron
Temperature: cooled by dry ice

❑ ToT values of seed pixel



❑ Injection vs ToT



- The MPV is decreased after neutron irradiation of 1 x $10^{15} n_{eq}/cm^2$.

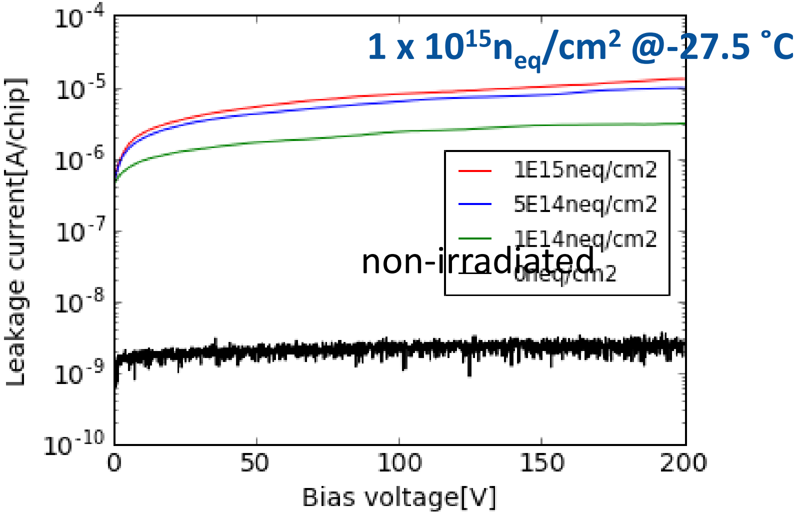
This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

Radiation hardness (NIEL)

Chip: MONOPIX
DAC setting: Default
Bias voltage: -200V
Temperature: -23C, -27.5C

- The neutron irradiation test was done in JSI and the MonoPix were annealed 80min @60C

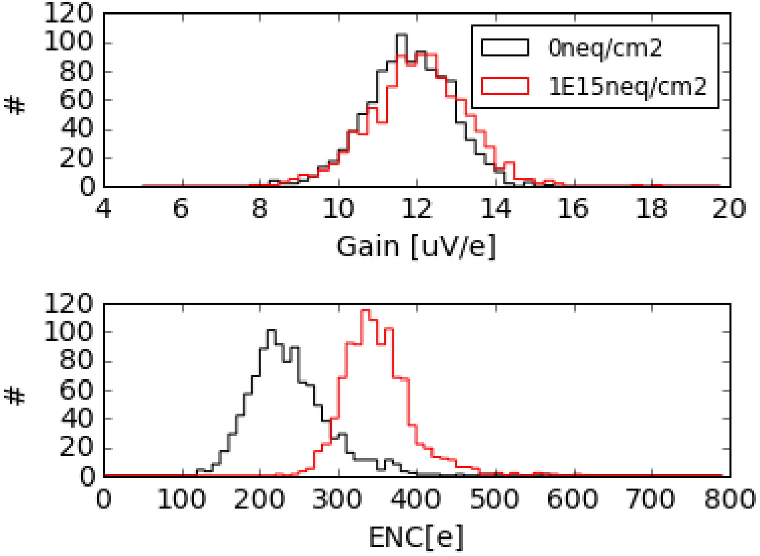
☐ I-V curve of MonoPix


$1 \times 10^{15} n_{eq}/cm^2$ @-27.5 °C

non-irradiated

- Breakdown voltage is higher than 200V

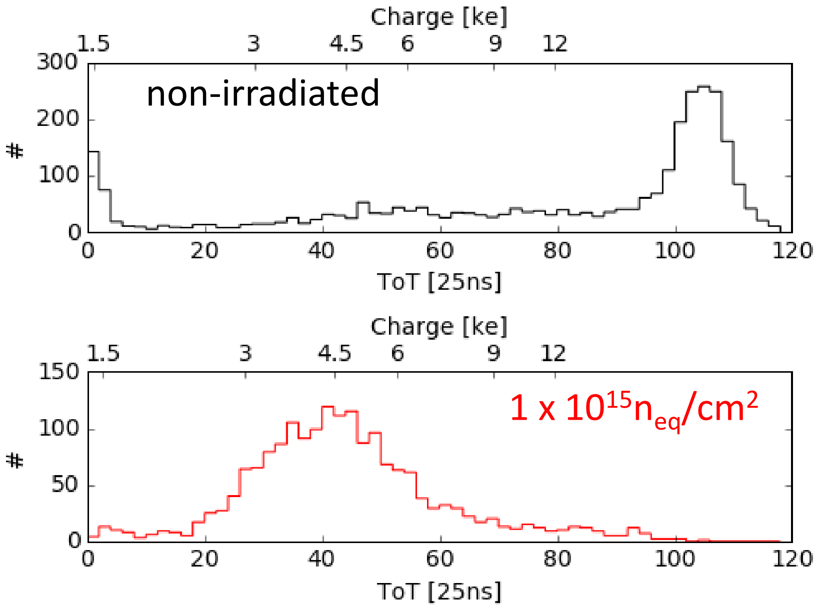
☐ Gain and noise



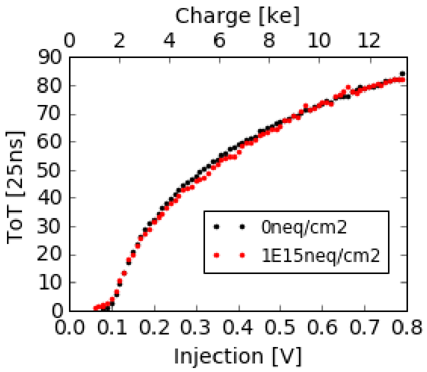
Radiation hardness (NIEL)

Threshold: 1500 e
Bias: -200V (0 n_{eq}/cm^2)
-130V (1 x $10^{15} n_{eq}/cm^2$)
Chip: MONOPIX
DAC setting: Default
Source: 2.5GeV electron
Temperature: cooled by dry ice

- ☐ ToT values of seed pixel



- ☐ Injection vs ToT

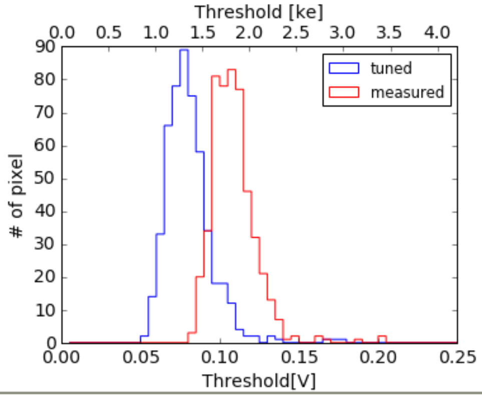


- The MPV is decreased after neutron irradiation of 1 x $10^{15} n_{eq}/cm^2$.

Threshold dispersion

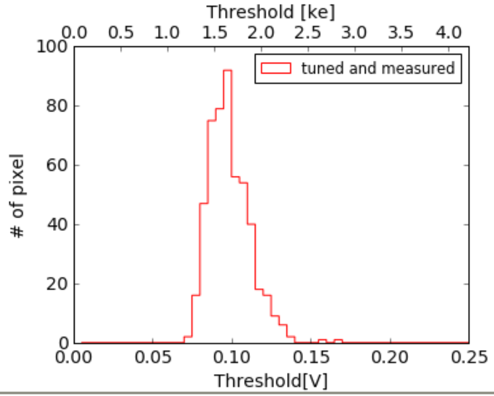
- Un-irradiated

Chip: MONOPIX un-irradiated
DAC setting: default
TH: tuned by noise + 4mV
Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
Enabled readout: col 16-20
HV: -200V
Temp: dry ice
Source: 2.5GeV electron



- $1 \times 10^{15} n_{eq}/cm^2$

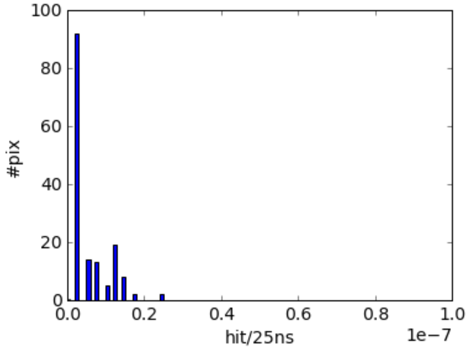
Chip: MONOPIX irradiated
DAC setting: default
TH: tuned by noise
Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
Enabled readout: col 16-20
HV: -130V
Temp: dry ice
Source: 2.5GeV electron



Noise occupancy

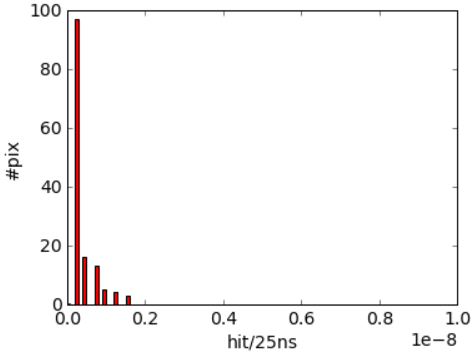
- Un-irradiated

Chip: MONOPIX un-irradiated
DAC setting: default
TH: tuned by noise
Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
Enabled readout: col 16-20
HV: -200V
Temp: dry ice
Source: 2.5GeV electron



- 1 x $10^{15}n_{eq}/cm^2$

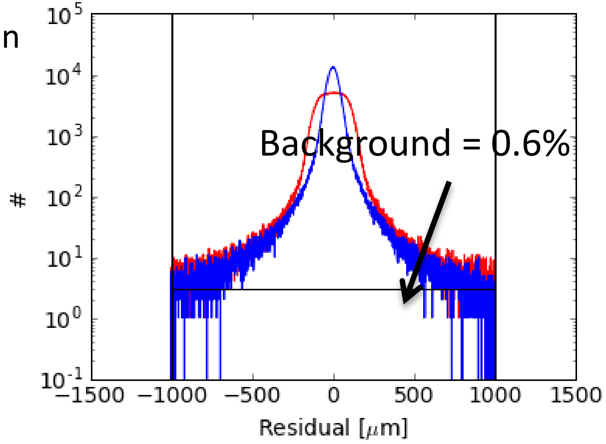
Chip: MONOPIX irradiated
DAC setting: default
TH: tuned by noise
Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
Enabled readout: col 16-20
HV: -130V
Temp: dry ice
Source: 2.5GeV electron



Residual

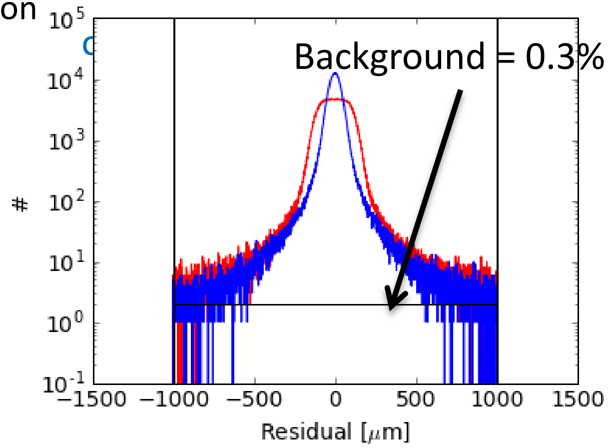
Thickness of chip: 750um
Chip: MONOPIX un-irradiated
DAC setting: default
TH: tuned by noise + 4mV
Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
Enabled readout: col 16-20
HV: -200V
Temp: dry ice
Source: 2.5GeV electron

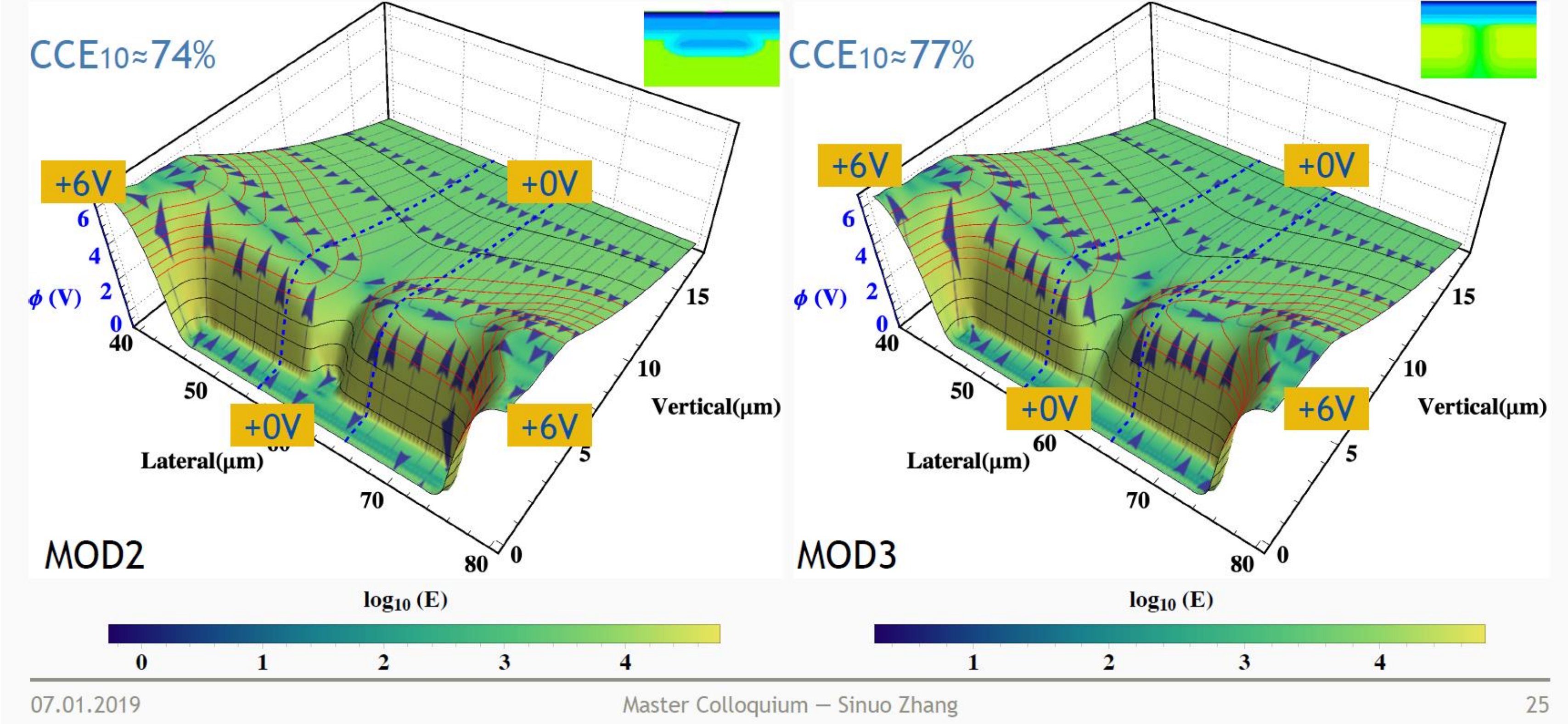
- Un-irradiated



Thickness of chip: 750um
DAC setting: default
TH: tuned by noise
Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
Enabled readout: col 16-20
HV: -130V
Temp: dry ice
Source: 2.5GeV electron

- $1 \times 10^{15} n_{eq}/cm^2$

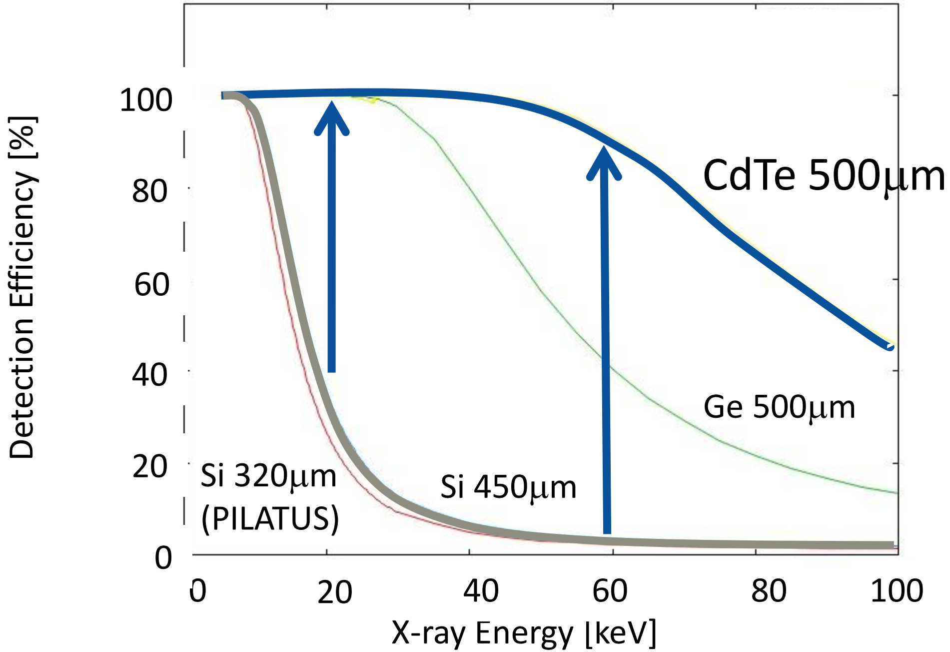




07.01.2019 Master Colloquium — Sinuo Zhang 25

Concepts

– Detection Efficiency of Sensors



CdTe has almost 100% detection efficiency up to 40keV, more than 50% at 60-100 keV where Si has only 1.5%

Concepts

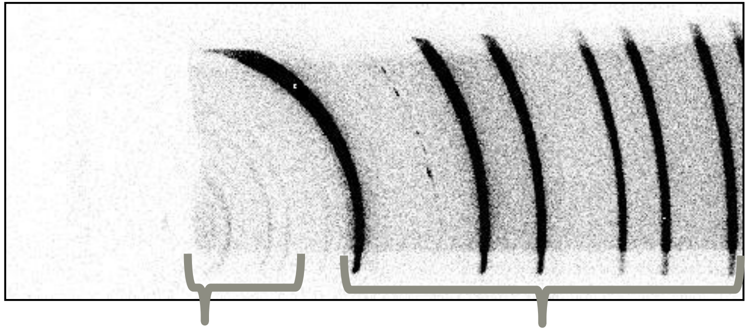
Detector that is suite for SPring-8….

- Photon-counting large-area hybrid pixel detector, like PILATUS, which are very powerful for SR experiments.
- High sensitivity in high energy X-ray region (15 - 100keV)
  ⇒CdTe sensor
- Function to cut high energy X-ray
  ⇒Readouts with a window-type comparator

Concepts

- Diffraction pattern of Si with lower-energy comparator only (without higher-energy comparator)

Lower energy comparator at 30.8keV
Monochromator at 37.8keV



113keV
(3rd order of 37.8keV)

37.8keV
(Target energy)

- Without higher-energy comparator, higher order X-ray from monochromator was mixed with the target energy X-ray in the detected image.

⇒Window-type comparator is required for low background images

Concepts

– 3 steps to realize a large area imaging detector

SP8-01

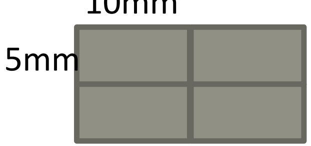
Pixel size : 200um x 200um
Number of pixel: 16 x 16 pixels
Chip size : 5mm x 5mm

Single chip

Small chip, large pixel
ASIC with many parameter switches
2 side buttable
Nov. 2008-2010

SP8-02

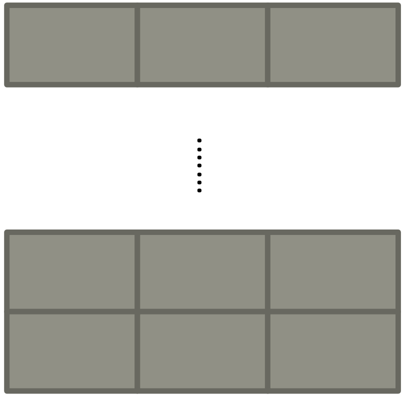
180um x 180um
32 x 16 pixels
10mm x 5mm



2 x2 chips/module

Multi-chip module, small pixel
Optimized ASIC
3 side buttable
2010-2011

SP8-03 (final design)



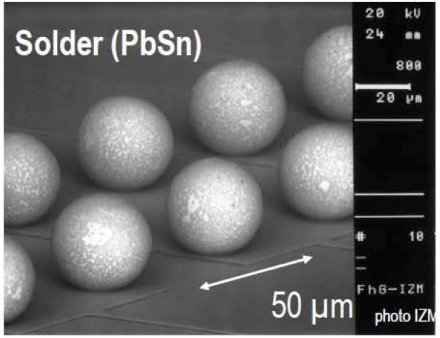
Large multi-chip module
4 side buttable
2012-2013

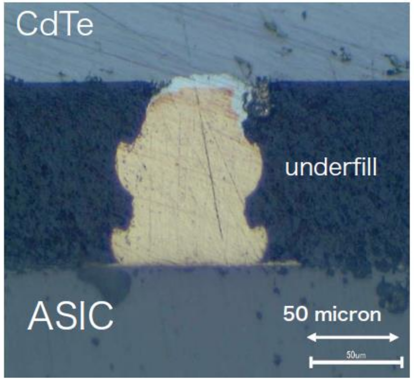
Specification of SP8-01

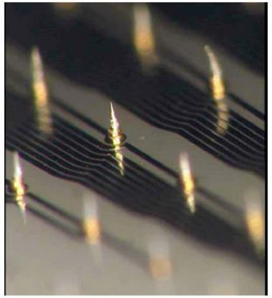
- Sensor
  - CdTe
  - 200 x 200 um/pixel, 16 x16 pixels/chip
- Contacts of sensors
  - In/CdTe/Pt-pixel, Al-pixel/CdTe/Pt, Pt-pixel/CdTe/Pt
  - **Gold-stud bonding**
- Readout with..
  - Analog amp. with time constant less than 100nsec
  - Readable both positive and negative charge
  - Switchable and adjustable gain: 15keV-40keV, 30keV-100keV
  - Poll-zero circuit and offset adjustor
  - Window-type comparator
  - 20 bits counter

Concepts

Gold-stud bonding







- Bump bonding
  - Wafer level process
  - High temperature and high pressure
  - ◎ Si
  - △ CdTe
- In/Au stud bonding (Developed by JAXA)
  - Chip level process
  - low temperature and soft process
  - **◎ CdTe**

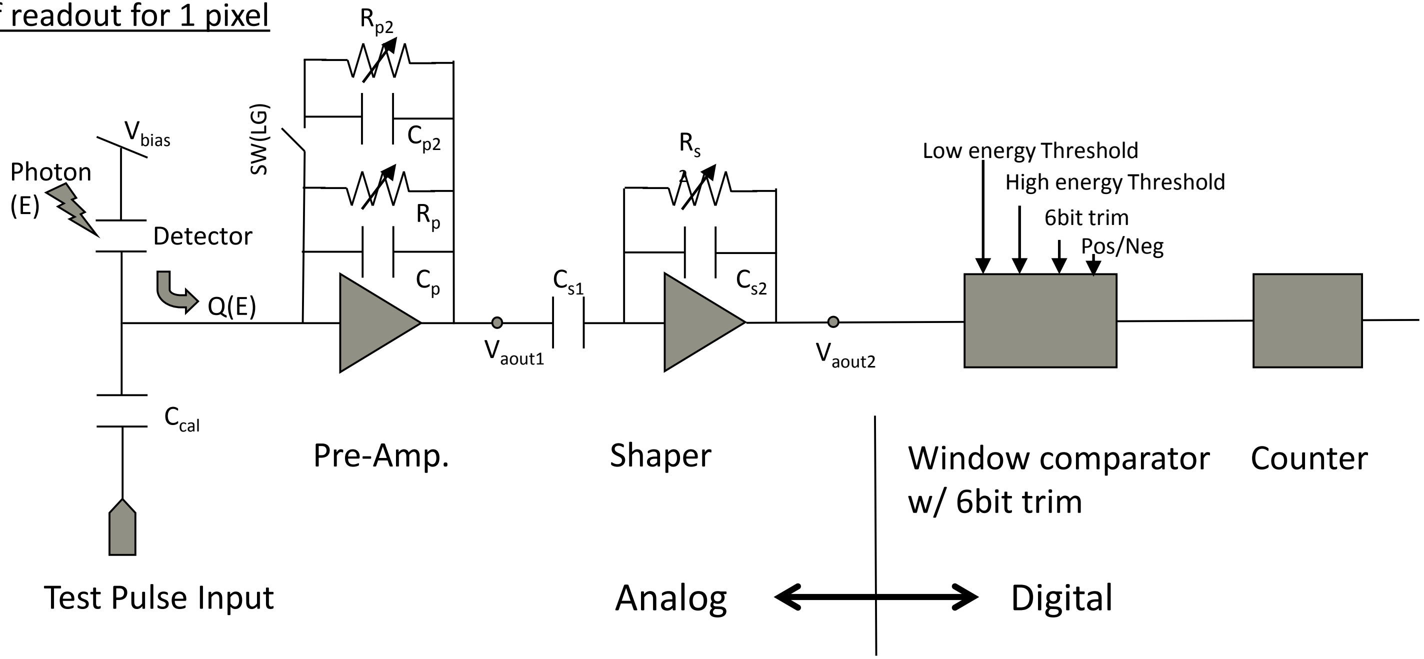
Specification of SP8-01

- Sensor
  - CdTe
  - 200 x 200 um/pixel, 16 x16 pixels/chip
- Contacts of sensors
  - In/CdTe/Pt-pixel, Al-pixel/CdTe/Pt, Pt-pixel/CdTe/Pt
  - Gold-stud bonding
- Readout with..
  - Analog amp. with time constant less than 100nsec
  - Readable both positive and negative charge
  - Switchable and adjustable gain: 15keV-40keV, 30keV-100keV
  - Poll-zero circuit and offset trim
  - Window-type comparator
  - 20 bits counter

Design of ACIS

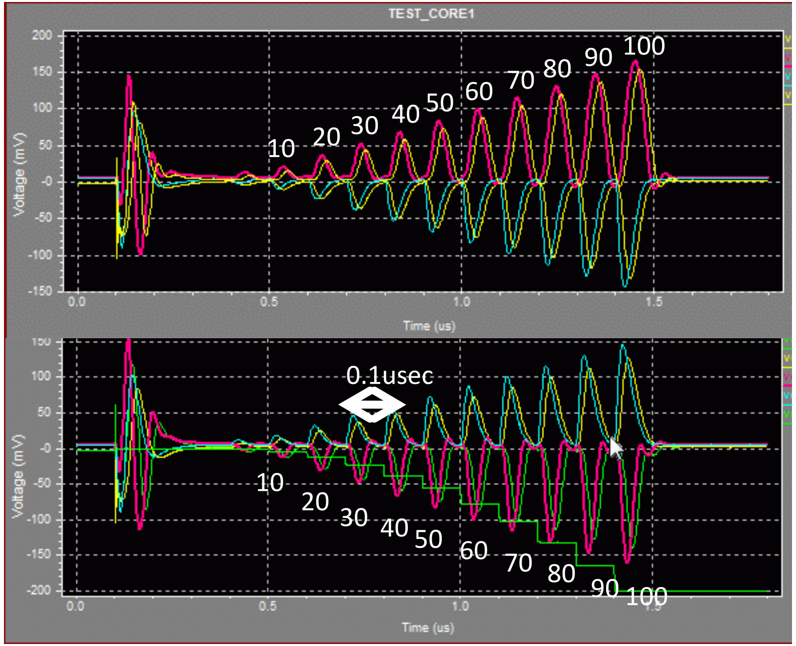
To realize all the requirements of the readout,⇒ Custom-designed ASIC for SP8-01 was developed

Block diagram of readout for 1 pixel



Design of ASIC

- Result of Simulation of Analog Amp.



🟩 Pre-amp output

🟥 Shaper output

+charge, low gain

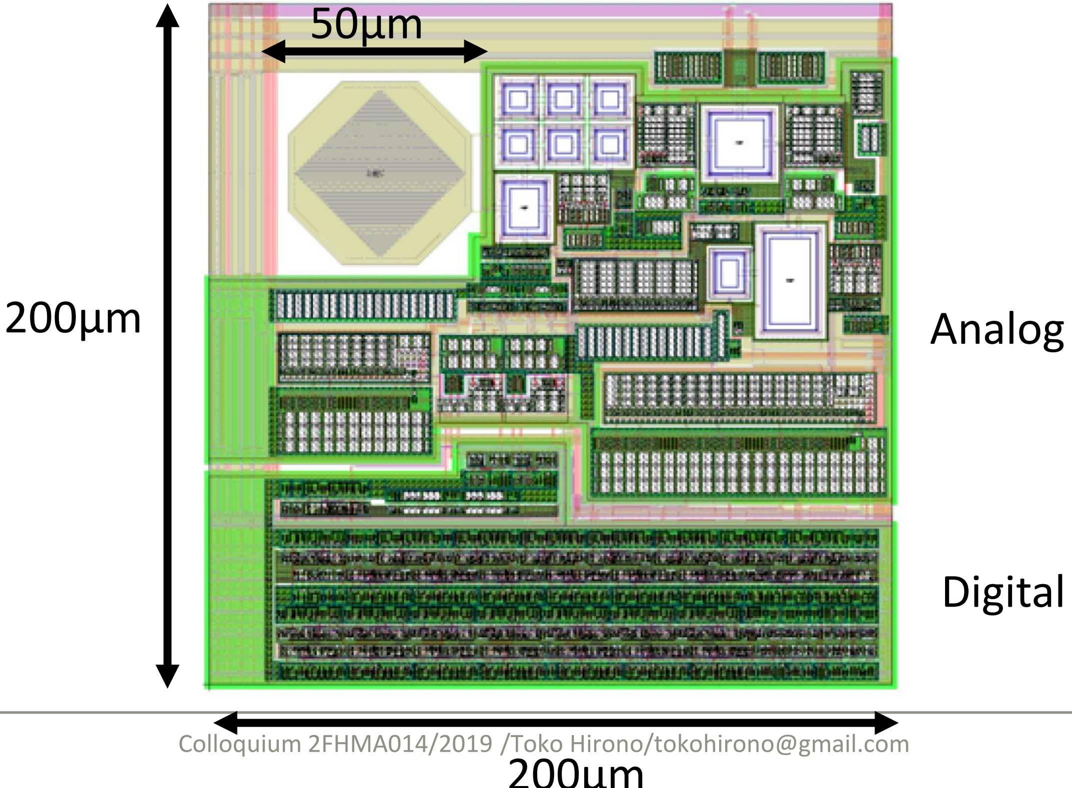
-charge, low gain

ASIC was simulated with input charge correspond to 10 -100keV in 100nsec

⇒All the parameter s of circuit was fixed to match requirements.

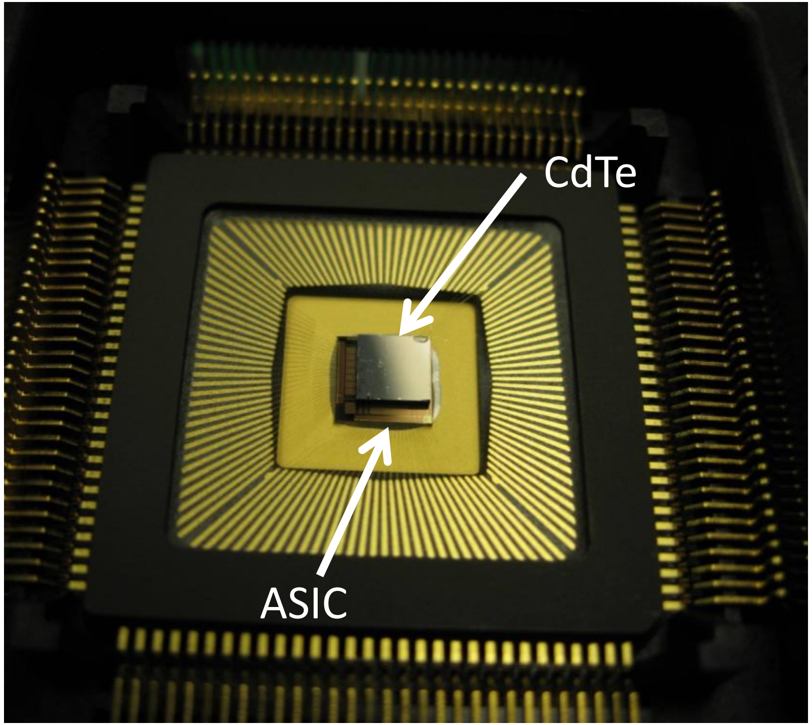
Design of ASIC

– Layout of a single pixel

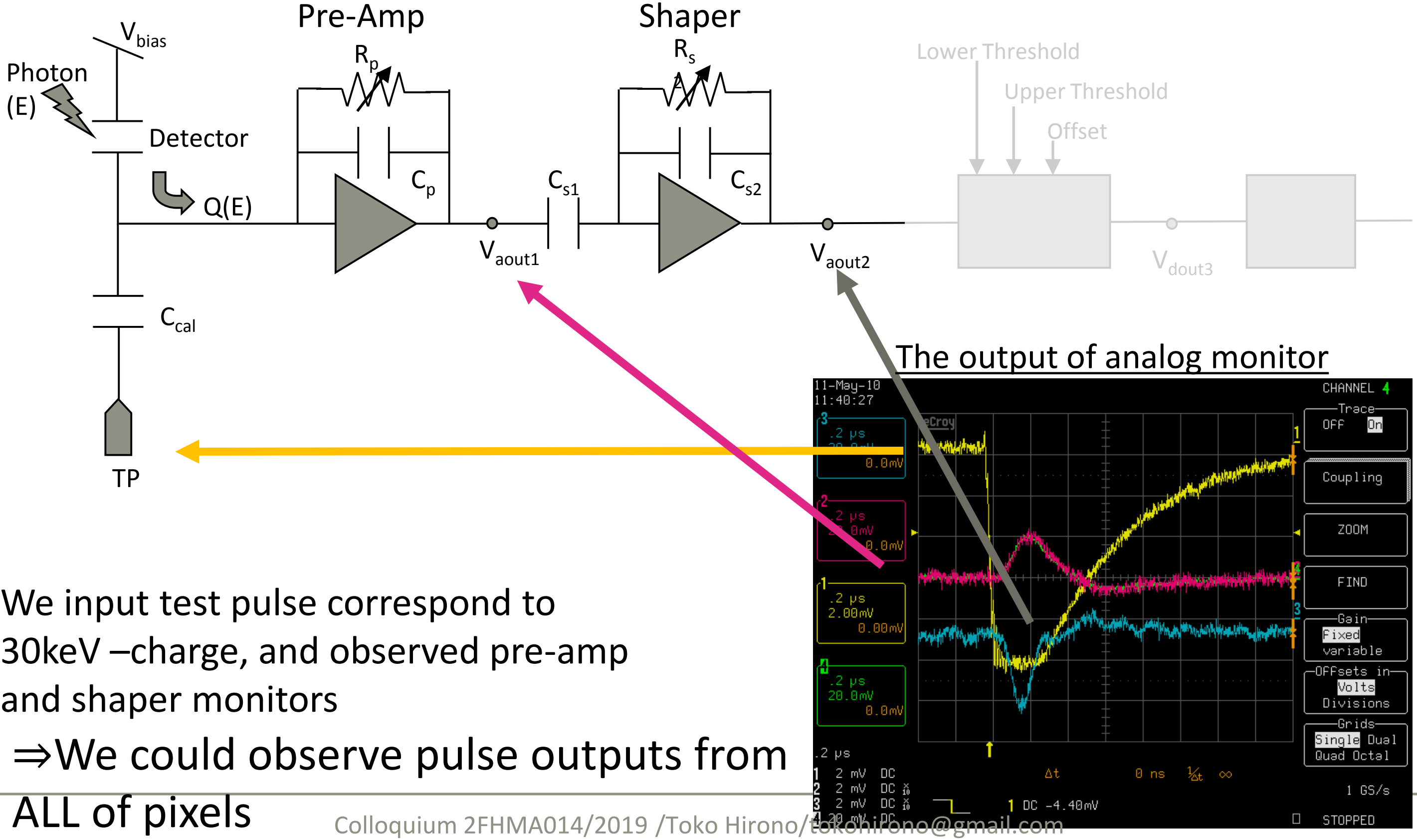


Fabrication of Detector

- ASIC was fabricated
  - TMC 0.25um
  - 5mm x 5mm
- and CdTe was bonded to the ASIC.
  - 500um thick
  - Gold-stud bonding
  - 3 types of electrode
    - Pt-pixel/CdTe/Pt
    - Al-pixel/CdTe/Pt
    - In/CdTe/Pt-pixel



Performance of ASIC



The output of analog monitor

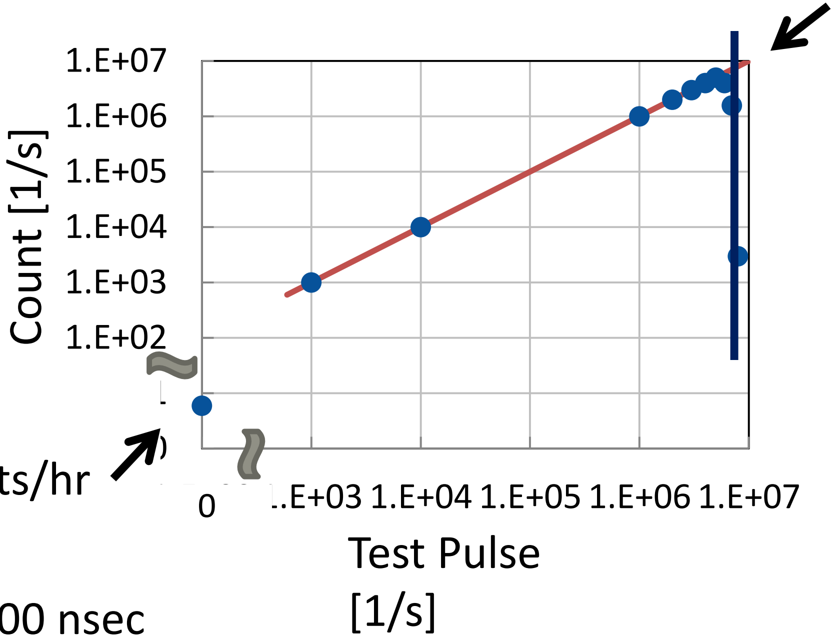
We input test pulse correspond to 30keV –charge, and observed pre-amp and shaper monitors

⇒We could observe pulse outputs from ALL of pixels

Performance of ASIC

– Time Constant of Readout

- Test pulse was counted by changing test pulse frequency.
- Counts of counter was as same as input pulse up to 5Mcounts/s



5 x 10^6counts/s

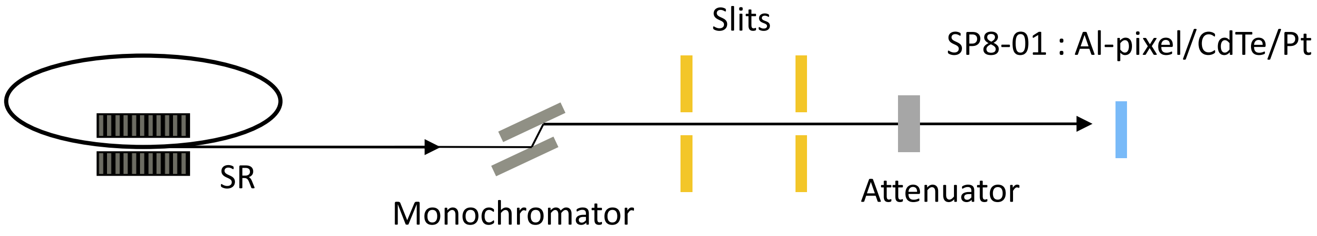
0.6counts/hr

⇒Time constant was 200 nsec c.f. designed =100 nsec

⇒Background noise 0.6 counts/hr/pixel with window-comparator 20-30 keV

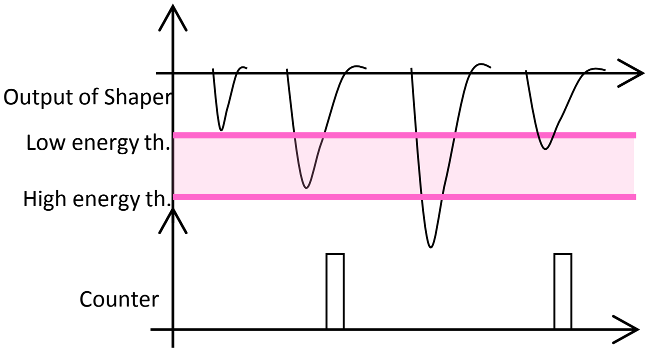
Results of Beam Test

- Beam test was performed at BL46XU, BL14B2/SPring-8



◻ Lower-energy threshold scan

⇨ to examine whether X-ray of 30 – 120 keV can be detected by SP8-01



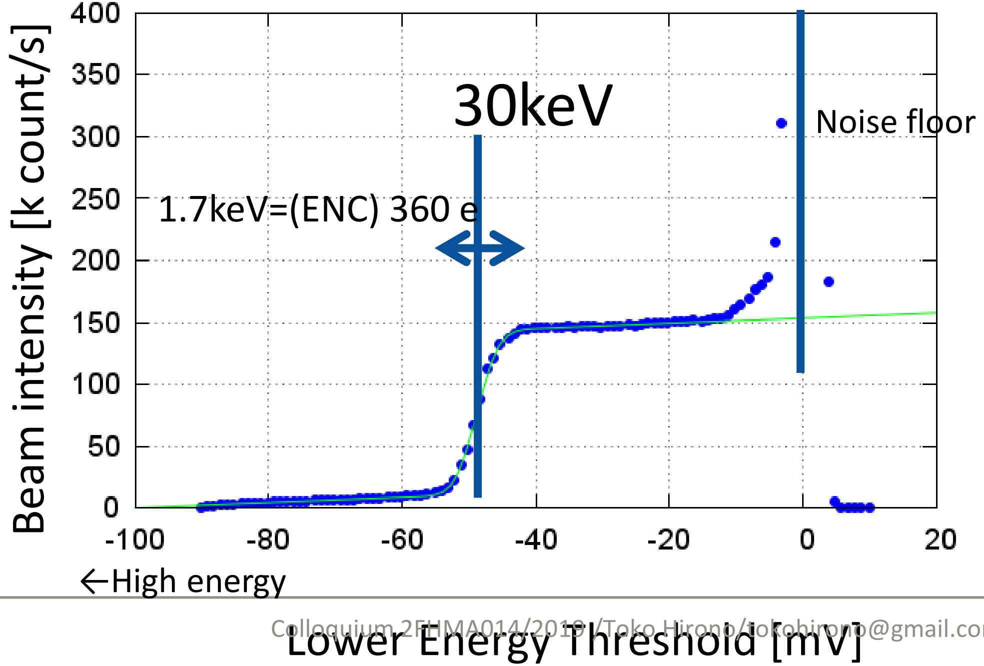
◻ Window scan

⇨ to demonstrate window comparator

Results of Beam Test

– Lower-energy threshold scan at 30keV

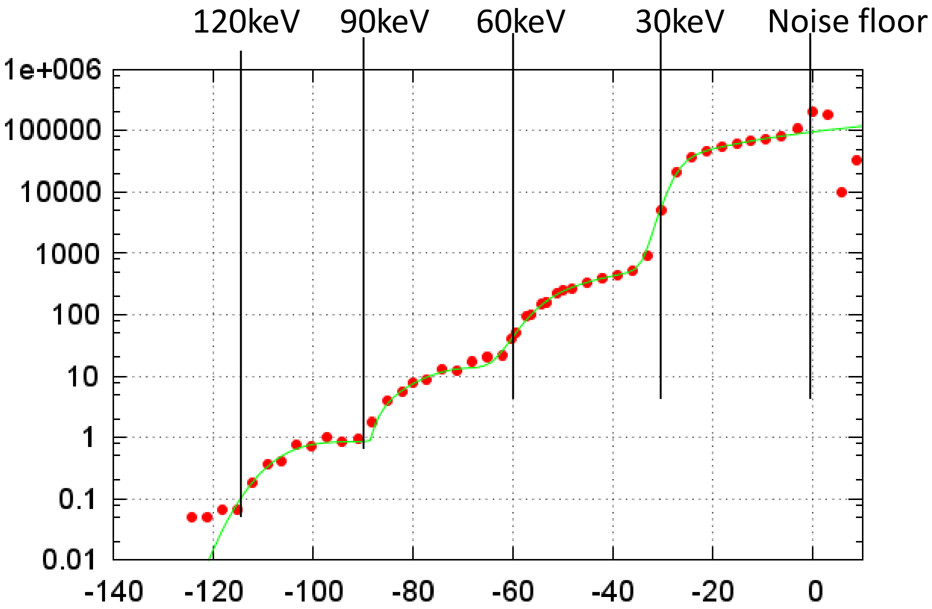
- S-curve at -49.5mV ⇒30keV
- The slop at 30keV corresponds to Equivalent Noise Charge of 360 e-



Al/CdTe/Pt (-charge)
Gain : Hig Gain
X-ray Energy : 30keV
HV: -300V
Exposure time : 0.1s

Result of Beam Test

- Lower threshold scan

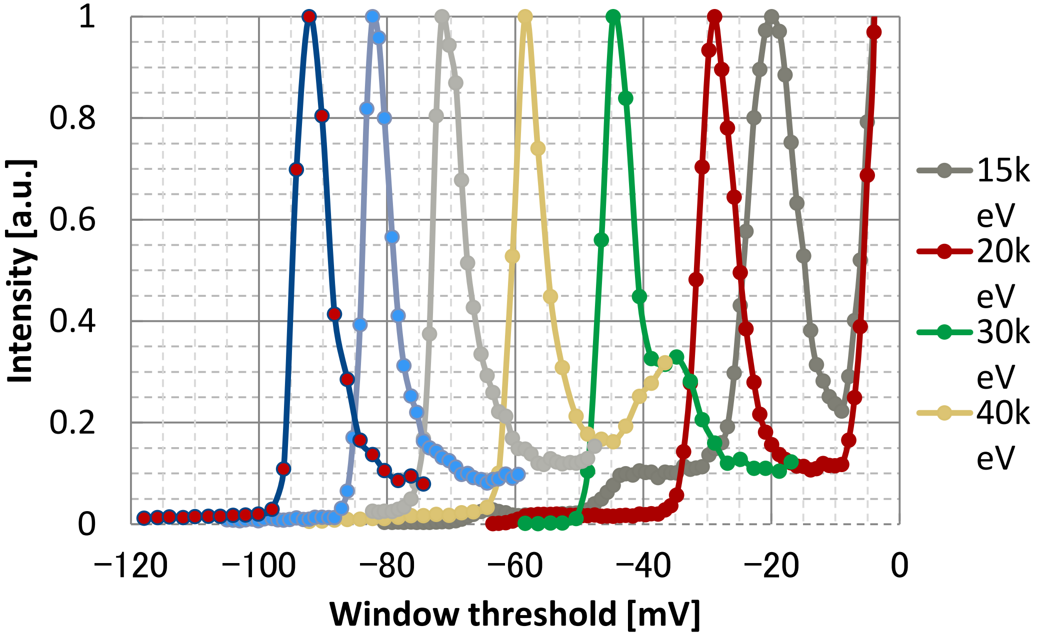


Al/CdTe/Pt (-charge)
HV : -500V
Gain : Low ,
(-66mV,-66mV)
Exp time: 5, 60sec

→X-ray up to 120keV was detected by SP8-01

Results of Beam Test

- Window scan
  - Higher/lower energy th. was scan both in same time.



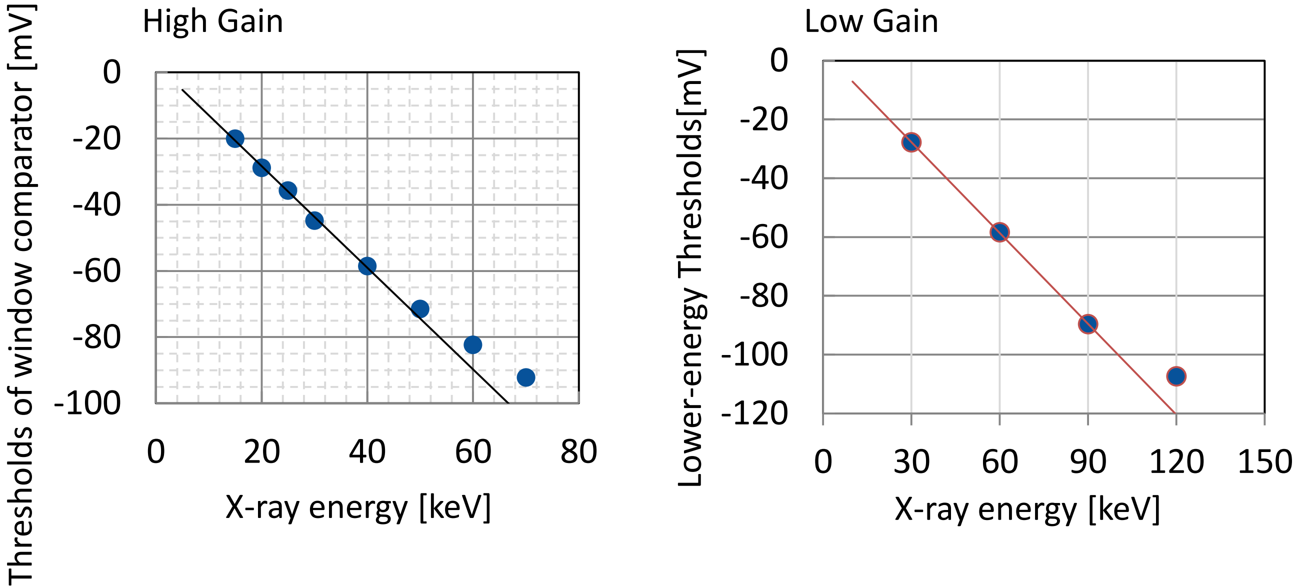
Al-pix/CdTe/Pt (-charge)
Gain : Hig Gain
HV: -300V
Exposure time : 1s
Window width :5mV

(3.2keV)
Intensity was normalized at peak.

Window comparator worked fine.

Results of Beam Test

Energy linearity of readout



- Linearity of high gain in 15-40 keV : 98%

  low gain in 30-120keV: 90%

Even more

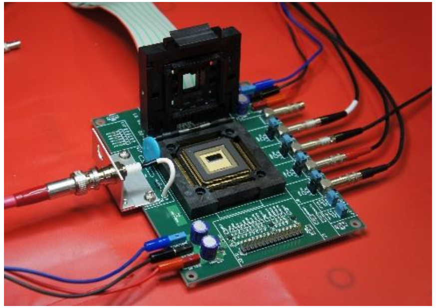
Other works

☐ CdTe detector development

CdTe has high sensitivity in 30-100 keV

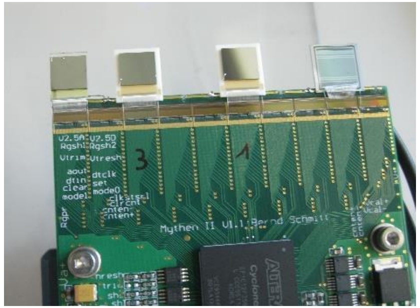
Pixel detector

CdTe + Custom-made ASIC



Strip detector

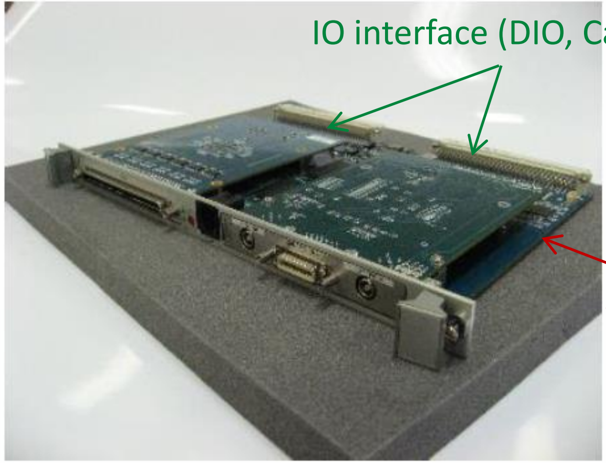
CdTe + Mythen (PSI) readout



- ASIC simulation
- Characterization of prototypes

☐ Upgrade and maintenance of control and DAQ system for beamlines

FPGA board with VME interface



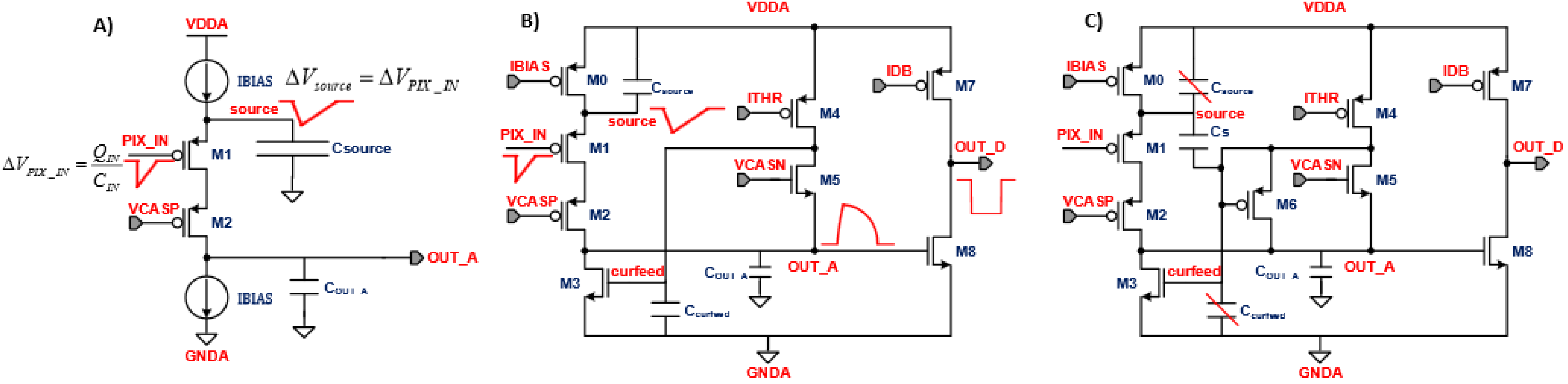
2 mezzanine cards

IO interface (DIO, CameraLink etc)

Base board

VME interface

FPGA



Kim et al,

Figure 4. Pixel front end schematic A) principle B) practical implementation C) presented circuit.

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