LUXE e^+e^- Silicon Pixel Tracker

Inputs for the Letter of Intent

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A candidate technology for the LUXE silicon pixel tracking detector is discussed. The proposal is to base the LUXE phase-0 tracking detector almost entirely on the technology used for the upgrade of the inner tracking system of the ALICE experiment at the LHC. The LUXE tracker will be assembled out of four/five layers staggered at each of the two sides of the beamline downstream the dipole magnet. Each "half-layer" is built from nine 3 cm$\times$1.5 cm ALPIDE monolithic active pixel sensors lined up to cover an area of 27 cm$\times$1.5 cm. Each "layer" comprises of two "half-layers" placed one behind another in the beam direction with a few centimetres of overlap in the transverse direction such that a total transverse length of ~ 50 cm is achieved. The ALPIDE sensors pixel-size itself is 27$\times$29 μm resulting in a spatial resolution of $\sigma \sim 5$ μm. A time resolution of a few μm was demonstrated, with a very low probability for dark current appearance, orders of magnitude lower than for hybrid pixels. These features are packed in a very low material budget of $0.05\% X_0$ per layer (sensor only).

Despite of being a relatively new technology, ALPIDE-based assemblies are already planned in several near-future experiments, besides ALICE. The performance, quality, availability, and low-cost of the end-point layers (including the sensors and all associated services) makes this solution particularly appealing for LUXE's phase-0 at least, with minimal adaptations and at a cost that can be kept well below 500 k€.

Contents

1 Introduction

The LUXE detector will provide precise position, timing and energy deposition measurements of the e^+e^- pairs produced at the interaction point (IP) between the laser and the electron/photon beam. To accomplish that, the produced pairs are first separated into electrons and positrons according to their energy by a dipole magnet placed right after the IP. The separation induced by the dipole in the horizontal direction (transverse to the beamline) is expected to reach a maximum of ~ 50 cm on each side of the beamline, while the spread in the vertical direction (also transverse to the beamline) is expected to be smaller than ~ 1 cm. It is expected that the signal e^+e^- occupancy at the detector would range from $\sim \mathcal{O}(1)$ to $\sim \mathcal{O}(1000)$ pairs per electron bunch per laser shot, depending on the different experimental setup options and notably on the laser power.

The deflected signal pairs then pass through the detector volume and interact with it to leave hit-clusters and energy depositions along their trajectory of flight. Operating with a multilayer detector along the beamline ultimately enhances the respective accuracy of the traversing particles measurement. Moreover, as different types and levels of background are expected, the multilayer approach enables to operate in "coincidence mode", as well as to constrain the origin of the particles at the IP. Hence, this approach enables a better rejection of backgrounds compared to the case where simple counters are used.

Different background sources are expected depending on the experimental setup. In the case of the electron-induced setup, backgrounds arise e.g. due to high flux of electron beam remnants which do not undergo any interaction at the IP or due to the deflected Compton-electrons. In the case of the photon-induced setup, backgrounds arise due to the interaction of beam photons with the material around the detector area (mostly shielding).

To count the e^+e^- pairs, it is in principle enough to look only at the positron content of an event (on one side of the beam) since most of the positrons seen at the detector volume can in principle only come from the IP. However, besides the ability to reconstruct the parent photon, measuring both positrons and electrons on the two sides of the beam provide a better coincidence and enables to better constrain the signal while also separating it from the different backgrounds.

Another advantage of a multilayer concept is that the energy of the charged particles can be measured more accurately from the trajectory angle with respect to the beamline axis, while knowing the precise magnetic field created by the magnet. This can be done in principle with only a few tracking layers. Nevertheless, particles can already be produced with small angles relative to the beamline and therefore the energy measurement based on the trajectory angle alone could be biased. For this reason, an independent energy measurement is needed, e.g. from a calorimeter placed downstream the tracking layers. Doing so, the resulting tracks can be matched to calorimeter clusters which provide both an independent energy measurement as well as another layer of positioning effectively.

In the sections below, a candidate technology for the LUXE tracking detector is described based on the planned upgrade of the inner tracking system (ITS) of the ALICE experiment at the LHC [1, 2]. In the heart of ALICE's ITS lies the ALPIDE [1] silicon pixel sensor [3, 4]. ALPIDE is a monolithic active pixel sensor (MAPS), i.e. integrating the sensing volume and the readout circuitry in one cell. Further developments that could be relevant for the phase-1 of LUXE are pursued, e.g. going from MAPS to fully depleted MAPS (DMAPS) as described in [5].

The entire detector is to be triggered by the laser pulses which are expected to arrive at a maximum rate of 10 Hz, i.e. the time windows when the detectors are up registring data will be synchronised with arrival time of the laser pulses. With each such trigger, the detector is read out

[1] ALPIDE stands for "ALice PIxel DEtector"

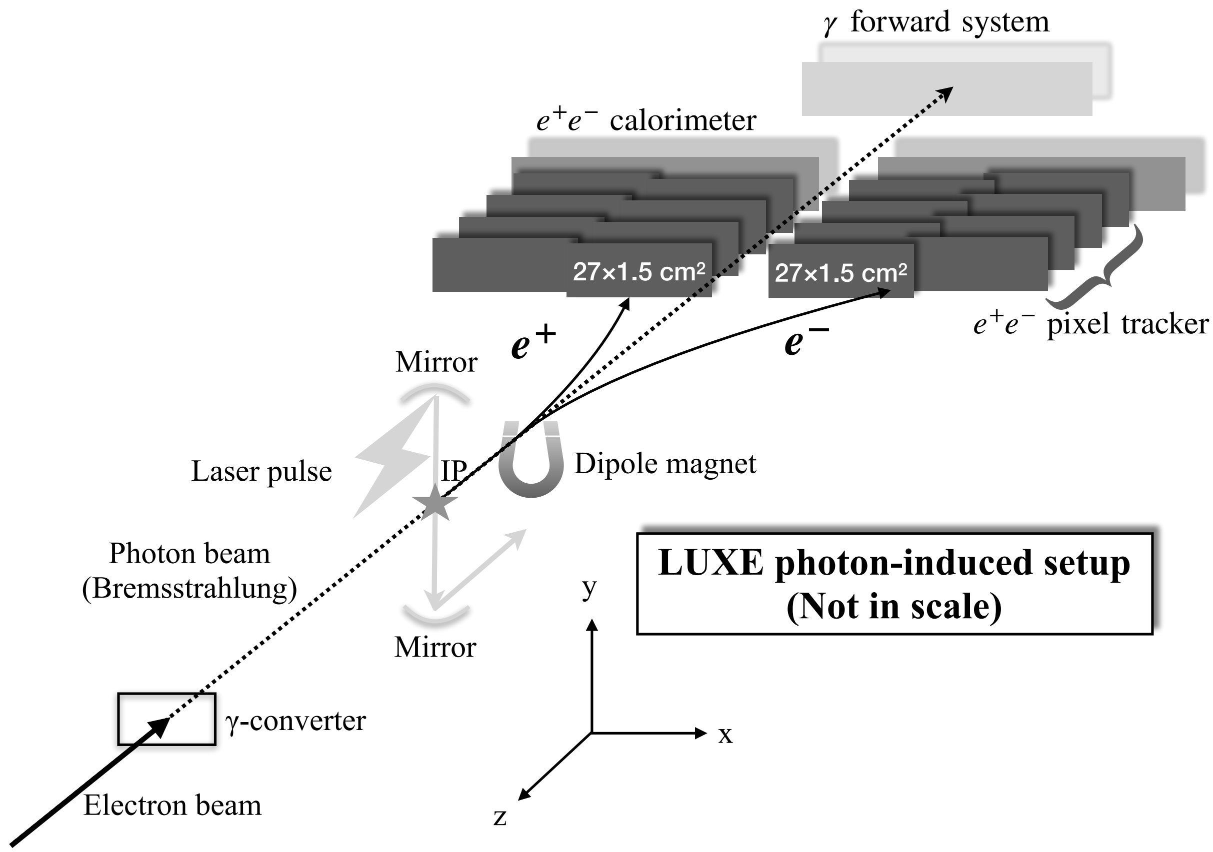

Figure 1: A conceptual layout of the LUXE detector proposal (not in scale), placed downstream the interaction point and the dipole magnet. The calorimeter and the forward photon system are shown in the layout but are not discussed in this text further.

and the raw information is stored for for later analysis.

A proposed layout of the LUXE detector in the experimental setup around the IP is shown in figure 1. It shows the e^+e^- tracking layers and calorimeter, as well as the forward photon detector system. The latter two are not discussed further in this text.

2 Technology

2.1 Monolithic Active Pixel Sensors

The common pixel sensor technology, used in most HEP experiments so far has been hybrid. Hybrid pixels constitute a relatively large material budget, typically more than $1.5\%X_0$ per layer (e.g. in the ATLAS IBL). This thickness is distributed among the module components, the cooling and support structures. The hybrid module production including bump-bonding and flip-chipping is complex and leading to a large number of production steps. Consequently, hybrid pixel detectors are comparatively expensive.

Modern CMOS imaging sensors instead make use of 3D integration to combine high resistivity and fully depleted charge collection layers with high density CMOS circuitry, forming monolithic (rather than hybrid) pixel sensors in which pixel sensor and electronics circuitry form one entity. While a combination of fully depleted high resistivity silicon with CMOS readout is in fact a requirement from particle physics, it has also independently evolved to be the standard in commercial electronics applications like smartphone image sensors.

In MAPS, the sensing volume is effectively an epitaxial layer (epi-layer) grown on top of the lower quality substrate wafer and hosting the CMOS circuitry. The thickness of this epi-layer typically is in the range of 1–20 μm, where thicker layers are often used in processes addressing CMOS camera applications. In the first MAPS, for particle detection the charge deposited in the epi-layer can be as large as $4000e^-$ for a typical thickness of 15 μm. Since the epi-material usually has low resistivity and the allowed biasing voltages are low in CMOS technologies, the epi-layer usually is depleted only very locally around the charge collection node. The deposited charge of a traversing particle therefore is mostly collected by diffusion rather than by drift. This renders the signal generation relatively slower and incomplete (i.e. not all charges arrive at the collection node). Due to the relatively longer time and path for charge collection, MAPS have usually a lower radiation hardness. Furthermore, other n-wells, e.g. those hosting PMOS transistors, act as competing nodes for charge collection. The latter can and must be cured by additional deep p-well protections. However, since the expected radiation level for HL-LHC heavy ion collisions is over three orders of magnitude lower than for LHC pp-experiments, the ALICE ITS upgrade [1, 4] has chosen the MAPS technology based on the 180 nm CMOS node offered by TowerJazz [6].

Improved development lines have been pursued leading to depleted monolithic active pixel sensors (DMAPS) [5] with the goal of employing a commercial CMOS technology with some modifications to obtain sufficient signal and fast timing in monolithic CMOS designs, while maintaining charge collection via charges drifting in an electric field inside the chip's substrate. By construction, this development should increase the radiation hardness of the sensors. To date, the DMAPS technologies are not yet as mature as "simple" MAPS. Further, the expected limited-in-time and low-rate operation in LUXE implies that the enhanced performance of the DMAPS is not strictly needed and MAPS can be used, at least for phase-0 of the experiment.

For a review of both hybrid and monolithic pixel sensors technologies, see [7].

2.2 The ALPIDE sensor

The ALPIDE chip is a 30 mm×15 mm large MAPS containing approximately 5×10^5 pixels, each measuring about 27 μm ×29 μm arranged in 512 rows and 1024 columns that are read out in a binary hit/no-hit fashion. It combines a continuously active, low-power, in-pixel discriminating front-end with a fully asynchronous, hit- driven combinatorial circuit.

The ALPIDE technology is based on the TowerJazz [6] 180 nm CMOS imaging process. The design of ALPIDE takes full advantage of the process features offered, in particular of the high integration density given by the availability of six metal layers and the small structure size as well as of the deep p-well. The latter allows PMOS transistors to be fabricated on a p-type epitaxial layer without penalising the charge collection, by shielding their n-well from the epitaxial layer as shown schematically in figure 2.

The availability of sizeable CMOS circuitry inside the pixel matrix allowed the read-out concept to be changed moving away from the classical rolling shutter readout that is usually employed in MAPS towards more power-efficient schemes. Another important feature is the availability of high-resistive (> 1 kΩcm) epitaxial layers that allow for better charge collection. It is also possible to moderately (< 10 V) reverse bias the substrate, which has been proven to significantly improve the charge collection.

The in-pixel circuitry consists of a continuously active discriminating amplifier and a multiple-event memory into which data may be strobed. The rise time of the amplifier is below 2 μs and defines the event time resolution while its shaping time is longer and makes it act as an analogue delay line. This allows data to be discriminated and strobed with a trigger latency of some 2 μs into the in-pixel buffers in a global shutter mode of operation. Strobing can also be done with fixed spacing and over longer periods, making the circuit record data continuously.

The in-pixel multiple-event memory is read out asynchronously by means of a priority encoder circuit in each double column. This is both fast and power efficient as the expected occupancies are low and only hit pixels are read out in a hit-driven fashion [8]. Data is collected at the periphery and shipped off detector by means of a high-speed serial link. The sensor is flip-chip mounted to the supporting printed circuit board using laser-soldered solder balls that are distributed over the full area of the chip.

The total power consumption is 180 mW, which corresponds to a power density of about 40 $mWcm^{-2}$. However, most of this power (about 150 mW) is dissipated by the digital interface circuitry and the high-speed output data links, which are located in a small area of about 30 mm$\times$1.5 mm close to one (long) edge of the chip. Only about a sixth of the total power is dissipated in the pixel matrix, which corresponds to a power density of about 7 $mWcm^{-2}$.

The ALPIDE prototypes have been extensively tested at laboratories as well as at a number of test beam facilities in the past few years. The chips have demonstrated very good performance both before and after irradiation For example, in [3], the chip was irradiated with the combined dose of 1 MRad and 10^{13} $n_{\mathrm{eq}}/\mathrm{cm}^2$ and it was observed to yield a signal to noise ration (SNR) ranging between 11 and 23, resulting in particle detection efficiencies above 99.5% and 98% before and after irradiation respectively. These levels of irradiation are relevant for the ALICE experiment and not for LUXE but generally, high tolerance for irradiation is going hand in hand with better time response and this is desirable for LUXE. In [4], the sensor has shown a detection efficiency above 99%, a fake hit rate much better than 10^{-5}, a spatial resolution of around ~ 5 μm and a peaking time of around 2 μs, while being radiation-hard to some $10^{13}\,1\,\mathrm{MeV}\,n_{\mathrm{eq}}/\mathrm{cm}^2$ (neutron radiation).

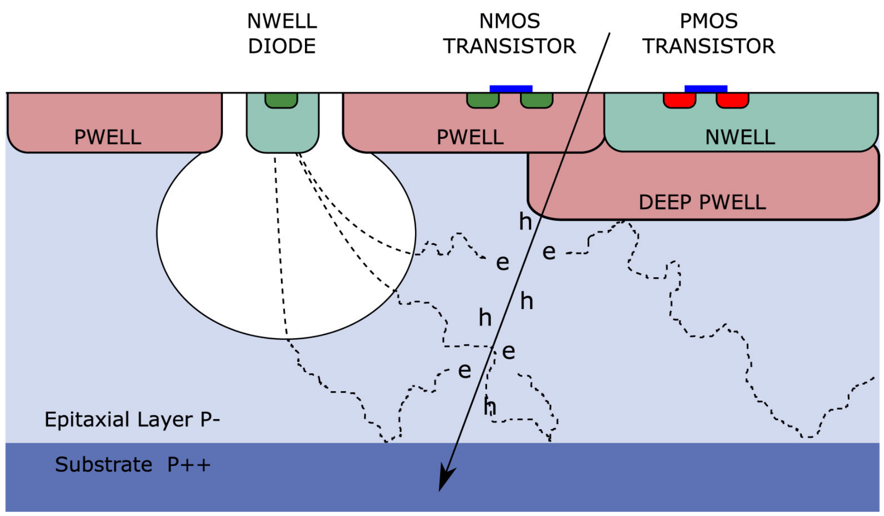

Figure 2: Schematic cross-section view of the ALPIDE pixel. The ionisation charge generated by the incident charged particle in the 25 μm thick epitaxial layer is collected by the n-well. A region in the epitaxial layer gets depleted as indicated in white by applying the bias voltage. In this zone ionisation charge is collected by drift in the electric field. Outside this region, charge motion is dominated by diffusion, hence the induced signal will be relatively slower and ionisation charge is relatively more prone to trapping, i.e. by radiation induced charge traps.

3 Detector

3.1 Staves & Layers

Each "half-layer" is built as identical assemblies named "Staves" (in ALICE), which are based on the following elements:

- **Space Frame**: a carbon fibre structure providing the mechanical support and the necessary stiffness;
- **Cold Plate**: a sheet of high thermal-conductivity carbon fibre with embedded polyimide cooling pipes, which is integrated into the space frame. The cold plate is in thermal contact with the pixel chips to remove the generated heat;
- **Hybrid Integrated Circuit (HIC)**: an assembly consisting of a polyimide flexible printed circuit (FPC) onto which the pixel chips and some passive components are bonded.

Each Stave is instrumented with one HIC, which consists of nine pixel chips in a row connected to the FPC, covering an active area of 15 mm×270.8 mm including 100 μm gaps between adjacent chips along the stave. The interconnection between pixel chips and FPC is implemented via conventional Aluminium wedge wire bonding. The electrical substrate is the flexible printed circuit that distributes the supply and bias voltages as well as the data and control signals to the pixel sensors. The HIC is glued to the "cold plate" with the pixel chips facing it in order to maximise the cooling efficiency. The polyimide cooling pipes embedded in the cold plate have an inner diameter of 1.024 mm and a wall thickness of 25 μm. These are filled with water during operation.

A schematic drawing and a photograph of the stave are shown in figures 3 and 4, respectively. An extension of the FPC, not shown in the figure, connects the Stave to a patch panel that is served by the electrical services entering the detector only from one side.

The overall structure mean thickness is $X/X_0 = 0.357\%$, with the material budget broken down to fractions of the total width as: $\sim 15\%$ silicon sensor (with absolute thickness of 50 μm), $\sim 50\%$ electrical substrate (FPC) including the passive components and the glue, $\sim 20\%$ cooling circuit and $\sim 15\%$ carbon spaceframe.

In LUXE, each stave would serve as a "half-layer" such that the total transverse length of one layer (on each side of the beam) would be roughly 50 cm as can be seen in figure 1. The two staves of one layer could be either staggered behind each other with a small ($\sim$ 2 cm) overlap, or in a

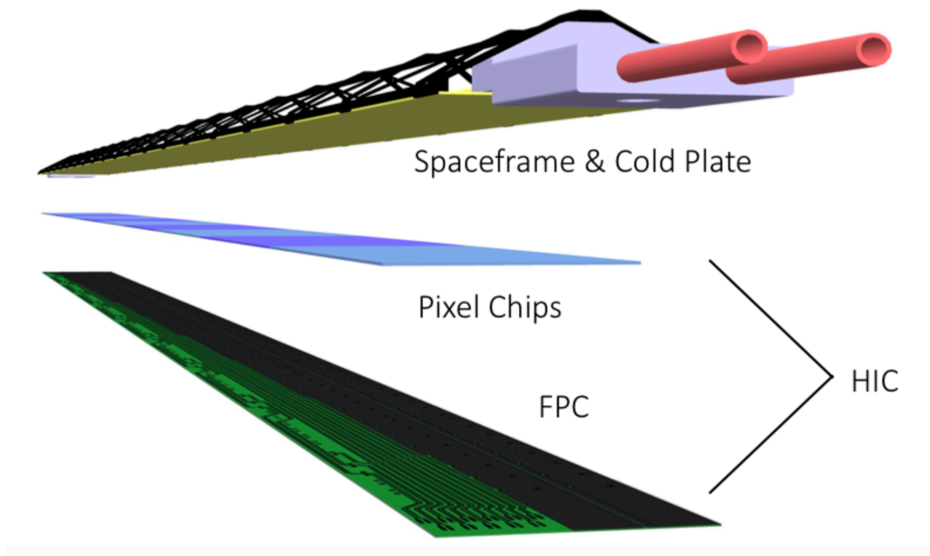

Figure 3: Schematic layout of a single stave. Nine pixel sensors are flip-chip mounted on a flexible printed circuit (FPC) to form a hybrid integrated circuit (HIC). The HIC is glued on a carbon fibre support structure (Spaceframe), which integrates a water cooling circuit (Cold Plate). An extension of the FPC, not shown in the figure, connects the Stave to a patch panel that is served by the electrical services entering the detector only from one side.

row, creating a small gap between the staves. To cover for the 100 μm gaps between the sensors of one stave, the layers would be placed with a small offset with respect to each other. so that any given track would be measured by at least three layers.

3.2 Readout electronics and computing

The FPCs of all staves are connected to a patch panel that is served by the electrical services entering the detector only from one side. Each sensor has its own readout line with 2 Gb/s with a standard Samtec cables transmitting the signal. Two readout frameworks can be used. Namely, the MOSAIC readout system developed in Bari, Italy, which can read a few staves simultaneously or the ALICE readout unit (one per stave) which can be connected via a GBT link PCI express. One DAQ PC can in principle handle 24 staves although some redundancy should be considered. **To be completed soon.**

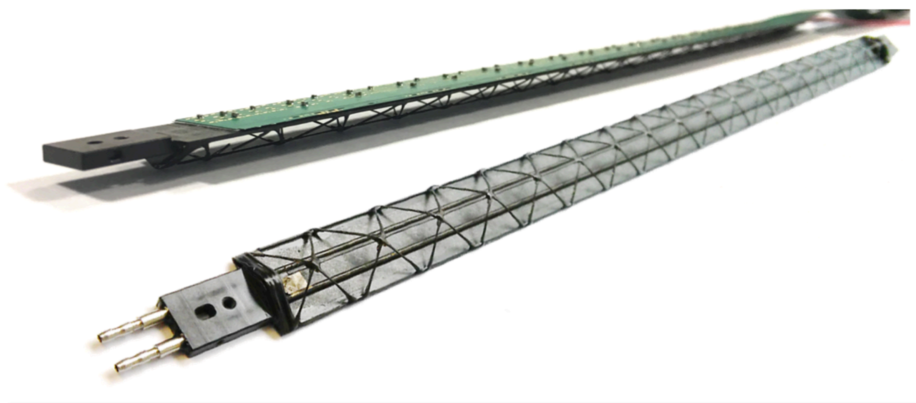

Figure 4: Photograph of a production sample of a single stave.

3.3 Services

Here I don't yet have a good feeling about what we need exactly. I would need to have the drawings of the beam area where we plan to place the detector and sit with the engineering people at WIS on the design of the stands, motorised stages, etc. Besides that, I will meet with Luciano M. at CERN in early July to understand better what we need in terms of services.

Here we assume four layers positioned behind each other on the two sides of the beam, stretching to ~ 50 cm in the transverse direction. The entire structure would have to be mounted on two, remotely controlled motorised stages, which in turn should sit on an anti-vibration stand. The motorised stages are important in view of the expected limited access to the beam area during the operation of the XFEL. The movable stages should allow aligning the two sides of the detector independently with respect to the beam and IP and therefore, three degrees of freedom are needed. The staves of each stage will be pre-aligned on surface before mounting it in the beam area.

TBD: High- and low-voltage power supply would be needed. Air and water cooling would be needed. Cabling, Shielding and all that...

3.4 Simulation

TBD. Detailed simulation software, featuring a complete geometry and material description for the ALICE staves exists in [9]. Currently this software is based on GEANT3 although it is in principle also compatible with GEANT4. The workflow is as follows: particles→hits→clusters→tracks, where "particles" stands for the physics part (coming e.g. from a particle gun), the "hits" part is the digitised detector response and finally, "clustering" and "tracking" is the tracks reconstruction part. This software has to be interfaced with the output of the physics simulation of the e^+e^- pair production in the different setup options of LUXE. This simulation should be used to optimise the engineering design of the LUXE detector beyond the staves themselves, e.g. the distances between layers along the beamline etc.

4 Costs

The cost and availability of all tracker elements is discussed in table 1. The staves are assumed to be of the "gold category" which means, less than 50 dead pixels per sensor (i.e. 50 dead out of ∼500k). The integration and adaptations of all components requires some careful engineering work which not be negligible cost-wise. **TBD: all items in the table beyond the stave should be estimated still. The total cost, including the staves, will most probably not be below ∼500k CHF.**.

Item	Source	Unit price [kCHF]	Quantity	Total price [kCHF]
Stave	CERN	13	16+2	234
HV power supply	x	**TBD in July**	x	x
LV power supply	x	**TBD in July**	x	x
Cabling	x	**TBD in July**	x	x
Cooling	x	**TBD in July**	x	x
Anti-vibration stand	Thorlabs	5	2	10
Motorised stage	Thorlabs	13	2	26
Readout electronics	CERN	**TBD in July**	x	x
Computing	x	x	x	x

Table 1: Detector cost breakdown.

5 Summary

This document describes one possible and conceptual realisation of the LUXE tracker. It is built on the basic ALPIDE MAPS technology, and moreover, on the integrated ALICE ITS staves which provide an almost-complete solution for a single tracking layer. A spatial resolution of $\sim 5\ \mu$m could be achieved, with a peaking time of a few μs, and hence, given the expected 10 Hz laser pulse rate (i.e. the detector trigger rate) this option is more than suitable for LUXE's physics program. The cost for the tracker is expected to be well below 500 k€with the staves alone for four ~ 50 cm long layers being approximately ~ 240 k€. The lead time for a complete tested "gold category" stave is in principle immediate with initial support from the ALICE/CERN experts in terms of simulation, assembly and operation.

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