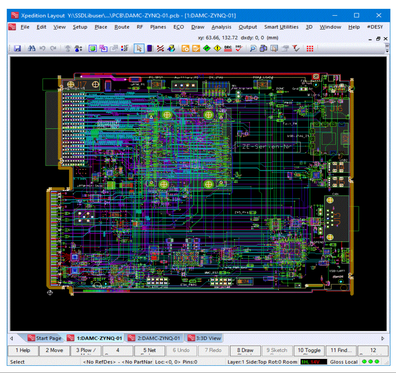
Elektronikentwicklung bei FE.

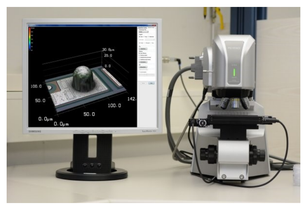
M. Zimmer (FEA), P. Göttlicher (FEB), K. Hansen (FEC)

Aufgaben

- FE ist organisiert in 3 Fachgruppen
  - **FEA** Digitale Elektronik und Datenerfassungssysteme
  - **FEB** Analog Elektronik
  - **FEC** Mikroelektronik und Aufbau/Verbindungstechnik
- Zentrale Elektronikentwicklung für alle Bereiche bei DESY
- Zentrale Bereitstellung von Werkzeugen zur Elektronik Entwicklung für DESY Anwender
  - Mentor Graphics xDesigner / Xpedition
  - CADENCE IC Design Tools
  - XILINX Tools



Laser Scan Mikroskop

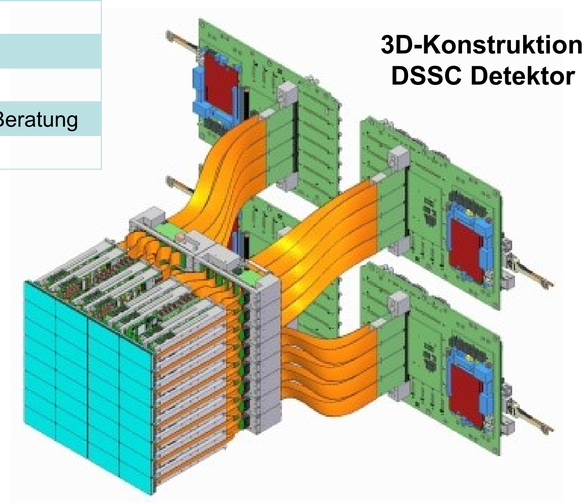


Kernkompetenzen

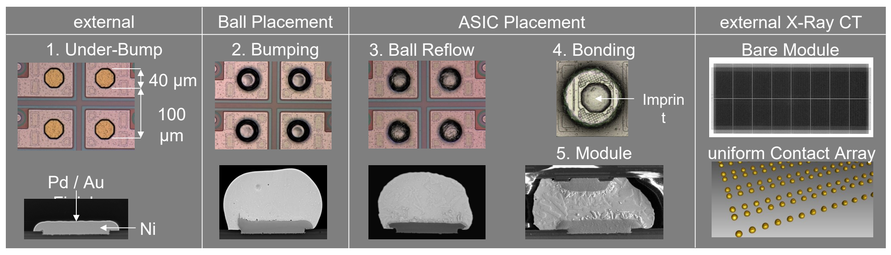
Schnelle FPGA - basierte Datenerfassungssysteme xTCA, PXI, PCIe, schnelle serielle Links, 10G/100G-Ethernet
Auslese und Aufbereitung empfindlicher Analogsignale
ASIC-Entwicklung (Analog, Mixed Signal, Digital), Mikroelektronik, Silicon Photonics
Aufbau- und Verbindungstechnik, Flip-Chip bonden, Drahtbonden, Klebetechniken, Mikroskopie
PCB Schaltungsentwicklung und Layout
Hardwarenahe Firm- und Softwareentwicklung
Komplexe Messtechnik
Systemdesign, Simulation, EMV, Systemintegration, Beratung
Elektromechanik, 3 D-Konstruktion

Datenerfassungskarte mit 4 * 10GBit/s Ports

3D-Konstruktion DSSC Detektor

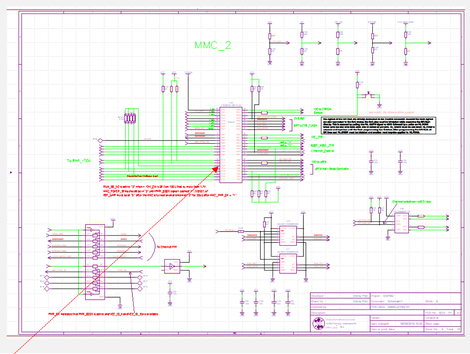


Bump Bonding Prozess

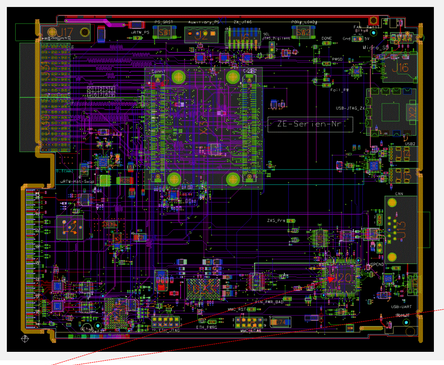


Von der Idee zur Leiterplatte

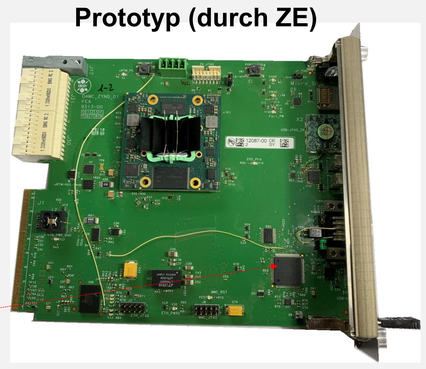
Schaltplanentwicklung



Layout



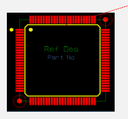
Prototyp (durch ZE)



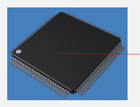
Bauteilerstellung für ECAD System

Bauteil (Mikrocontroller)

Symbol für Schaltplan

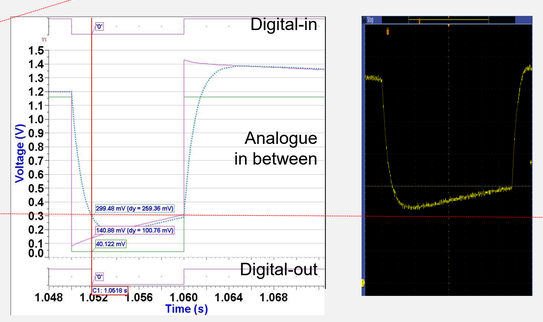


Footprint für Layout

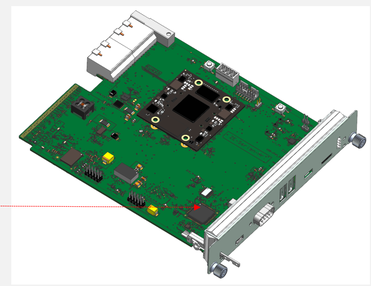


3D-Modell

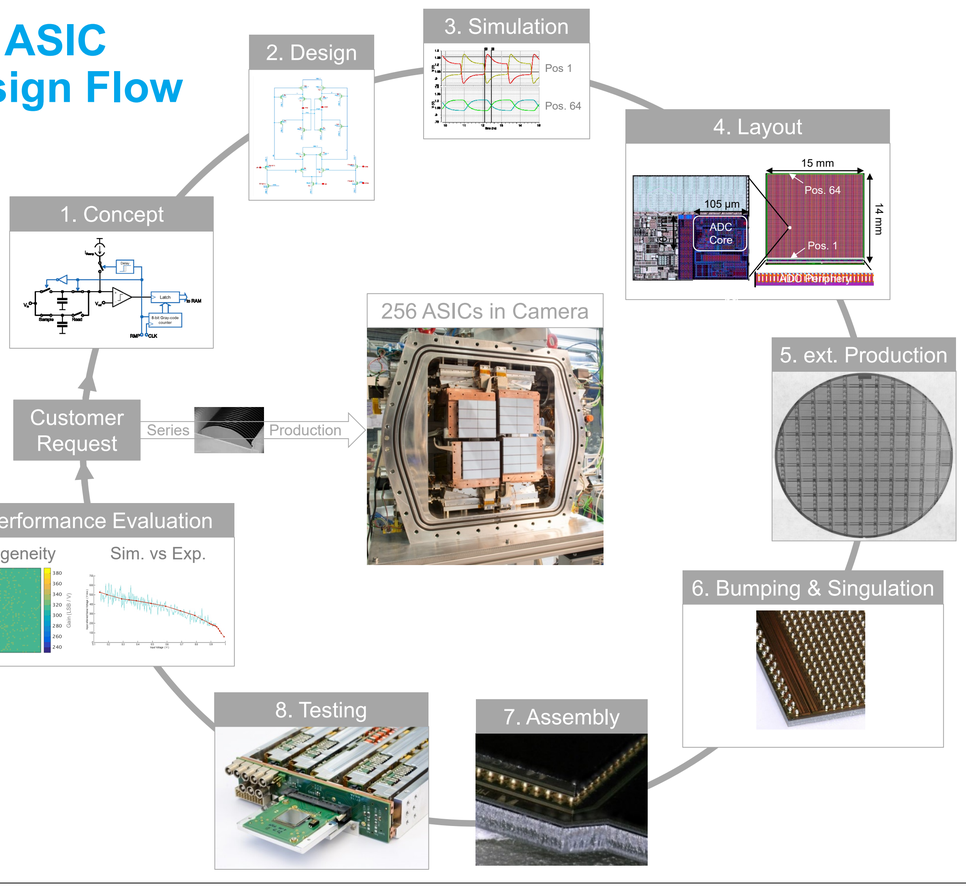
Simulation



3D-Modell für Konstruktion



ASIC Design Flow



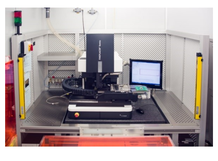
Blick in unser Mikroelektronik Labor

Das Labor wird auch regelmäßig von Kolleg*Innen außerhalb FE's benutzt

Manuelle Probe Station

Automatische Probe Station

System zur Platzierung der Lötbälle (FlipChip)



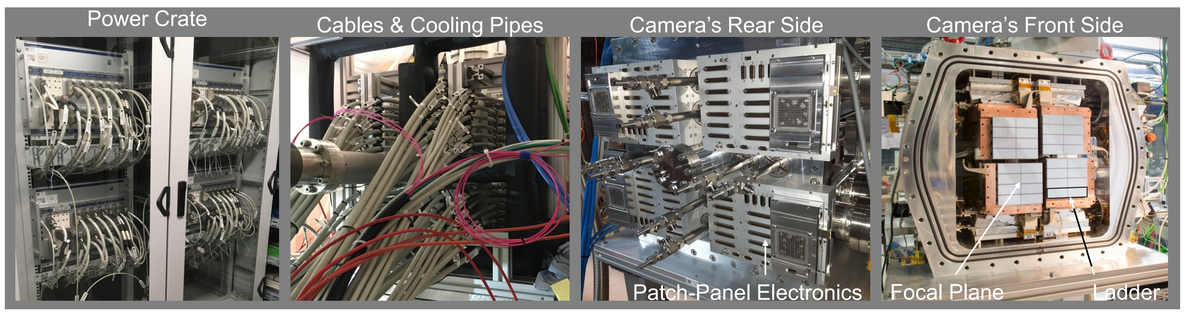
FlipChip Bonder

Halbautomatischer Draht Bonder

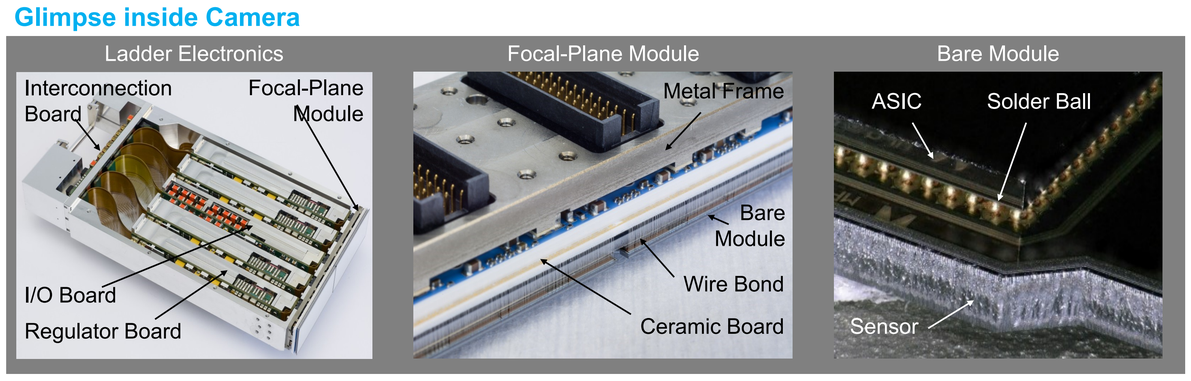
Electronics Development Group FE : Recent Key Projects.

M. Zimmer (FEA), P. Göttlicher (FEB), K. Hansen (FEC)

DSSC: World's fastest soft X-ray mega-pixel imager for the European XFEL



Glimpse inside Camera



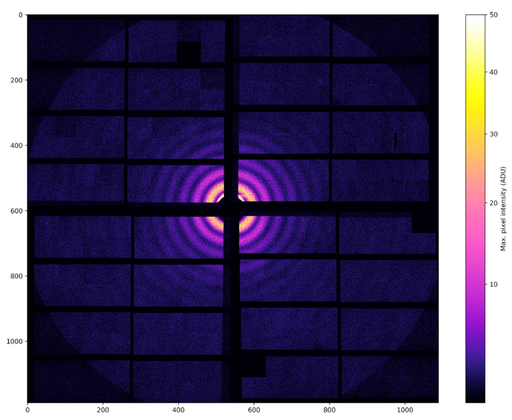
Contributions from DESY-FEC

- PCBs (exc. I/O board) & mechanics
- Patch-panel electronics
- Cabling & power crate
- Ceramic board & mechanics
- Pixel-level 8-bit 4.5-MSps ADC with adjustable gain & offset
- On-chip clock- & data distribution
- Bandgap & reference current distribution

Unique Features

- Pixel-level digitization & digital storage of ≤ 800 frames at 4.5 MHz
- Power pulsing (total 260 W: 245 µW per Pixel)
- Ultra-high vacuum capability < 10^{-7} mbar
- Very low-noise of 60 electrons
- Future upgrade with active DEPFET sensors

First photons seen at SCS instrument



Commissioning: Single-shot diffraction image of pinholes with 707-eV photons

DSSC Consortium

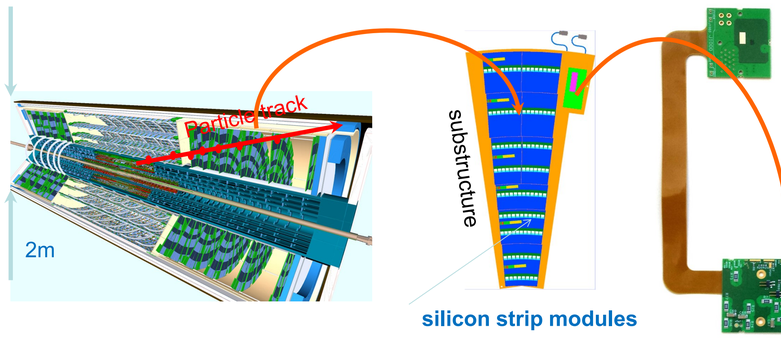
- ASIC team
  - ✓ Politecnico di Milano
  - ✓ Università di Bergamo
  - ✓ University of Heidelberg
  - ✓ DESY-FEC
- Module team
  - ✓ University of Heidelberg
  - ✓ DESY-FEC
- Integration team
  - ✓ XFEL
  - ✓ DESY FS-DS
  - ✓ DESY-FEC
- Mini-SDD sensor from MPG-HLL

With support from

- DESY-ZE
  - ✓ PCB procurement
  - ✓ PCB assembly
- AEMtec GmbH, Berlin
  - ✓ Mounting & wire bonding

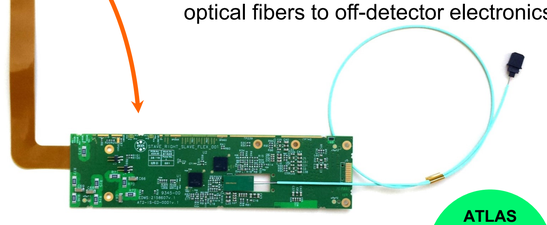
Contact:
Karsten Hansen, FEC

Electronics for the ATLAS Inner Tracker End-of-Substructure Card EoS



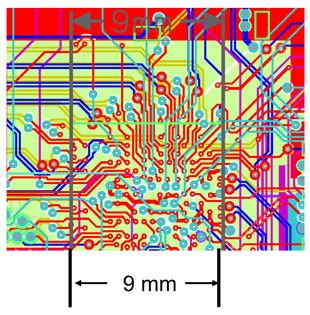
Functionality

- External communication via 2 * 10Gbit/s in LHC protocol
- Control of frontend modules, which collect hits in silicon strips from the particle flying through it
- Multiplex the data from modules and send them on optical fibers to off-detector electronics



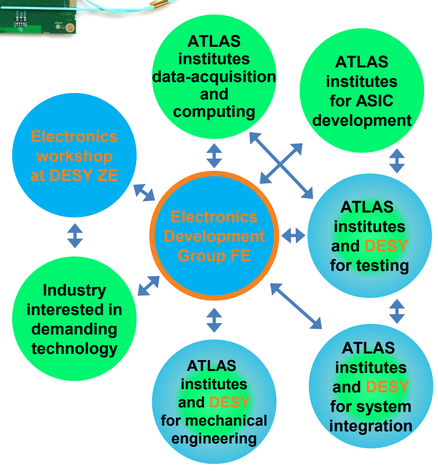
Challenges

- Demanding reliability
- Dense signaling
- Fast signals
- Low noise
- Thermal contacts
- Small outline



Collaborative Design

- Concurrent engineering
- Continuous technical communication and coordination between partners from institutes and industry

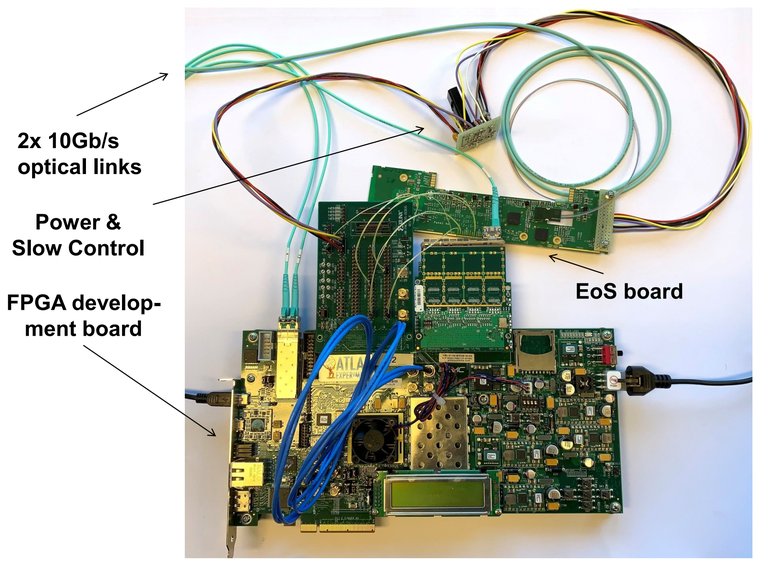


Contact:
Peter Göttlicher, FEB

EoS Test System

Automated series test for the production about 2000 boards

- Prototype of test setup
- Programming and reading of the configuration registers
- Test of Bit Error Rates for 10GBit/s uplinks and 2.5 Gbit/s downlinks
- Test of clock outputs



FPGA based high speed DAQ Systems

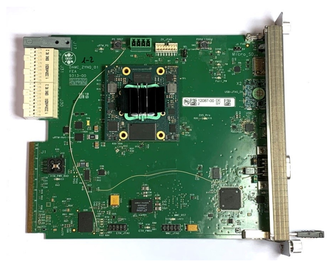
MicroTCA.4 developments

- Crate standard introduced by telecommunication industries
- MTCA.4: Programmable front-board with application specific Rear Transition Module (RTM)

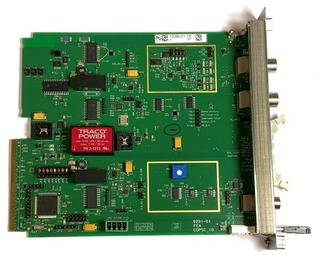
Control system for accelerator magnet power supplies (COPSC)

- FE's latest MTCA development together with MCS
- Will replace outdated control system
- Cost effective MTCA.4 compatible CPU board based on a ZYNQ SoC with essential peripheral interfaces
  - USB, SD-card, CAN-Bus, RTM Connector
- I/O Board for analogue and digital I/O from magnets
- Several hundred boards will be produced in future

DAMC-ZYNQ CPU board



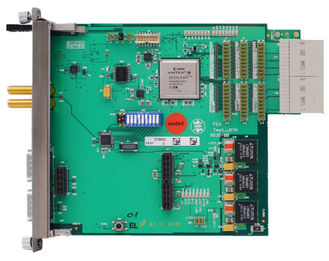
I/O board



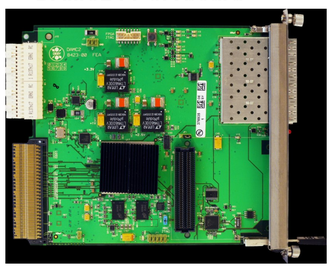
XFEL / FLASH machine control system

- DAMC2 (more than 800 boards in use)
- Used for several applications with different RTMs

Rear Transition Module



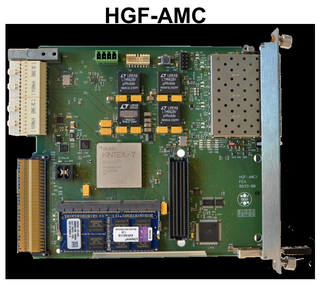
DAMC2 FPGA board



HGF AMC

- Powerful version of DAMC2 with 10GBit/s Ethernet
- Common Development together with KIT
- Used by HGF institutes KIT, HZDR, FZJ

HGF-AMC



100GBit/s developments

- Future detector systems require very high Bandwidth
- Routing of PCBs with 25GBit/s traces is very delicate (PCB Material, trace geometries etc.)
- Test board (without FPGA) was developed for systematic studies of signal quality and bit error rates depending on trace length and signal conditioning with repeaters