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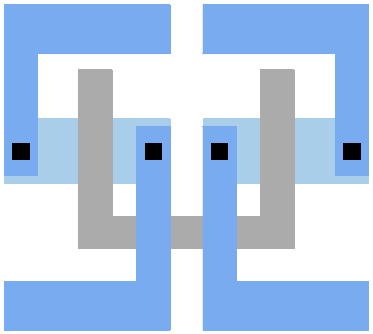
Fast(er) Emergency Shutdown



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PXD Workshop

Hamburg

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Introduction

- Objective: Improve shutdown time on beam-loss conditions.
- Current situation:
  - All interlocks are received via the VLHI system, which provides only a slow signal (up to 8 ms response time of the output module).
  - On power-off, the charge in the module is only drained parasitically.

- Two (mostly) independent subprojects identified:
  - Add an additional interlock input directly from the DCU.
    ⇒ Start the shutdown procedure earlier.
  - Actively short the power supply outputs.
    ⇒ Speed up the shutdown.

- Both subprojects require modifications to the power supply hardware, but in different areas.
  ⇒ Implement at the same time?
- With both projects implemented, we still will not completely power off before the beam dump is complete.

Direct Interlock from the DCU

The Plan

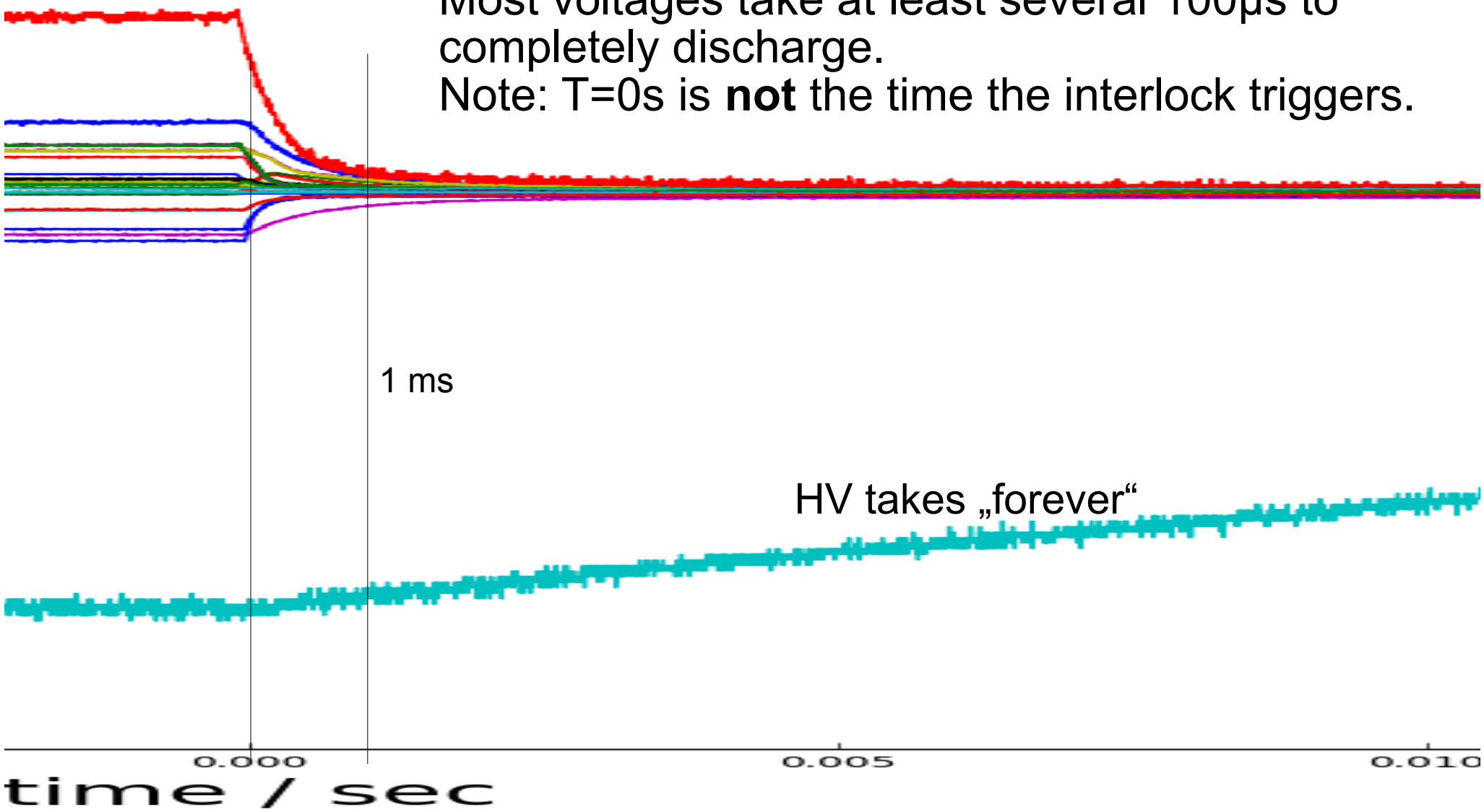
- Add an additional direct interlock line from DCU to PXD PS.
  - A suitable signal is already available on top of Belle.
  - It's a single NIM signal, so my proposal is to receive it once and then distribute internally (between Backplanes).
- Modify the interlock cabling to connect this as the second interlock of the PS unit.
- Add circuitry to disable the interlock to the Backplane.
  - The „normal“ interlock can be controlled via the VLHI.
  - The new diamond interlock also needs some sort of control.
  - Proposal: Modify the PS backplane to make the interlock switchable from the Crate Controller:

    We are lucky: The CC design was for four PS units per backplane, we have only three.
    ⇒ There is one more control bit available. We should be able to use that.
    ⇒ We need only modify the (hopefully cheap) backplane, not the more complex CC.

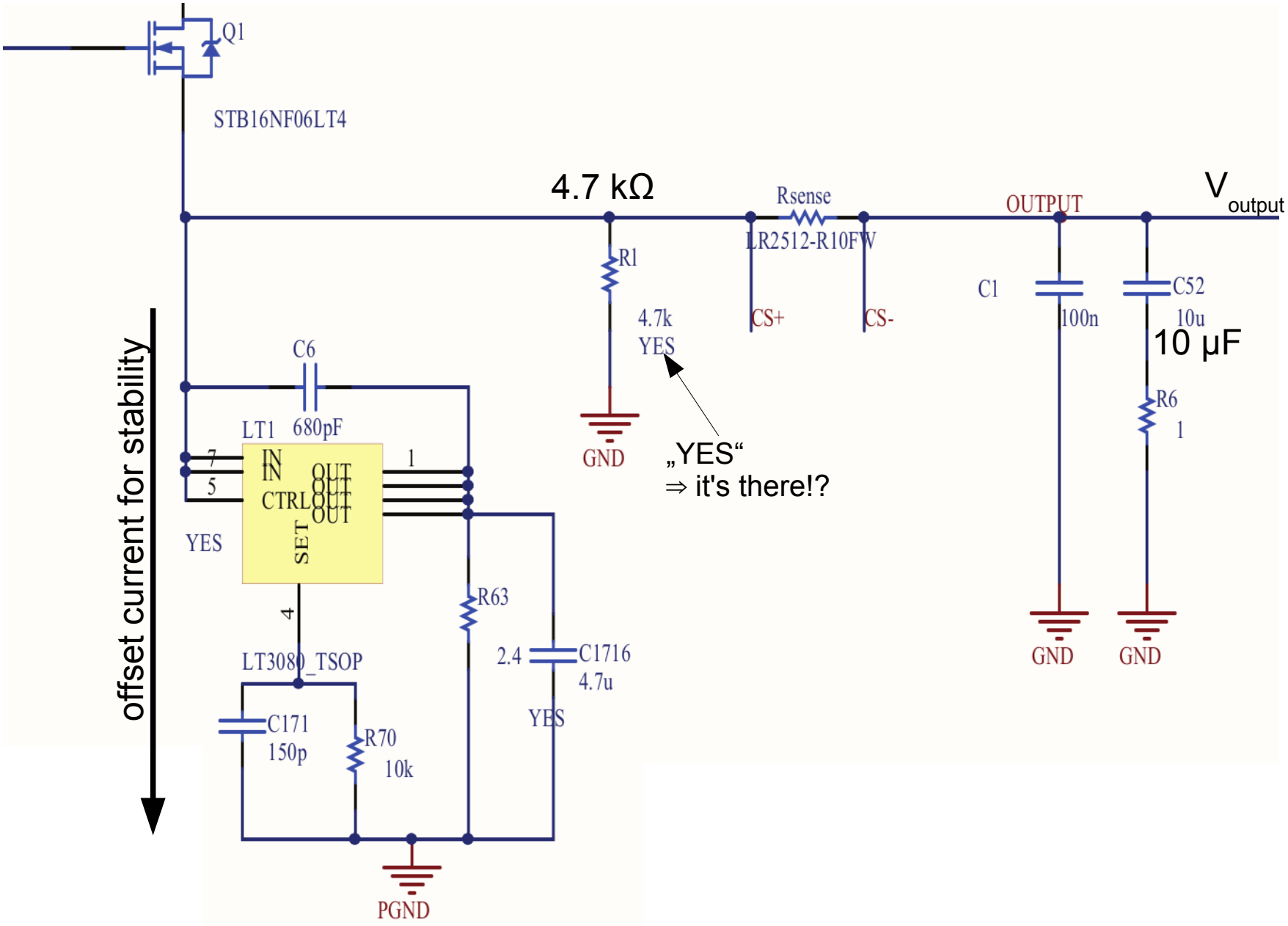
Active Power-Off

Where We Are Coming From

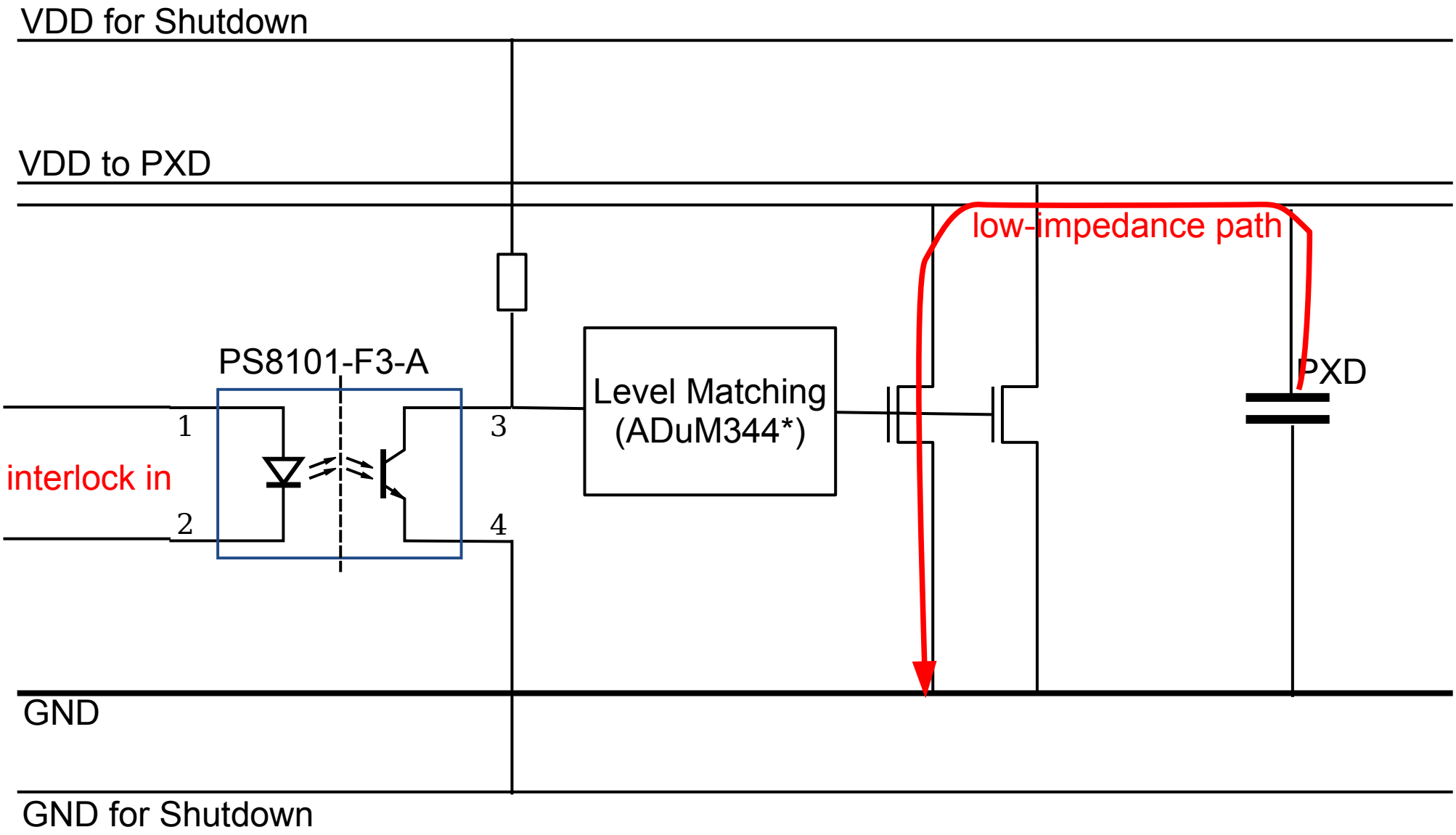
- Philipp's and Markus' measurements of the shutdown timing:
  Most voltages take at least several 100µs to completely discharge.
  Note: T=0s is **not** the time the interlock triggers.



Unipolar Output Stage



The Basic Idea (First Test PCB)

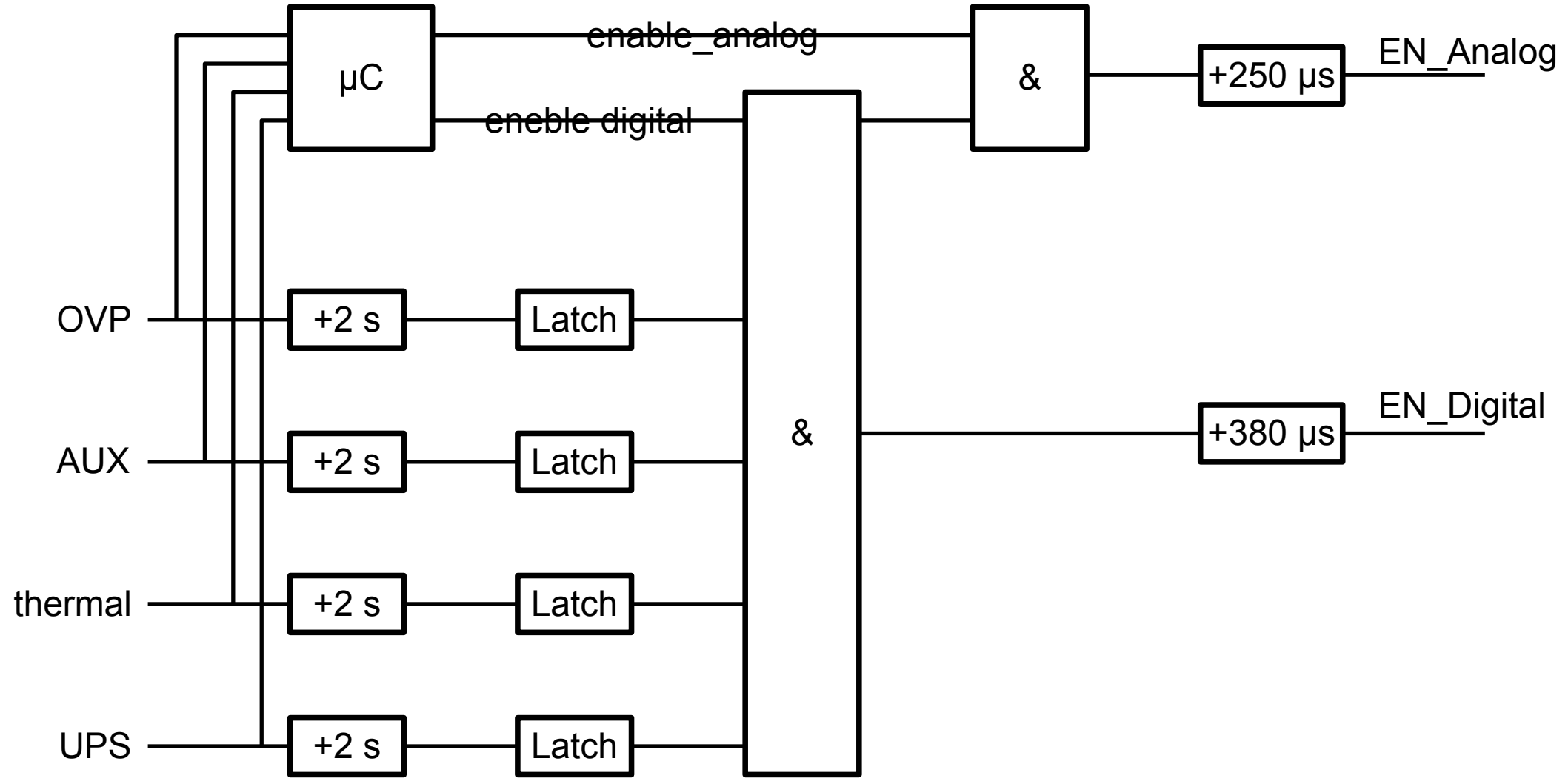


LMU PS Design

- The PS is a modular design with
  - Back PCB
  - Front PCB
  - MCU card
  - Regulator cards (3 different kinds)
  - DC/DC card
  - OVP card
- All cards can be replaced independently.
- The interlock connectors are on the back PCB.
- Interlock handling is on the MCU card.
- Connections between all cards are on the Front PCB.
  - Also the output connectors.
  - ⇒ This is **the** central place.

Delays within the PS Unit

- Fixed delays to ensure „analog off first“.
- Purpose of the 2 second(!) delay at the input unclear.

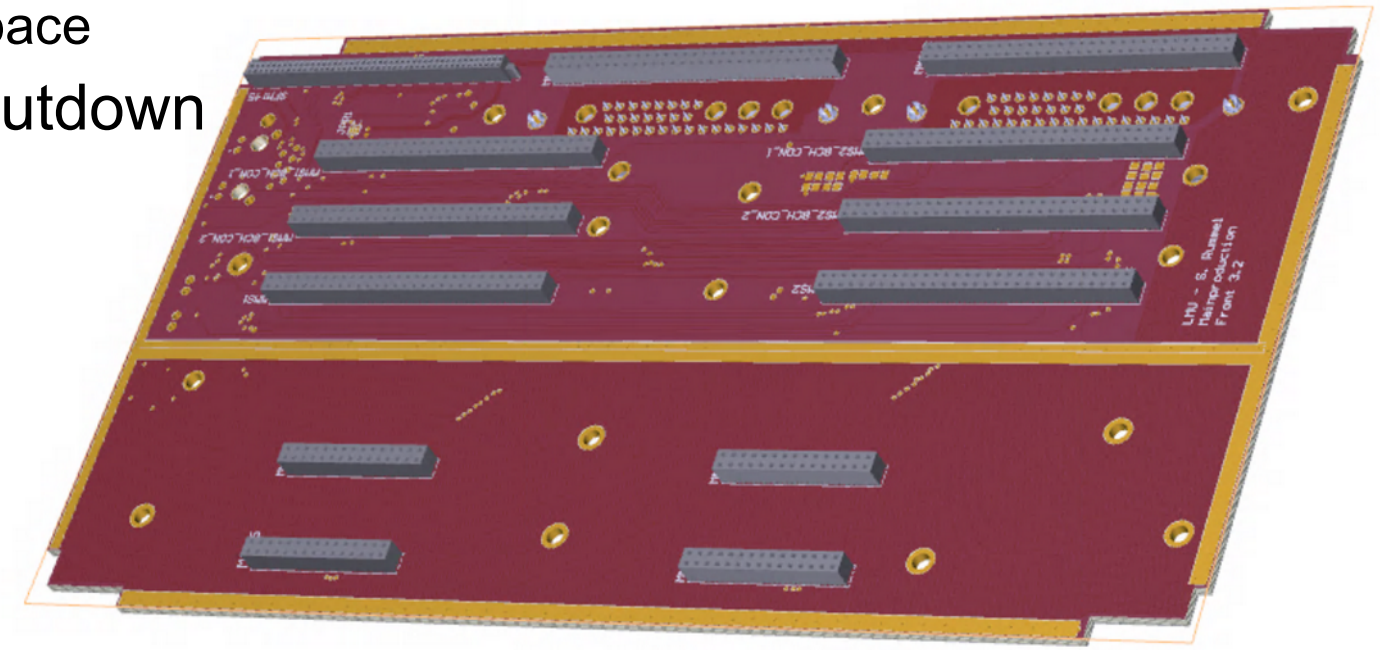


The Plan

- Remove all fixed delays inside the PS unit.
  - Just remove the parts and shorten input and output pads.
  - All on the MCU card.

- On the Front PCB we have
  - All output signals.
  - GND/5V for all floating power domains.
  - The „enable“ signals, but not the interlock signals.
  - quite a bit of space

⇒ Place the fast shutdown circuitry here.



Are There Other Options?

- The PS is a convenient place for the circuitry.
- But it's not the only one: There's also the Dockboxes
  - We can access all the voltages.
  - We can bring in a control signal.
  - The resistance to the modules is lower.
  - Problem: There's no fixed supply for each floating power domain.

- Shorting the outputs is an obvious improvement.
- Are there more ideas?

Next Steps

Next Steps for DCU Interlock

- Design the interlock receiver for the PS backplane.
- Verify the availabilty of the interlock signal on site (during B2GM).
  - Plan the cable routing for the last stretch to the PS rack.
- Understand the current interlock distribution cabling @ KEK.
- Verify availability of parts required for new batch of the PS Backplanes.

Next Steps for Fast Shutdown

- Finish the layout of the test PCB.
- Modify one PS unit to remove all hardwired delays.
  - At this time check if it's suitable to access the interlock signal.

    Side remark: We always talk about „Fast **Emergency** Shutdown“.
    We do get that when we use the enable signals.
    With the interlock signal, its a „Fast **Interlock** Shutdown“.
    ⇒ We need to decide what we actually want.
- Re-do the shutdown measurements with the modified PS and the test board.
  - Possible problems might come from initially very high currents when shorting a charged capacitor.
  - Measure discharge time.
  - Observe dhp-io.
  - ⇒ Hopefully confirmation that the idea is good.

  ⇒ Go / No Go decision.
- Verify availability of parts required for new batch of the Front PCB.

Thank you!

RC (C only on Kapton)

net	R	C	R×C
clear-off	6 Ω	2.2 µF	13.2 µs
clear-on	4 Ω	2.2 µF	8.8 µs
dcd-amplow	2 Ω	22 µF	44 µs
dcd-avdd	1 Ω	66 µF	66 µs
dcd-dvdd	2 Ω	22 µF	44 µs
dcd-refin	11 Ω	22 µF	242 µs
dhp-core	3 Ω	22 µF	66 µs
dhp-io	5 Ω	22 µF	110 µs
gate-off	5 Ω	2.2 µF	11 µs
gate-on[123]	17 Ω	2.2 µF	37.4 µs
source	20 Ω	2.2 µF	44 µs
sw-dvdd	61 Ω	2.2 µF	134.2 µs
sw-sub	4 Ω	2.2 µF	8.8 µs