MicroTCA activities in KEK and J-PARC

Oct. 06, 2019

J-PARC/KEK, Accelerator division

MR Control group

Norihiko Kamikubota

Menu today

- 1. MTCA in KEK
- 2. MTCA in J-PARC
- 3. my experience
- Add) MTCA in SPring-8
- The last page as Summary

About myself (Norihiko Kamikubota)

- Norihiko has been in change of **controls for J-PARC Main Ring (MR)**
- Many of this ppt pages are from **RF members** in KEK and J-PARC
  - Thanks to Sugiyama-san, F.Tamura-san, T.Kobayashi-san, and more
  - Their developments were shown also in past LLRF workshops and IPAC

1. MTCA in KEK

$e^{\pm}$ accelerators complex

LINAC:
Injector for synchrotrons

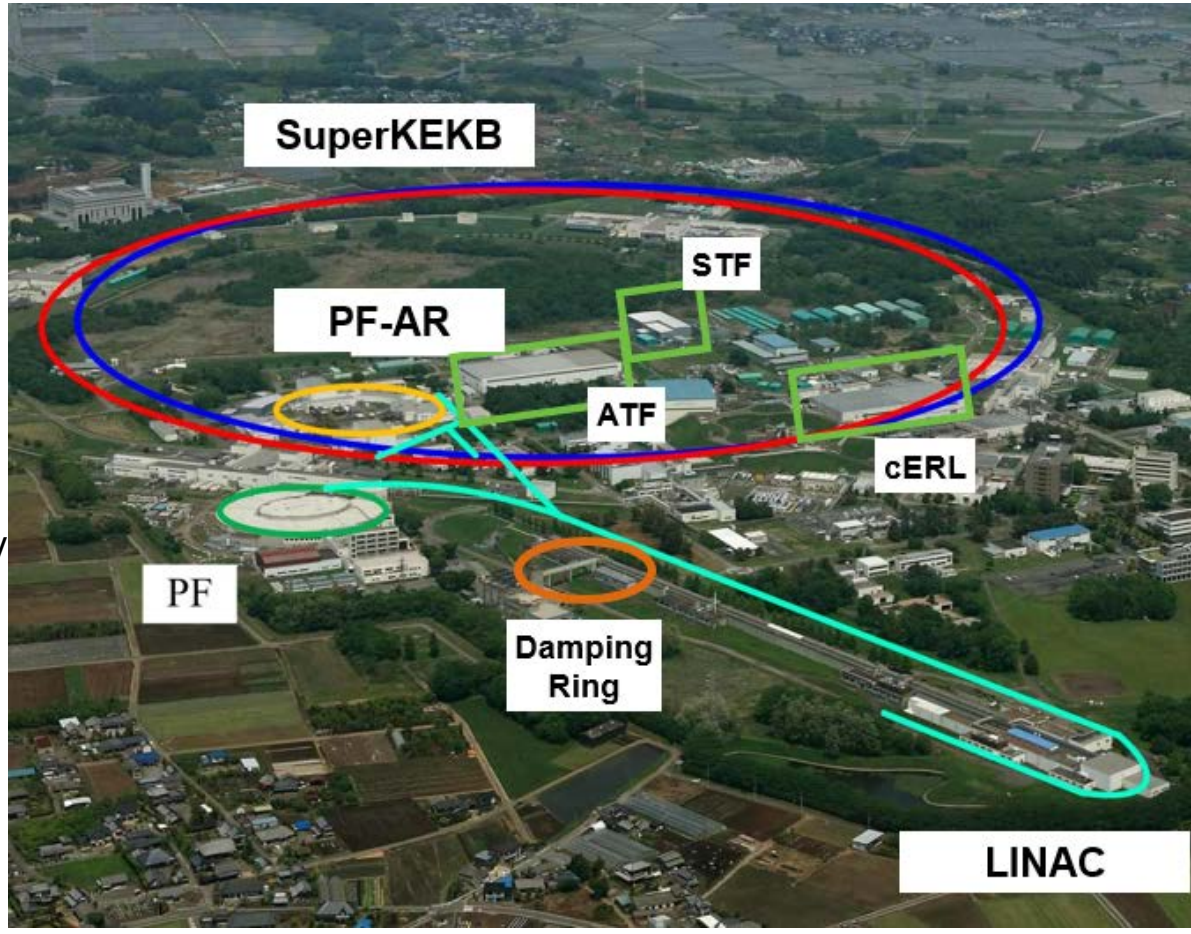
SuperKEKB: $e^{\pm}$ collider for HEP experiment (Belle2)

Photon Factory(PF)
/PF-AR: SR photon source

STF: Superconducting RF Test Facility for ILC

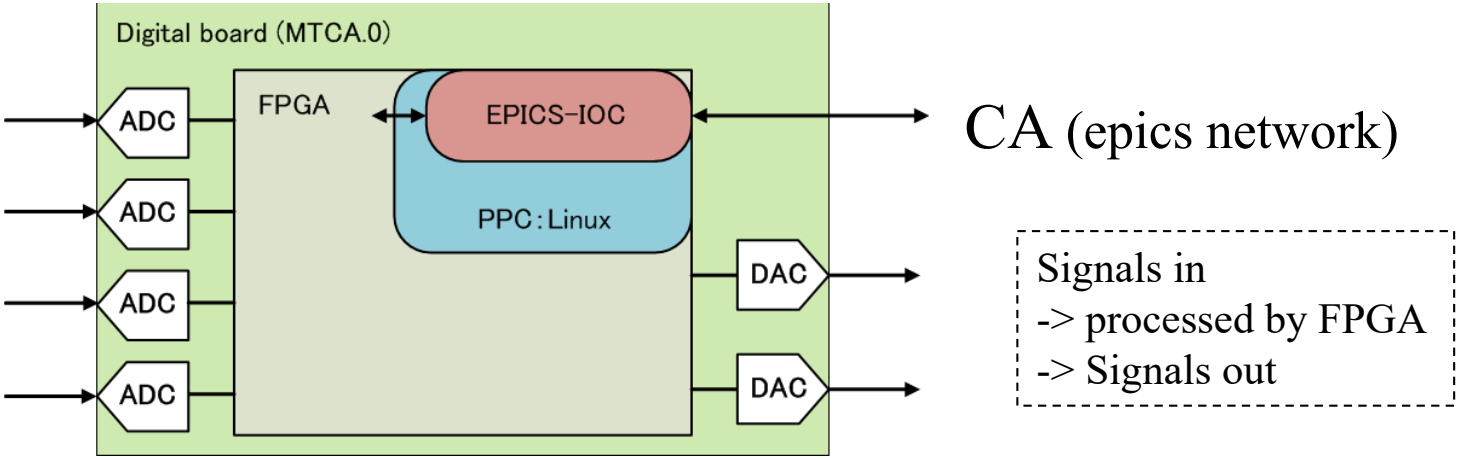
ATF: Accelerator Test Facility for ILC

cERL: Test Facility for a future 3-GeV Energy Recovery LINAC (ERL)

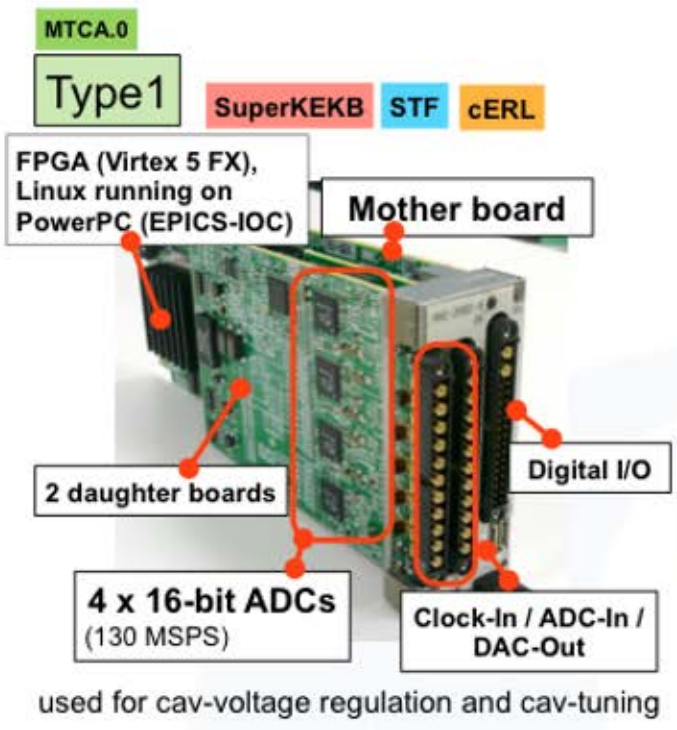


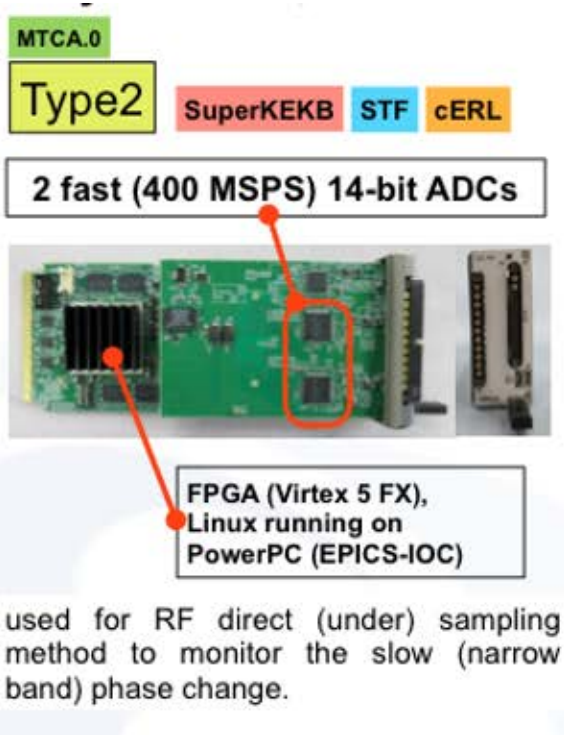
1. MTCA in KEK (continued)

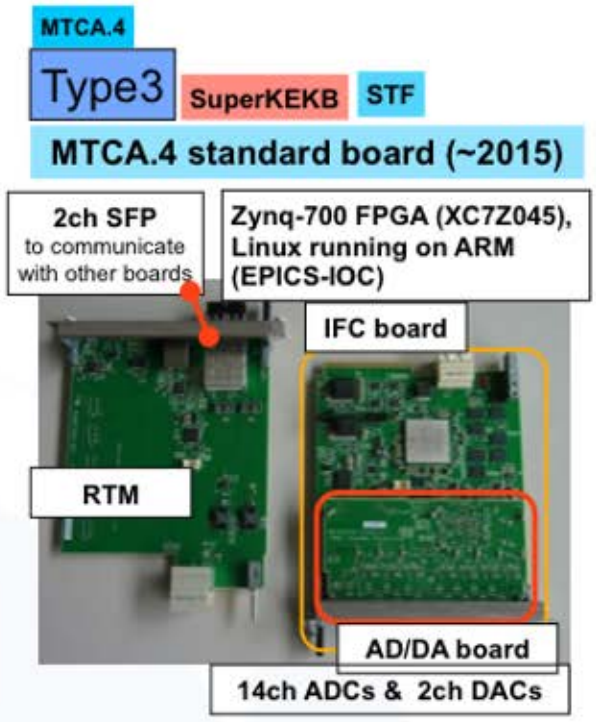
- In 2008, a development of digital board based on **MTCA.0** was started, for **common use at RF** control among SuperKEKB, cERL, and STF in KEK. => **Type 1, Type 2**
- In 2013, the development of the module based on **MTCA.4** for the LLRF system of STF. => **Type 3** (with SFPs for external comminication)
- Modules made by **Mitsubishi Electric TOKKI systems Co.,Ltd**
  - EPICS-IOC is running on the LINUX installed on the CPU in the FPGA



1. MTCA in KEK (continued)







- Our development using **μTCA(.0)** was started **2009 as common-use hardware** for these facilities. Mainly these are applied to Low Level RF control for cavity-voltage regulation and cavity tuning.
- 2 types of μTCA(MTCA.0) boards (Type1&2) : They were successfully worked in beam operation.
- New development using MTCA.4 (Type3) standard was started last year for STF-2. They have not yet used for beam operation. Beam test operation is scheduled next year.

(Text is at Dec,2016)

1. MTCA in KEK (continued)

- Example: SuperKEKB Type 1

superKEKB LLRF
- Cavity field feedback
- Cavity tuning
replaced 9 of 30 old systems (~2015)

by T.Kobayashi

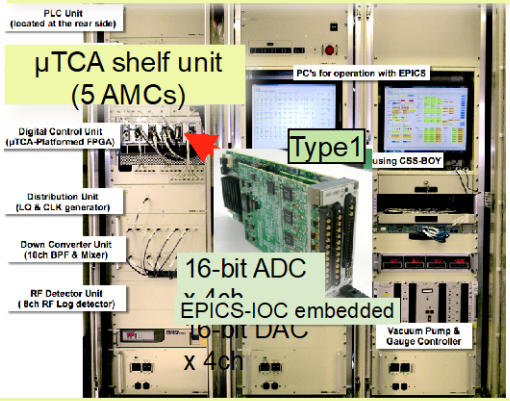
New LLRF control system

with high accuracy and flexibility for superKEKB

Existing analog LLRF system for KEKB

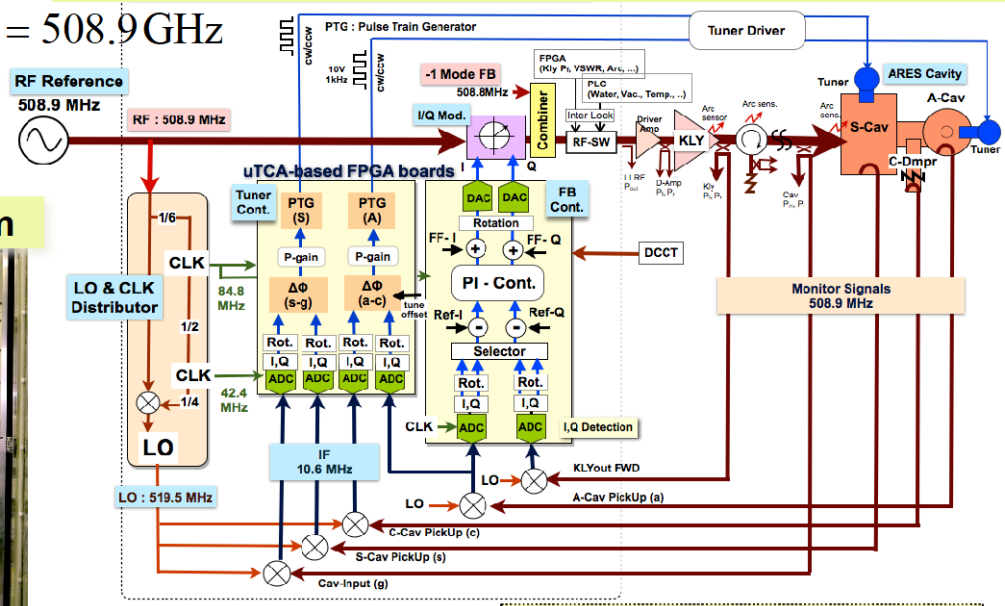
replace

New LLRF Control System

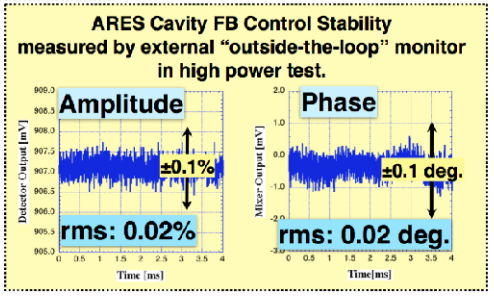


Mitsubishi Electric TOKKI System Co., Ltd.

Block Diagram of Vc-FB & Tuner Control



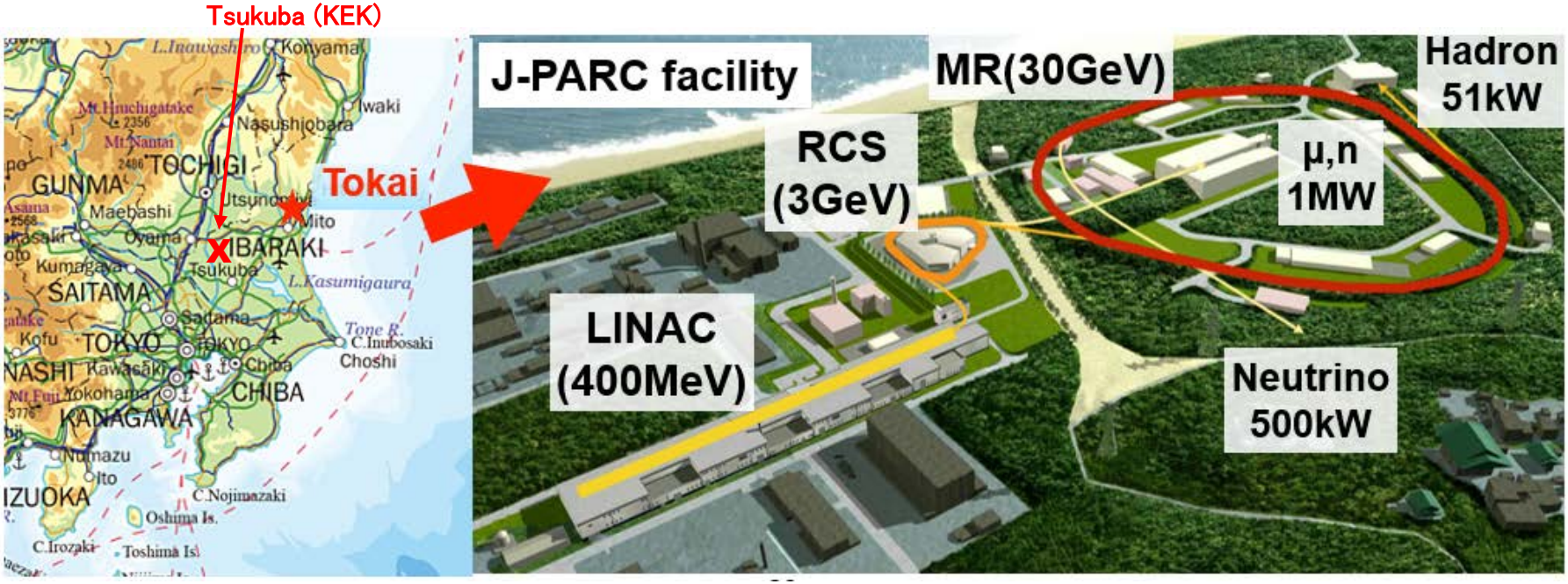
I/Q-sampling for 10.6-MHz IF



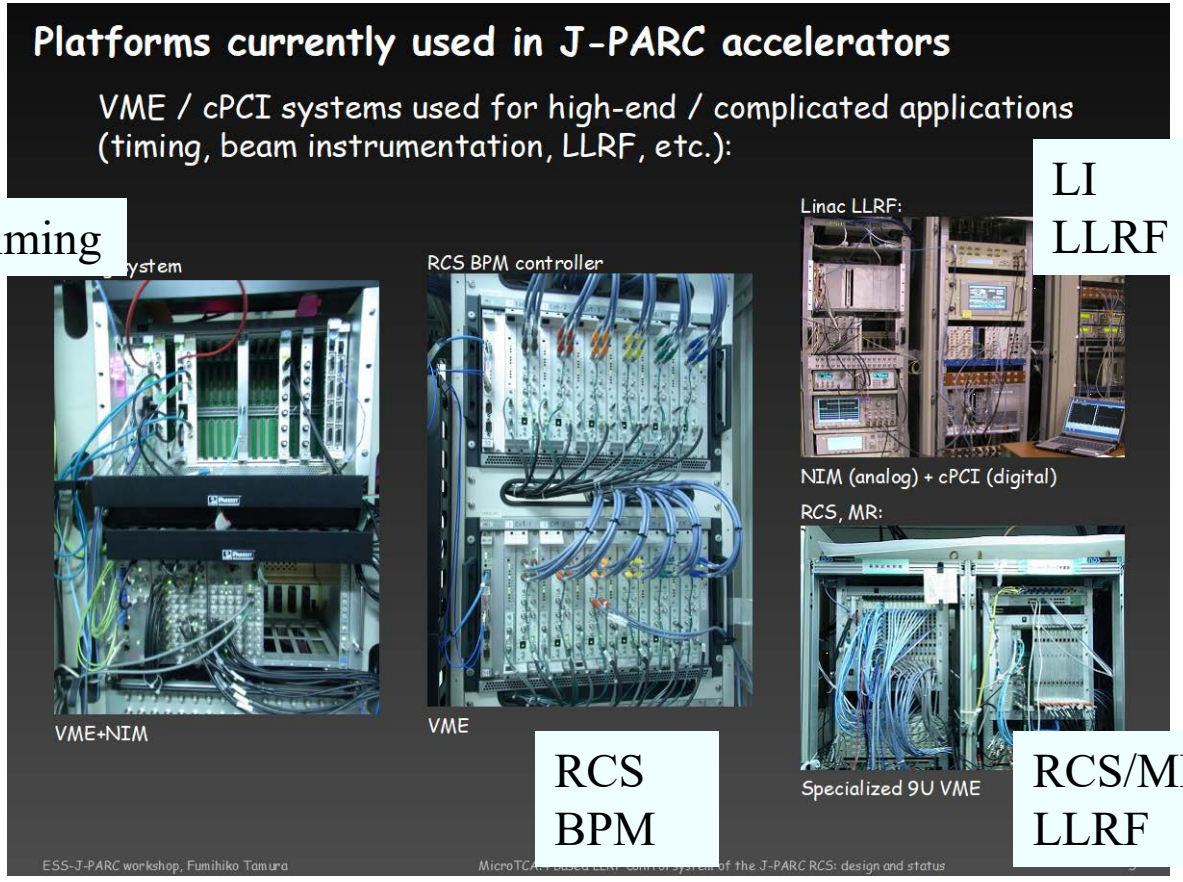
- Consisting of μTCA-platformed **FPGA boards** & **PLC.**
- Type1 board is used for Cav. field **FB control**, **Cavity Tuning** and RF-I/L.
- **EPICS-IOC** with Linux-OS embedded in each board.
- The regulation stability is **0.02%** in amplitude and **0.02 deg.** in phase.

2. MTCA in J-PARC

- J-PARC is an accelerator complex, located in Tokai-mura, Japan
  - Linac(LI), Rapid-Cycle Synchrotron (RCS), and Slow-cycle Main Ring (MR)
  - Jointly operated by JAEA and KEK
    - JAEA: 400MeV **LI,** 3GeV **RCS** ; 25Hz
    - KEK: 30GeV **MR** ; 2.48s(NU) or 5.20s(HD)
    - **2006/2007/2008** - 1st beam to **LI/RCS/MR**



2. MTCA in J-PARC (continued)



Among candidate of replacement, the RCS LLRF is on going with MTCA. (next page)

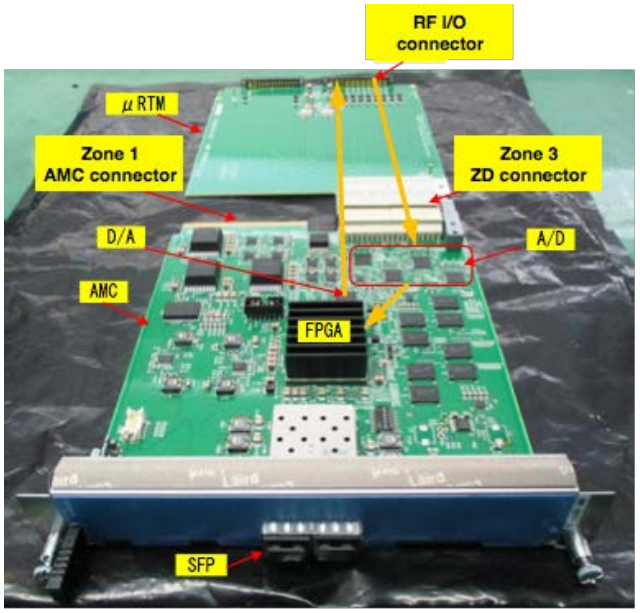
Timing and RF

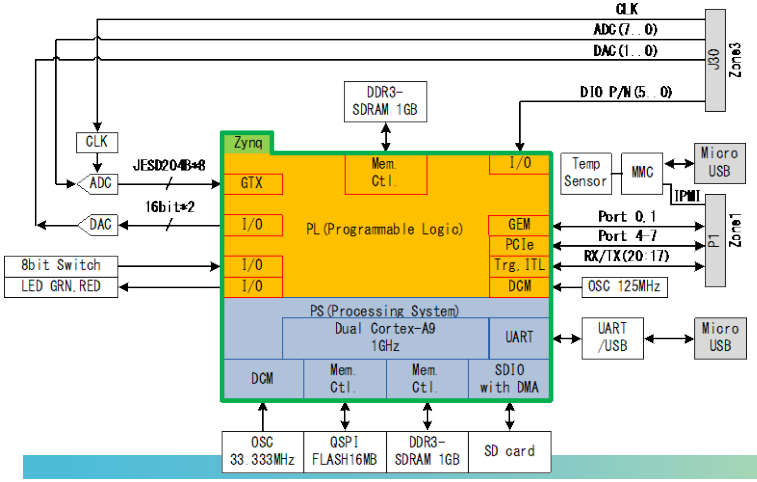
VME, NIM, cPCI modules were used more than 10years old
=Difficulty in the maintenance due to discontinued modules and outdated FPGA.

Need more functionalities for higher intensities and stability.

2. MTCA in J-PARC (continued)

- RCS LLRF
  - beam-loading compensation to achieve high-intensity operation
  - VME-based feedforward modules -> MTCA-based
- AD/DA AMC module for RCS
  - 8 ADC and 2 DAC
  - Analog signals - through Zone3 connector
  - PCI-ex and GbE - through Zone1 AMC connector
  - EPICS-IOC on embedded Linux on Zync FPGA
  - Developed by Mitsubishi TOKKI company



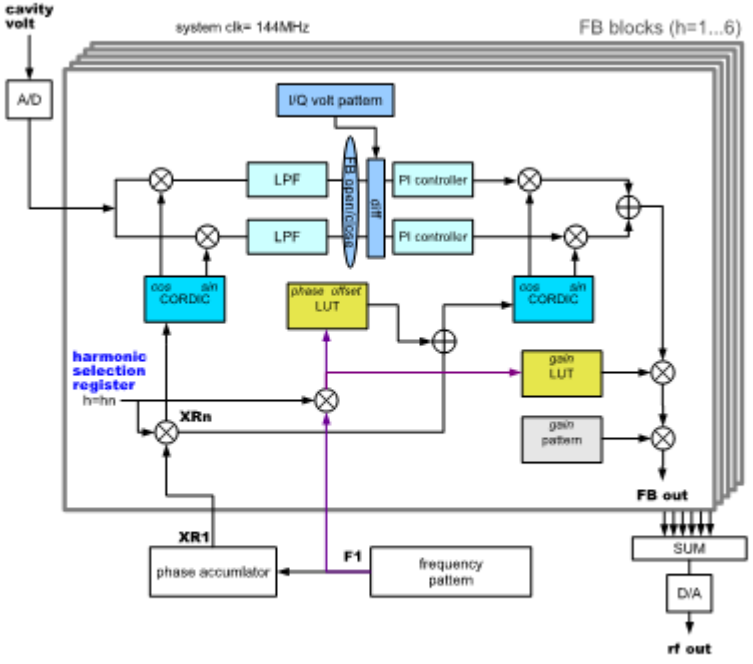


FPGA	Zynq XC7Z045-1FFG900C
OS	Xilinx Linux (EPICS-IOC)
RAM	DDR3-SDRAM 1GiB×2 (PL, PS)
FPGA Configuration	QSPI FLASH-ROM 16MiB, SD Card, Remote Update
ADC	8ch, 16bit, 370MSPS max., BW 800MHz
DAC	2ch, 16bit, 500MSPS max.
Zone1 (AMC Connector)	Port[0:1]:1000BASE-BX, Port[4:7]: PCI Express Gen2 Port[17:20]:M-LVDS, IPMB: IPMI v1.5 support
Zone3 (ZD connector)	Class A1.1(RFin×8ch,DCout×2ch,CLKin×1,DIO×6pair,TCLKout)
SFP	2ports
Switch	8bit DIP-switch
Front Panel LED	Hot swap status (blue), Error status (red), Running status (green)
Size	PCIMG MTCA.4 Double-Width Full Size 148.5*28.95*181.5 [mm]

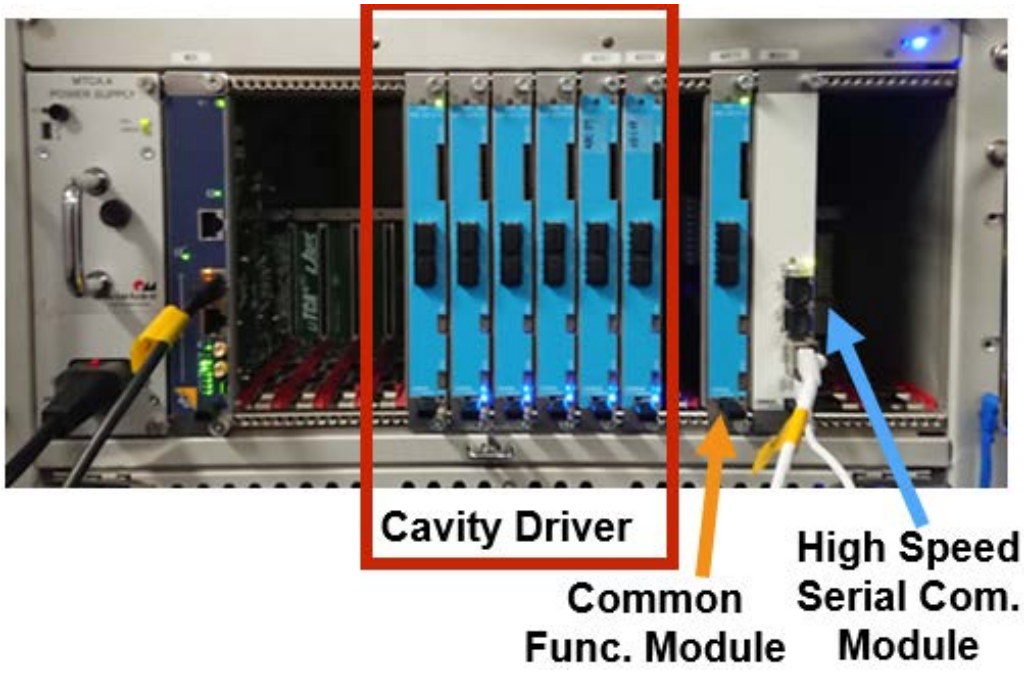
2. MTCA in J-PARC (continued)

RCF LLRF

- Single MTCA.4 shelf can supports modules for the all the 12 cavities for RCS.
- Shelf and Modules are fabricated in FY2018 and under debug for the installation during this summer (2019).



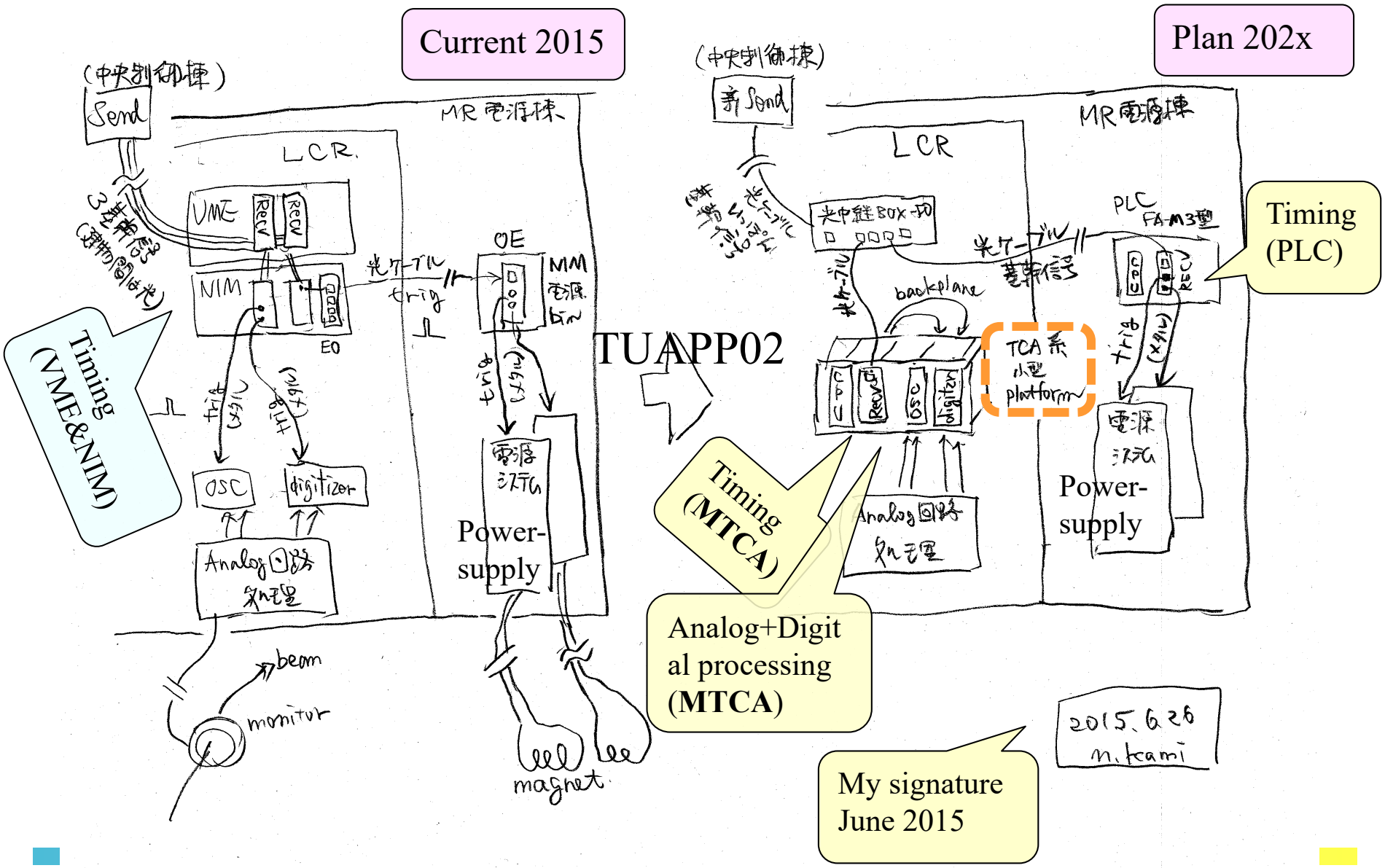
Cavity Driver IQ Vector FB block



3. My experience

- J-PARC timing system
  - was developed during 2002-2005, and has been used since 2006.
  - **VME-modules** (to control) and NIM modules (to generate signals)
  - Discussion for the next decade in 2015-2016
- As a next infrastructure after VME
  - **MTCA is an attractive** candidate
  - **I suggested to introduce MTCA** for timing and beam-diag. modules for J-PARC (next page, 2015)
- But failed .. Why ?
  - Discussion with a company showed **very high cost** for us
  - beam-diag. group showed **less interests to change VME**
  - New timing system (hardware) -> **use VME modules again**
    - Some "New" timing modules (i.e. a new timing master/VME), started operation Oct.01.2019
    - more "new timing of J-PARC" will be reported in next icalepcs ..

3. My experience (continued)



追加) MTCA in Spring-8

Information from: Oshima-san and Fukui-san

- Spring-8
  - Located in Hyogo, western part of Japan
  - Injector, Spring-8 ring (SR 8GeV), SACRA (XFEL 4-8GeV)

- Plan to inject electrons from SACLA to SR (instead of an old-injector)
  - Use low-emittance beam of SACLA for SR

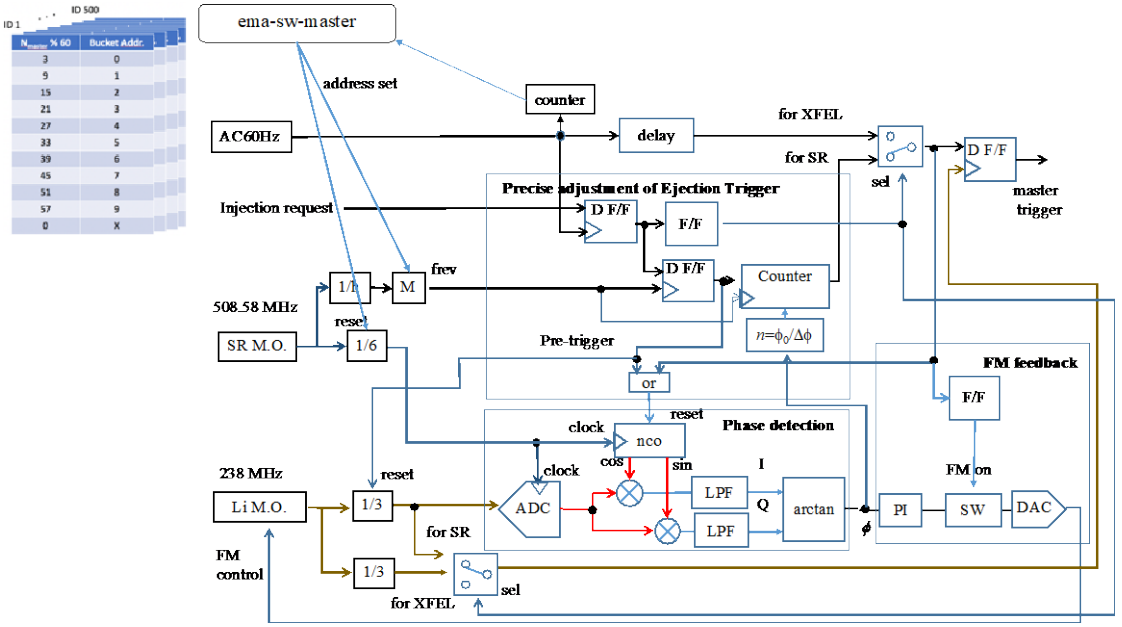
追加) MTCA in Spring-8 (continued)

- A MTCA.4 system to control bucket-injection timing
  - Timing control (delay calculation) for bucket injections from SACLA to SR
  - Tested in 2018-2019, will be used in operation after 2020

16bit 125Msps digitizer AMC (struck)

Firmware (FPGA) by Mitsubishi TOKKI

RTM (candox)

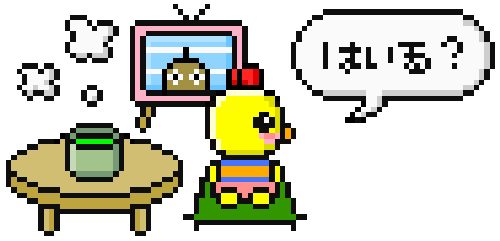


Ref) IPAC19 THPRB034, or
TUAPP02 of Icalepcs2019

The last page.. (Summary)

Thank you
For your attention

- MTCA in KEK
  - Three types of MTCA units (MTCA.0, MTCA.4) were developed
  - Many RF teams have used them, even for small groups
- MTCA in J-PARC
  - Development for new LLRF system for RCS(Ring) is on going
- my comment
  - We still keep using old infrastructure (VME for both KEK, J-PARC)
  - When we replace an old system (llrf, timing,..), sometimes MTCA was selected (sometimes not)
  - One company (Mitsubishi TOKKI) can make MTCA modules in Japan, and this would cause higher cost in Japan
- MTCA in SPring-8
  - A MTCA.4 system was reported in IPAC19 THPRB034
  - Spring-8 control group has interested in “mass introduction” of MTCA, as a replace of VME infrastructure -> Icalepcs2019 TUAPP02 by Fukui-san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MTCA-AMC types used in each Facility

Facilities	MTCA standard	AD / DA / FPGA / Software		Application
SuperKEKB	µTCA (MTCA.0)	ADC : 4 x 16-bit (LTC2208, 130 MSPS) DAC : 4 x 16-bit (AD9783, 500 MSPS) Virtex-5 FX, Wind River Linux on PowerPC	Type1	LLRF control & BPM for IP-FB
		ADC : 2 x **14-bit** (ADS5474, **400 MSPS**) Virtex-5 FX	Type2	Optical delay cont. for RF-Reference
	MTCA.4 (~2015)	ADC : 2 x 16-bit (AD9650, 105 MSPS) DAC : 12 x 16-bit (AD9783, 500 MSPS) Zynq-700 FPGA, Xilinx Linux on ARM	Type3	Orbit FB@IP
STF STF-2	µTCA (MTCA.0)	ADC : 4 x 16-bit (LTC2208, 130 MSPS) DAC : 4 x 16-bit (AD9783, 500 MSPS) Virtex-5 FX, Wind River Linux on PowerPC	Type1	LLRF control (Cav-Vc & Tuner)
	MTCA.4 (~2015)	ADC : 14 x 16-bit (AD9650, 105 MSPS) DAC : 2 x 16-bit (AD9783, 500 MSPS) Zynq-700 FPGA, Xilinx Linux on ARM	Type3	LLRF control (Cav-Vc & Tuner)
cERL	µTCA (MTCA.0)	ADC : 4 x 16-bit (LTC2208, 130 MSPS) DAC : 4 x 16-bit (AD9783, 500 MSPS) Virtex-5 FX, Wind River Linux on PowerPC	Type1	LLRF control (Cav-Vc & Tuner)

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J-parc accelerators

- JAEA: 400MeV **LI,** 3GeV **RCS** ; 25Hz
- KEK: 30GeV **MR** ; 2.48s(NU) or 5.20s(HD)
- 2006/2007/**2008** - 1st beam to LI/RCS/**MR**
- J-PARC (and S.KEKB also) is a …
  - *challenging machine toward extreme performance*
    - Long-term plan to design goals（need >10 years）
    - design powers: MLF 1MW, MR 750kW (→ now >1MW powers are discussed)
    - Many parameters: ~100k points to monitor and control
    - Updates, improvements: very frequent (Accelerator complex itself is an experiment)
      (opposite example is a medical accel.)

Control system must support such activities

- safety – **extendability** - reliability