MTCA.4 at the European Spallation Source

Timo Korhonen
Chief Engineer, Integrated Control Division
European Spallation Source ERIC
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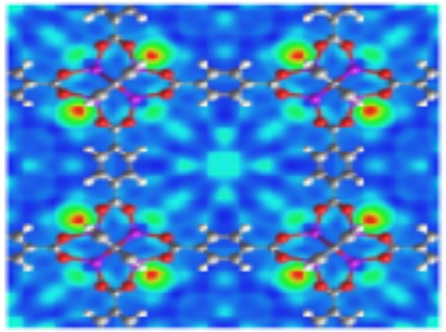
Outline

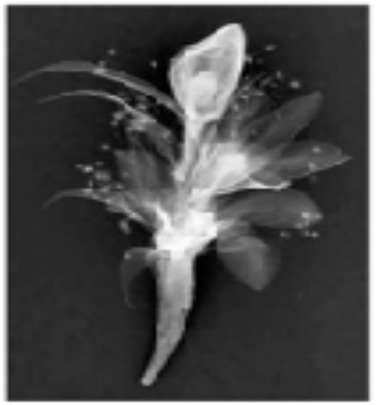
- Brief recap of the European Spallation Source
- Application areas for MTCA.4 in ESS
- Portfolio of MTCA.4 equipment
- Software and firmware infrastructure
- MTCA.4 from user's perspective
- Summary

The European Spallation Source

- ESS is a neutron spallation source for neutron scattering measurements.
- Neutron scattering can reveal the molecular and magnetic structure and behavior of materials:
  - Structural biology and biotechnology, magnetism and superconductivity, chemical and engineering materials, nanotechnology, complex fluids, etc.
- Neutrons are complementary to X-Rays (synchrotrons, X-FEL)
- High beam power will open up new possibilities for neutron scattering experiments
  - Traditiona



Neutron scattering of hydrogen in a metal organic framework



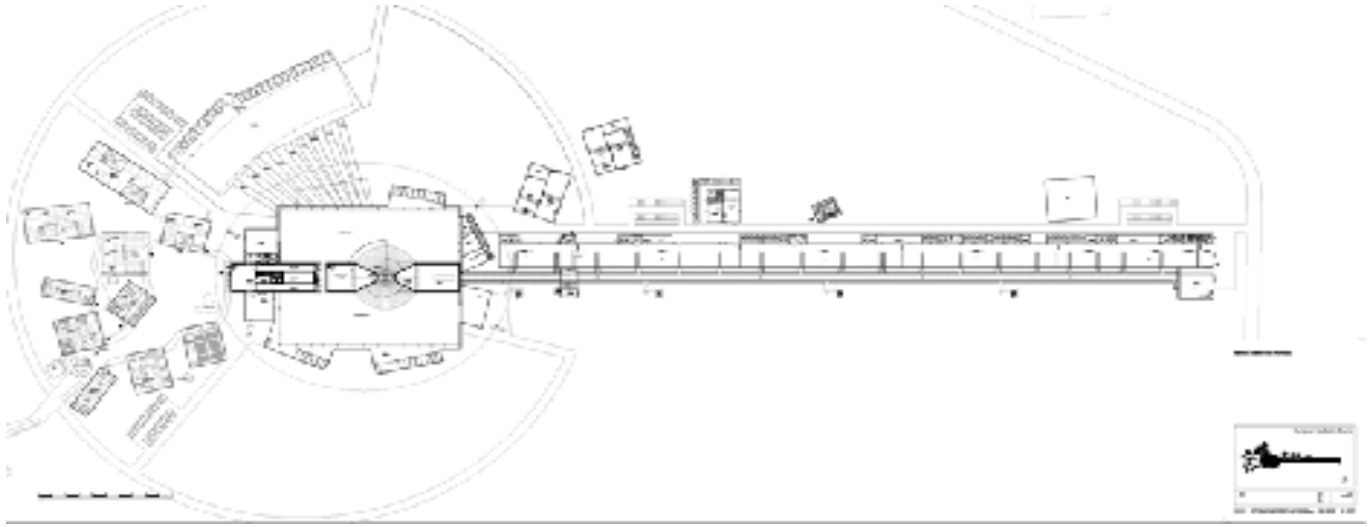
Neutron radiograph of a flower corsage

X-Ray Image

Neutron radiograph

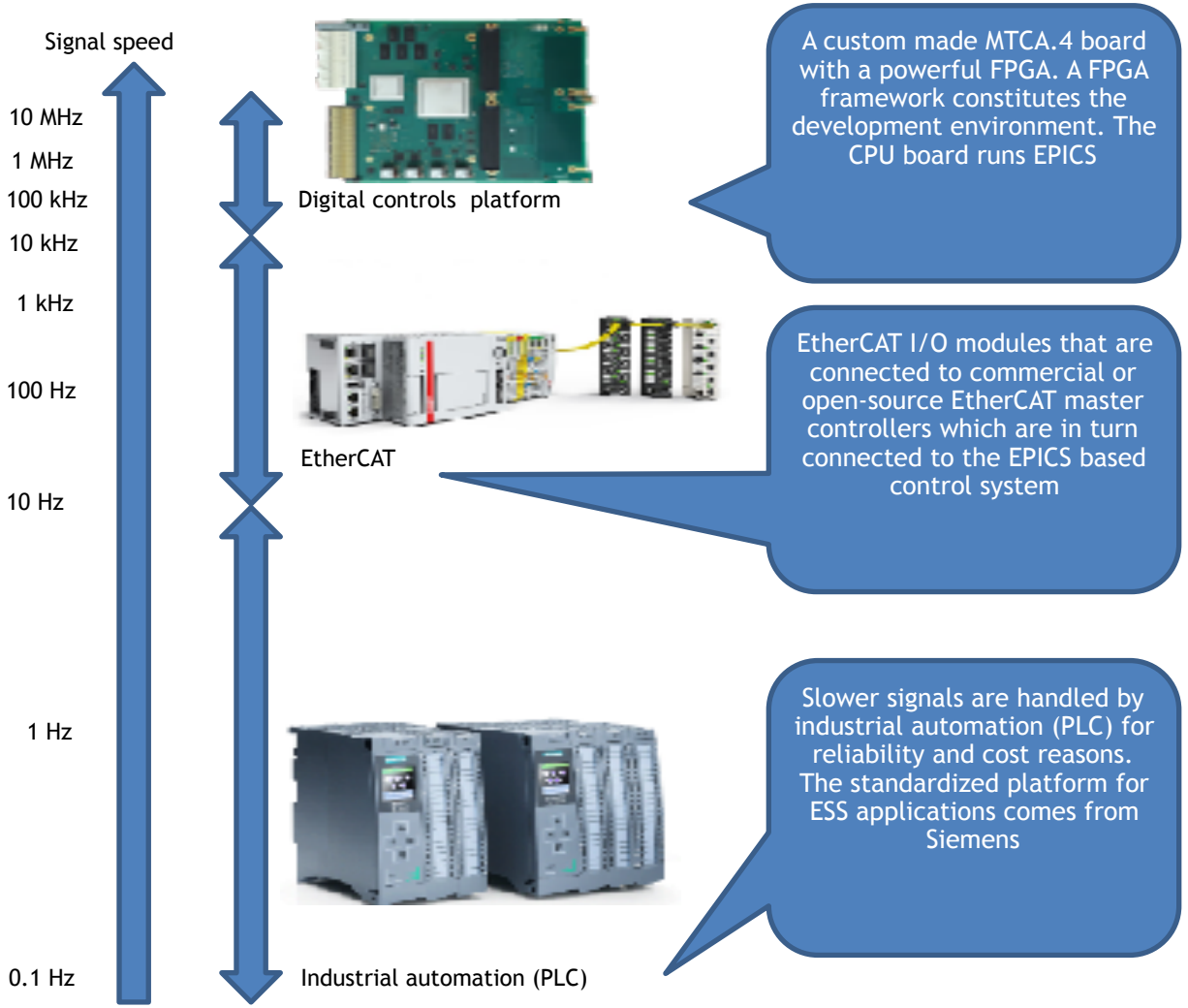
The European Spallation Source

- The European Spallation Source (ESS) consists of :
  - a pulsed accelerator that shoots protons into…
  - a rotating metal (tungsten) target to produce neutrons
  - (up to) 22 neutron instruments for various experiments



- ESS control system
  - Is EPICS-based
  - Covers the whole facility
    - Accelerator
    - Target
    - Neutron instrument controls (excl. experimental data processing)
  - Is built by the ICS Division, for all of the above
  - Uses a variety of hardware technologies, for different purposes
    - A few backbone standards
    - Next slide

Three layer strategy for control systems at ESS



- **ICS has adopted a three layer strategy for implementing the control system based on signal processing needs**
  - MTCA.4 for applications with data acquisition exceeding few kHz
  - These applications require a FPGA and custom, high-speed signal processing in system.
  - For slower signals, EtherCAT will be used as a real-time fieldbus with good price/performance ratio
  - Synchronization and event information are key for applications where a full custom platform solution would be too costly
  - Low speed signals are handled with commercially available PLC systems
  - This is a cost-effective solution that addresses ESS reliability and maintainability requirements
  - The PLCs are connected to EPICS for further integration into the control system

MTCA.4 Application areas

- RF Systems: LLRF, fast RF protection (RF-LPS)
- Machine Protection System: fast beam interlock system (FBIS)
- Timing System (MRF)
- Beam Instrumentation

- All of these use heavily FPGAs
  - Pay attention to flexible and standardized interfaces
- Much ICS effort goes into
  - Supporting FPGA development
  - Low-level drivers and operating system support
  - Long-term maintainability

Applications #1: RF Systems

- 150+ RF systems using MTCA
  - LLRF
    - One of the earliest MTCA-developments at ESS
    - Collaboration between ESS and many European labs and countries
  - RF-Local Protection (RF-LPS)
    - Also a collaboration, but MTCA part developed for/by ESS
    - Fast protection and monitoring implemented on a MTCA FMC carrier
  - LLRF and RF-LPS integrated into same MTCA crates
    - Equipped with timing and other infrastructure

MTCA Applications #2: Machine Protection System

- Beam Interlock System, fast part, aka FBIS, implemented using MTCA
  - High damage potential, stringent requirements on Machine Protection
  - Lots of diverse systems to be connected
    - Some slow ones (limit switches, temperatures, power converters)
    - Some fast and complicated
      - Beam Loss Monitors
      - Beam Current Monitors
      - (at least a part of) Beam Position Monitors
  - Fast reaction time required
    - ~10 us in low energy part, somewhat more (~20 us) in high energy part of linac
      - Low energy beam causes damage faster – Bragg peak energy deposition
- In-kind collaboration with ZHAW, Switzerland

The Fast Beam Interlock System

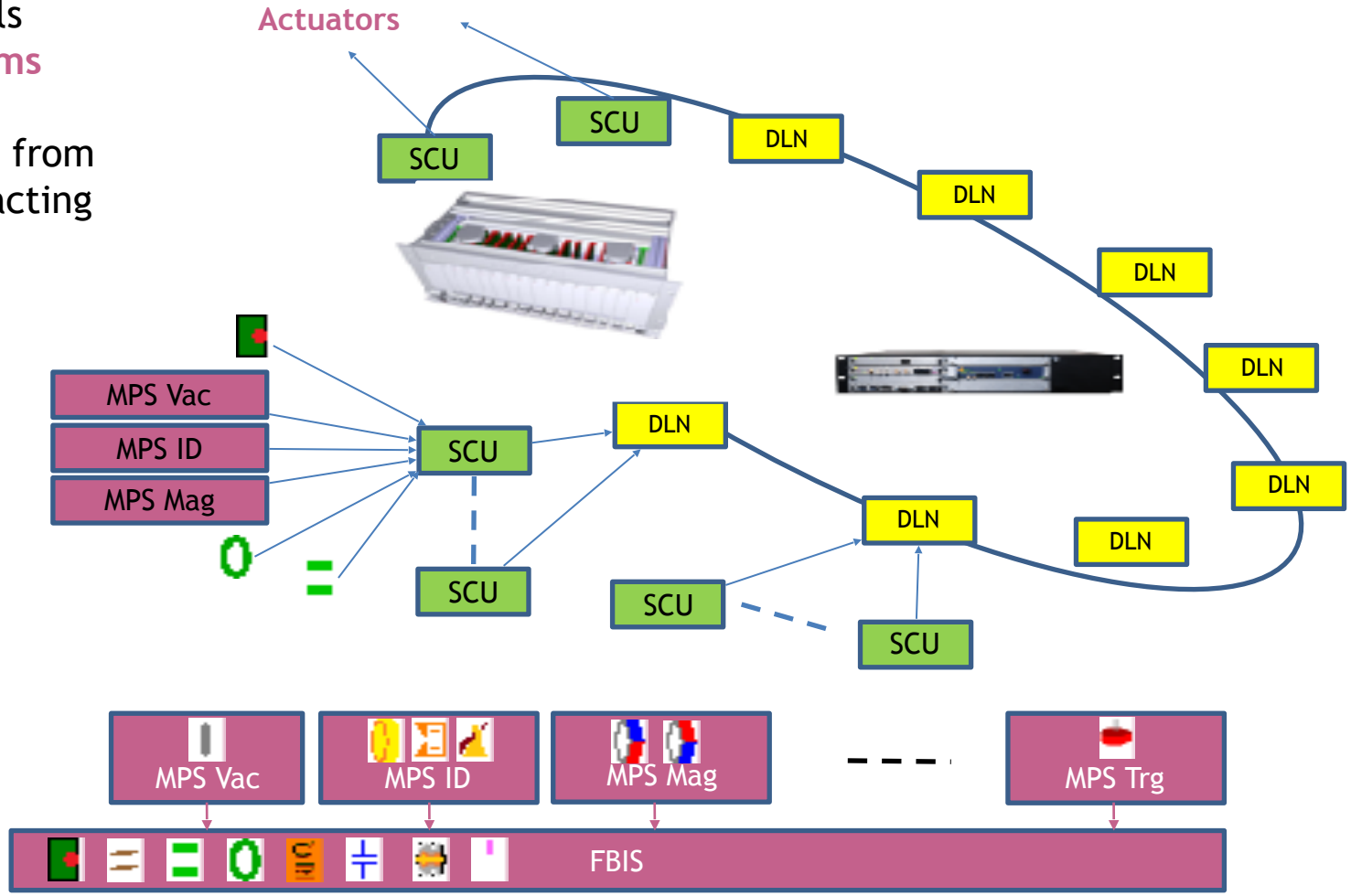
- SCU (Signal Converter Unit) concentrating signals from Sensor Systems and MPS PLC based systems

- DLN (Decision Logic Node) concentrating signals from several SCUs, deriving global beam permit and acting on Actuators to stop Beam

FPGA based systems, Fast ! Reaction time ~ 5us

DLNs connect to Optical Protection Line

- Light is intercepted by a DLN when an interlock situation is detected
- No hierarchical tree or other structure, no “master” node



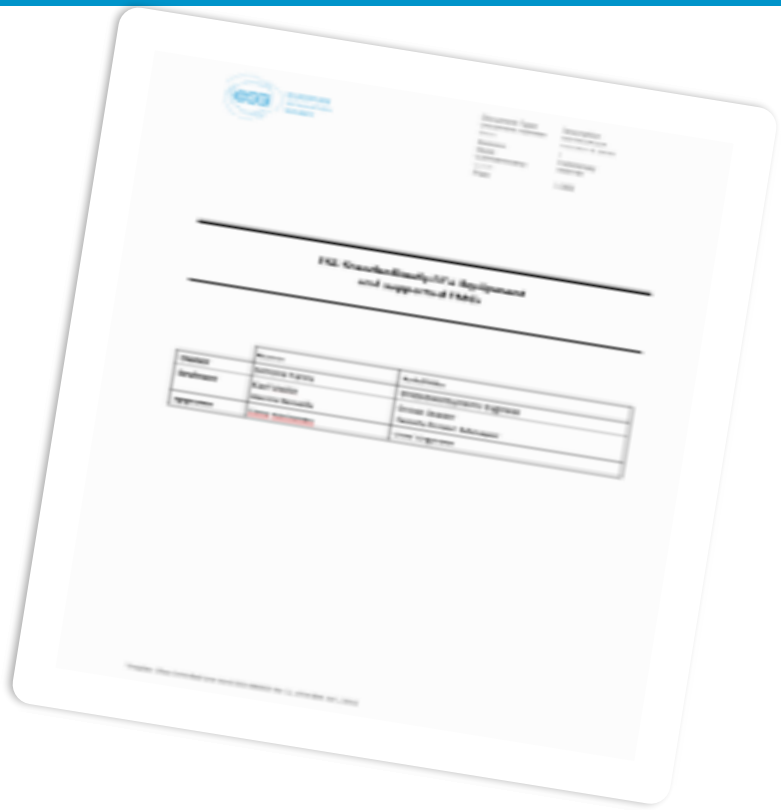
Applications #3: Beam Diagnostics Systems on MTCA

- Beam Current Monitors
- Beam Loss Monitors
  - Crucial for Machine Protection
- Beam Position Monitors
- Some Target Monitoring systems
  - Camera-based, processing (partially) in FPGA
- Faraday Cup signal acquisition
- Emittance Meter Units
- Wirescanners
- All of these need data acquisition and processing in (several) MHz speed range
  - No time to go into details in this talk.

Standardization Process for MTCA

Comprehensive list of equipment including:

- Infrastructure components:
  - Chassis
  - Power modules
  - MicroTCA Carrier Hubs
  - Chassis replacement parts
- Specialized AMC cards:
  - High performance CPU
  - Data Acquisition
  - Timing synchronization
- Versatile AMC cards:
  - FMC carrier
  - RTM support card
- RTM cards
- FMC modules



MicroTCA infrastructure components

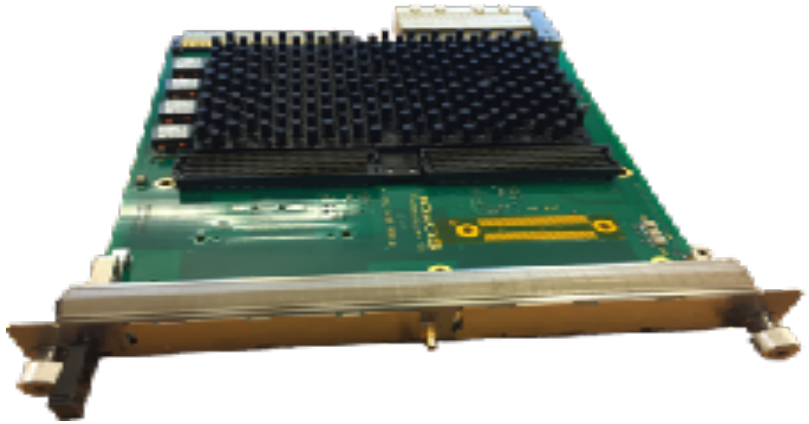
- 12 slots 9U for systems requiring more than 6 AMCs and/or more than 4 RTMs or redundant low noise power modules;

- 6 slots 3U to reduce system space in racks.

Power Modules: Wiener (1KW), N.A.T. (600W)

Concurrent Technologies AM900 (now obsoleted, use AMG6x in future

MicroTCA AMC FMC carrier



IFC1410, by IOxOS SA

in-kind contribution from PSI, Switzerland

Processing System:

- NXP T2081 PPC running at 1.8GHz
- 2GB DDR3L (upgrade path to 4GB with ECC)
- 64 MB SPI Flash memory
- 512MB NAND Flash
- PCIe x4 gen.3 connection to Programmable Logic (no direct connection to backplane)

Programmable Logic:

- Xilinx Kintex Ultrascale KU040 (vertical migration KU060)
- 2x 512MB DDR3L
- 3 PCIe End Points (x4 gen.3 to backplane)
- 2 HPC FMC support
- Support for non-standard form factor mezzanine card (ie FBIS connection) on AMC side 1 or 2
- Zone3 connector (RTM support) compliant to class D1.4

MicroTCA AMC ADC

Similar in function to IFC_1420
- Used in e.g., LLRF and BPM

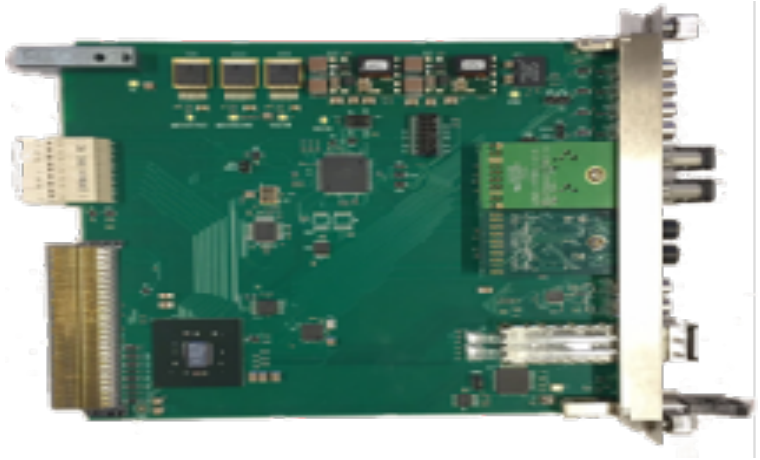
SIS8300-KU:

COTS AMC card

Programmable Logic:

- Xilinx Kintex Ultrascale KU040
- 2 GB DDR4
- x4 gen.3 PCIe End Point to backplane
- 10 ch ADC 125MSPS 16-bit
- 2 ch DAC 16-bit
- Internal, Front Panel, RTM and Backplane Clock Sources
- Support for up to 2 SFP+ modules for high speed system interconnect
- 2 front panel RJ45 for external I/Os (eg BIS connection)
- Zone3 connector compliant to class A1.1CO

MicroTCA AMC Timing, Event Receiver and Generator/Master



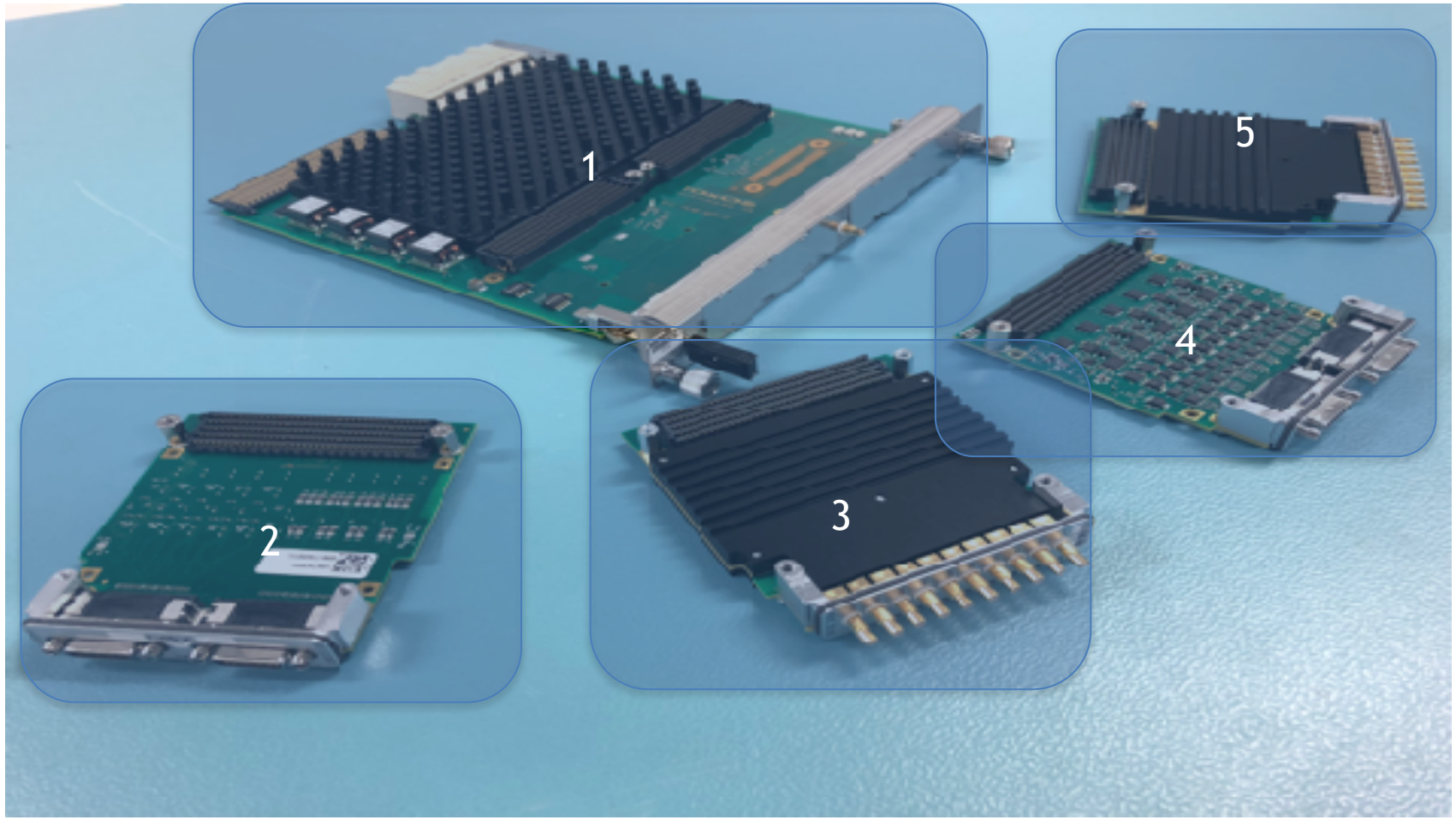
Timing system EVR:

- clocks from/to TCLKA/TCLKB
- driving/receiving differential triggers AMC RX/TX ports 17 to 20 (MLVDS)
- front panel 4 x TTL outputs, 2 x TTL inputs
- front panel 2 Universal I/O modules
- Delay compensation with feedback

Timing system EVM (Event Master: Generator and Fanout)

- Compatible with other 300-series form factors (VME, cPCI)
- Dual functionality: Event Generator or Fanout module
  - 1-to-7 fanout
- Integrates also two Event Receivers
- EPICS integration tests ongoing

FMC I/O cards



I/O interface cards:

1. IFC_1410 AMC
   - Carrier board
2. DIO_3118
   - Digital in/out
3. ADC_3110
   - 250 MSPS ADC, 8 Ch
4. ADC_3117
   - 5 MSPS ADC, 20 Ch
5. ADC_3111
   - Like #3 but DC-coupled

Cards not in photo but available:

- ECATS
  - EtherCAT slave interface
- FMC-Cameralink
  - Integration of cameras
- PICO-FMC
  - Low current measurements

MicroTCA AMC DAQ IFC1420

piggyback slot for ESS Beam Interlock System interface

IFC1411 + DAQ1430:

Intended for use with RTMs that conform to the Class A1.1 recommendation: Downconverters, signal conditioning

Processing system and programmable logic:

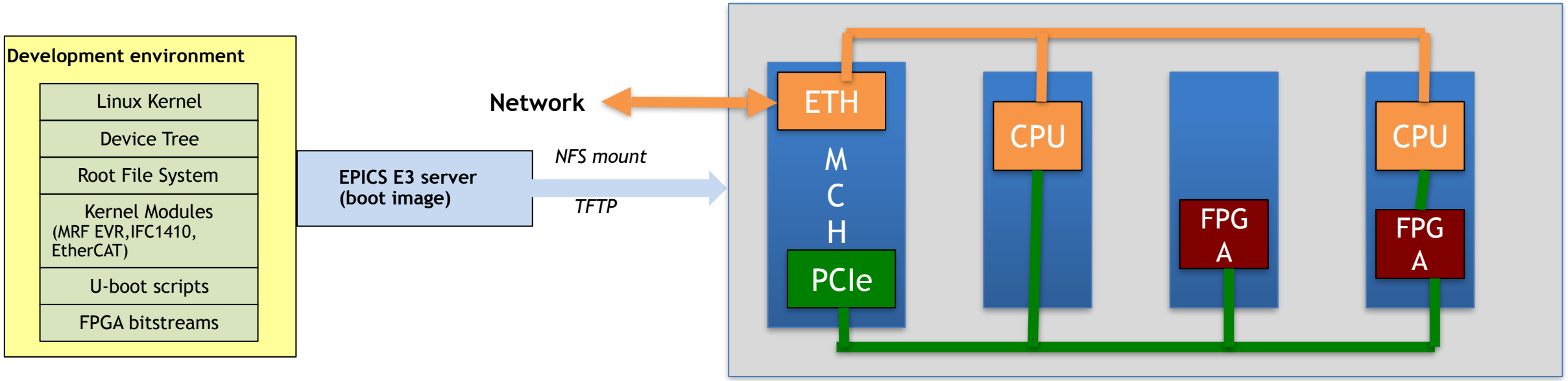
Same characteristics as IFC1410

Acquisition Mezzanine:

- 10 ch ADC 250MSPS 16-bit (DAQ1430)
- 4 ch DAC 2.5GSPS 16-bit (DAQ1430)

- Internal, Front Panel and Backplane Clock Sources
- 1 HPC FMC support
- Support for non-standard form factor mezzanine card (ie FBIS connection) on AMC side 1 or 2
- Zone3 connector (RTM support) compliant to class A1.1CO

MicroTCA software&firmware architecture



- Multiprocessing architecture: central + local CPUs
  - Eventually, not all established yet…
- Operating System(s): Linux (Yocto, or CentOS) with Realtime (RT) Patch
  - EPICS on either a central CPU, on the IFC local CPU, or both (scalability, application-specific processing)
- All software/firmware modules are in an on-line BitBucket/GitLab repository
  - All updates of e.g., kernel modules or new FPGA firmware versions

MTCA.4 from user's perspective

- These are my views, however based on discussions with my colleagues
- Pros
  - Management
    - Status monitoring
    - Remote power cycling, board-wise
  - Performance
    - Both data transfer and signal processing quality – what we have seen so far
  - Modularity
    - Add and replace modules for different functions
  - Less cabling due to signals on the backplane
    - Clocks, triggers
  - Future-proof
    - New features can be added in a backwards compatible way to new versions of the standard

MTCA.4 from user's perspective

- These are my views, however based on discussions with my colleagues
- Cons
  - Learning curve (aka "complicated")
    - With powerful features comes a certain complexity. But what is often meant is difficulty to get started.
  - Different backplane configurations cause surprises
    - Standard allows a lot of customization – good for some, bad if you do not pay close attention to details.
  - Configuration can be confusing
    - Example: CPU could not recognize AMCs. Problem was in BIOS configuration and large BAR sizes in AMCs.
    - Another example: several clock drivers for PCIe were conflicting. Select one, disable others.
      - Nobody's "fault" – but took a while to figure out why the system was unstable.
  - Real estate - somewhat
    - AMC size (has not been a big issue), mechanics (connectors, etc.) can be a challenge
  - Limited industry support – still
    - Few manufacturers for central components (power supplies, MCH,…)
    - Most prominent players do not always seem to be eager to collaborate.

MTCA.4 from user's perspective

- What would be nice (from my perspective):Improve support for multiprocessing
  - Now still mostly a "single CPU, many I/O" model
    - Conceptually simple but has its limitations
  - When data volumes rise (as they do), a single CPU, no matter how powerful, becomes a bottleneck.
  - Multiprocessing would improve scalability
  - Technically, the capability is there
    - But in practice, very little support to be found.
- Wish for the community
  - Forum for sharing experiences, mutual support
    - Workshops are great but not very frequent, not everybody can go every time
    - Something more agile would be welcome

Summary

- ESS uses MTCA in several high-speed applications
- Standard selection of components
  - To help and guide the users and to make future support possible
- Mostly commercial and in-kind contributed components
  - Limited internal staff to drive in-house (hardware) developments
  - Much effort put into firmware and low-level software support
- User experience
  - Many good features
  - Some cons, too
  - And a few wishes for the user community