FPGA developments in MicroTCA.

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2019-10-06

at MTCA workshop at ICALEPCS 2019

MicroTCA TECHNOLOGY LAB

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

DESY.

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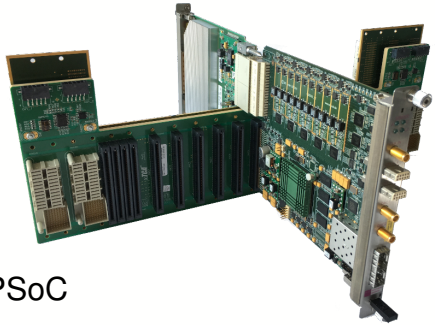
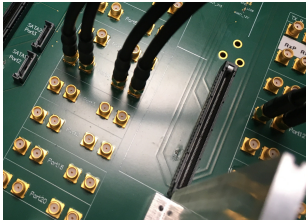
Outline

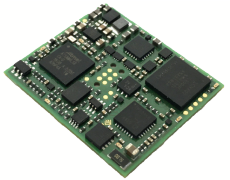
- Backplane from FPGA perspective
- FPGA boards in MicroTCA
- Data transfer in MicroTCA
  - PCI Express
  - Between FPGA and ARM in Zynq MPSoC



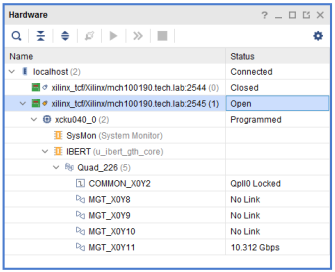


Backlane from FPGA perspective

- Management
  - Mostly invisible to FPGA
  - E-keying for Zone 3 and backplane links
  - Possibility for out-of-band firmware update
- Gigabit Ethernet
  - Useful for CPU boards and Systems on a Chip (e.g. Zynq)
- PCI Express
  - Most widely used protocol in experimental physics
- P2P links
  - Transceivers directly between FPGAs, non-switched fabric
- MLVDS
- Clocks
- JTAG
  - Useful for debugging large or non-accessible systems



DMMC-STAMP
MMC on a module



JTAG over MCH (JSM) from Vivado

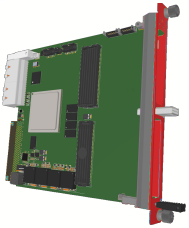
FPGA boards

FPGA boards

A lot of boards available on the market are based around an FPGA. Vendors usually provide Board Support Packages and reference designs for their boards





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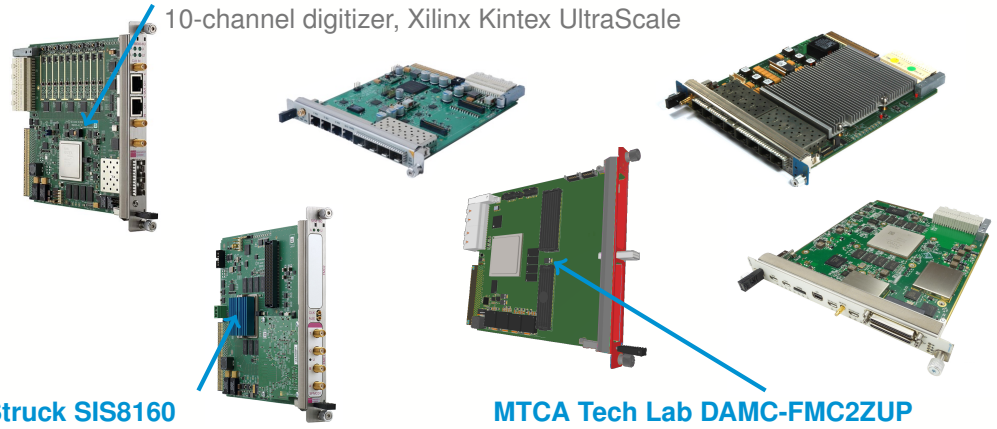


Struck SIS8300-KU
10-channel digitizer, Xilinx Kintex UltraScale

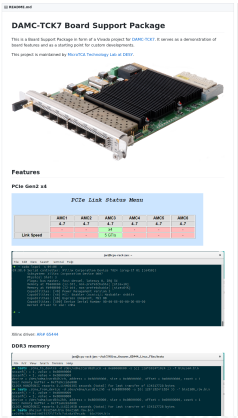
Struck SIS8160
FMC carrier, Xilinx Kintex UltraScale

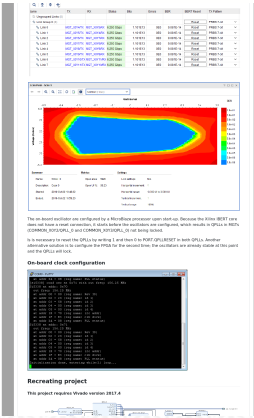
MTCA Tech Lab DAMC-FMC2ZUP
FMC+ carrier, Xilinx Zynq UltraScale+ MPSoC

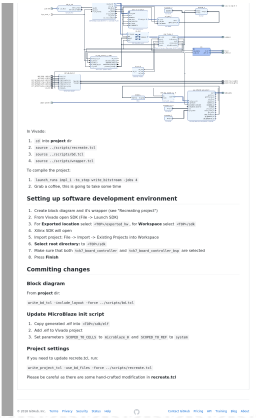
Reference designs for our boards

DAMC-TCK7: Vivado project including support for PCIe, DDR3, clock configuration, IBERT on SFP+ and UDP/IPv4 beacon on AMC port 0; available under permissive license (3-clause BSD)

Available on our GitHub page: `https://github.com/MicroTCA-Tech-Lab`







Data transfer in MicroTCA

Data transfer in MicroTCA

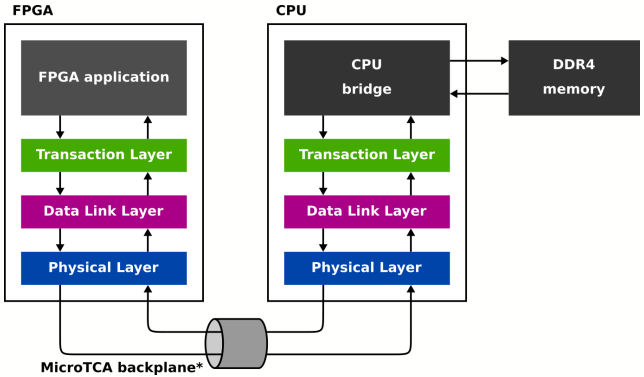
There are several options to move the data between the boards in MicroTCA and out of the MicroTCA crate. Some of the most commonly used options are:

- PCI Express to a CPU
- from FPGA-side to Zynq, Zynq runs data server
- 10/40G Ethernet
- Serial Rapid IO
- ...

PCI Express

PCI Express is high-speed protocol for PC extension cards. Different form-factors are also available. Link out of 1, 2, 4, 8 or 16 lanes, lane rate 2.5 GT/s, 5.0 GT/s, 8.0 GT/s and 16.0 GT/s.

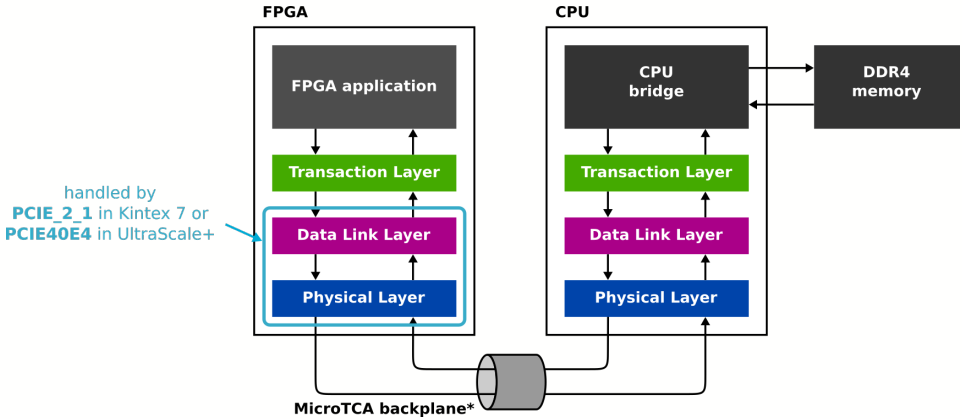
PCI Express link is composed from several layers, each responsible for a dedicated task.



* real PCIe link in MicroTCA system includes a PCIe switch in MicroTCA Carrier Hub (MCH)

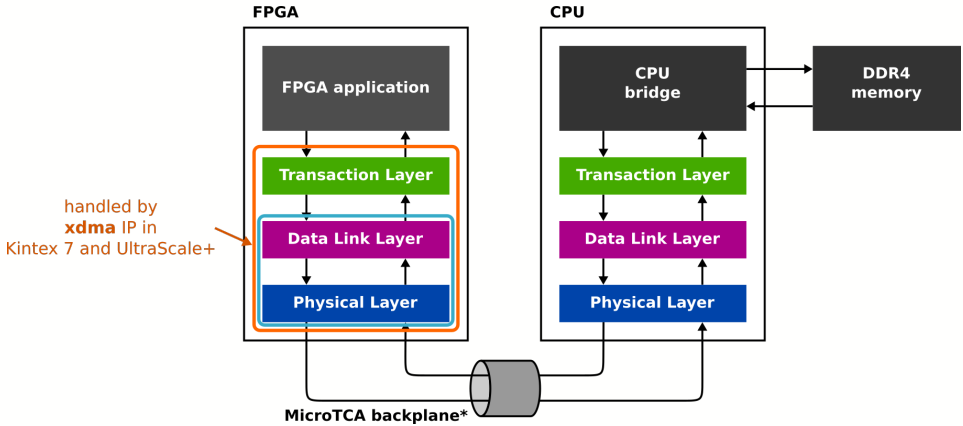
PCI Express

When using modern FPGAs, the lower two layers of the protocol are already implemented in silicon (so called hard IP):

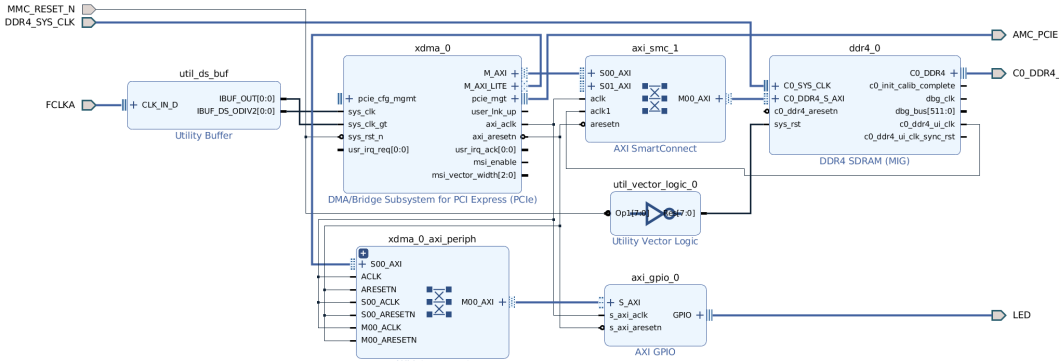


PCI Express

Recently (a couple of years ago) Xilinx has started offering DMA Subsystem for PCI Express which implements the entire stack:

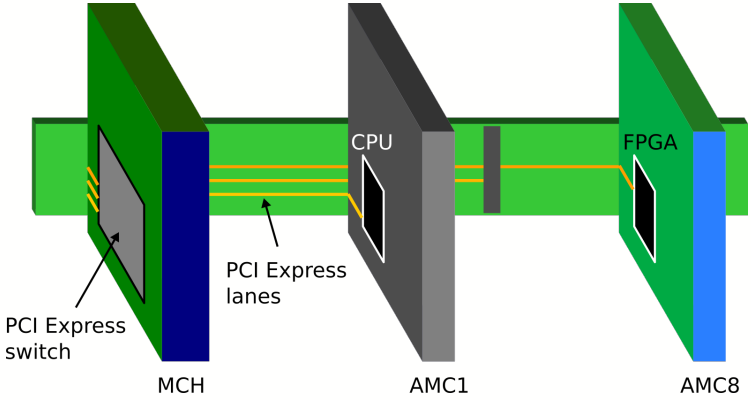


A minimal system (PCI Express + memory controller for DDR3/4) with such an IP looks something like this:



DMA performance evaluation

The performance of the DMA (and the entire system) is evaluated by transferring large quantities of data between CPU board and FPGA board.



DMA performance evaluation

Both CPU and the boards with xdma are running PCI Express links at 8.0 GT/s, x4.

N.A.T. MCH presents the information about the link in several ways, here is a relevant page from the Web Interface:

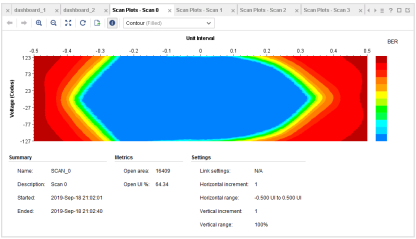
PCIe Link Status Menu

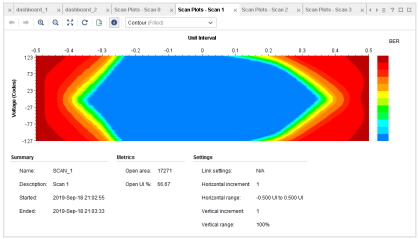
	AMC1	AMC2	AMC3	AMC4	AMC5	AMC6	AMC7	AMC8	AMC9
	4..7	4..7	4..7	4..7	4..7	4..7	4..7	4..7	4..7
	x4	x4	-	-	-	-	-	x4	-
Link Speed	8 GT/s	2.5 GT/s	-	-	-	-	-	8 GT/s	-

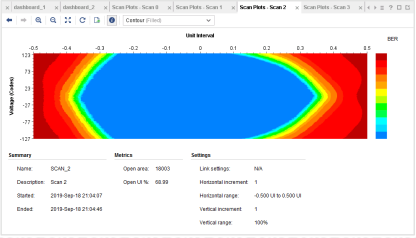
PCI Express link quality

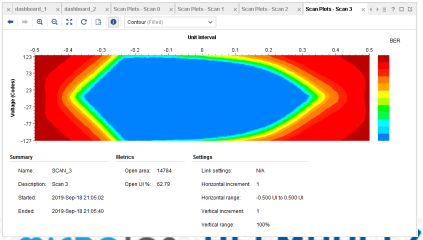
Eye-diagrams show us the quality of the physical link. Using the "In-system IBERT" option in xdma one can observe the quality of the links at the FPGA receivers.

5.0 GT/s with Struck SIS8300KU in nVent Schroff 7-slot (cube) crate:



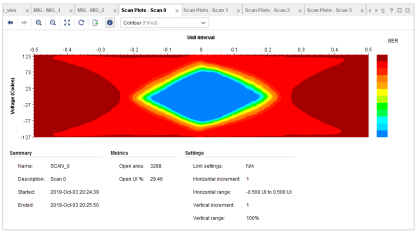


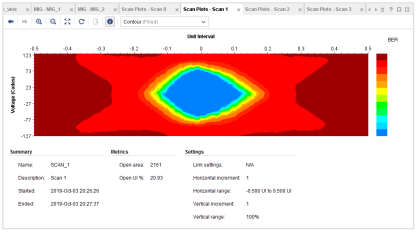


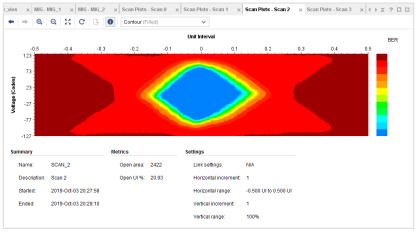


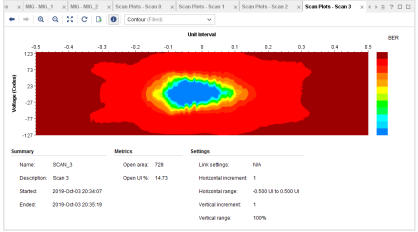
PCI Express link quality

8.0 GT/s with Struck SIS8160 in nVent Schroff 12-slot (9U) crate:





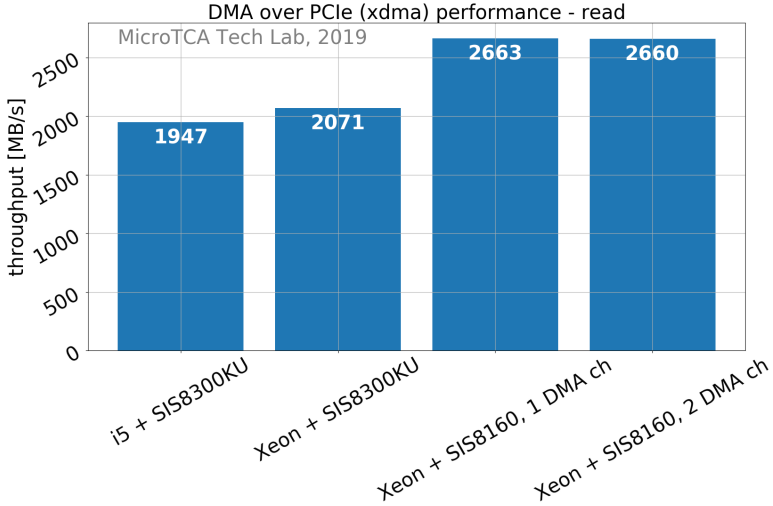




The eyes are still open - link can reliably operate at 8.0 GT/s (i.e. full PCIe gen 3 speed).

PCI Express performance

Transferring 1 GB from on-board DDR4 over PCIe (8.0 GTs/, x4) to CPU memory. For SIS8160 the data is transferred from two memory banks at the same time.
(theoretical maximum = 4 * 1 GB/s * 128/130 * 256/(256+12) = 3762 MB/s)



PCI Express performance

Transferring 1 GB from CPU memory over PCIe (8.0 GTs/, x4) to on-board DDR4. For SIS8160 the data is transferred to two memory banks at the same time.
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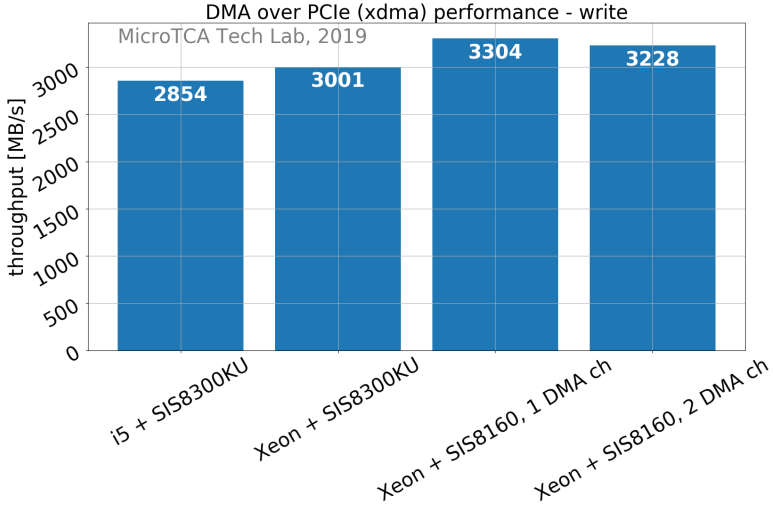
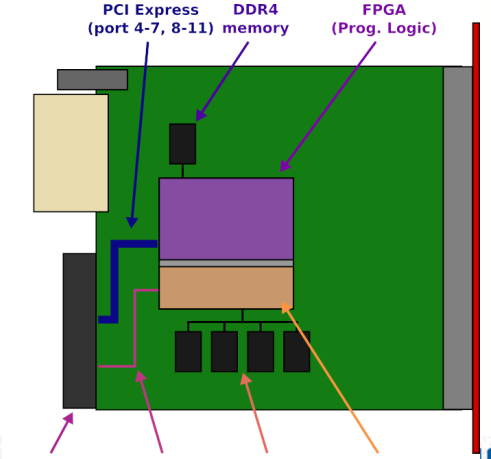


From FPGA-side to Zynq MPSoC

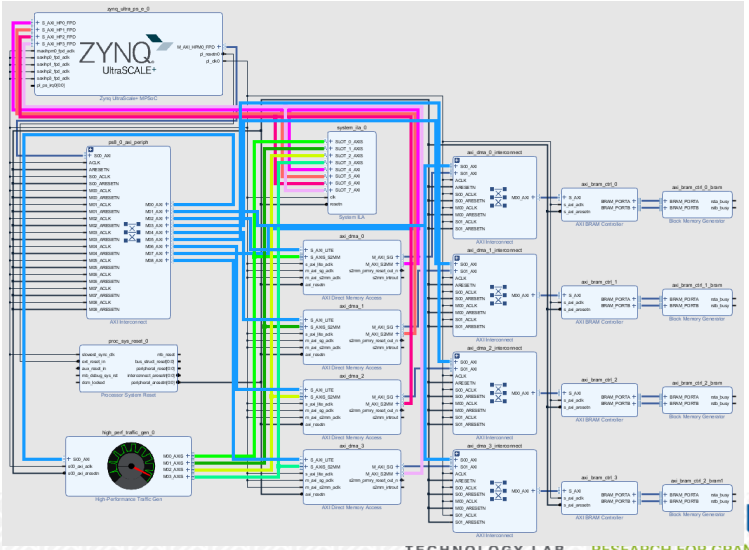
The data is captured by the FPGA part (e.g. from ADCs) and we want to transfer the data to CPU side - either for post-elaboration or to provide the data through a data server (e.g. EPICS IOC).

Schematic diagram of DAMC-FMC2ZUP:



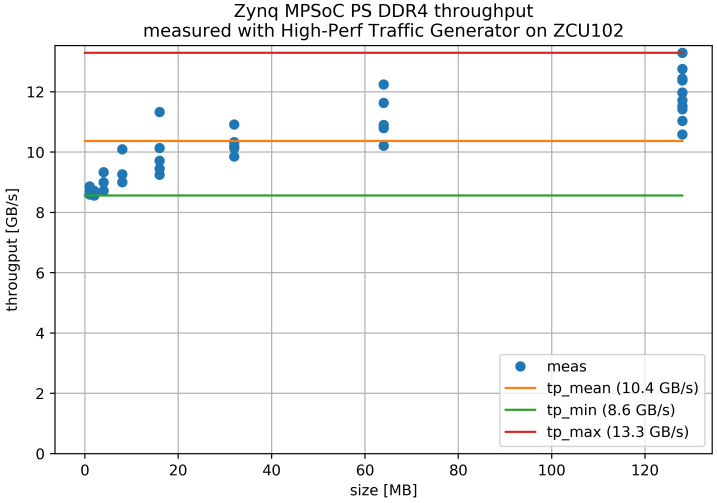
Measurement setup

We have prepared an FPGA project, which instantiates High-Performance Traffic Generator (emulates 8 ch ADC with 12 bits, running at 800 MSPS) and connected it to a bank of DMAs.



Results

With such an architecture we can achieve relatively high throughput - the bottleneck is then transferring the data out of Zynq.

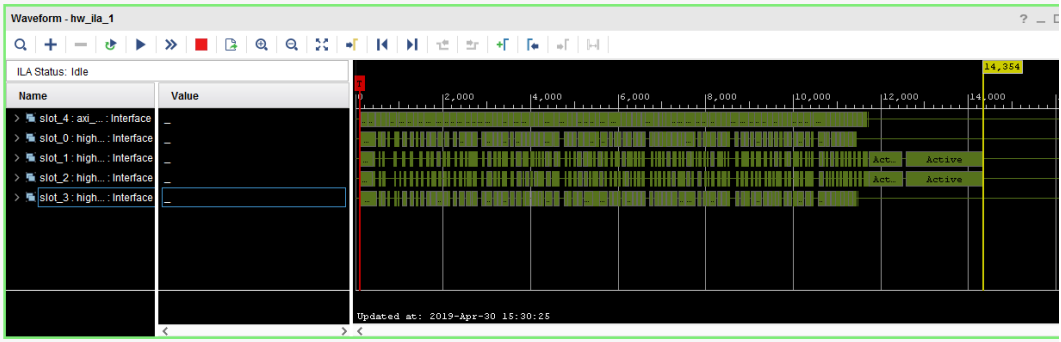


from J. Marjanovic: Zynq MPSoC DDR4 Performance Report, internal

Results

There are 4 PL to PS interfaces in Xilinx Zynq MPSoC, and they are connected to 3 ports on DDR4 memory controller. It can be observed that the two PS to PL interfaces connected together are slower than the other two.

Bus utilization on all 4 PL to PS interfaces:



from J. Marjanovic: Zynq MPSoC DDR4 Performance Report, internal

Conclusion

Conclusion

- FPGAs are widely used in MicroTCA due to their versatility
- Reference designs and BSPs are provided by vendors and research institutes
- PCIe is most-commonly used protocol to communicate between FPGA and CPU in MicroTCA
- Zynq MPSoC provides different possibility for system architecture
- MicroTCA is a modular platform, offering virtually limitless solutions for any data acquisiton (DAQ) and digital-signal processing (DSP) system

Thank you

https://techlab.desy.de

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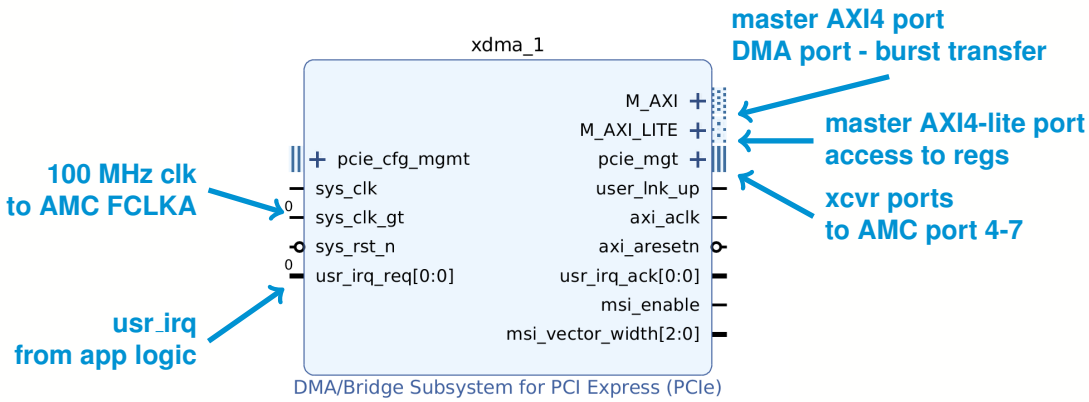
A Research Centre of the Helmholtz Association
Notkestr. 85, 22607 Hamburg, Germany

Backup slides

PCIe sub-system

This is how the Xilinx DMA Subsystem for PCI Express looks in Vivado:



Interface to user space

On the other side (towards the user space), Xilinx DMA driver provides several char devices:

```
$ ll /dev | grep xdma
drwxr-xr-x  3 root root          60 Jun 20 17:19 xdma
crw-rw-rw-  1 root root     238,  36 Jun 20 17:19 xdma0_c2h_0
crw-rw-rw-  1 root root     238,   1 Jun 20 17:19 xdma0_control
crw-rw-rw-  1 root root     238,  10 Jun 20 17:19 xdma0_events_0
crw-rw-rw-  1 root root     238,  11 Jun 20 17:19 xdma0_events_1
[...]
crw-rw-rw-  1 root root     238,  24 Jun 20 17:19 xdma0_events_14
crw-rw-rw-  1 root root     238,  25 Jun 20 17:19 xdma0_events_15
crw-rw-rw-  1 root root     238,  32 Jun 20 17:19 xdma0_h2c_0
crw-rw-rw-  1 root root     238,   0 Jun 20 17:19 xdma0_user
crw-rw-rw-  1 root root     238,   2 Jun 20 17:19 xdma0_xvc
```

c2h
AXI4 port (DMA from device)

h2c
AXI4 port (DMA to device)

user
AXI4-Lite port

events_N
AXI4 port (DMA from device)

Measurement setup

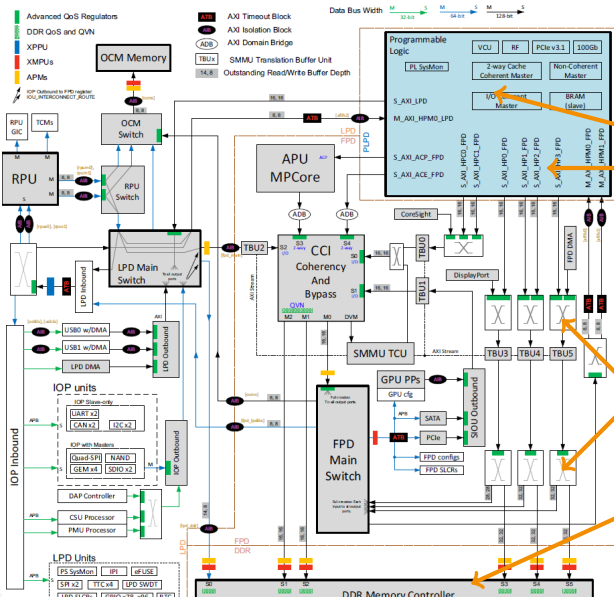


Figure 35-1: **PS-PL Interfaces**