





# PXD21

-- Module/Ladder Overview --





### Sensor production status



#### > Two batches in production

- $\rightarrow$  12 wafers PXD9-20  $\rightarrow$  to be finished early 2020, first sub-batch done
- $\rightarrow$  12 wafers PXD9-21  $\rightarrow$  on hold before metal deposition

	PXD9-20 (12 wafers)											
	W50	W51	W52	W53	W54	W55	W56	W57	W58	W59	W60	W61
Inner Forward	NA	0	100	100	100	99.8	99.8	100	100	100	0	100
Outer Forward 1	NA	NA	NA	99.9	NA	100	100	100	0	100	100	100
Outer Forward 2	NA	NA	NA	NA	NA	0	100	100	100	99.6	100	0
Outer Backward 1	100	100	99.5	100	100	99.8	100	100	99.5	100	99.4	0
Outer Backward 2	0	100	100	100	99.5	100	99.5	98.9	0	100	0	0
Inner Backward	0	100	99.8	99.5	100	100	100	100	99.3	100	100	99.5

PXD9-20a: Production accomplished

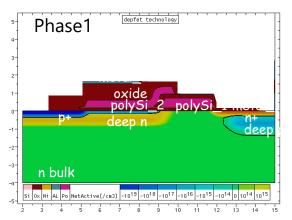
→ Module assembly

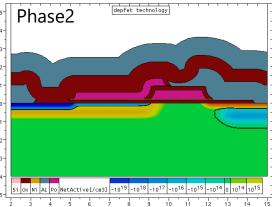
#### PXD9-20b: Production phase3 (thinning and copper)

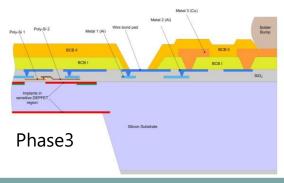
- 1. Handle wafer removal
- 2. Oxide removal on the back side
- 3. sputter Ti:W barrier and Cu seed layer

This week — 4. lithography for electro-plating

- 5. Cu electro-plating
- 6. removal of the seed layer and barrier layer
- 7. Cu conditioning (wet etching, thermal)
- 8. tests on flying needle probe station
- 9. final passivation BCB
- 10. cut lithography, cutting











# PXD9-20a: ATG testing and singulation

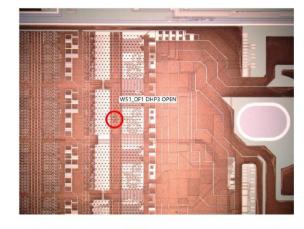


WIILL

	W50	W51	W52	W53	W54	W55
IF	pass	pass	pass	pass	pass	pass
OF1	pass	1 x OPEN	pass	pass	pass	pass
OF2	Pass	pass	pass	pass	pass	pass
OB1	pass	1 x SHORT	pass	pass	pass	pass
OB2	pass	pass	pass	pass	pass	pass
IB	pass	pass	pass	pass	pass	pass

- On Wafer 51 one L2 sensor not usable
- > Sadly, this wafer was destroyed at laser cutting
  - - → 4 L1 pairs + IF for module assembly

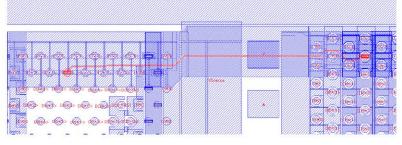
PXD9-20 Wafer #51, OF1 – 1 x OPEN

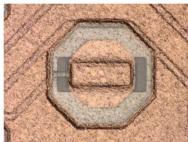




- DHP3 one GND contact is covered with some resist
- Module can be used without re-work

PXD9-20 Wafer #51, OB1 – 1 x SHORT





- DCD1 DO7<3> shorted to GND
- short is not visible





### ASIC inventory and module batch PXD21-2



- ▷ DCD, DHPT okay
- SWB2.1: 240 bumped at IZM, 120 tested at KIT
  - → Still 120 left untested at KIT
  - → Tested chips at HLL: **75 SWB2.1, 30 DCDs, 35 DHPTs**

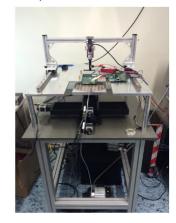
Test Setup at the Institute for Data Processing and Electronics, December 2019

Number of tested switcher chips:

120

#### Main tests:

- Read JTAG ID
- JTAG User Register
  - → Default Bias Current
  - → Boost Bias Current
- Current Consumption (1.8V and HV)
- 64 HV-channels tested with 16-to-1 MUX
- SerOut



Switcher Chips	Read JTAG ID	Current Consumption (1.8V)	Current Consumption (HV)	64 HV- Channels	Bias Current	Boost Current
120	<b>√</b>	<b>√</b>	<b>√</b>	1	1	1



- > 4 L1 pairs, 1 single IF
- Current status: SMD assembly started
  - → About 8 working days for flip-chip at HLL





# L1 and L2 module assembly status



- ⇒ 3 L1 pairs (batch PXD21-1) from old sensor production
  - → Replacement of SWB2.2 successful, passed all probe card tests
  - → Now at MPP for kapton attachment
    - → 2 already done and characterized, 4 still in the queue
- > 4 new L1 pairs on the way (batch PXD21-2) from PXD9-20a under way
- Depending on yield have to decide how many modules from PXD9-20b to assemble
- - → At MPP: 3 L2\_bwd +1 L2\_bwd from phase 2, 4 L2\_fwd
  - → At Bonn: 1 L2\_fwd from phase 2
  - → four more ladders possible (have already 10), need more L2 modules, how many??
- ▶ Please see google spread sheet for current inventory, check, comment and keep it up-to-date:

https://docs.google.com/spreadsheets/d/1ZU3I-t2vJgVT7OAx2ySn7hb0Rbm1TCBZlbcnbgNEwI4/edit?usp=sharing





#### Schedule shown at BPAC



