Latency comparison of ADCs with different interfaces .

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2020-09-24

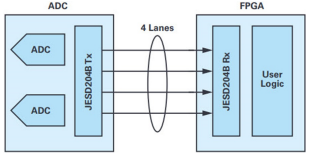
ARD ST3 2020

Motivation

- For some applications (e.g. LLRF, Klystron Lifetime Management) the latency of the entire signal processing chain (ADC+FPGA (DSP algorithm)+DAC) is extremely important
- Here we only consider the latency of the Analog Front End (AFE) + ADC internal pipeline + ADC-FPGA interface

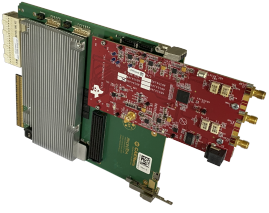
Digitizers in MicroTCA:

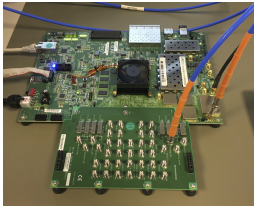
- A few different digitizers already available in MicroTCA form-factor, with several others being developed
- Wide variety of ADCs, from 16-bits 125 MSPS to 12-bits 4 GSPS
- Different interfaces (LVDS, JESD204B, RFSoC) between FPGA and ADC - different latencies



ADCs considered

ADC	Board	Interface	Resolutions [bits]	Sampling rate [MSPS]
AD9268	SIS8300-KU	LVDS	16	125
ADC12D800RF	DAMC-FMC2ZUP + DFMC-DS800	LVDS	12	800
ADS54J60	DAMC-FMC2ZUP + ADS54J60EVM	JESD204B	16	1000
XCZU28DR	ZCU111	RFSoC	12	4096



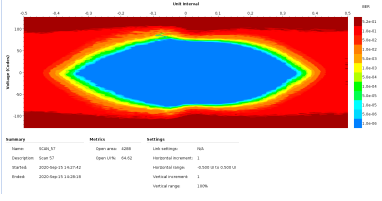


Interfaces

JESD204B

- Serial interface (Multi-Gigabit Transceivers)
- Link has different configurations
- LMFS = 4211 used in this test
  - 4 lanes
  - 2 converters
  - 1 octet per frame
  - 1 sample per frame
- subclass 1 $\rightarrow$ SYSREF ($\sim$ *MHz* signal) used for synchronization

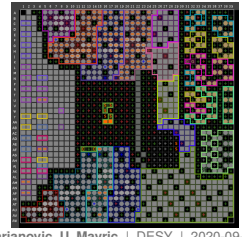
10 Gbps link on GTY transceivers:



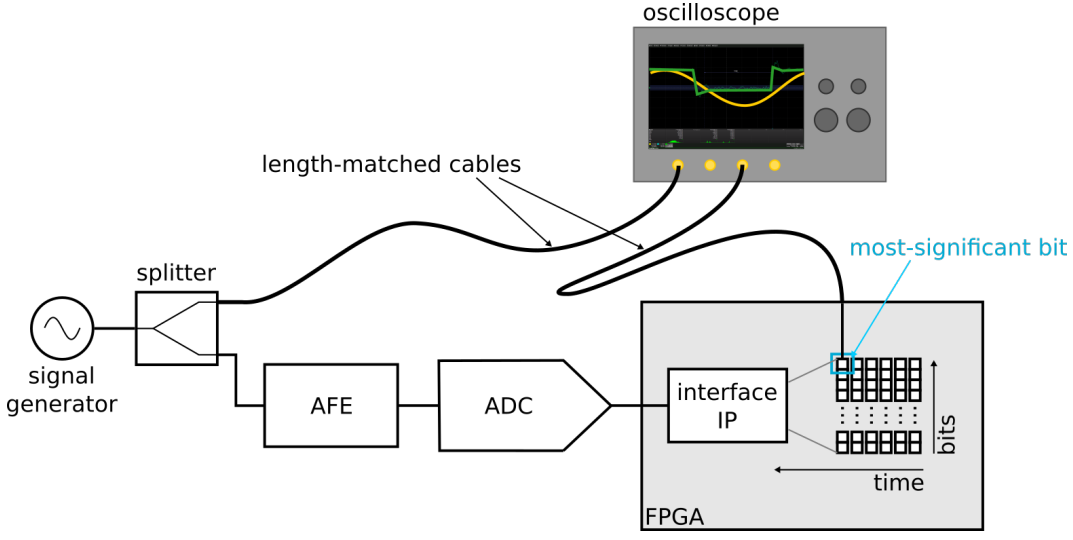
Xilinx RFSoC

- A single device combines:
  - 8 ADCs (12b, 4 GSPS)
  - 8 DACs (14b, 6.5 GSPS)
  - a large FPGA
  - a decent ARM CPU
- Interfacing between ADCs and FPGA is very simplified
- Data (N samples in parallel) + data valid into FPGA logic

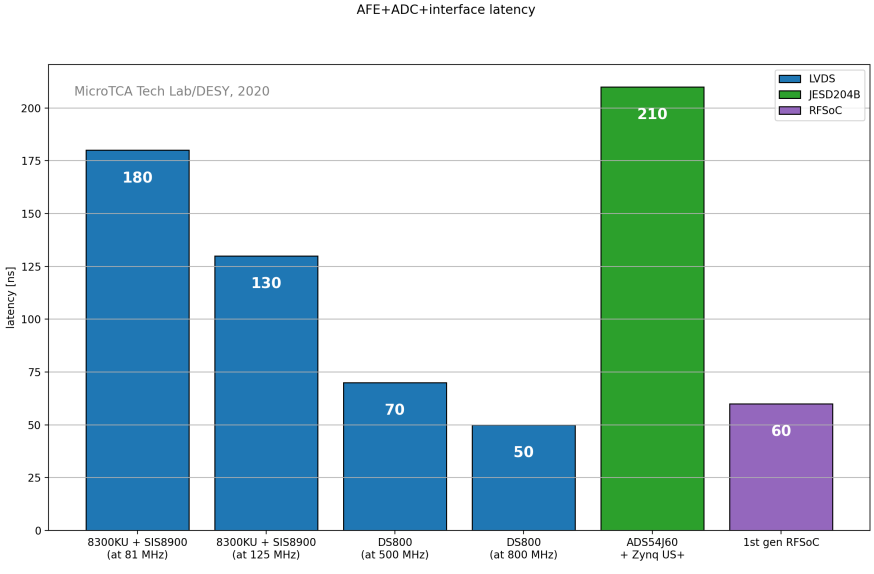
RFSoC footprint (ADCs and DAC on the left side):



Measurement method



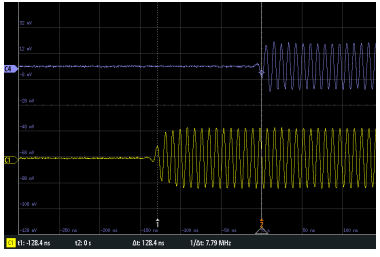
Results


AFE+ADC+interface latency
MicroTCA Tech Lab/DESY, 2020
LVDS
JESD204B
RFSoC
latency [ns]
0
25
50
75
100
125
150
175
200
180
130
70
50
210
60
8300KU + SIS8900
(at 81 MHz)
8300KU + SIS8900
(at 125 MHz)
DS800
(at 500 MHz)
DS800
(at 800 MHz)
ADS54J60
+ Zynq US+
1st gen RFSoC

Conclusions

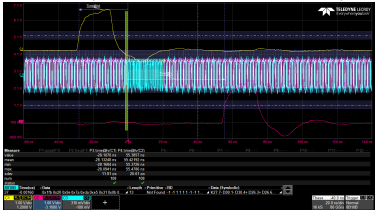
- Several ADCs were compared, with different interfaces
- We see that the latency of MGT transceivers (in JESD204B case) is high, but somehow comparable to other solutions
- Higher sample rate $\not\Rightarrow$ lower ADC+interface latency
- DFMC-DS800 and RFSoC have significantly lower latency than other solutions

RFSoC - 128 ns for ADC + DAC loopback:



GTYE4 MGT latency (at 6.25 Gbps):

83 ns (28 ns for TX, 55 ns for RX)



Thanks for your attention.