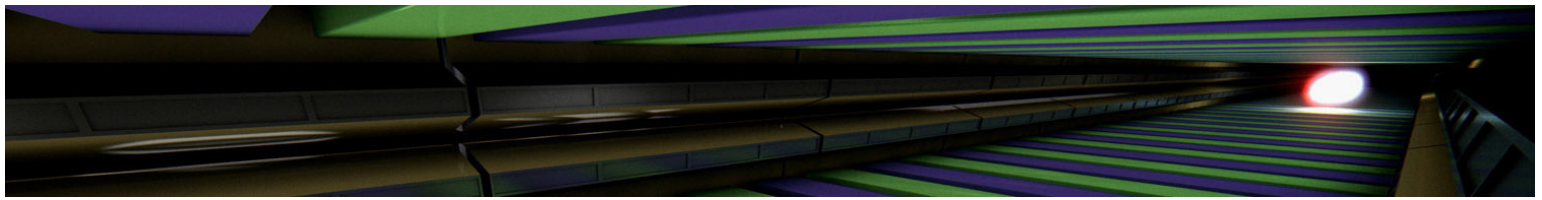
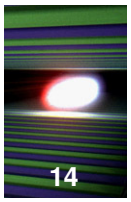


Discussion of Problems and how to overcome them

European XFEL

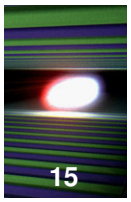
Some Problems



- Basic ADC Functionality needed with Interface to connect special Algorithms or simple Preprocessing to it
- Most Algorithms are developed in Matlab; reprogram everything in VHDL is time consuming
- Accessing a Cards Functionality could be done in many ways, but all need special Drivers or at least DOOCS Servers
- Problems on using VHDL and Verilog in parallel

European XFEL

Some Possible Solutions



- Provide standard Functionality for all with well defined Interfaces for special applications
- Investigate/use Matlab to VHDL compiler to simplify transfers of algorithms
- Define standard card access (registers) for similar card functions (e.g. ADC, DAC, …)
- Common management of DEVICE and VENDOR ID
- Work together on Specification for new common used Hardware (e.g. DAMC-2 and SIS8300)
- Focus un Xilinx FPGAs
- Develop List of Recommendations/Limitations