Upgrade of the CMS barrel pixel detector

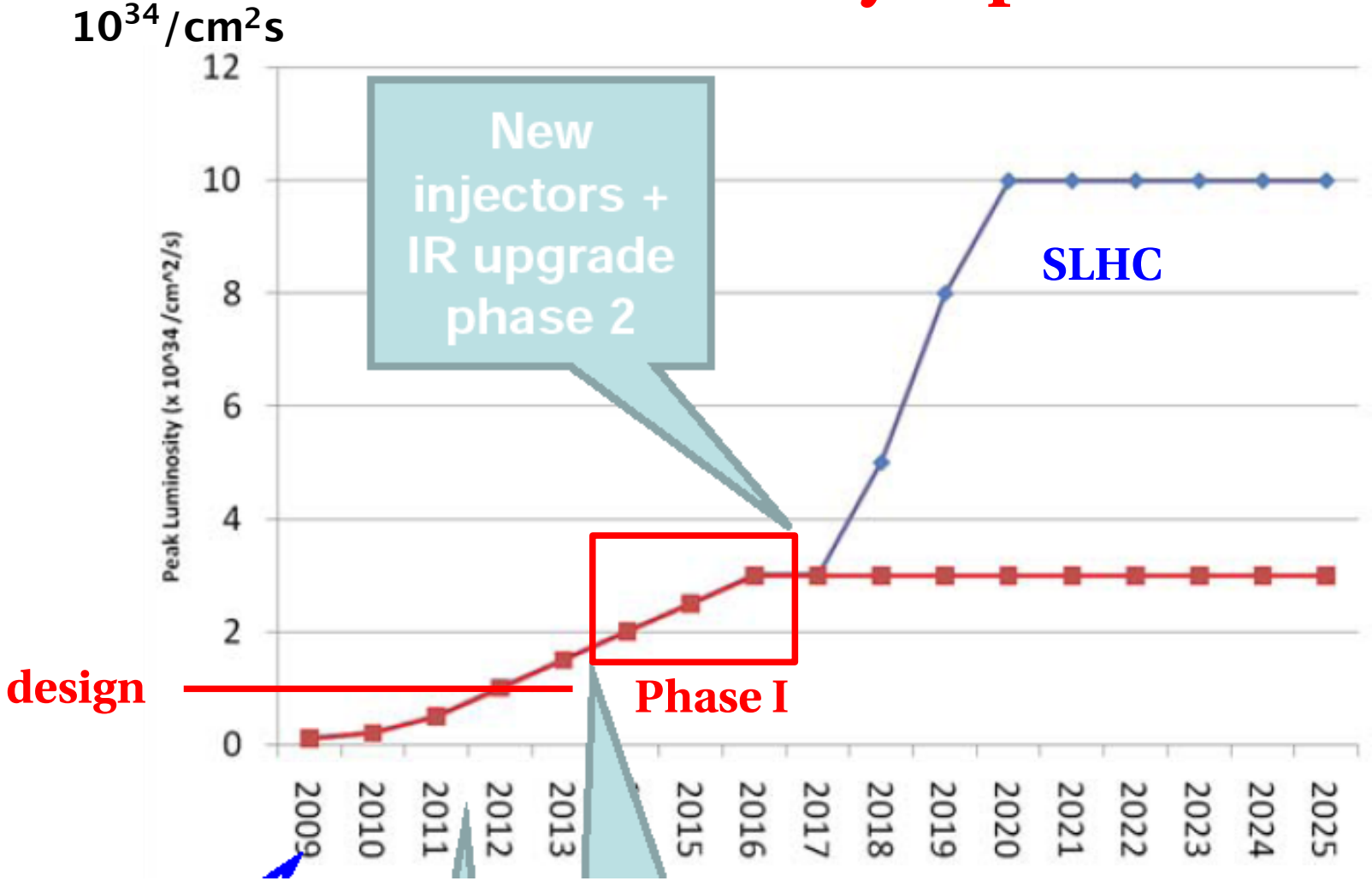
Daniel Pitzl, DESY

6.1.2010

CMS Hamburg

- Experimental motivation:
  - 4^{th} layer efficiency and resolution
  - Material budget reduction
  - Data loss at higher luminosity
- Assembly at DESY:
  - Bump bonding
  - testing

LHC luminosity expectation



expect schedule to evolve with experience

Lyn Evans, CERN Academic training lecture June 2009
http://indico.cern.ch/conferenceDisplay.py?confId=55041

SLHC physics goals

1. Improve measurements of new phenomena seen at the LHC. E.g.
   - Higgs couplings and self-couplings
   - Properties of SUSY particles (mass, decay BR's, etc)
   - Couplings of new Z' or W' gauge bosons (e.g. L-R symmetry restoration?)
2. Detect/search low-rate phenomena inaccessible at the LHC. E.g.:
   - $H \rightarrow \mu^+\mu^-$, $H \rightarrow Z\gamma$
   - top quark FCNCs
3. Extend sensitivity to high-mass scales. E.g.
   - New forces (Z', W_R)
   - Quark substructure
   - ....

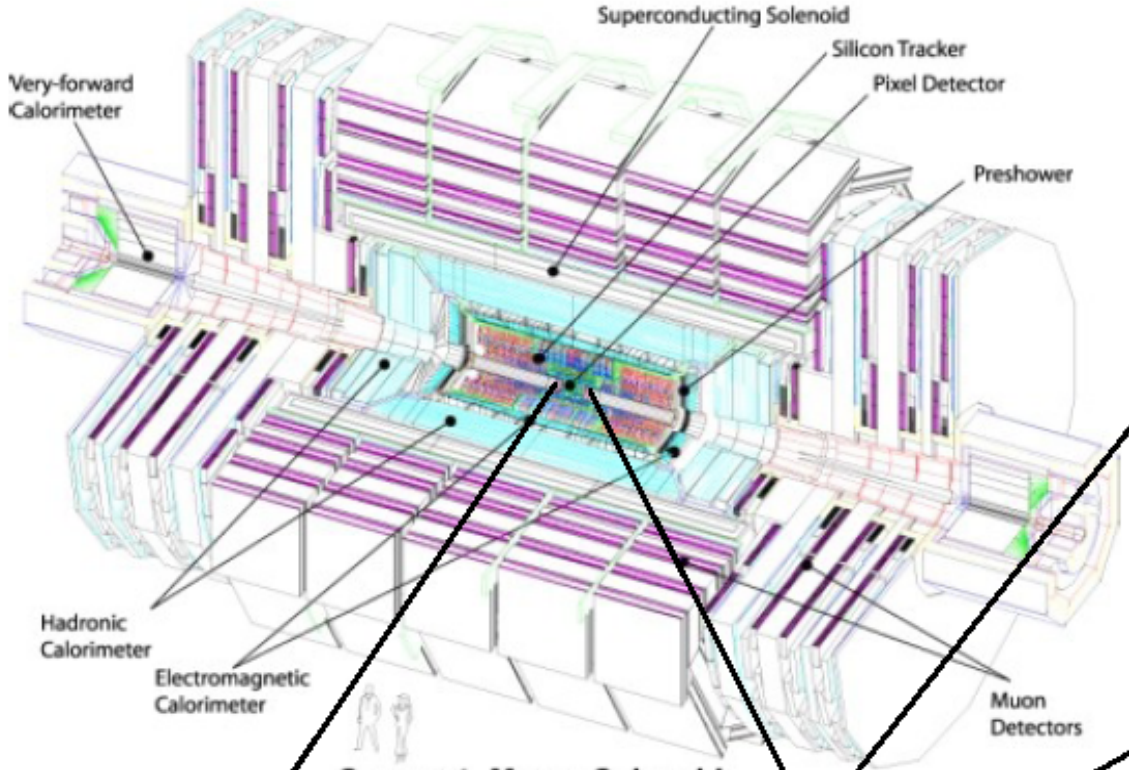
Energies/masses in the few-100 GeV range. Detector performance at SLHC should equal (or improve) in absolute terms the one at LHC

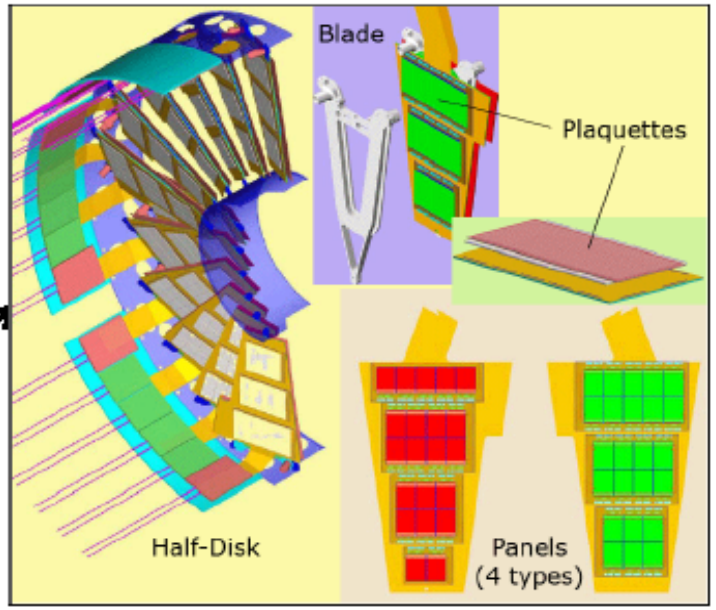
Very high masses, energies, rather insensitive to high-lum environment.
Not very demanding on detector performance
Slightly degraded detector performance tolerable

8

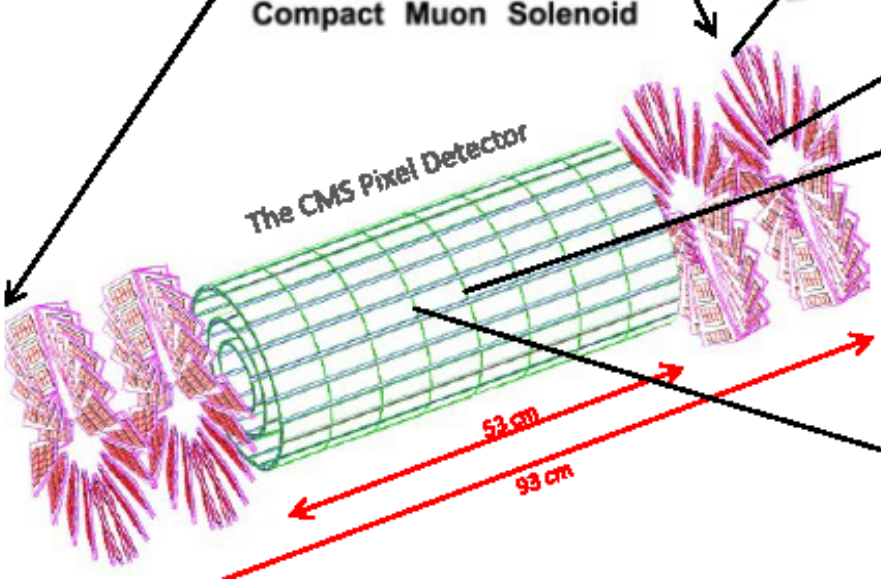
Michelangelo Mangano, CERN Academic training lecture June 2009
http://indico.cern.ch/conferenceDisplay.py?confId=55041

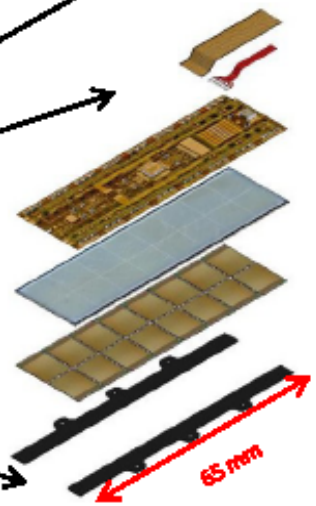
CMS Pixel detector





Panels of the Forward Pixel Detector





Modules of the Barrel Pixel

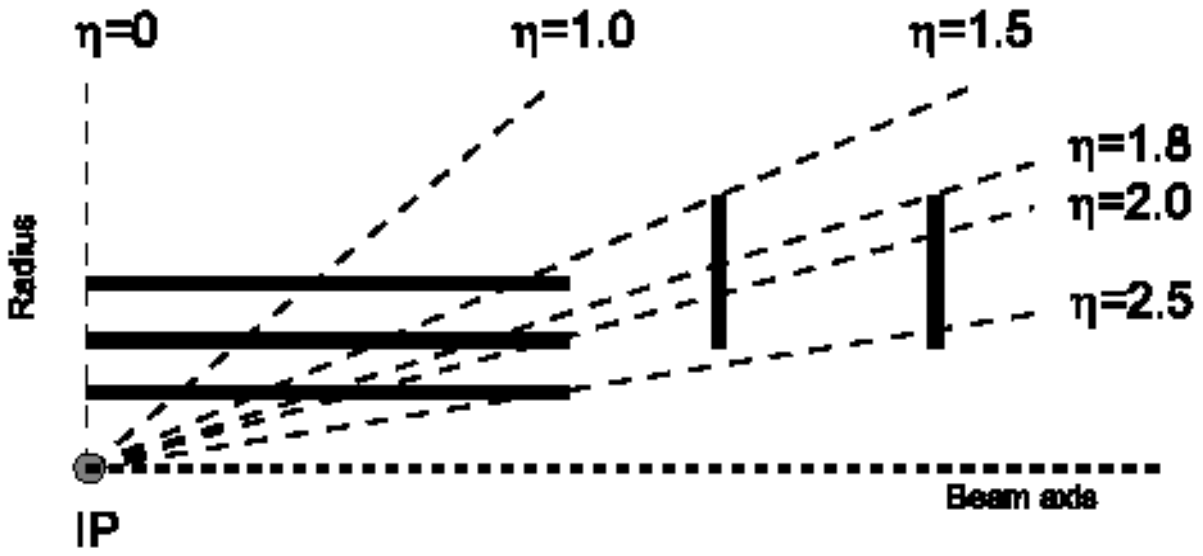
- Forward Pixel Detector (**FPix**) has two disks on each side at 34.5 cm and 46.5 cm
- FPix has 672 modules

- Barrel Pixel Detector (**BPix**) has 3 layers of radii 4.3 cm, 7.2 cm and 11.0 cm
- BPix has 768 modules

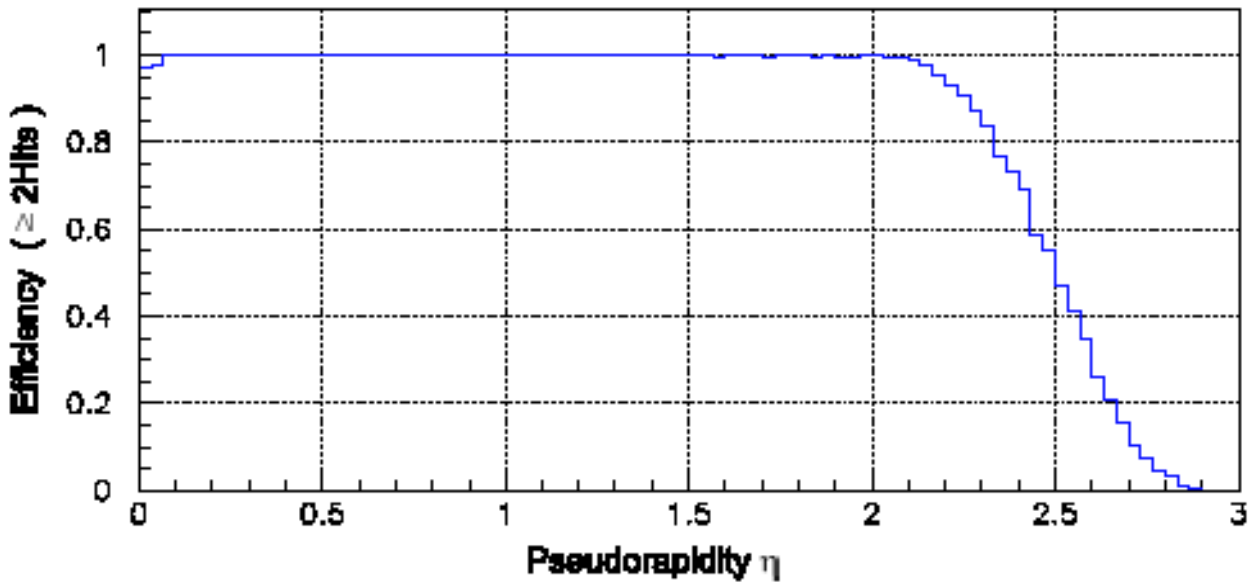
- Total of **~15,840 Readout Chips**

S. Das

CMS Pixel acceptance

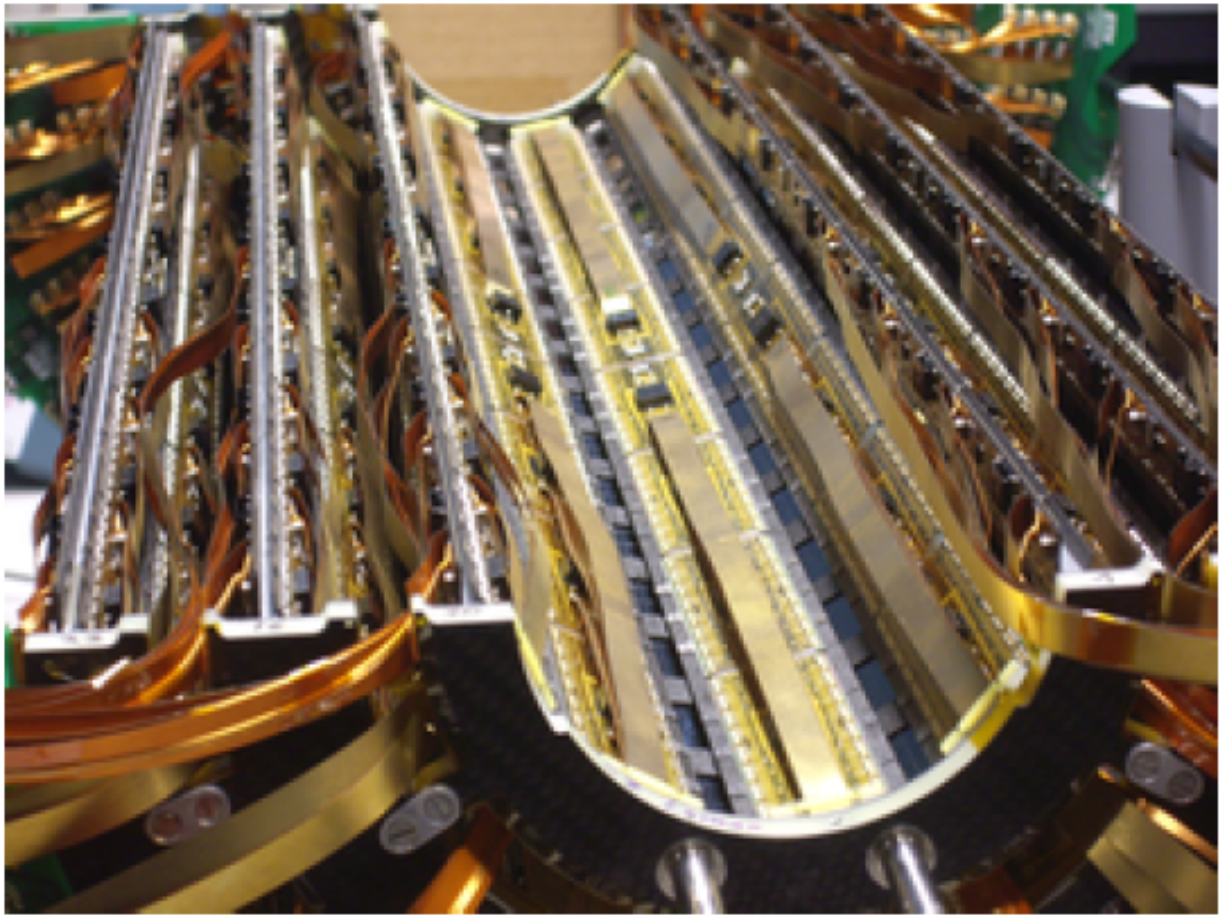


W. Erdmann



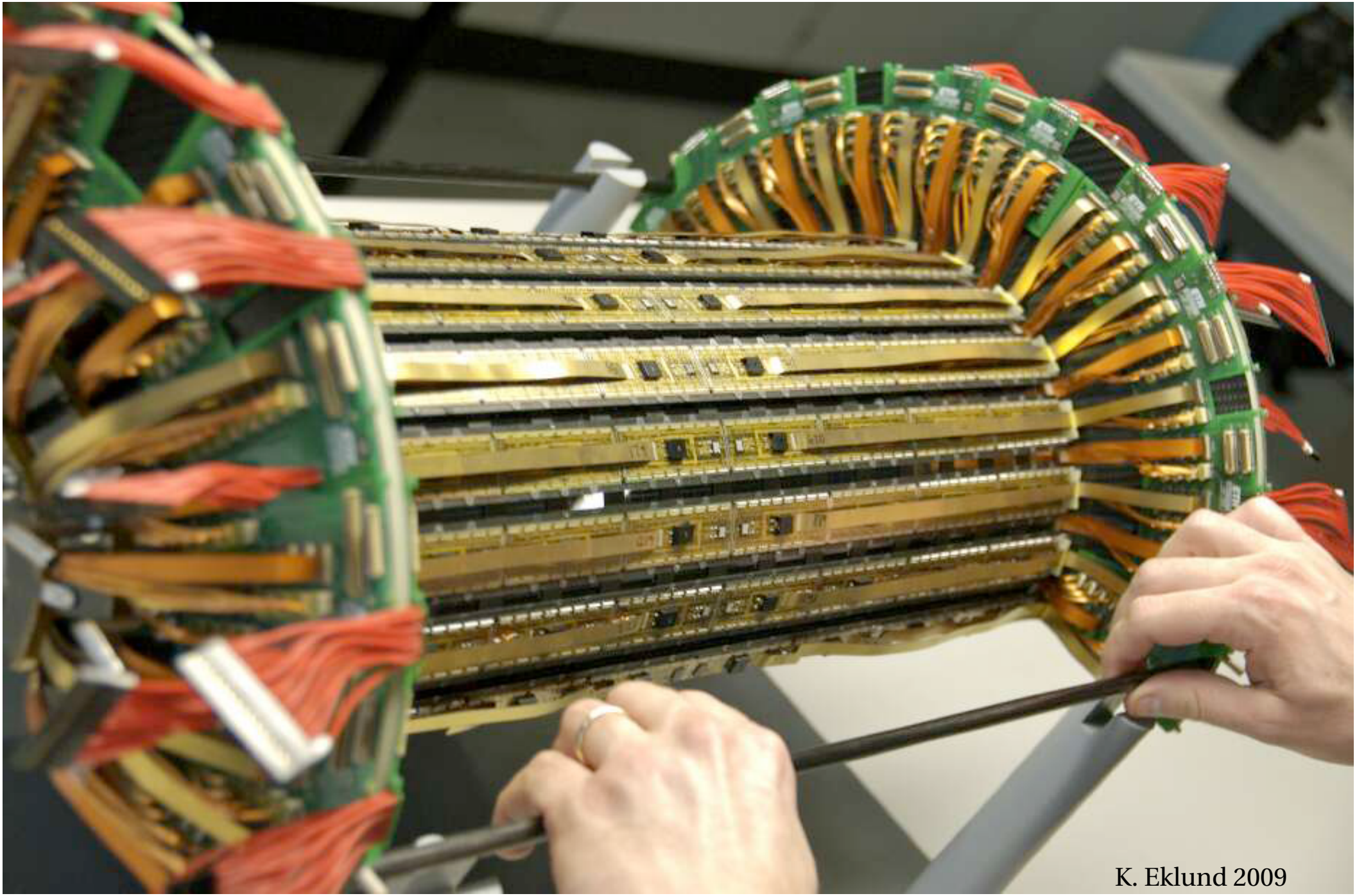
- 2-of-3 is fine for vertexing out to $\eta \sim 2.2$.
- Gaps between modules in z: ~3% inefficiency per layer
- Pixel track seeding requires 3-of-3 with about 90% efficiency at present.

3 barrel pixel layers

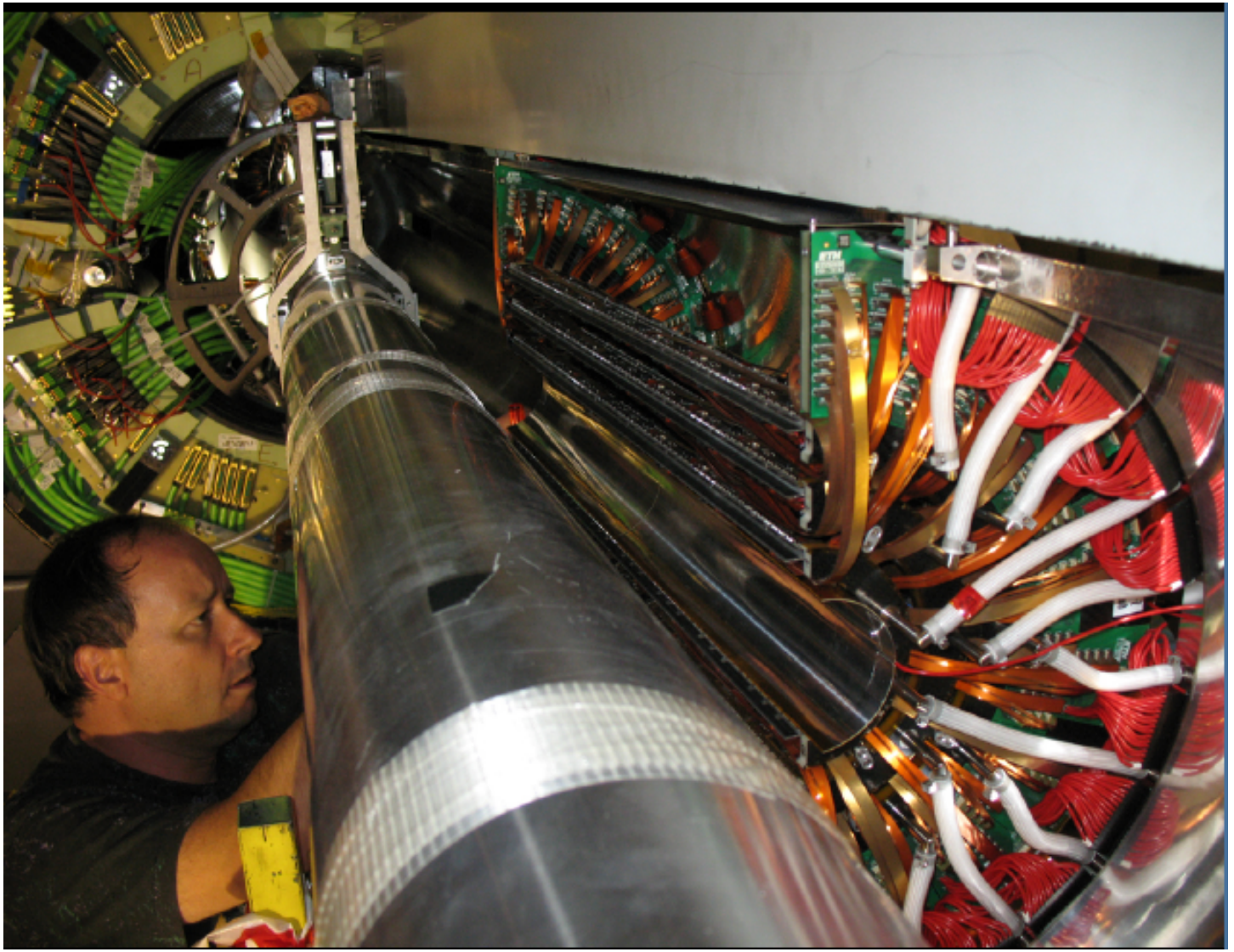


A. Starodumov

Barrel pixel detector



CMS Pixel insertion 2008

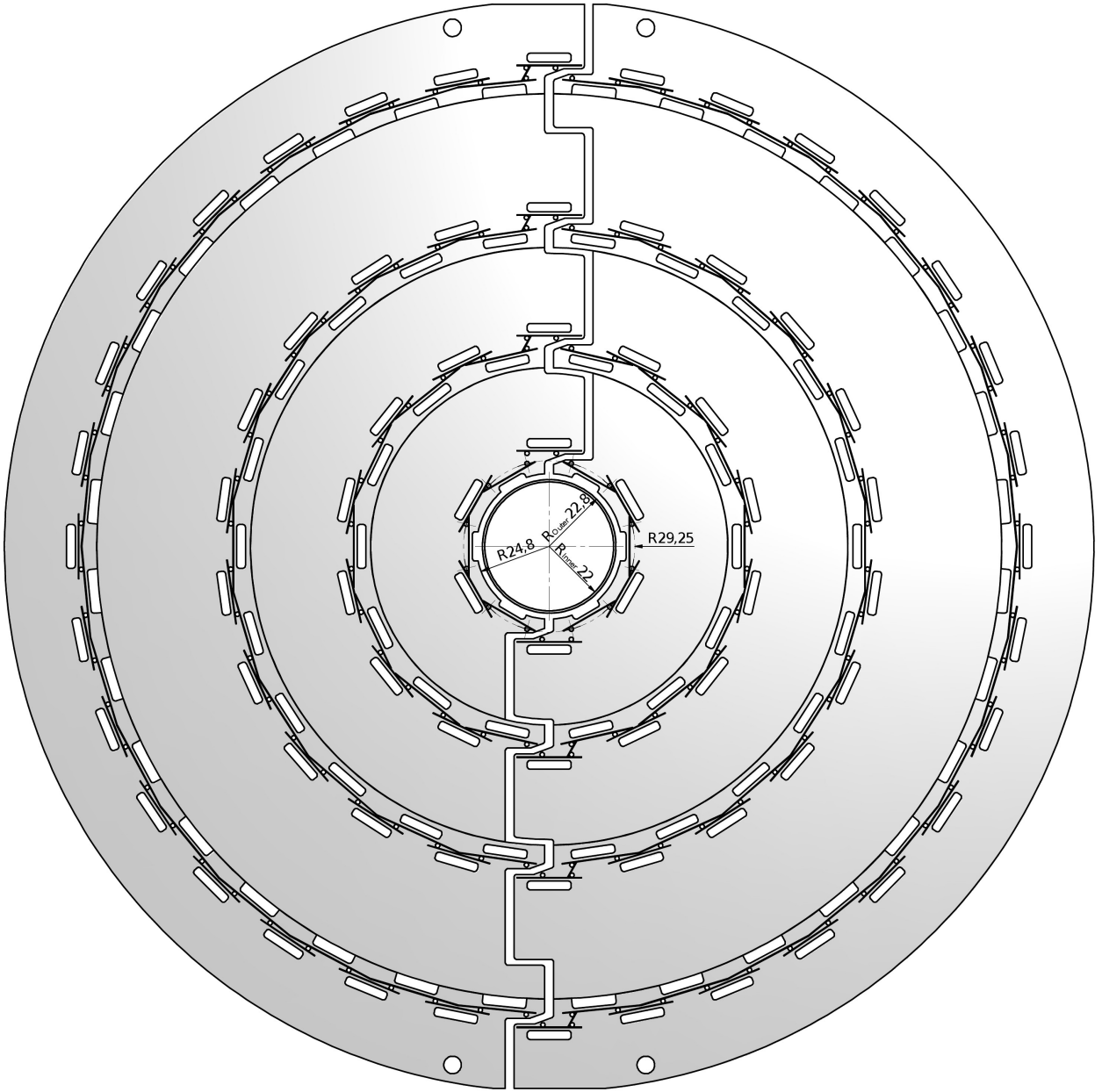


S. Streuli

D. Abbaneo

- Pixel detector accessible and removable in normal shutdowns.

CMS barrel pixel upgrade: 4 layers



2 identical half-shells.
1184 modules (79M pixels)
(1.6 × present barrel)

R_1 = 29 mm, 96 modules
(if R=22 mm beam pipe is possible) PSI

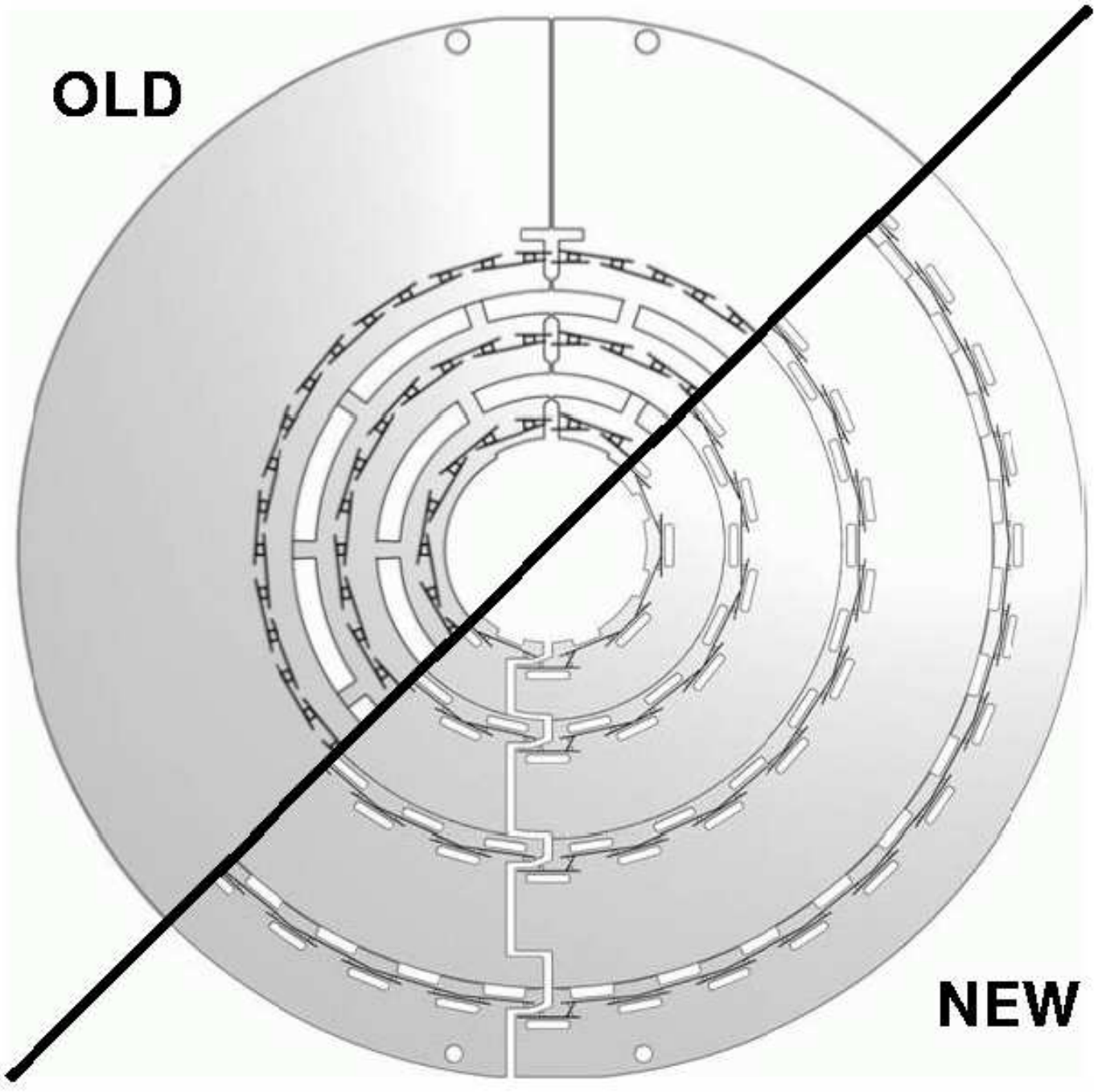
R_2 = 68 mm, 224 modules
PSI

R_3 = 109 mm, 352 modules
DESY

R_4 = 160 mm, 512 modules
Italy

R. Horisberger: Tracker Upgrade Steering Dec 2009
http://indico.cern.ch/conferenceDisplay.py?confId=75797

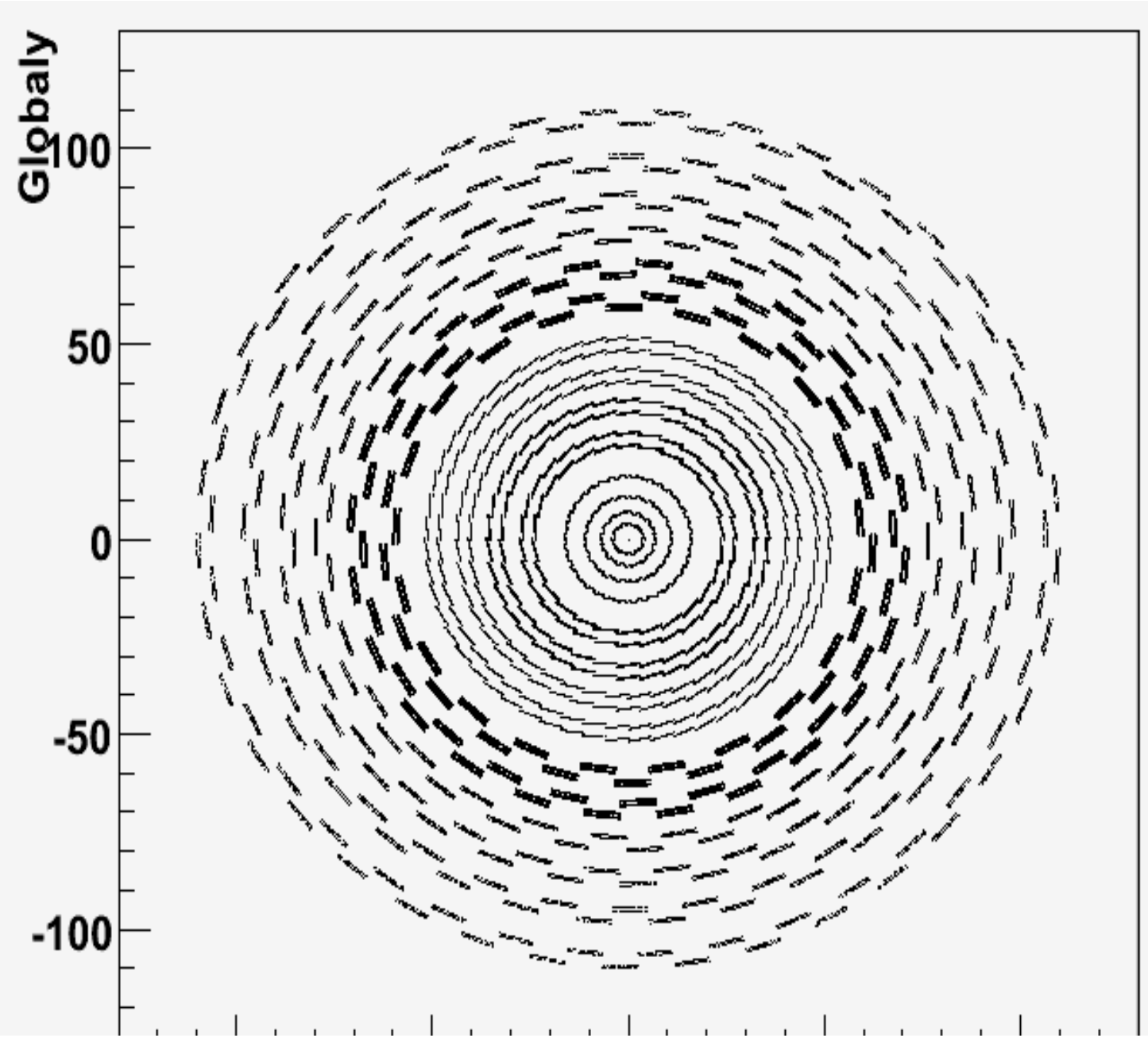
CMS pixel upgrade: 4 layers



- New design without half-modules: zig-zag vertical split
- Conservative version with present beam pipe radius.

S. König
Vertex Conf
Sep 2009

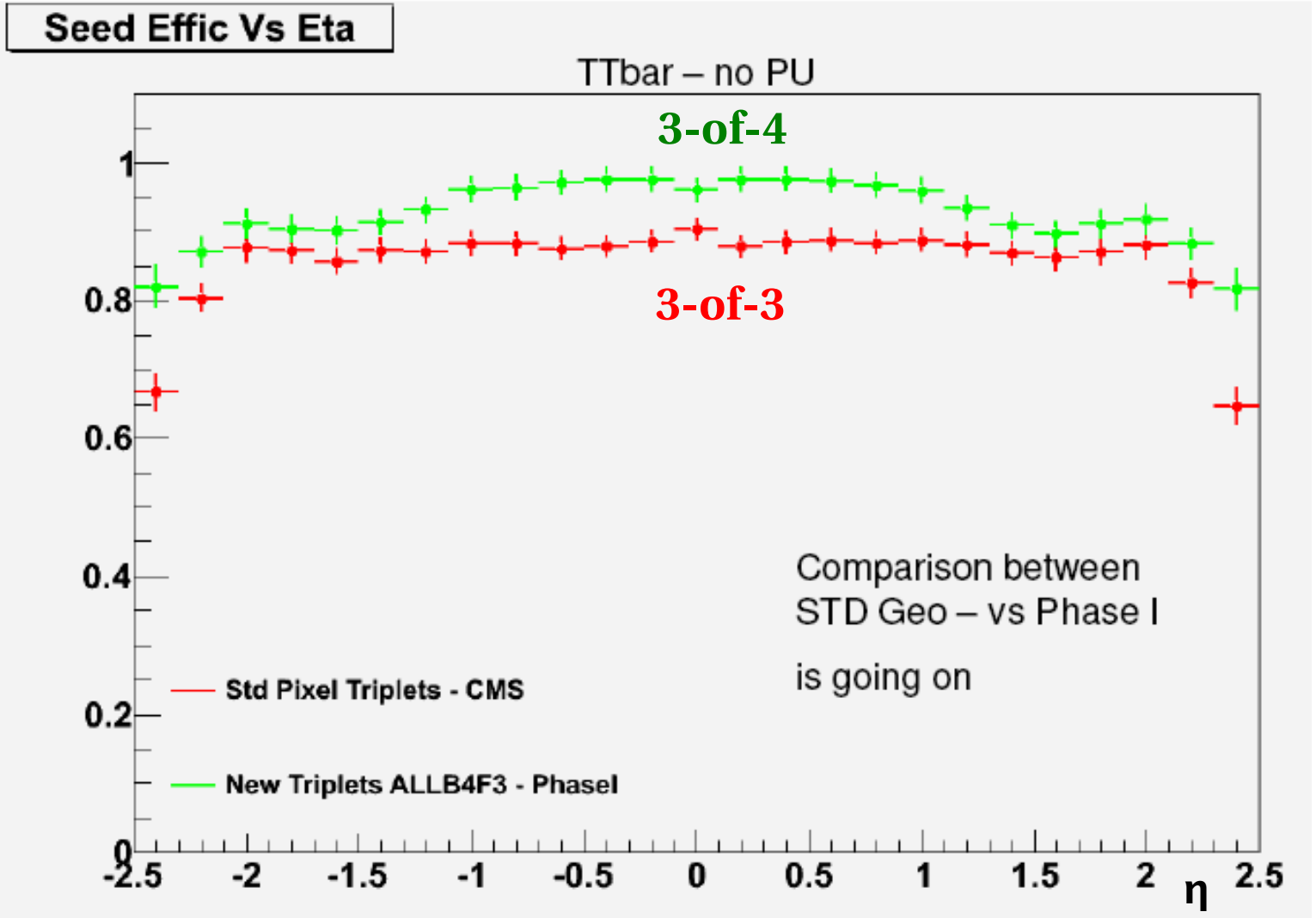
Phase I upgrade in CMS simulation



- 4-layer pixel implemented into CMS software: simulation and reconstruction.
- Silicon strip detector unchanged.

Alessia Tricomi
Tracker Upgrade Sep 2009
http://indico.cern.ch/conferenceDisplay.py?confId=47293

Track seeding

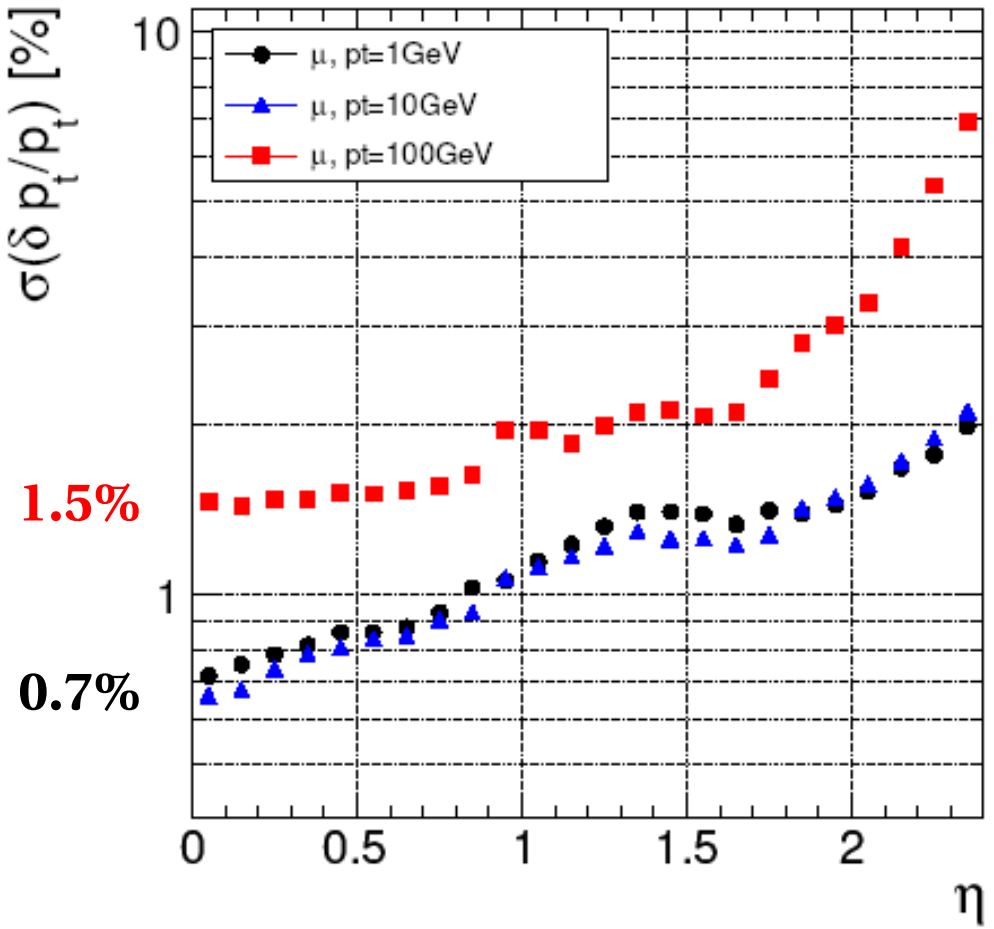


- Pixel triplets for track seeding:
- Obvious efficiency gain with 3-of-4 vs 3-of-3.

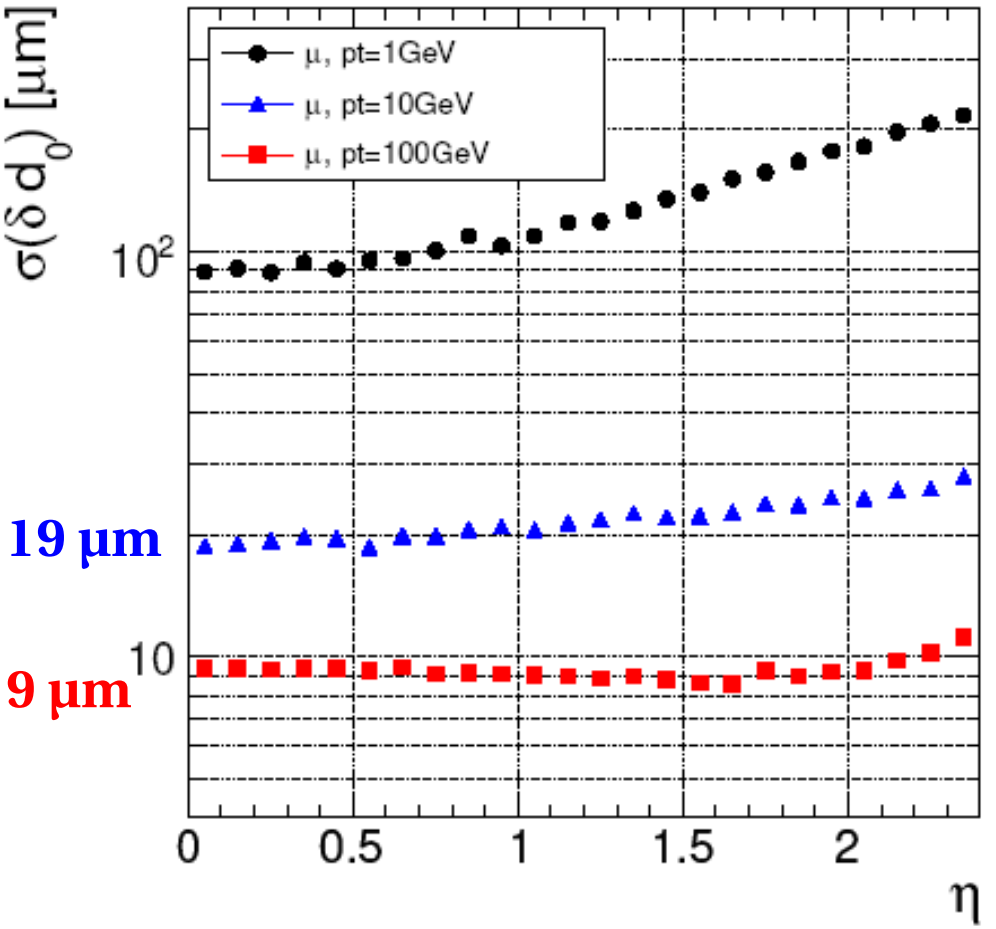
Alessia Tricomi
CMS Tracker week Oct 2009
http://indico.cern.ch/conferenceDisplay.py?confId=47301

present CMS tracker resolutions

momentum resolution



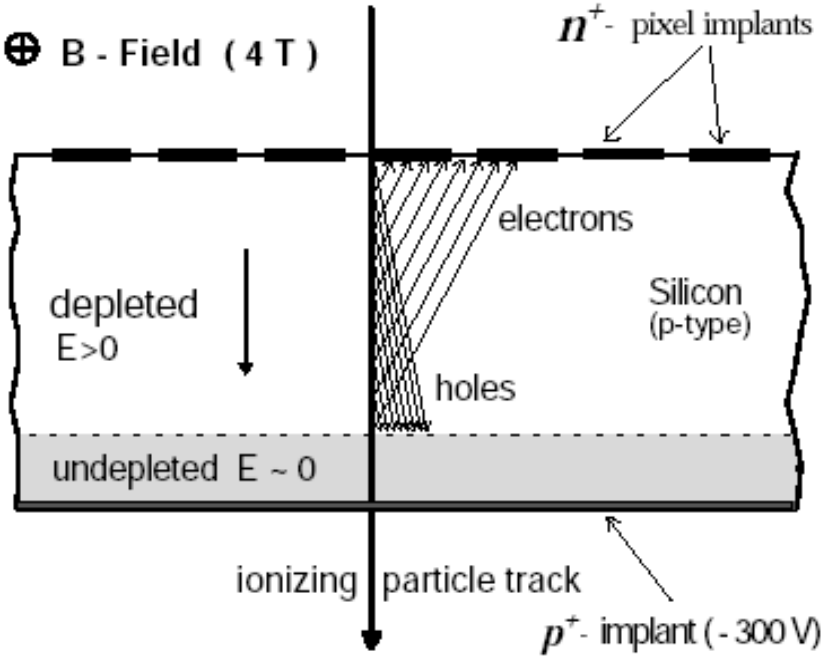
transverse impact parameter



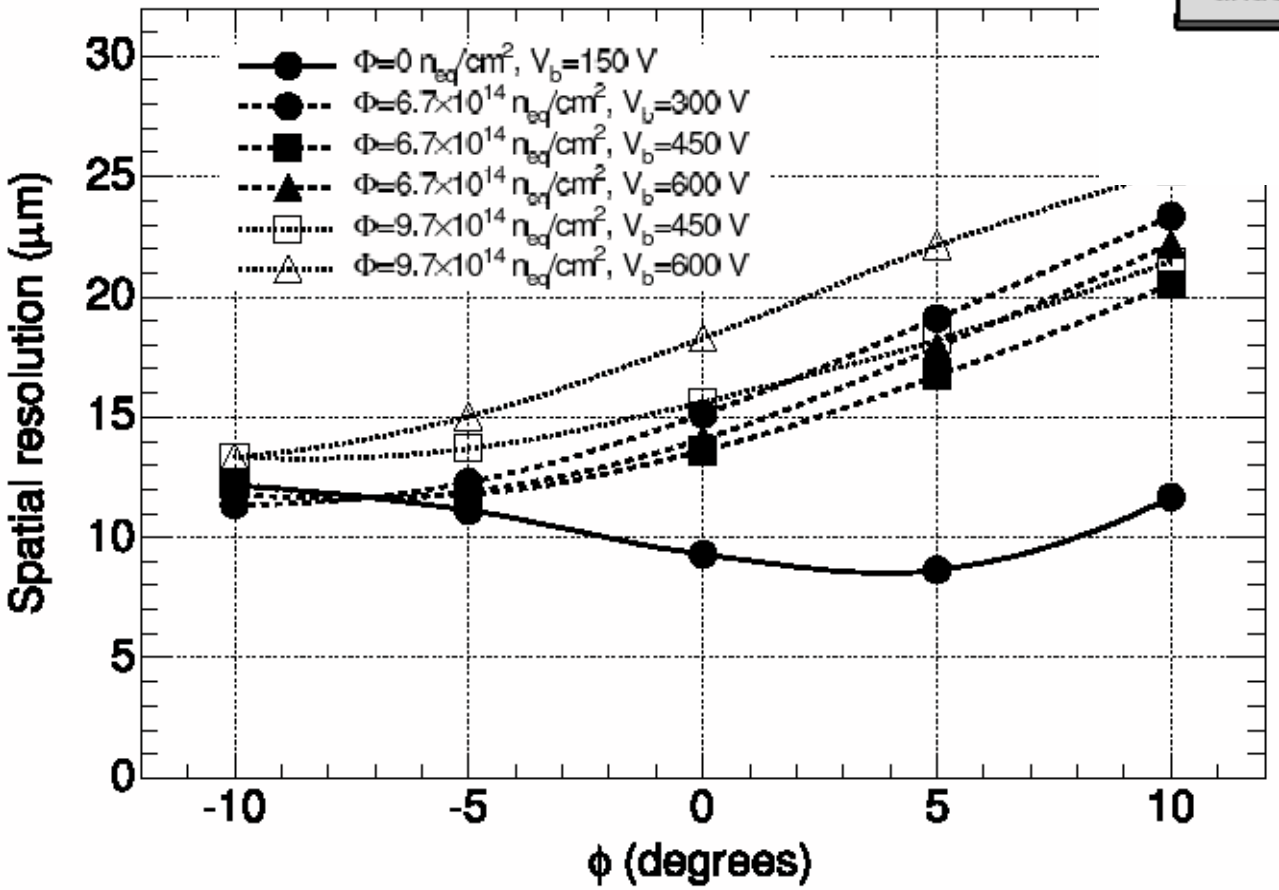
CMS detector, JINST 3 (2008) S08004

CMS Pixel hit resolution

Charge sharing by Lorentz drift in the solenoid field in $r\phi$:



Pixel resolution vs incident angle
Before and after irradiation:



10 μm resolution with 100 μm pixel size requires analog readout for interpolation

W. Erdmann

Broken line fit

Track model: broken helix from V. Blobel, implemented by C. Kleinwort.
Takes multiple scattering and intrinsic resolution into account.
Covariance matrix of helix curvature and impact parameter to the beam is calculated.

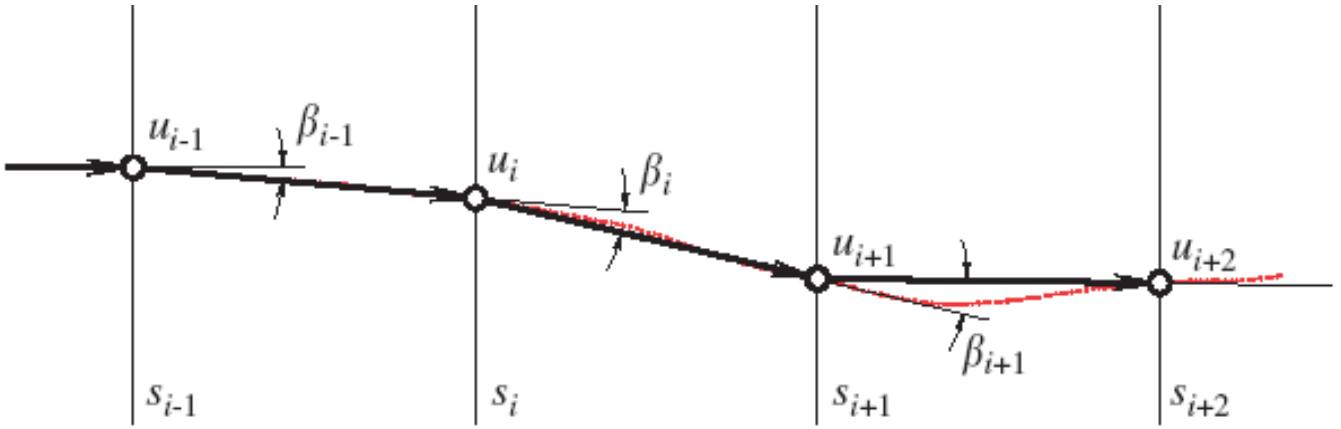
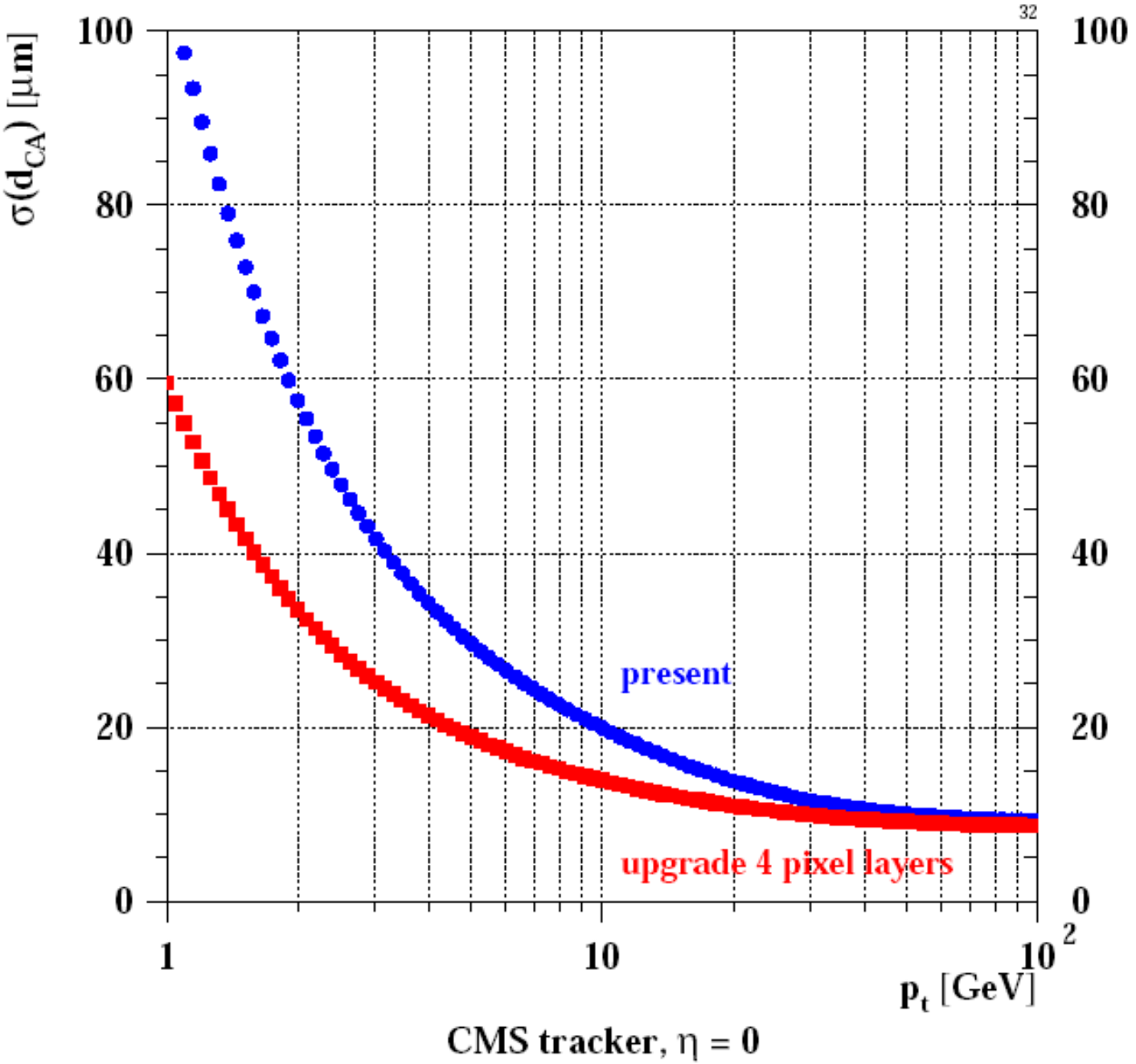


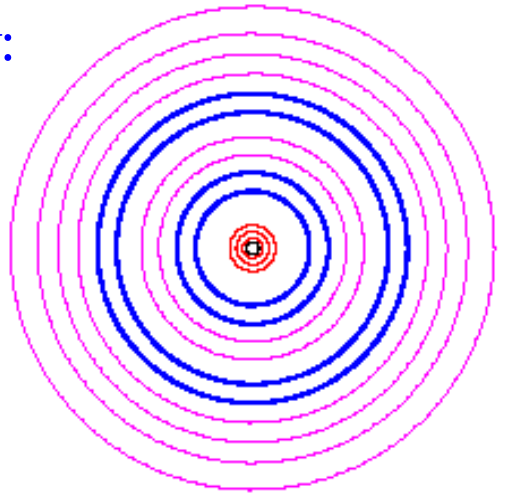
Fig. 3. Particle trajectory with fitted residuals u_i and kink angles β_i.

Volker Blobel, Nuclear Instruments and Methods A566 (2006) 14-17

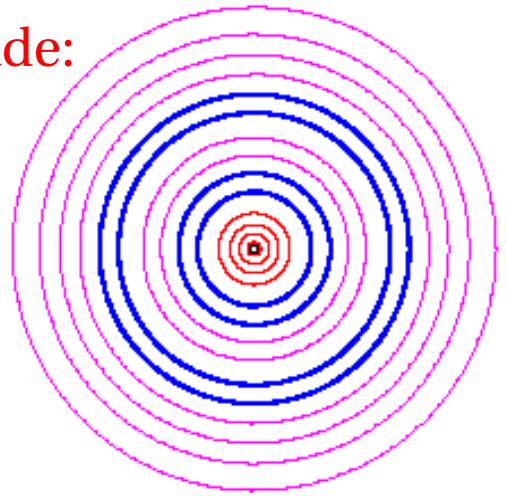
CMS impact parameter resolution



now:



Pixel upgrade:

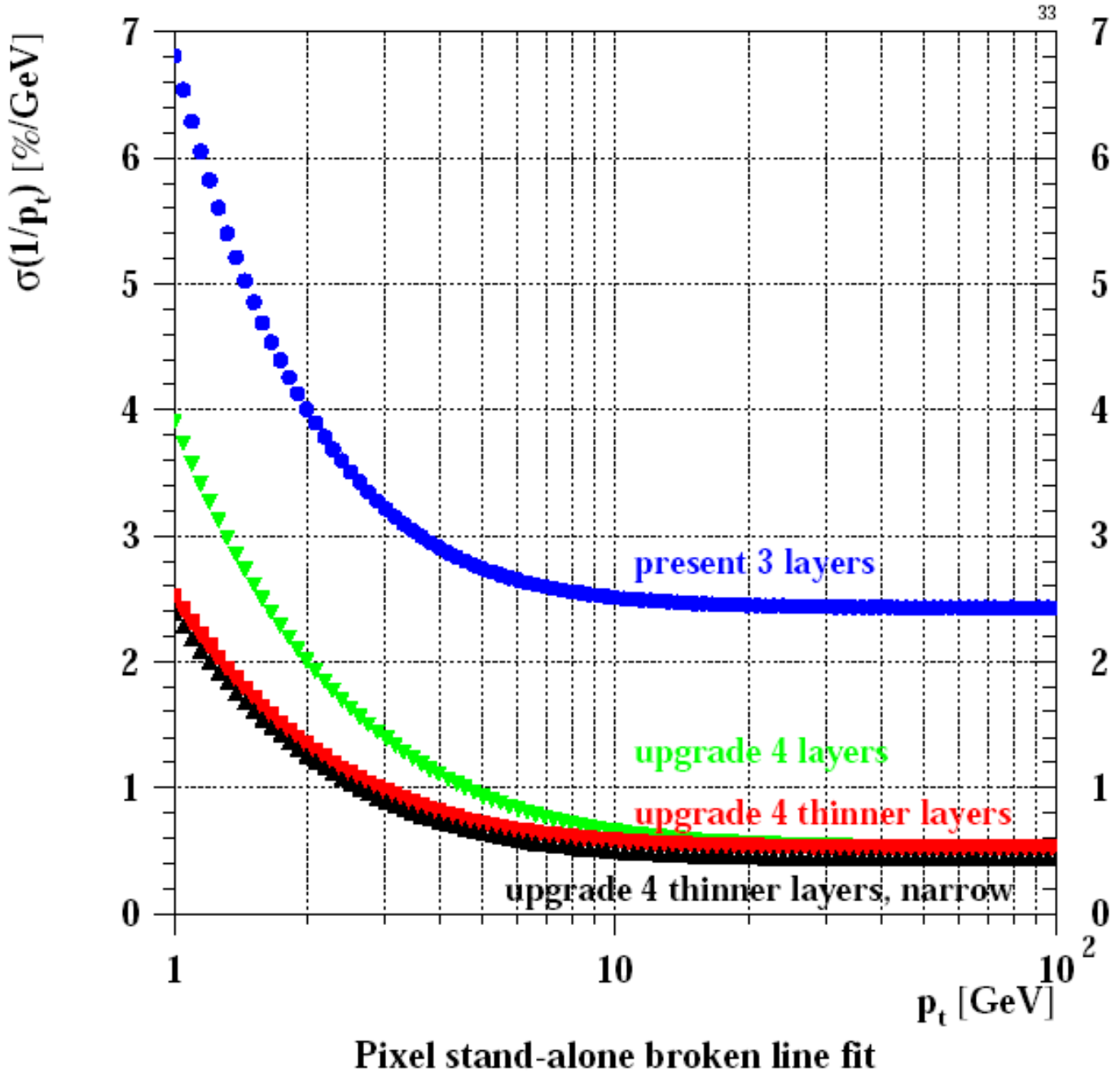


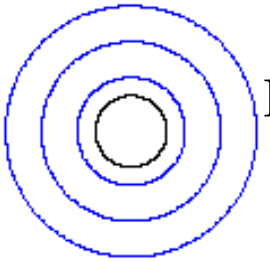
broken line simulation agrees with CMS paper for present geometry.

CMS pixel tracker resolution study

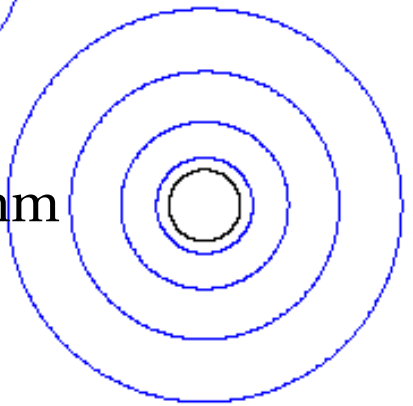
present:			4 layers:			4 thinner:			4 small BP:		
	R	X0		R	X0		R	X0		R	X0
	mm	%		mm	%		mm	%		mm	%
BP	29	0.5	BP	25	0.5	BP	25	0.5	BP	22	0.5
L1	44	2.5	L1	39	2.5	L1	39	1.5	L1	29	1.5
L2	73	2.5	L2	68	2.5	L2	68	1.5	L2	68	1.5
L3	102	2.5	L3	109	2.5	L3	109	1.5	L3	109	1.5
			L4	160	2.5	L4	160	1.5	L4	160	1.5

CMS pixel momentum resolution





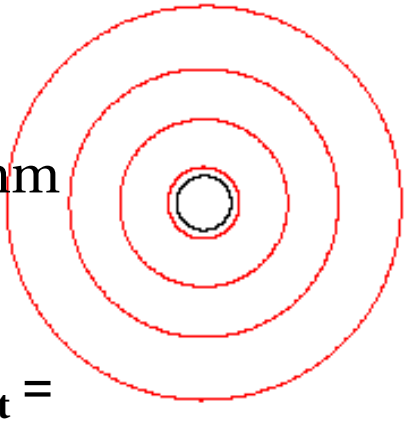
R_{BP} = 29 mm



R_{BP} = 25 mm

$\sigma(p_t) / p_t =$

$6.4\% \oplus 2.4\% \; p_t \; [GeV]$

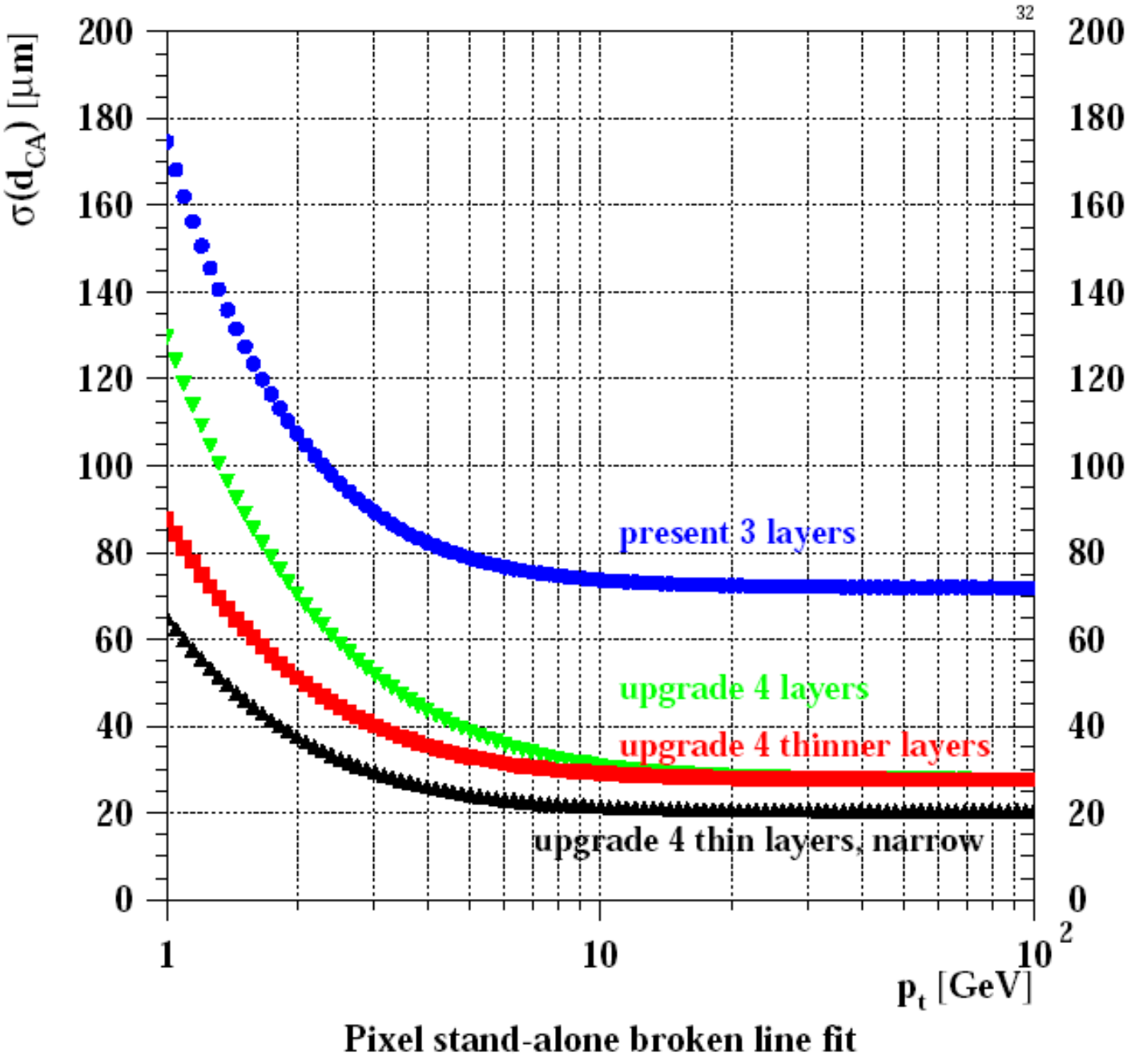


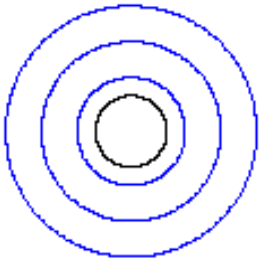
R_{BP} = 22 mm

$\sigma(p_t) / p_t =$

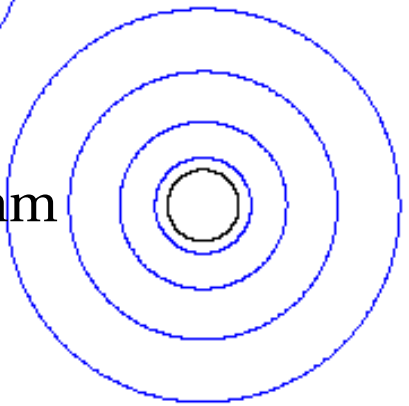
$2.5\% \oplus 0.4\% \; p_t \; [GeV]$

CMS pixel impact parameter resolution





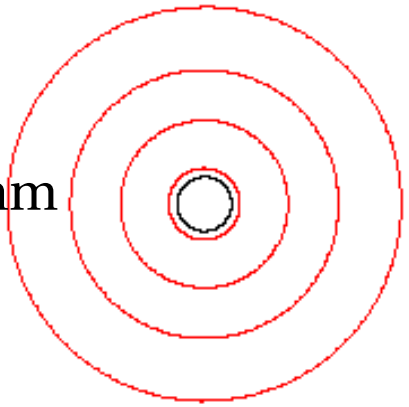
R_{BP} = 29 mm



R_{BP} = 25 mm

$\sigma(d_{CA})$ =

160 μm / p_t ⊕ 72 μm

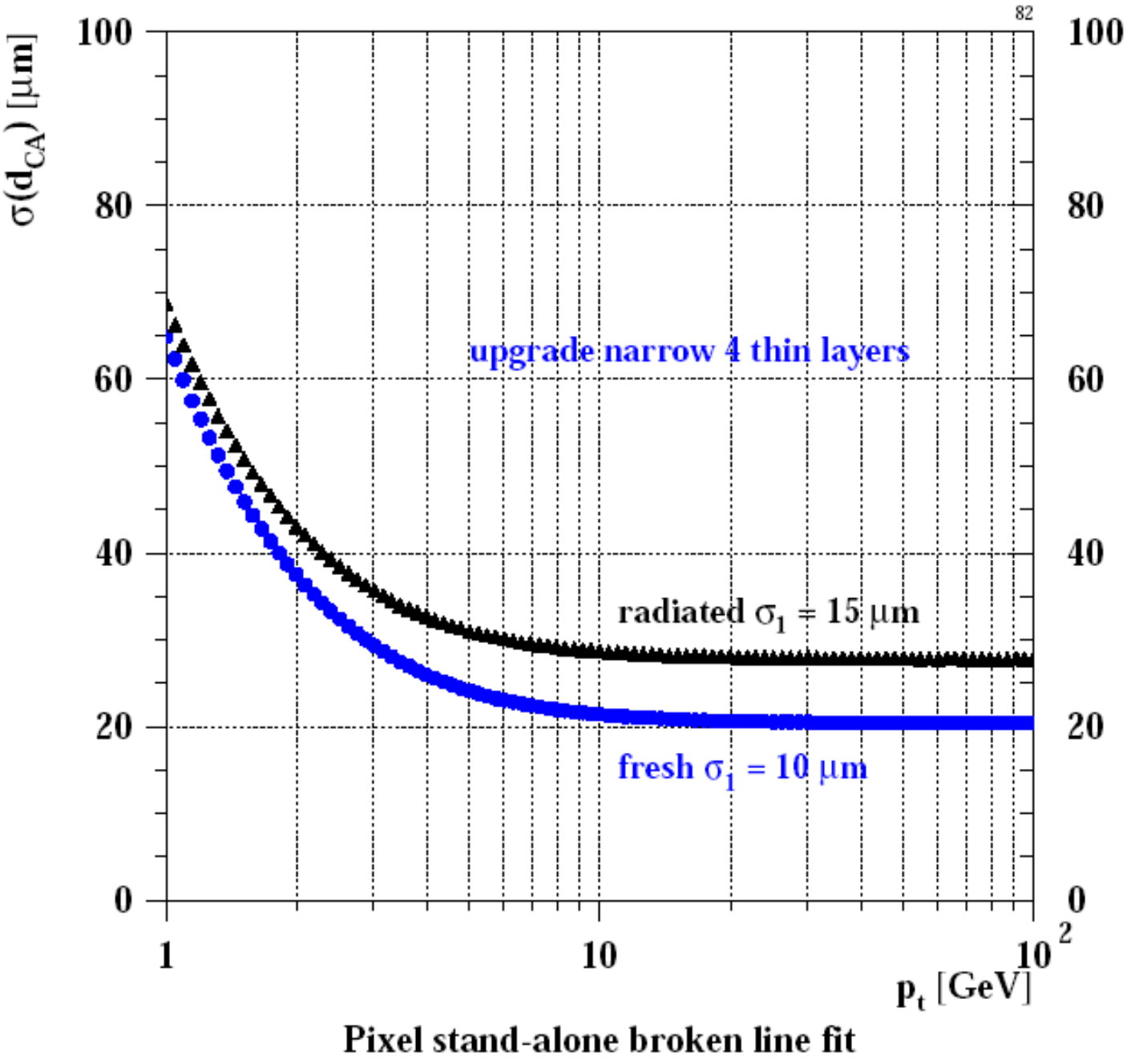


R_{BP} = 22 mm

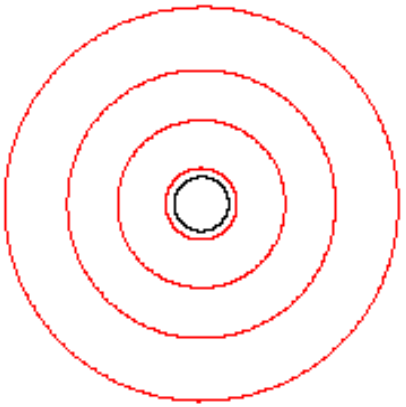
$\sigma(d_{CA})$ =

62 μm / p_t ⊕ 20 μm

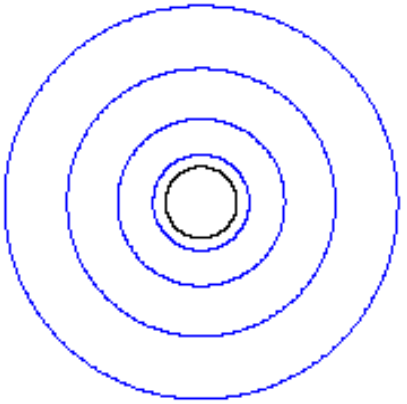
Radiation damage



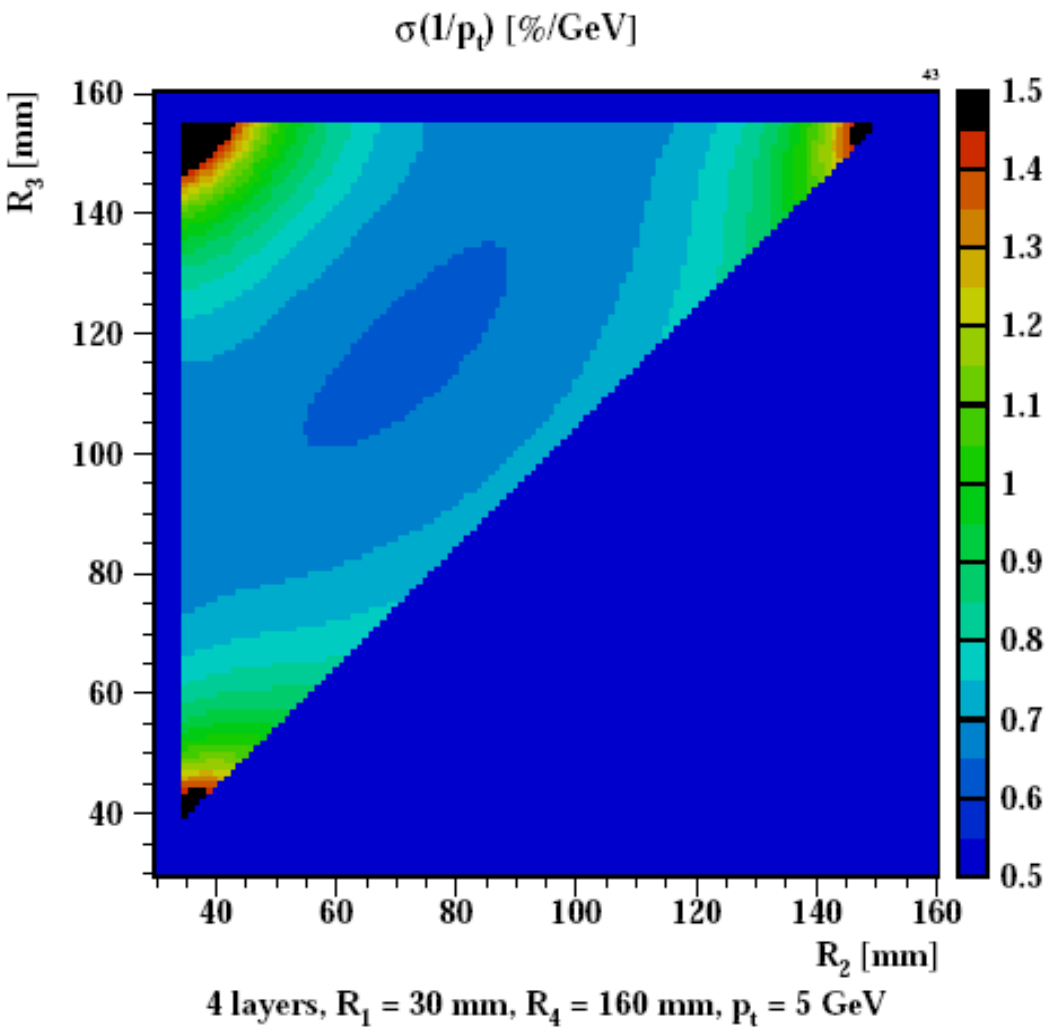
R_{BP} = 22 mm

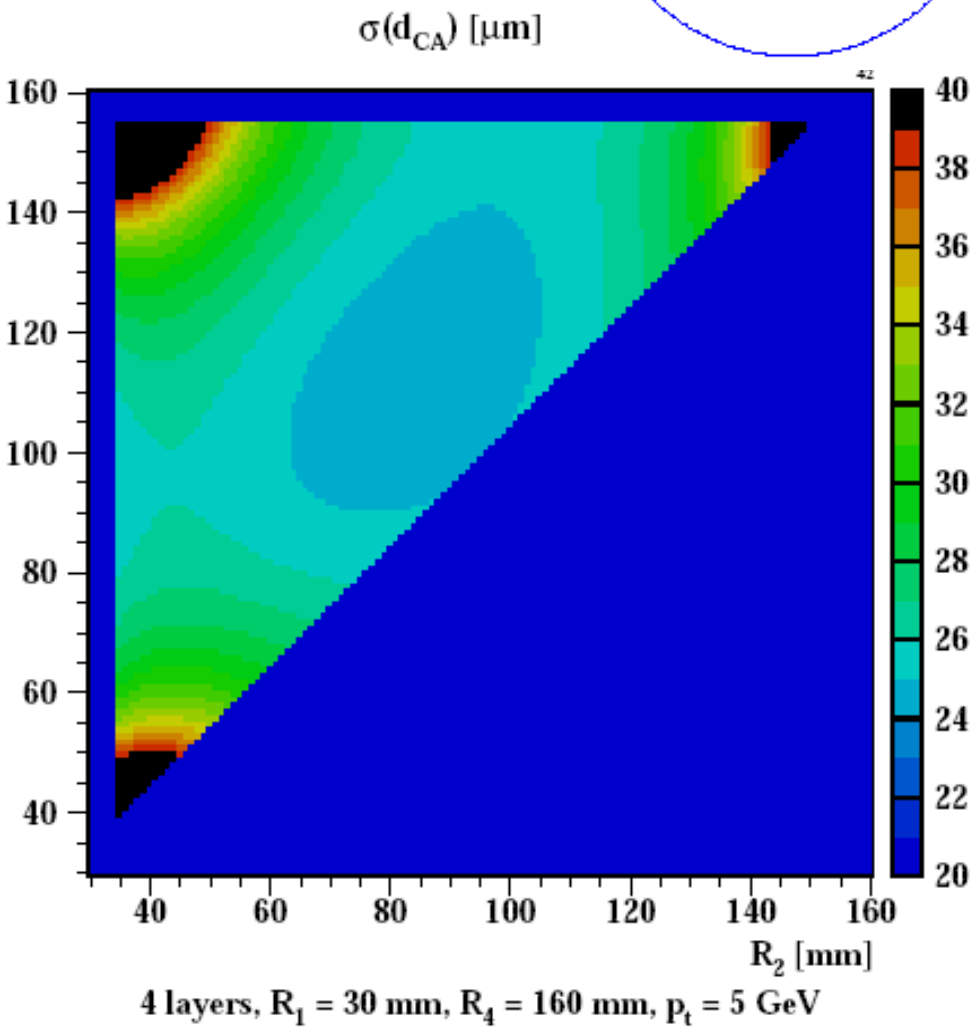


Pixel tracker design study



vary R_2 and R_3 for a 4-layer detector

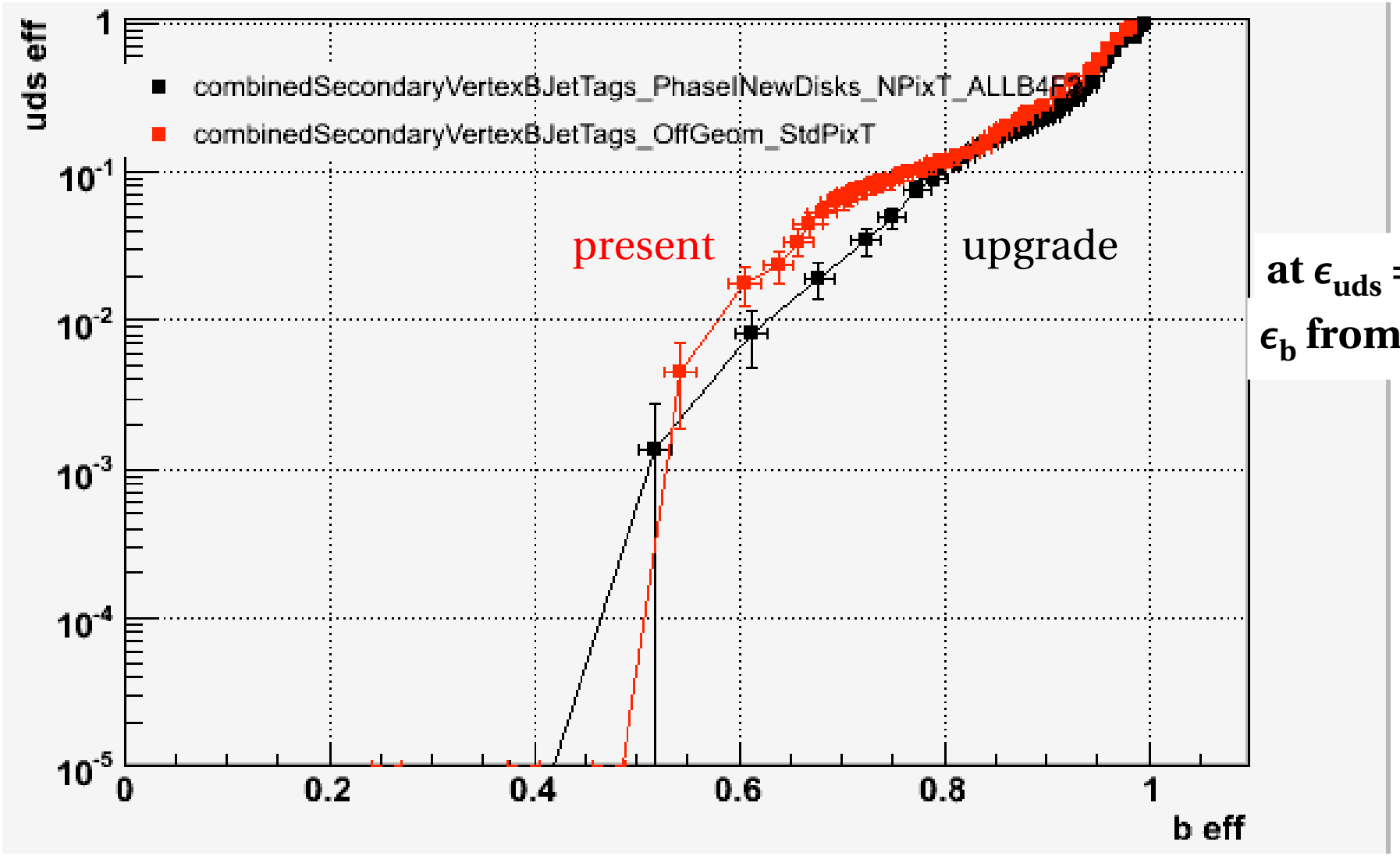




p_t optimum: $R_2 = 70$, $R_3 = 115$ mm

d_{CA} optimum: $R_2 = 85$, $R_3 = 115$ mm

B-tagging



t-tbar MC
no pile up

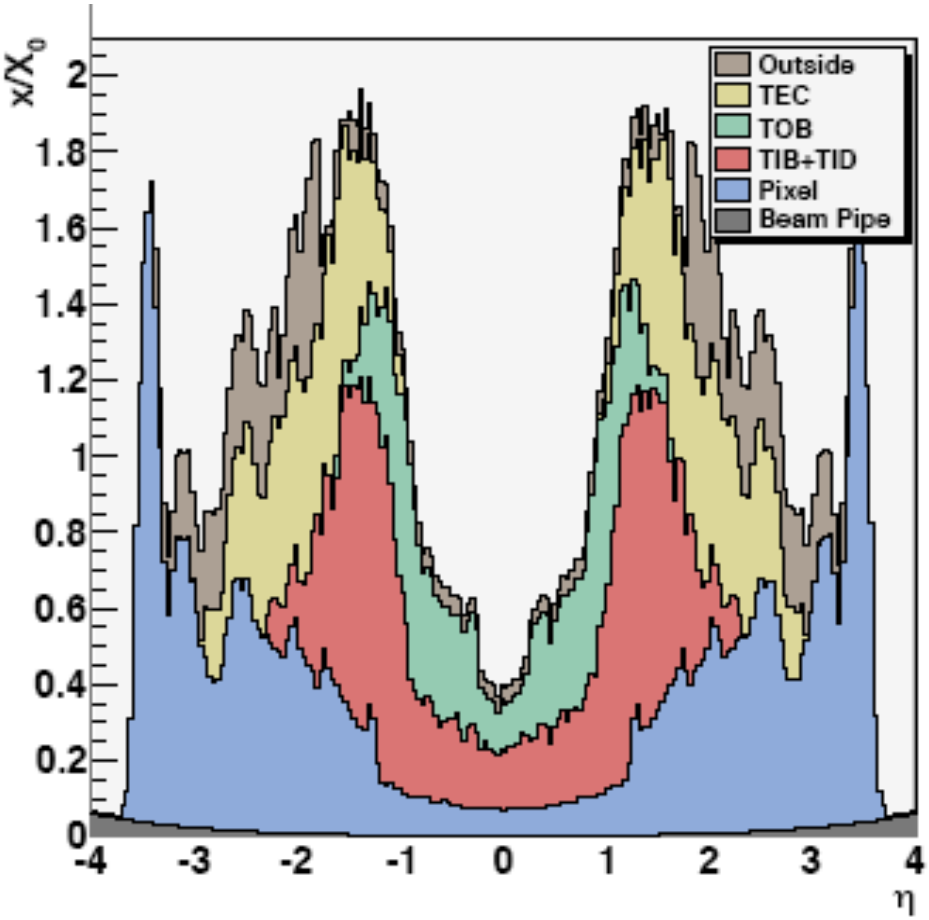
at ϵ_{uds} = 0.01

ϵ_b from 0.58 to 0.64

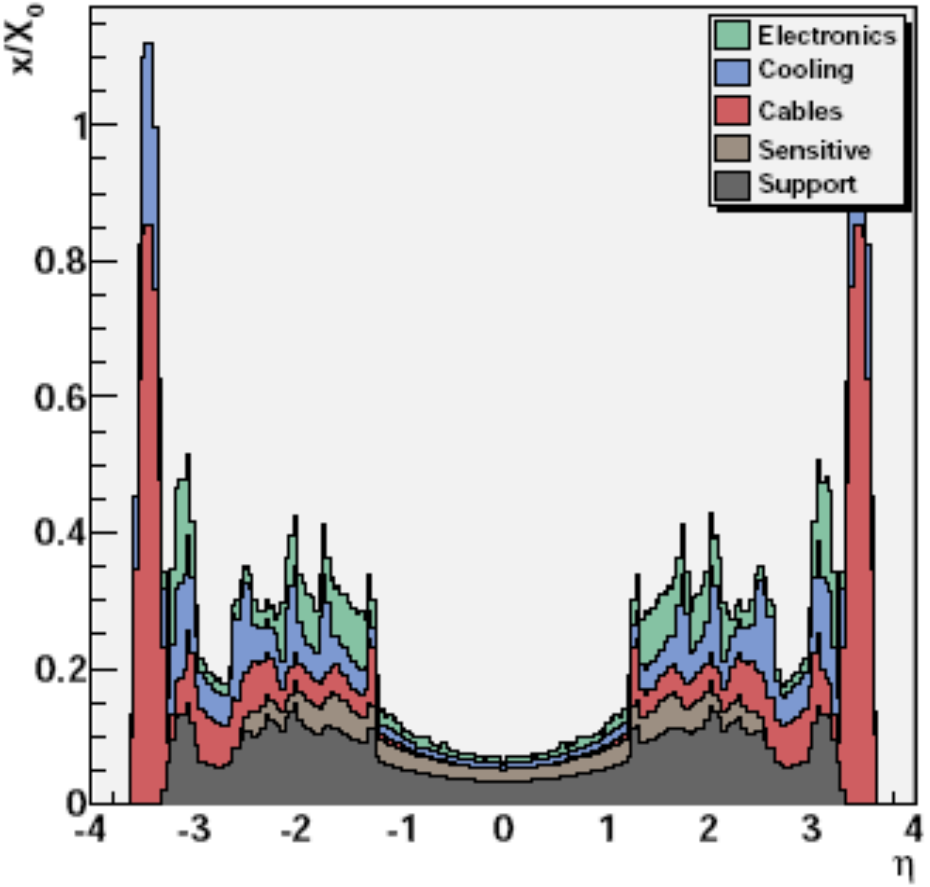
Alessia Tricomi
Tracker Upgrade Sep 2009
http://indico.cern.ch/conferenceDisplay.py?confId=47293

CMS tracker material

All trackers

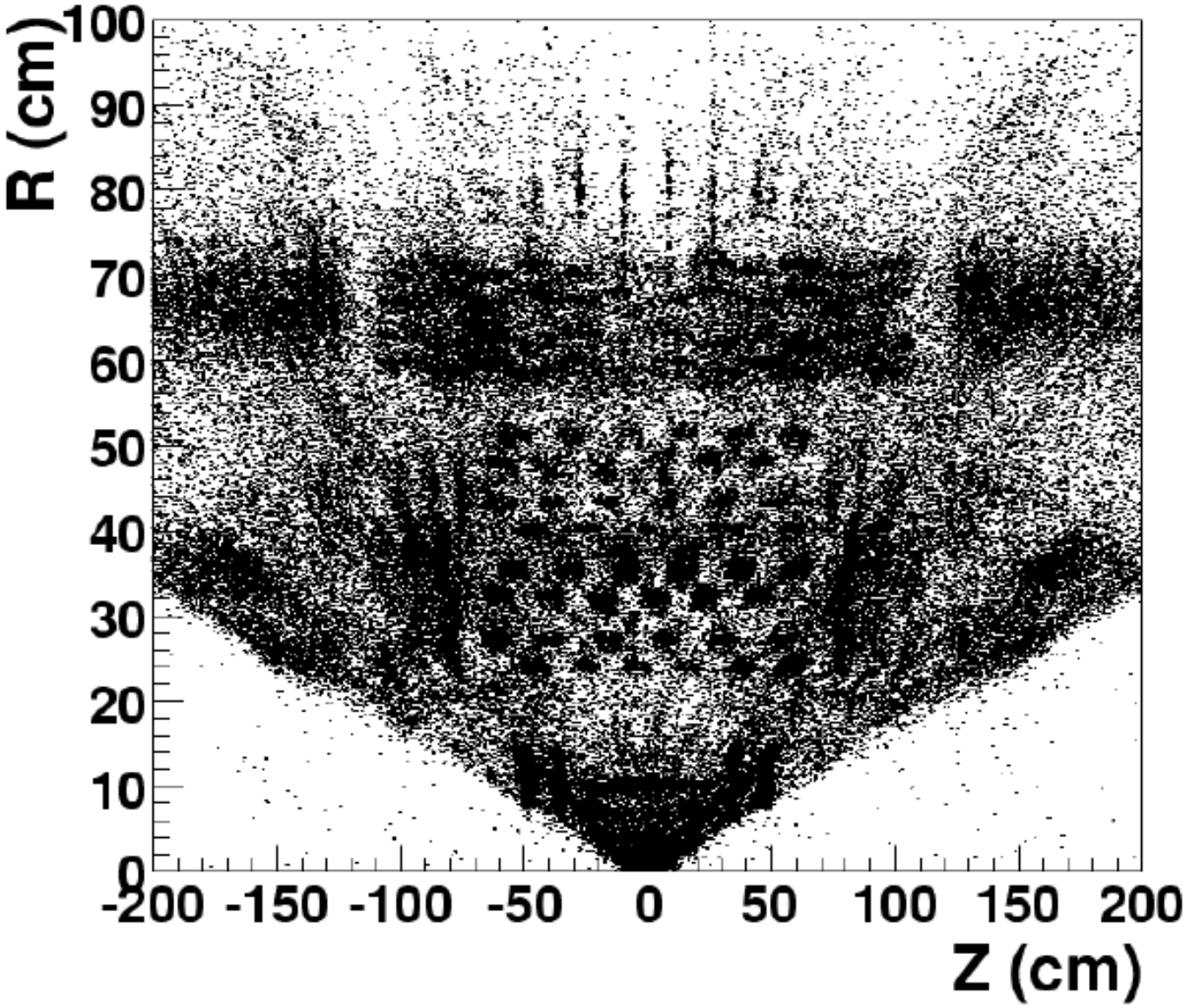


Barrel pixel



CMS Note 2009

reconstructed photon conversions (sim)



Nancy Marinelli, http://arxiv.org/abs/0710.2818v1

Tracking efficiency

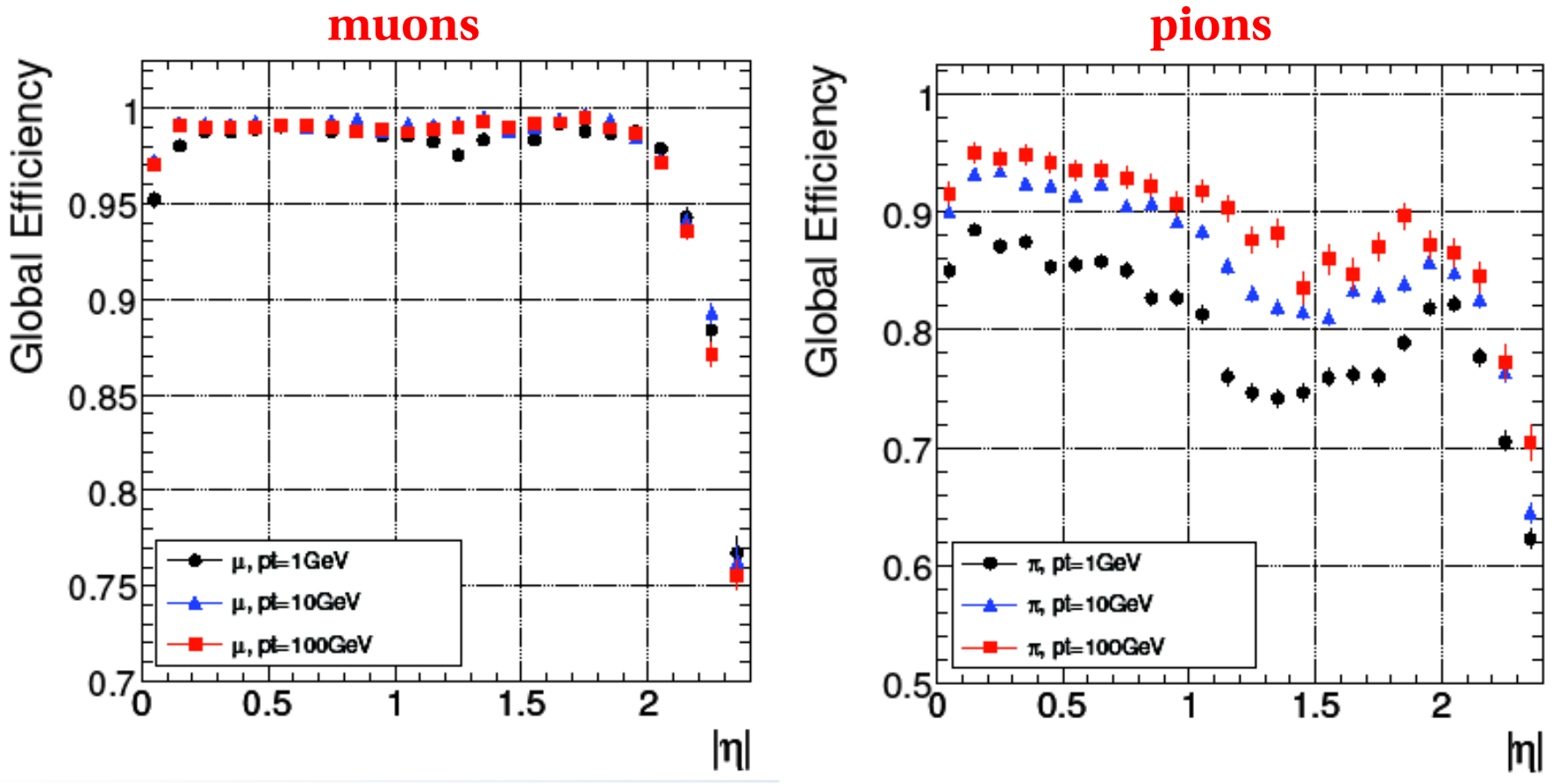
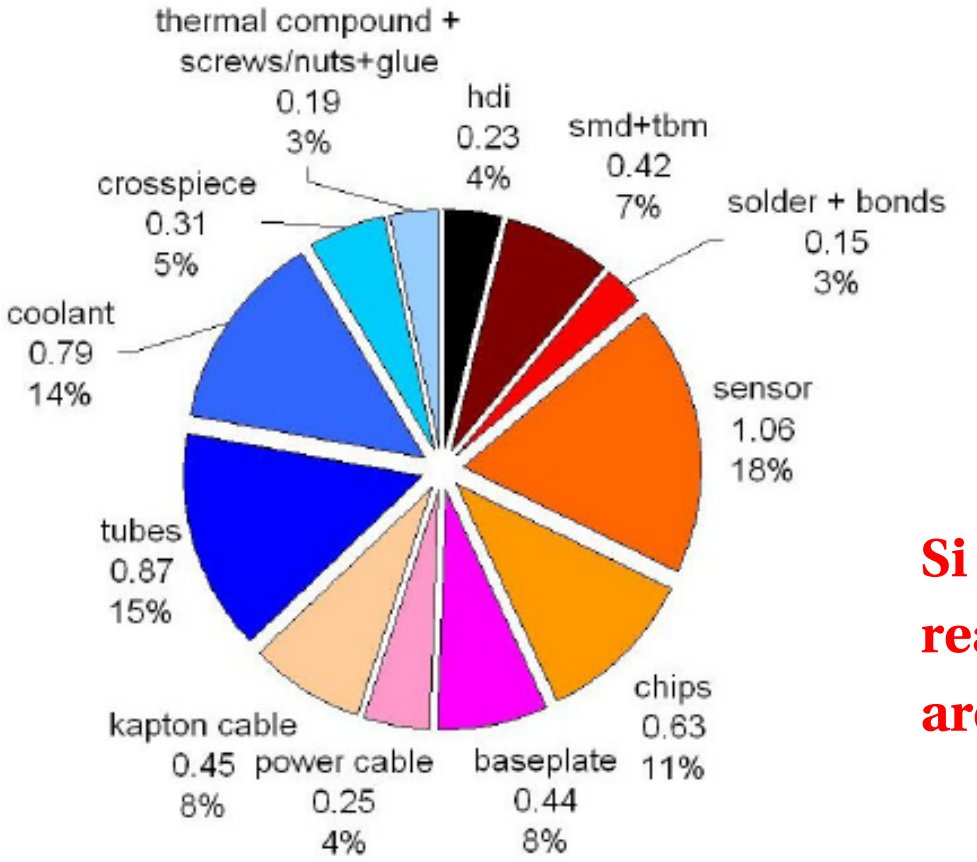


Figure 3: Track reconstruction efficiency for single muons and single pions [5]. Material interactions reduce the efficiency even for high momentum pions.

Alice Bean et al.: R&D for inner pixel layers
http://cmsdoc.cern.ch/Tracker/Tracker2005/TKSLHC/Bean_proposal_0208.pdf

Material budget for 3 pixel layers at $\eta = 0$

Cooling is largest contribution

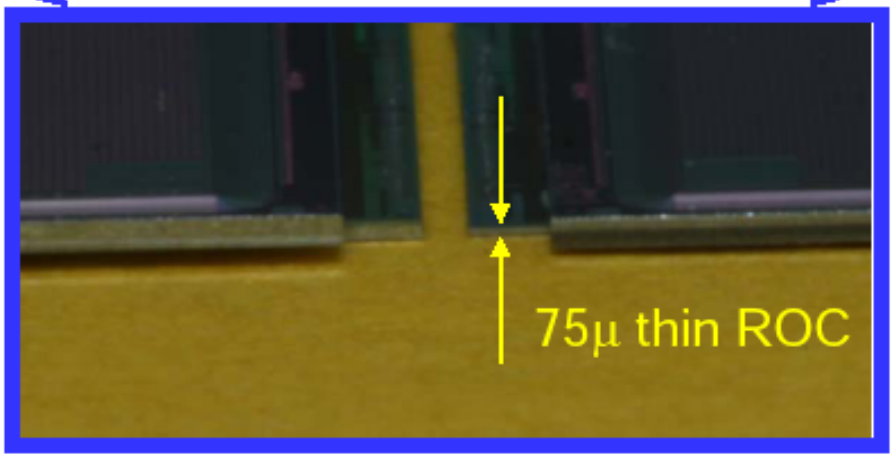


Si sensor and readout chip are 2nd largest

5.8% X_0 for 3 pixel layers

Roland Horisberger
4th CMS SLHC workshop Perugia Apr 2006
http://indico.cern.ch/conferenceDisplay.py?confId=a06865

CMS pixel upgrade material reduction



R. Horisberger
Jun '09

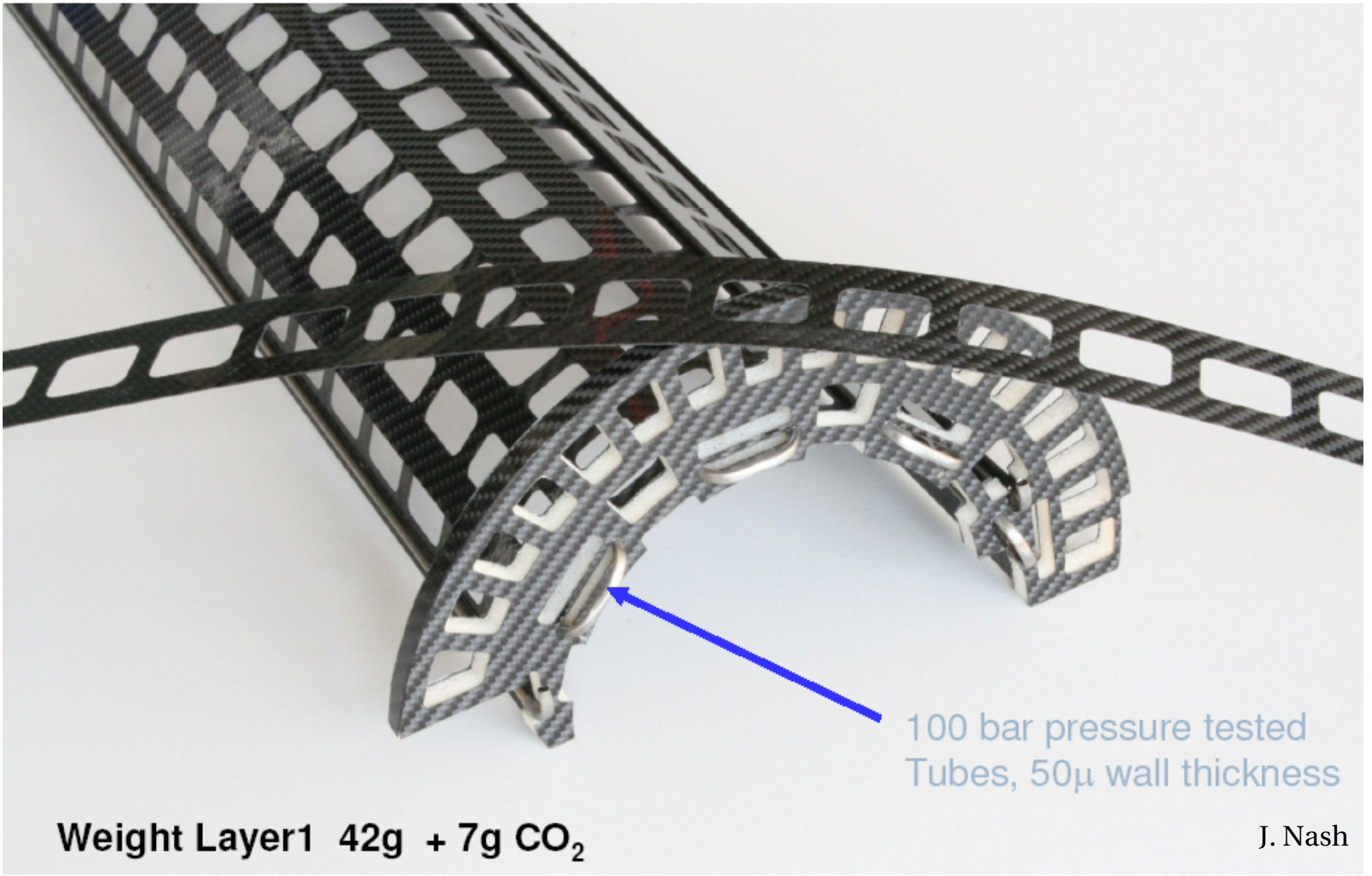
Sensor 225µ thick

Future bare module

weight = 0.89 gr

→ 65% of present

CMS pixel upgrade thin carbon fiber support

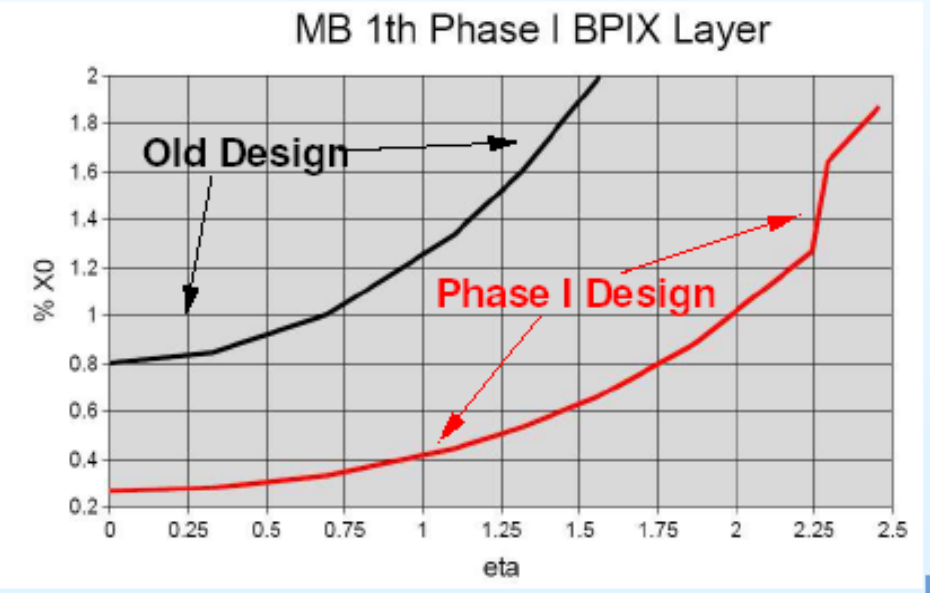


CMS pixel upgrade material reduction

Layer 1 prototype:

- 200 μm carbon fiber
- 4 mm Airex foam
- stainless steel tubes:
  - 1.5 mm OD, 50 μm wall
- tube bends:
  - 1.8 mm OD, 100 μm wall

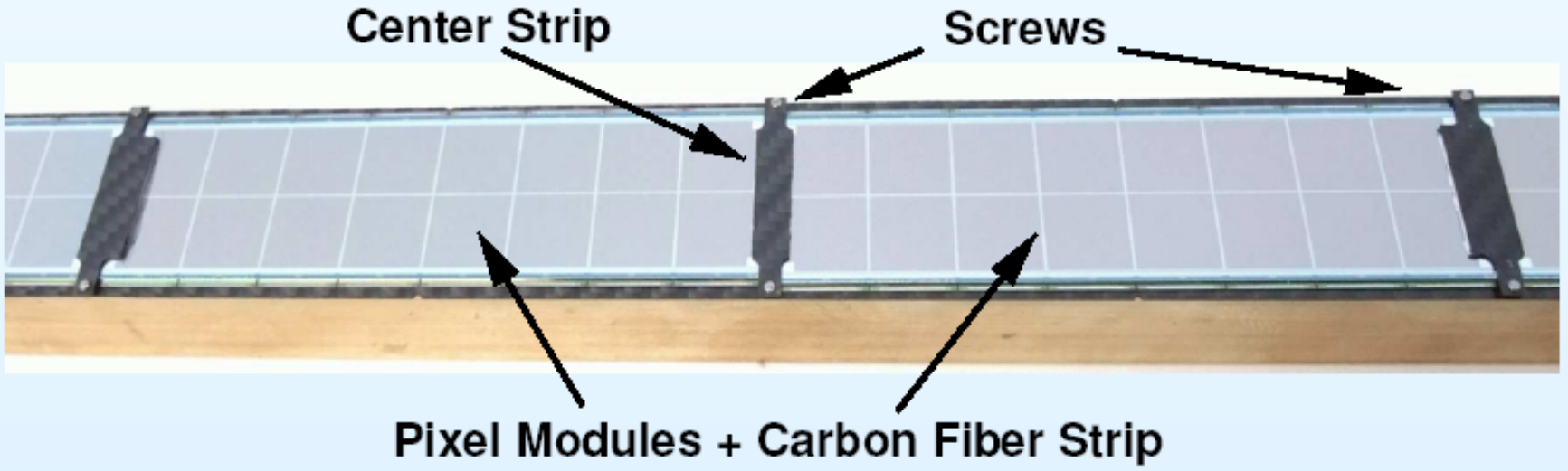
tested: ~100 bar & -10 °C..10 °C



S. König

CMS pixel upgrade

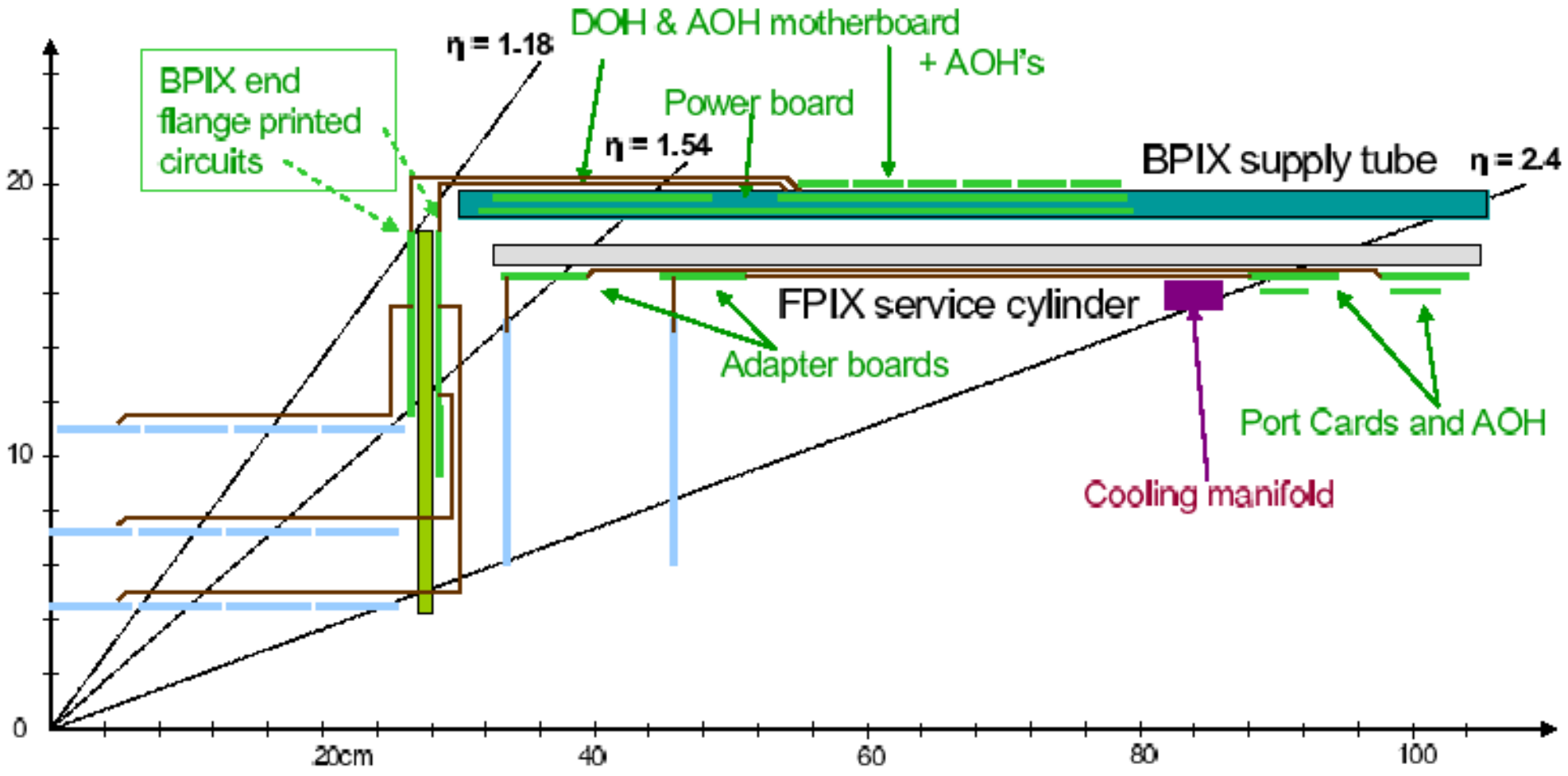
- carbon fiber strips glued to module
- screwed to structure
- one strip for each module + one at $\eta=0$
- MB ~51% of current fixation



S. König

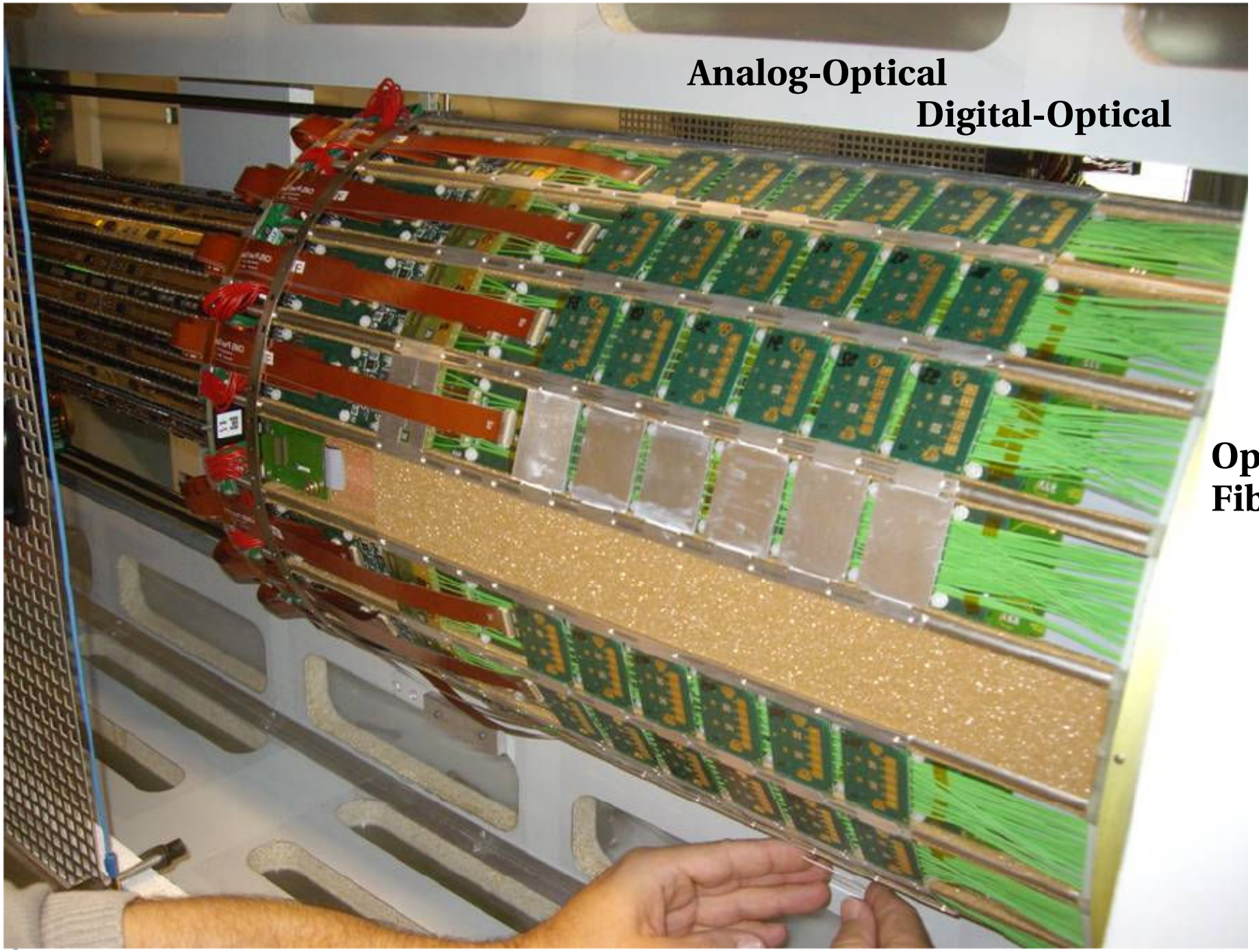
Present CMS Pixel mechanics

Digital and Analog Optical Hybrids presently inside the strip end cap tracker volume



W. Erdmann

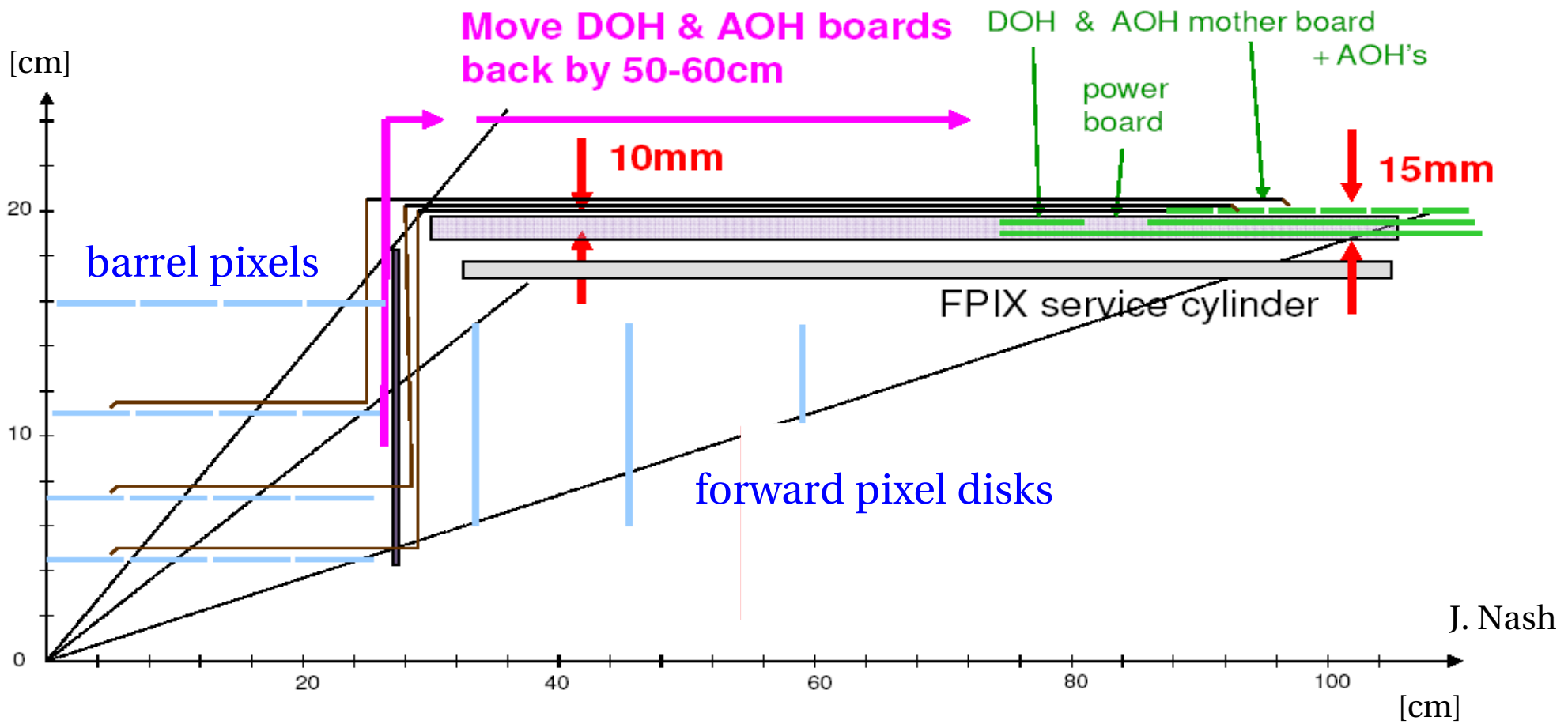
CMS Pixel services



J. Nash

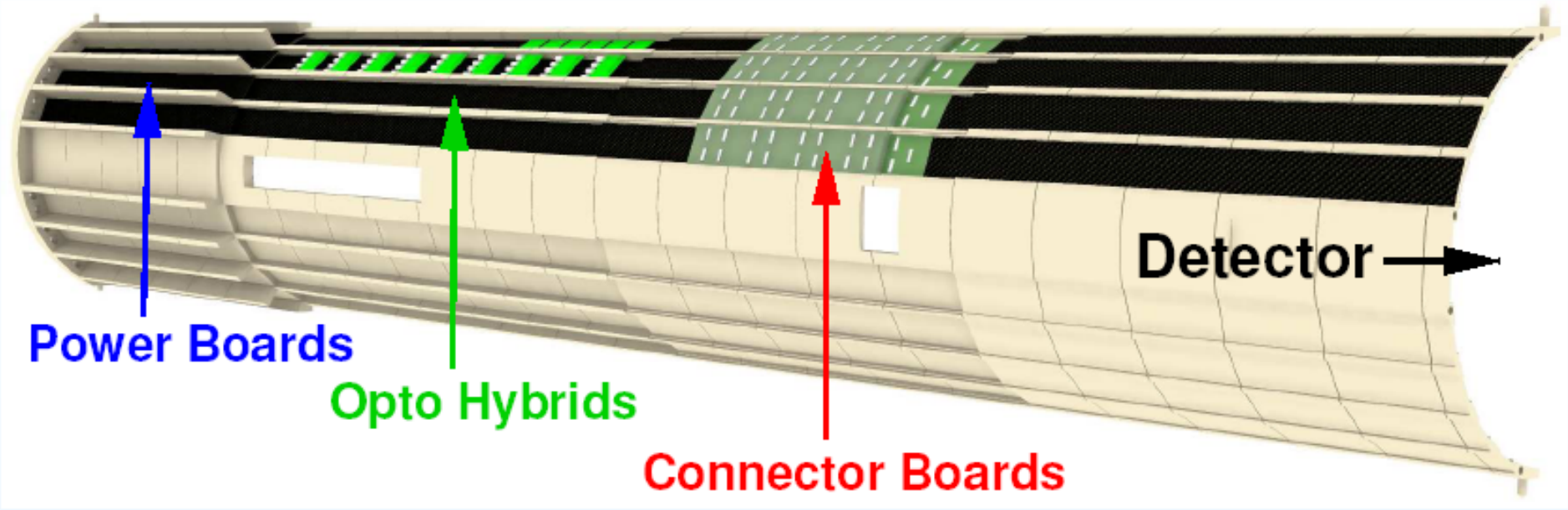
CMS pixel upgrade

Move Digital and Analog Optical Hybrids out of the strip end cap tracker volume.
Requires longer internal cables: micro twisted pairs.



J. Nash

CMS pixel upgrade: new BPIX supply tube



Layout:

- very low mass cable trenches
- module connectors:
  - layer 3+4 outside
  - layer 1+2 inside
- new opto hybrids
- 2:1 DC:DC converters

Under development at PSI

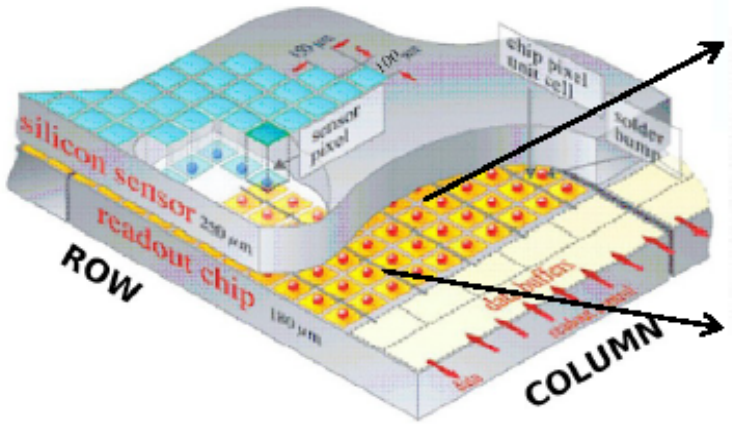
RWTH Aachen

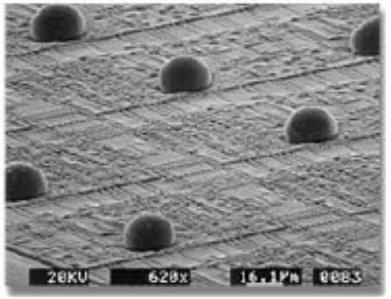
S. König

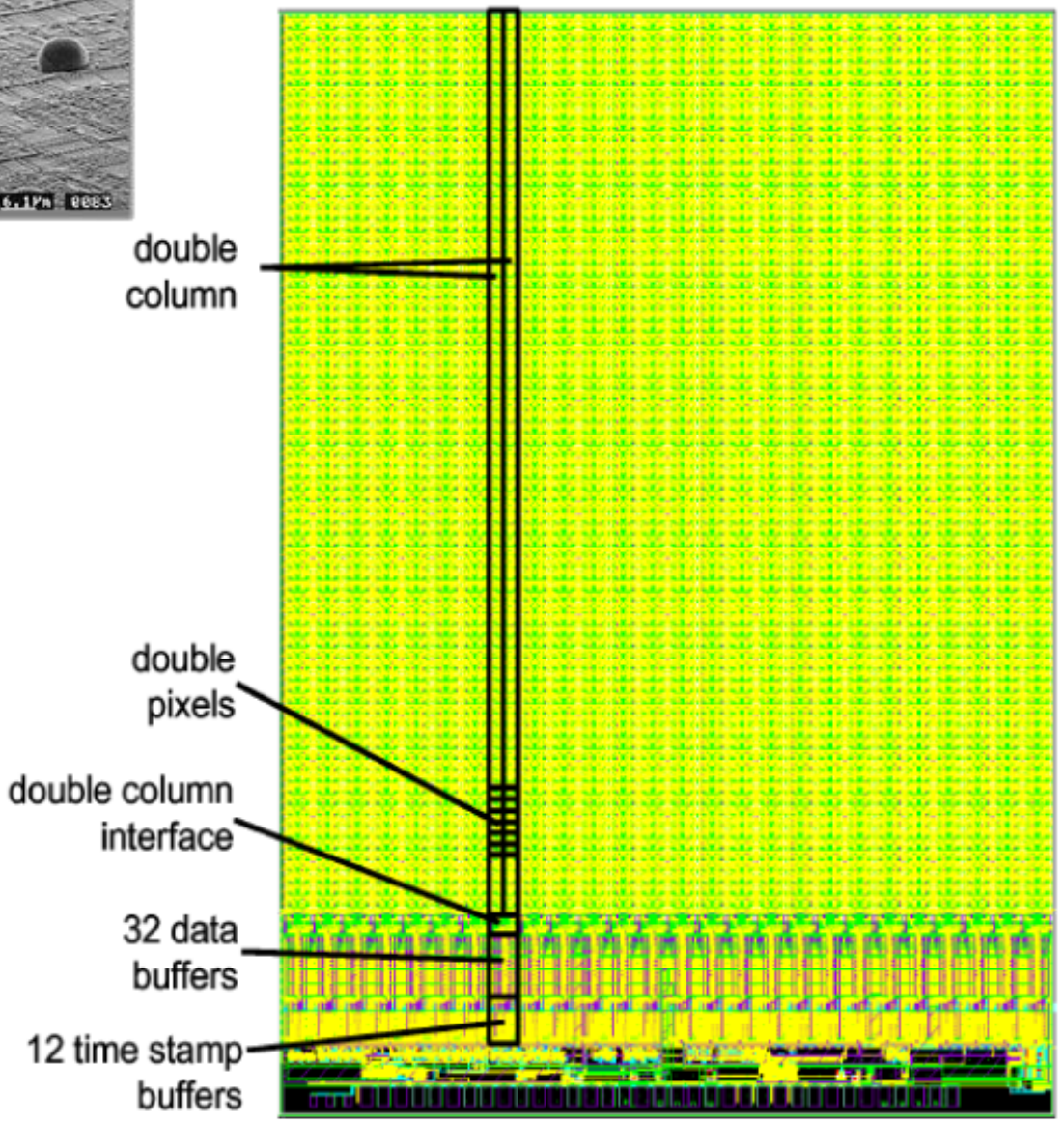
LHC tracking environment

- ~50 inelastic collisions per bunch crossing at $\mathscr{L} = 2.5 \cdot 10^{34}/\mathrm{cm}^2/\mathrm{s}$.
- $\mathrm{dN_{ch}}$ / $\mathrm{d}\eta$ ~ 6, flat within ±2.5 at 14 TeV.
- Factor 2 for loopers and secondary interactions
  - 3000 tracks / BC
- Pixel layer at R = 4 cm: $A = 2\pi RL \sim 1250\ \mathrm{cm}^2$
  - 100 MHz / cm^2, up to 250 MHz / cm^2 within $|\eta| < 1$
- Pixel size: $0.1 \times 0.15\ \mathrm{mm}^2$:
  - Pixel occupancy up to 0.001 per BC
  - Double column occupancy (160 pixels) up to 0.15 per BC
  - L1 trigger after 3.2 µs: need to store up to 17 tracks / double column
- Fluctuations and uncertainties on all particle rates.

CMS Pixel Chip







- ReadOut Chip (ROC) bump bonded sensor pixels.

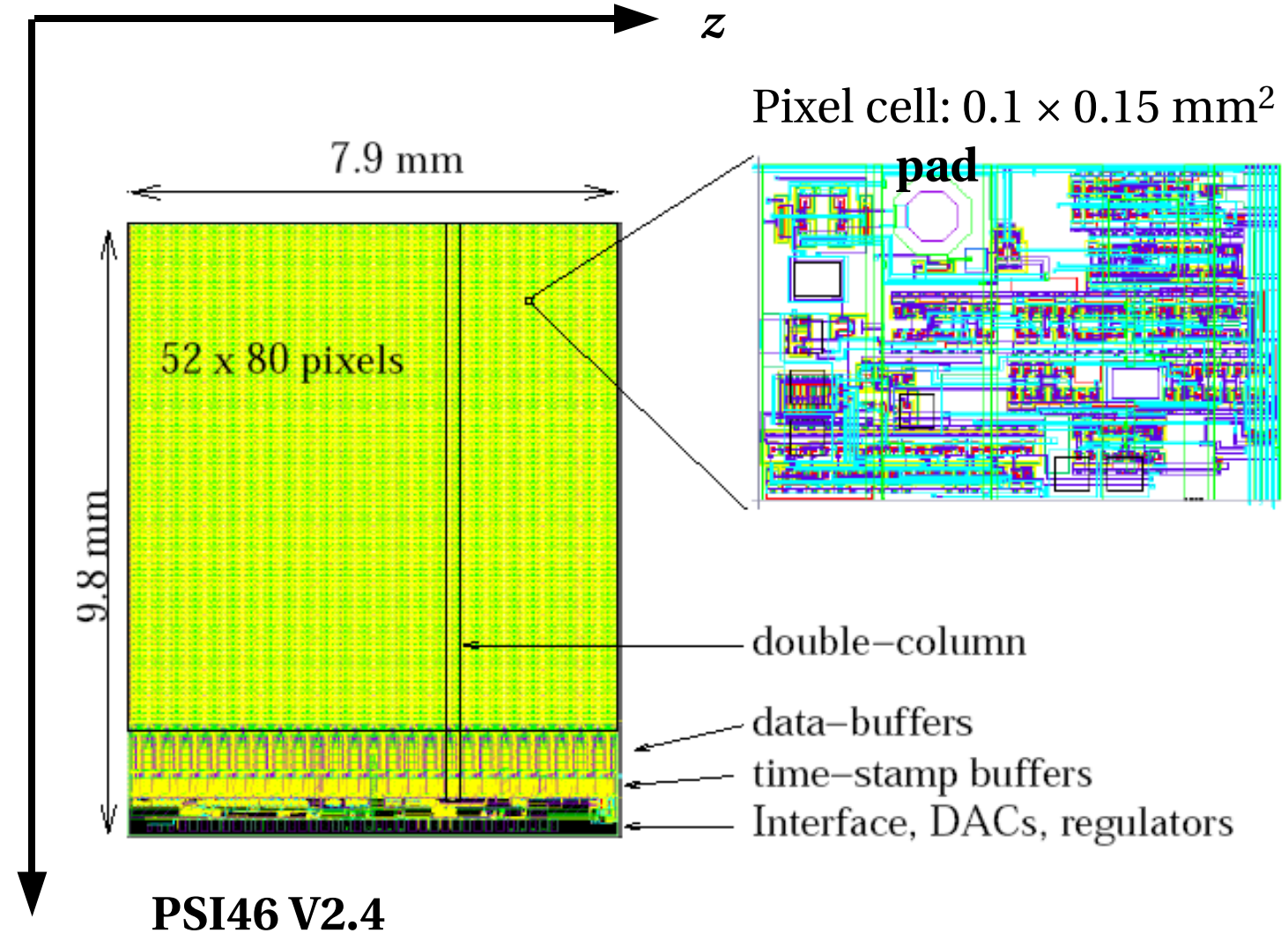
- 52 80 = 4160 pixels per ROC
- 15,840 ROCs
- 66 million pixels

- Automatic zero-suppression

- Each pixel has a programmable threshold (adjusting this is called *trimming*)

S. Das

CMS Pixel Chip



V_A = 1.5 V

V_D = 2.5 V

29 µW / pixel

0.12 W / chip

PSI46 V2.4

0.25 µm CMOS IBM proces

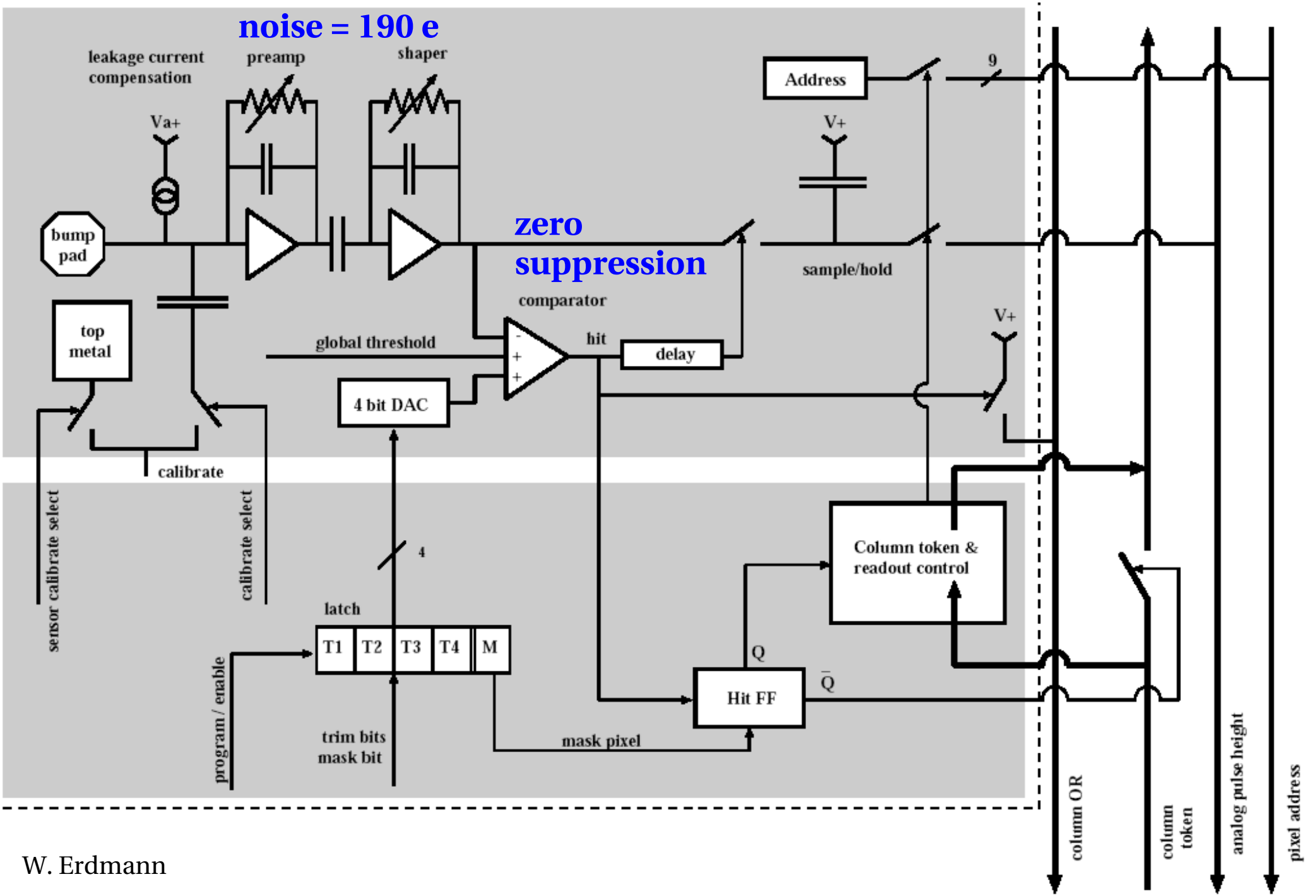
radiation hard design

1.3 M transistors

operational after 130 kGy γ irradiation

W. Erdmann

CMS Pixel cell



W. Erdmann

CMS Pixel readout

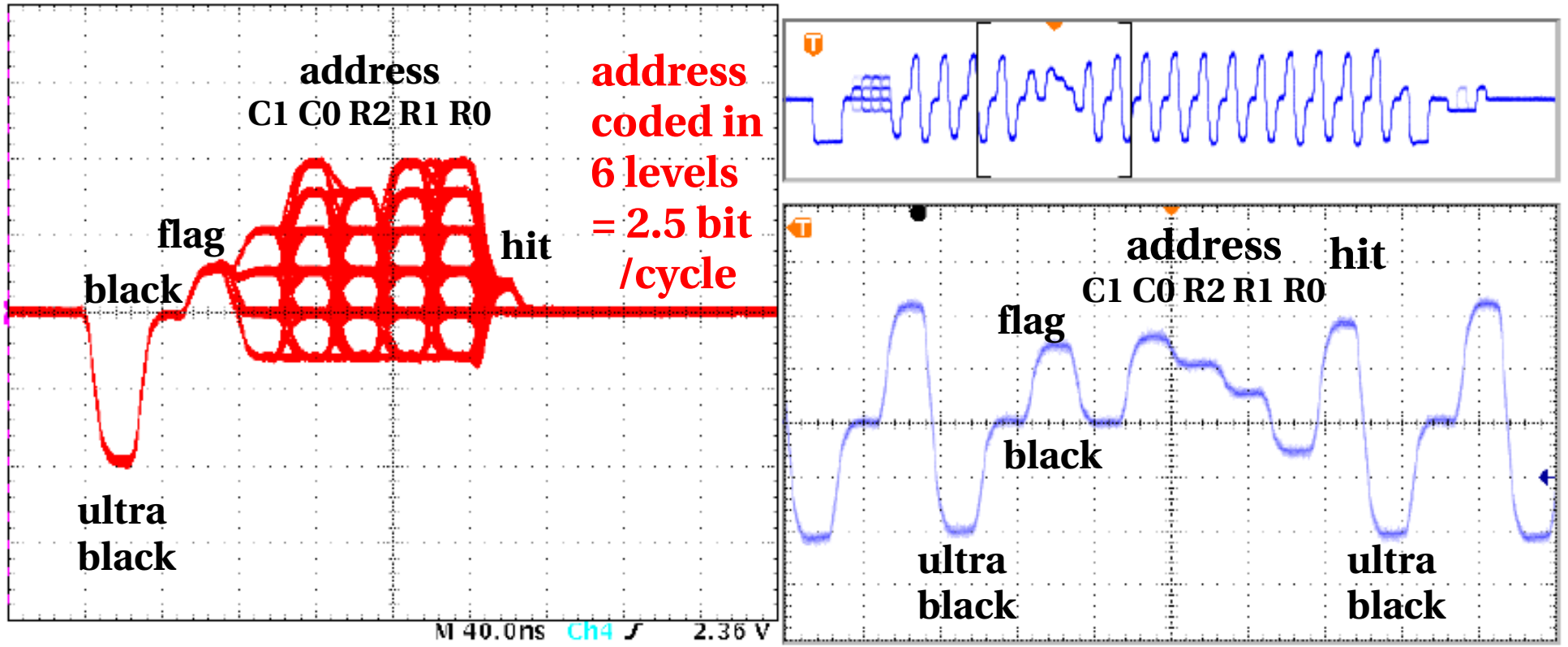
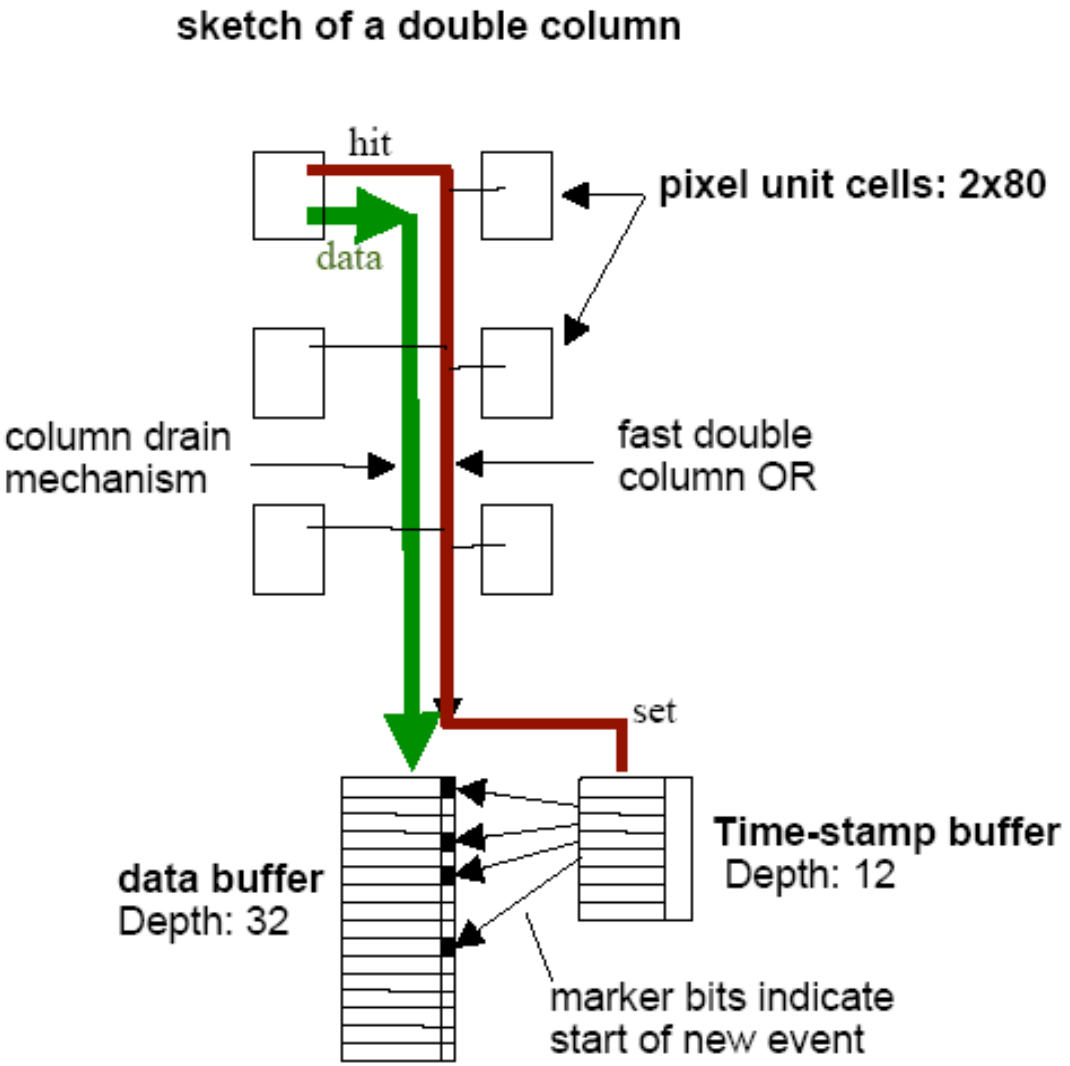


Fig. 1.8. An "Eye diagram" of the readout of a single chip with one pixel hit is shown on the left side. The horizontal axis is time, the vertical axis shows the amplitude of the chip output. All possible pixel positions are scanned and the oscilloscope traces superimposed. The first three 25 ns cycles are the chip header. It is always the same. The following five cycles encode the column and row of the pixel. The last cycle represents the pulse-height, which is constant in this case. The figure on the right shows the readout of a barrel module with a TBM and 16 chips. The TBM header contains an event counter. The fifth chip has one hit, the corresponding section is shown enlarged at the bottom.

W. Erdmann

Pixel double column readout



- Zero suppression in pixel cell
- Pixel hit information transferred to time stamp and data buffer
- Kept there during L1 trigger latency
- Double column stops data aquisition when confirmed L1 trigger ⇨ dead time starts
- Double column resets after readout ⇨loosing history (trigger latency)
- Serial readout: 8 (16) ROCs daisy chained. Controlled through readout token

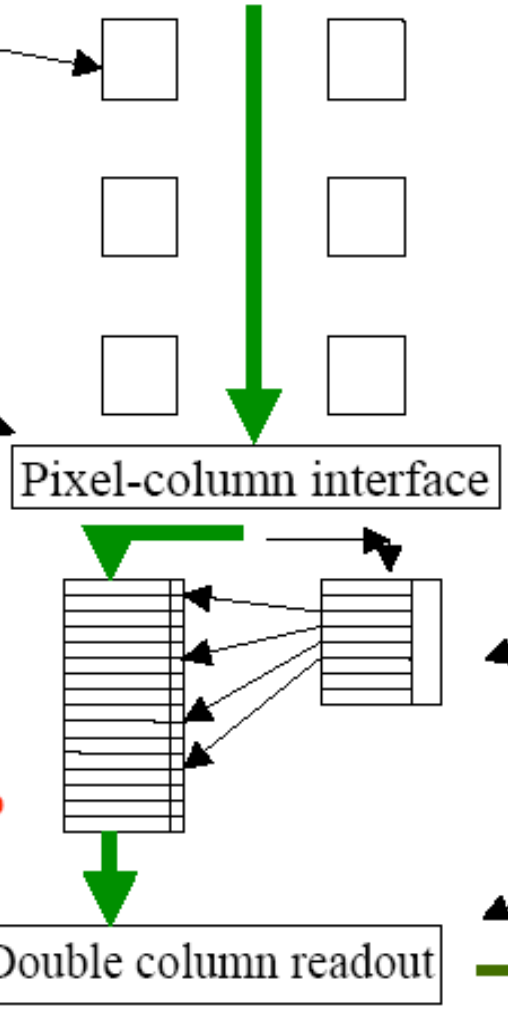
H.C. Kaestli, CMS Tracker upgrade workshop Feb 2007
http://indico.cern.ch/conferenceDisplay.py?confId=12094

Data loss mechanisms

Present PSI46 readout chip simulated at LHC design luminosity

Pixel busy:
0.04% / 0.08% / 0.21%
pixel insensitiv until hit transferred to data buffer (column drain mechanism)

Double column busy:
0.004% / 0.02% / 0.25%
Column drain transfers hits from pixel to data buffer. Maximum 3 pending column drains requests accepted



Timestamp Buffer full:
0 / 0.001% / 0.17%

Data Buffer full:
0.07% / 0.08% / 0.17%

Readout and double column reset:
0.7% / 1% / 3.0%
for 100kHz L1 trigger rate

- 1xLHC: $10^{34}cm^{-2}s^{-1}$
- 11 cm / 7 cm / 4 cm layer
- total data loss @ 100kHz L1A:
  - 0.8%
  - 1.2%
  - 3.8%

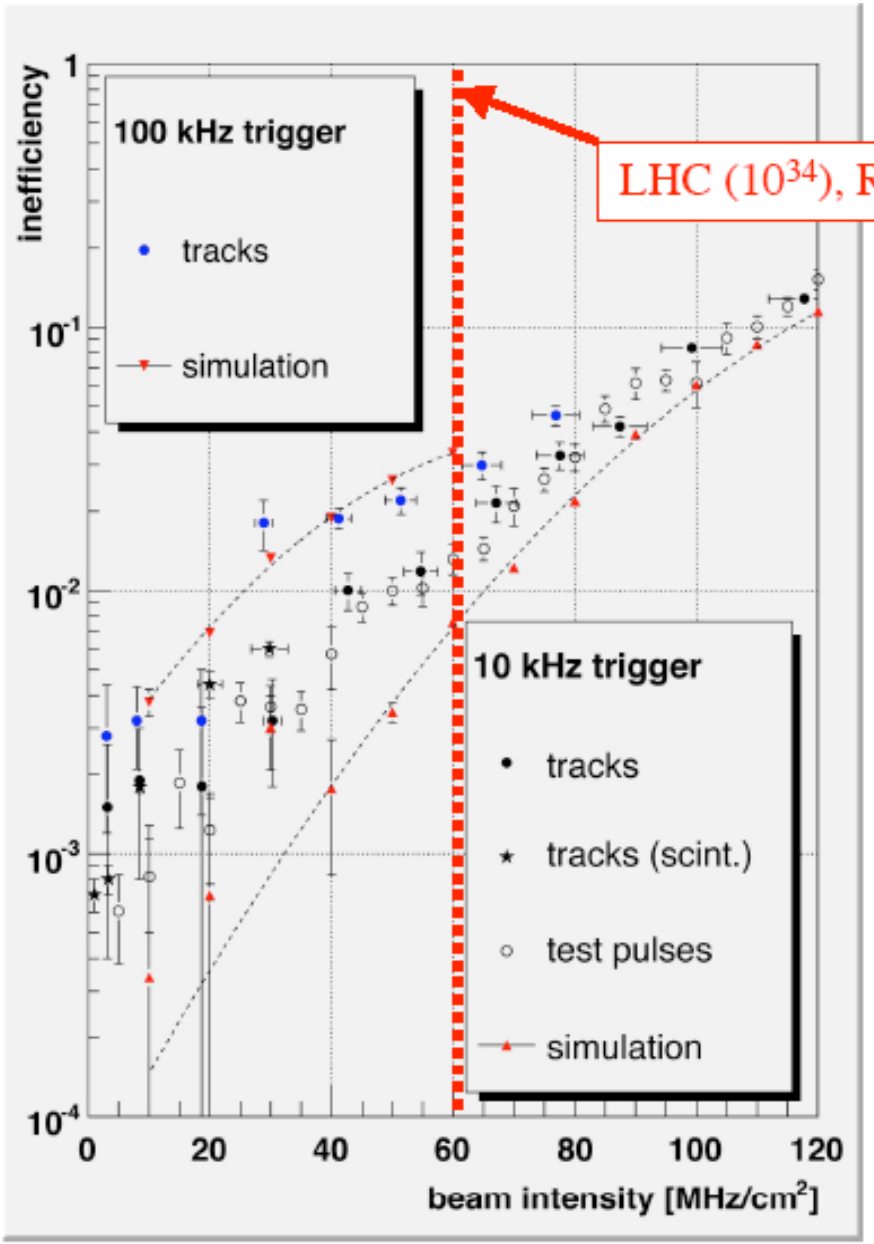
H.C. Kaestli, CMS Tracker upgrade workshop Feb 2007
http://indico.cern.ch/conferenceDisplay.py?confId=12094

High rate PSI beam test: pions

Measured inefficiency

- Plot shows
  - Test beam simulation
  - Beam measurements with tracks and with the scintillator (at low intensities)
  - Measurements with calibration pulse injection on top of beam induced activity
- Very good agreement at 100kHz L1A. Readout losses dominate here.
- For 10kHz L1A fairly well agreement. Slightly higher inefficiencies in data. Sensor losses not simulated

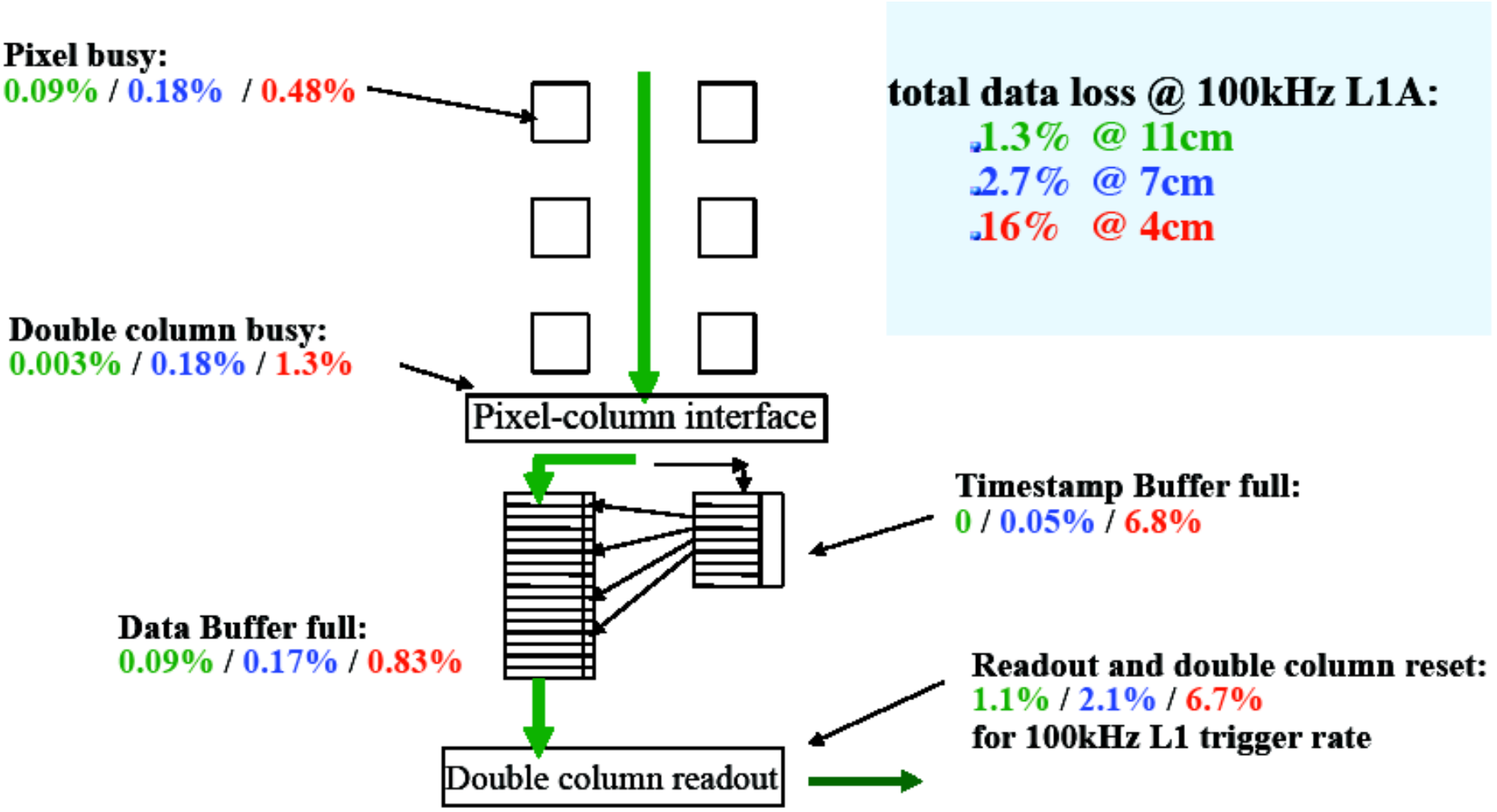
➔ **Data loss well understood**



H.C. Kaestli, CMS Tracker upgrade workshop Feb 2007
http://indico.cern.ch/conferenceDisplay.py?confId=12094

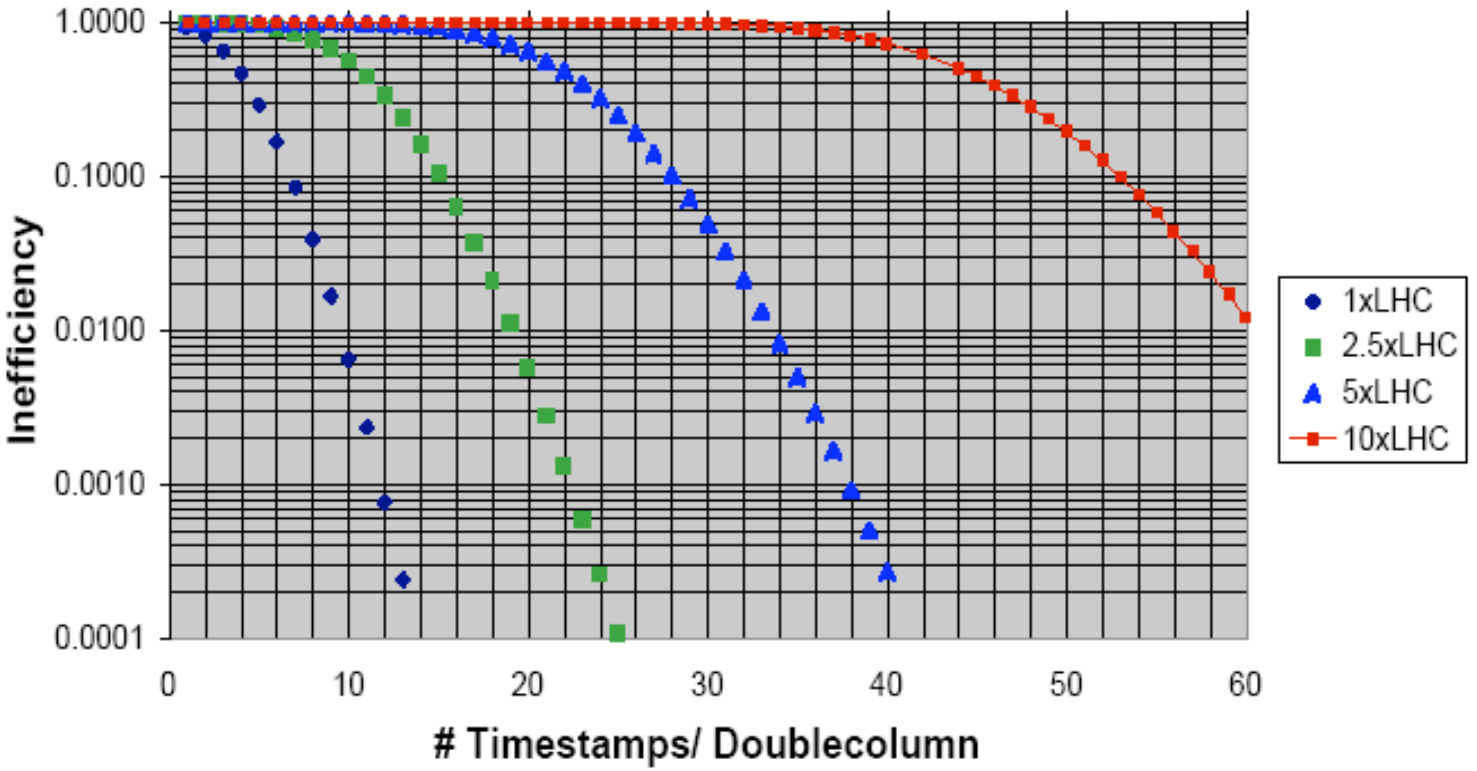
Data loss mechanisms

Present PSI46 readout chip simulated at 2× LHC design luminosity



H.C. Kaestli, Pixel upgrade meeting Oct 2008
http://indico.cern.ch/conferenceDisplay.py?confId=41745

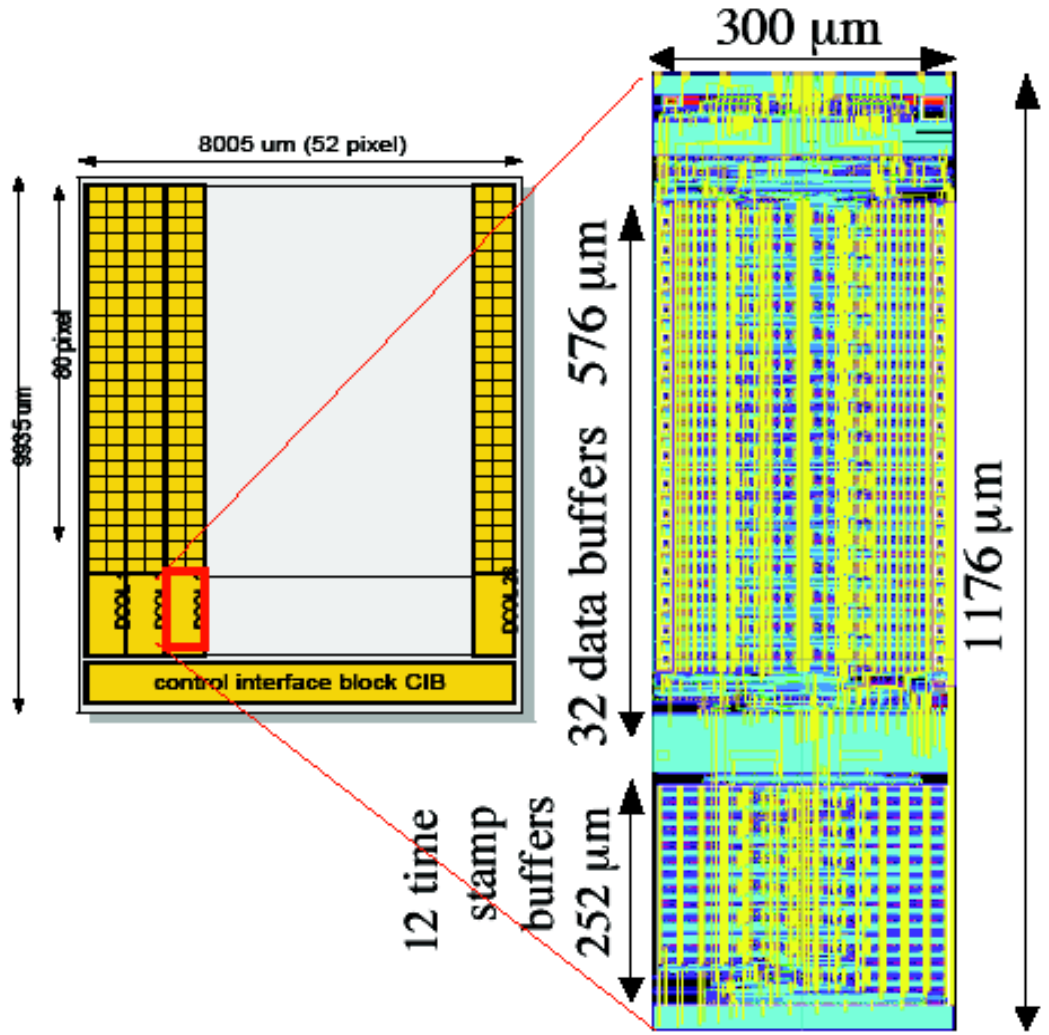
Influence of buffer size at R = 4 cm



- Present system: 12 time stamp buffers, 32 data buffers. Average pixel multiplicity:2.2
- Possible extension: doubling the buffer size (24/64). Enough for < $2.5 \times 10^{34} cm^{-2} s^{-1}$
- For 10×10^{34} need 60 timestamp buffers and 190 data buffers (average pixel multiplicity: 2.6).

H.C. Kaestli, CMS Tracker upgrade workshop Feb 2007
http://indico.cern.ch/conferenceDisplay.py?confId=12094

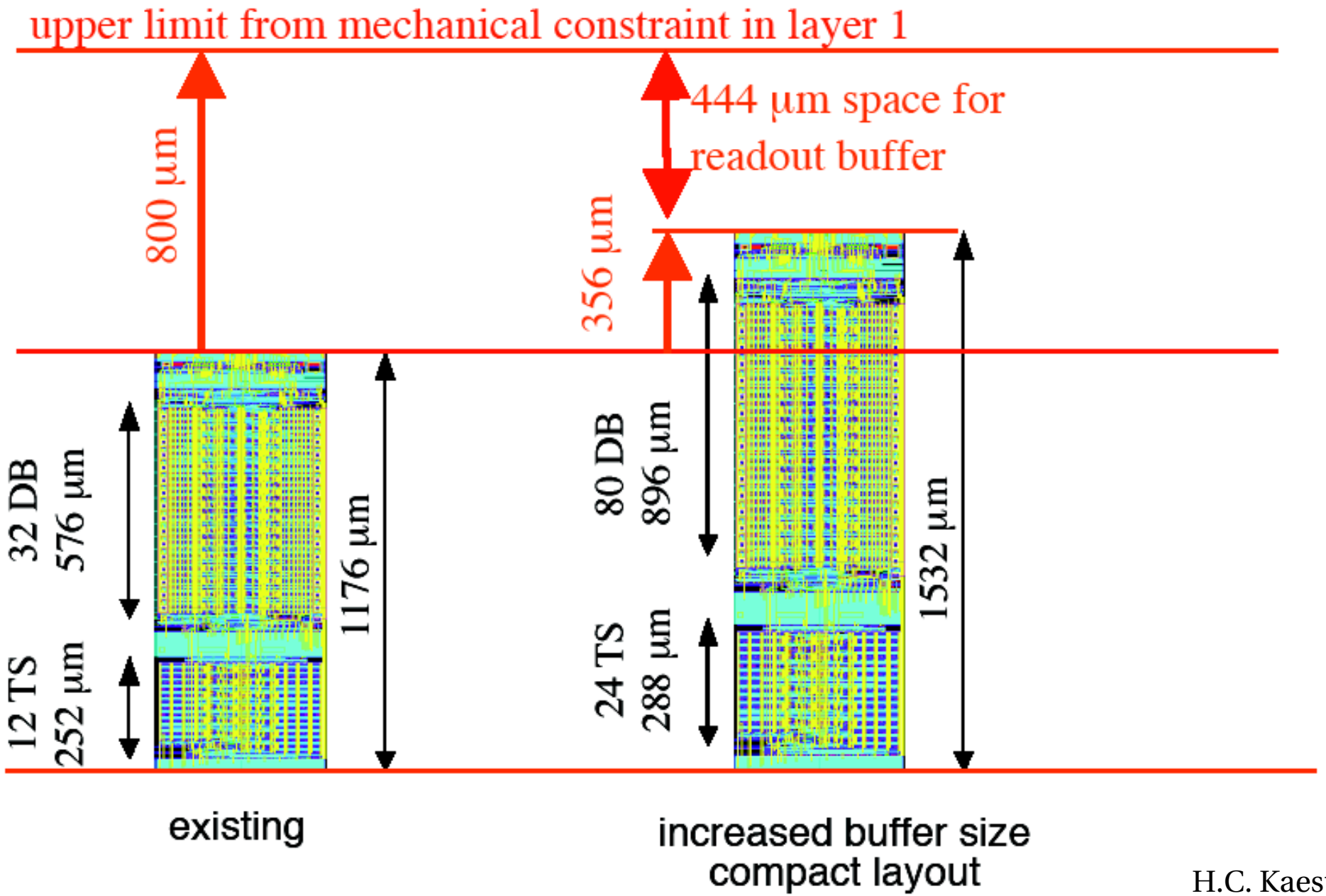
Enlarged L1 buffer



- **Dominant data loss mechanism → larger buffers needed**
- Data loss simulations performed
  - Data buffer from 32 to 80 cells
  - Timestamp buffer from12 to 24 cells
- Simple scaling would increase ROC size by >1.1mm
- 800 µm more space allowed with new detector mechanics
  - → Need more compact buffer layout

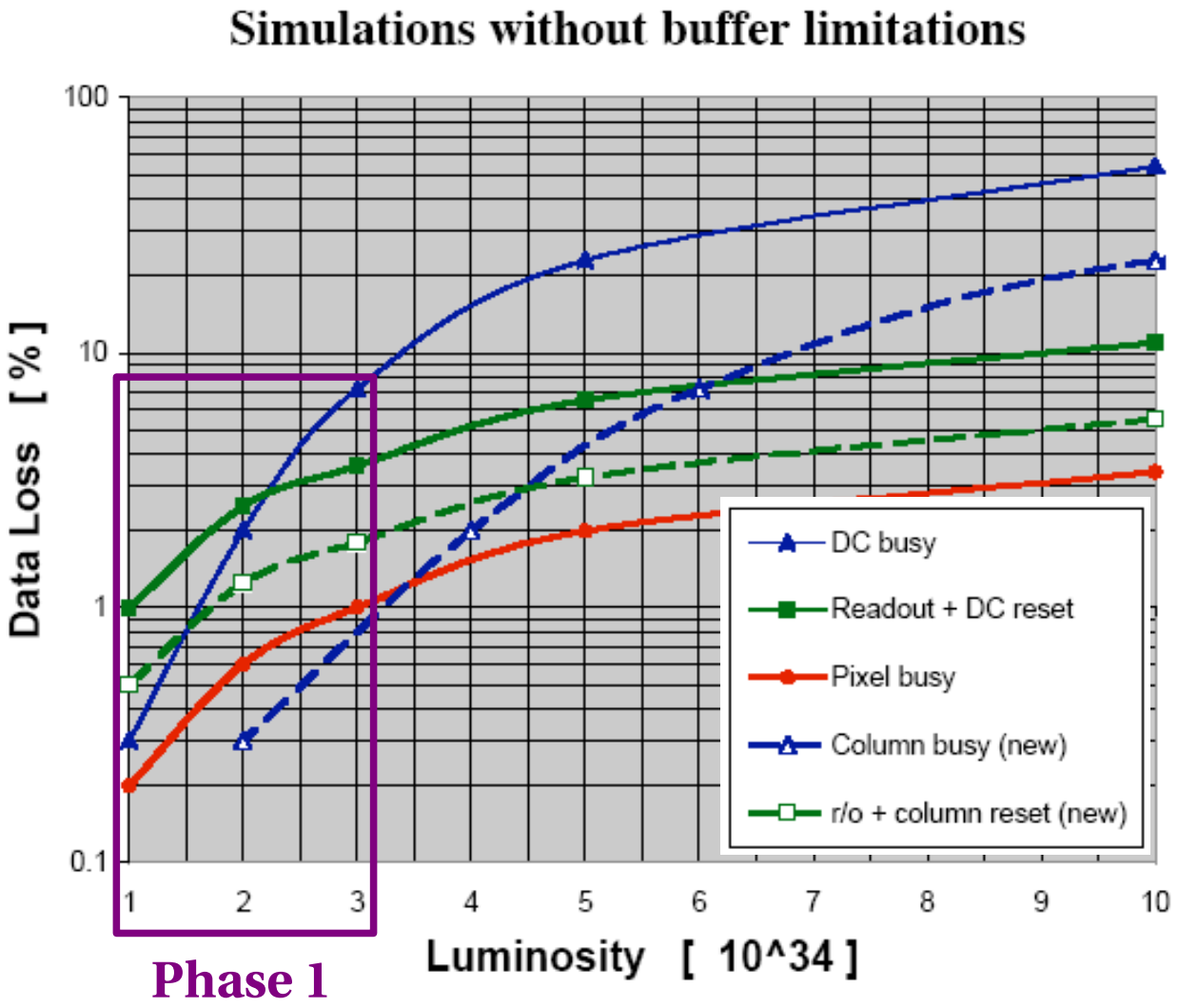
H.C. Kaestli
Oct 2009

redesigned double column interface



H.C. Kaestli
Oct 2009

further data loss mechanisms at R = 4 cm



- **Pixel busy never dominates → pixel size ok for all fluences. No need for smaller pixels.** Smaller pixels produce more data traffic, higher losses!
- Inefficiency < 7% up to $2{,}5 \times 10^{34} cm^{-2} s^{-1}$
- Dashed lines show inefficiencies in case of column drain per column, instead of double column (evetually possible in 0.25µm)
- Reaches 7% inefficiency at $4{,}5 \times 10^{34} cm^{-2} s^{-1}$

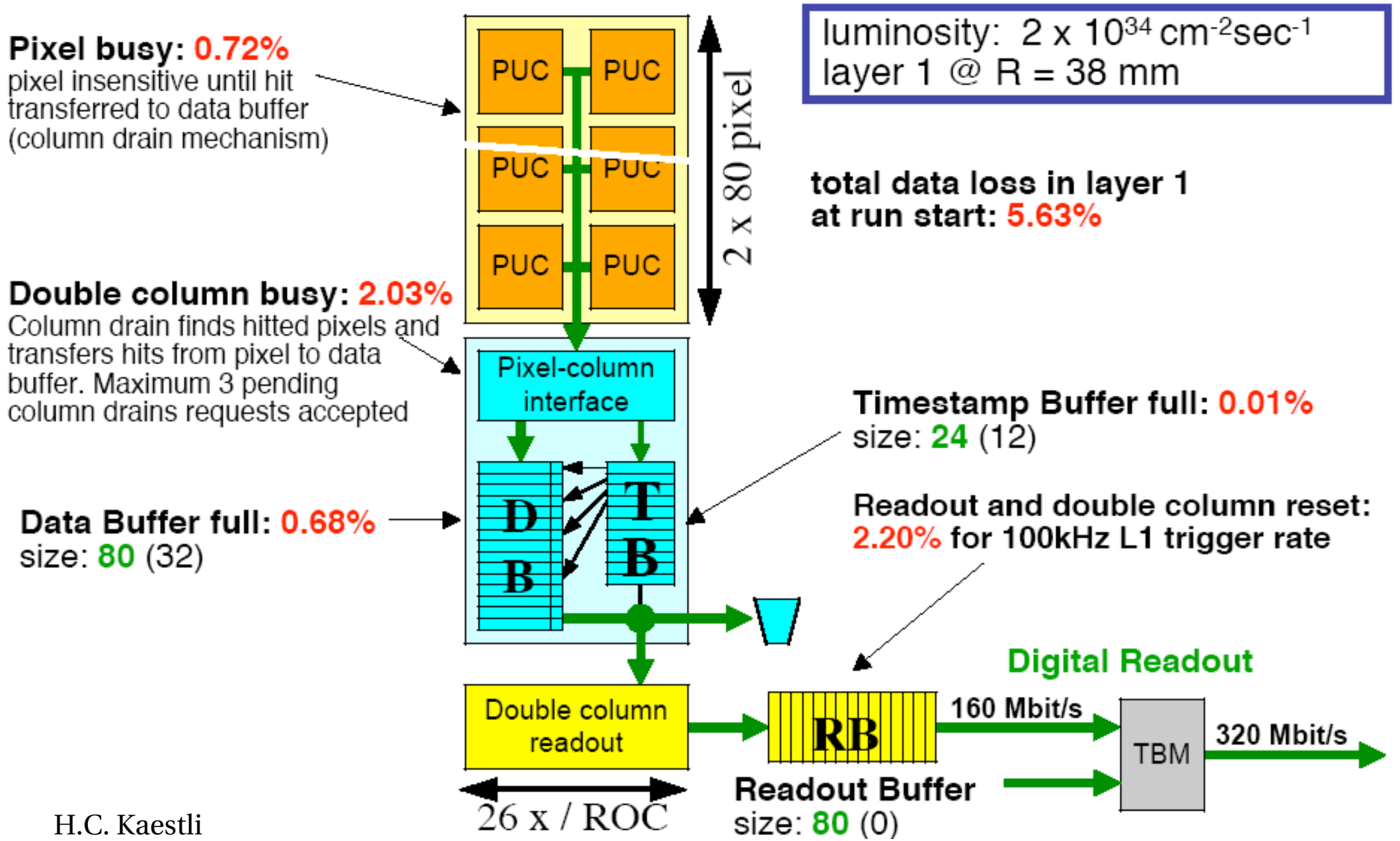
H.C. Kaestli, CMS Tracker upgrade workshop Feb 2007
http://indico.cern.ch/conferenceDisplay.py?confId=12094

Extra readout buffer stage

- With larger buffers leading inefficiency is waiting time for readout token
  - After L1A, double column stops until read out.
  - The waiting time for the r/o token can become long since the whole/half module (416/208 double columns) is daisy chained
- Solution: add ROC internal readout buffer.
  - ROC generates internal r/o token from trigger
  - Immediate digitization and transfer into r/o buffer
  - Double column resumes data taking
  - Hits wait in r/o buffer for module r/o token
- Further benefit: equalizes data fluctuations, can make better use of bandwidth
- Would leave double column logic exactly as today
  - Modification on ROC level only
  - Purely digital, 40MHz synchronous logic
- Need 23 bits x 80-100 words (size not critical, depends on space constraints)
- Design not yet started

H.C. Kaestli
Oct 2009

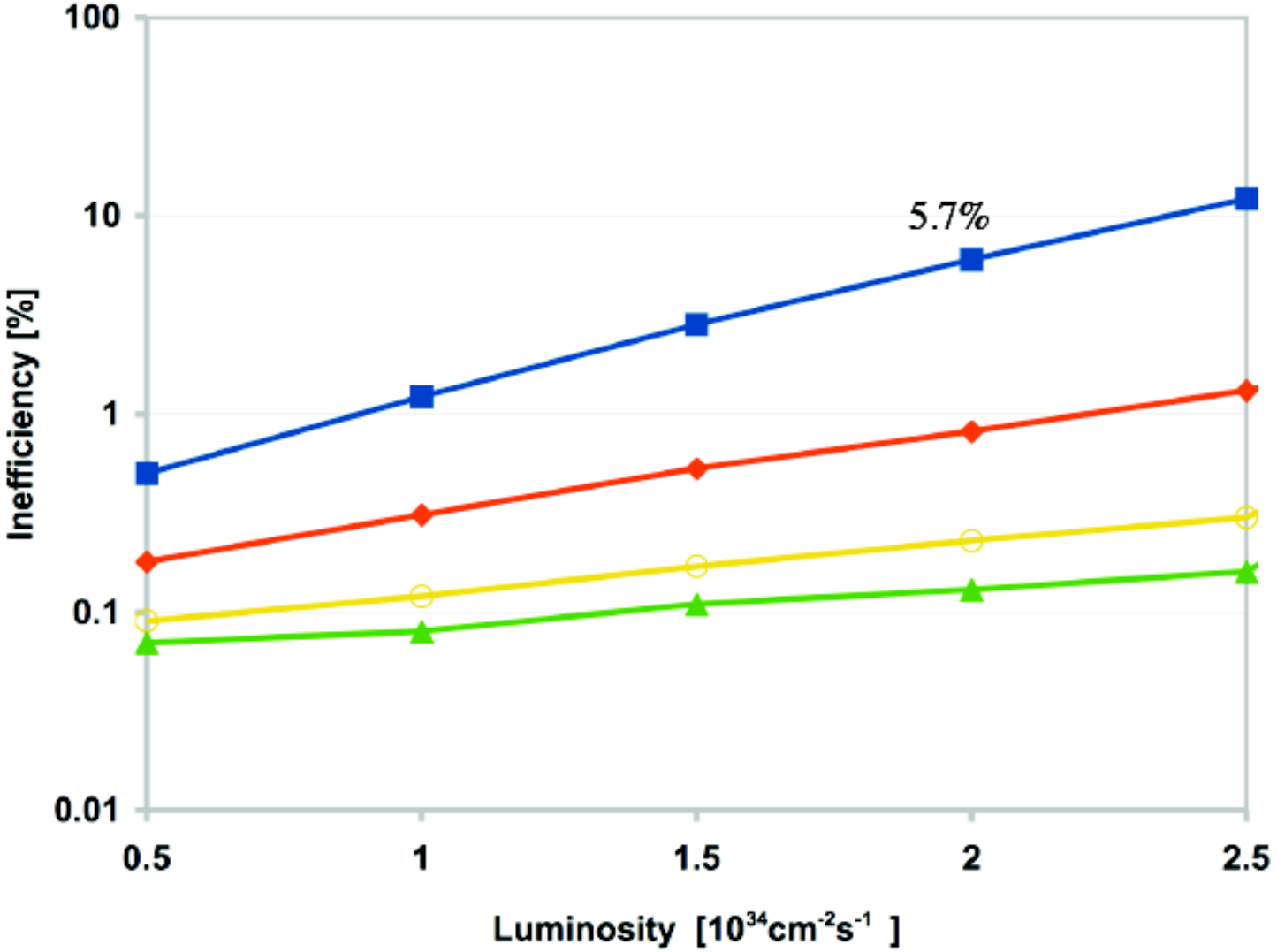
Data loss mechanisms



H.C. Kaestli
Oct 2009

Data loss vs luminosity

Pixel readout chip simulation with increased buffering



Factor ~3 improvement compared to the present chip.

Inefficiency averaged over a luminosity fill is factor 2 smaller.

H.C. Kaestli
Oct 2009

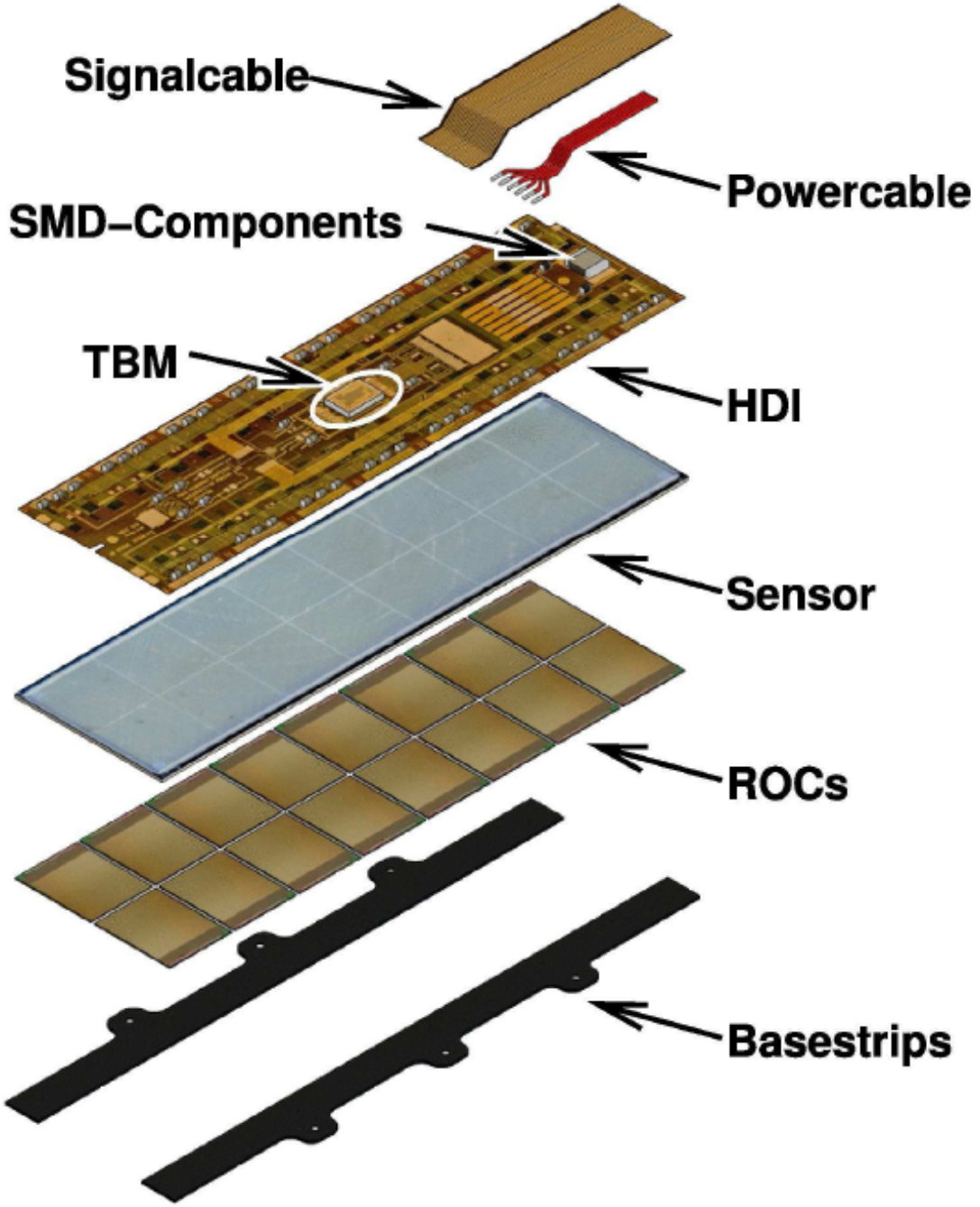
Pixel upgrade motivations

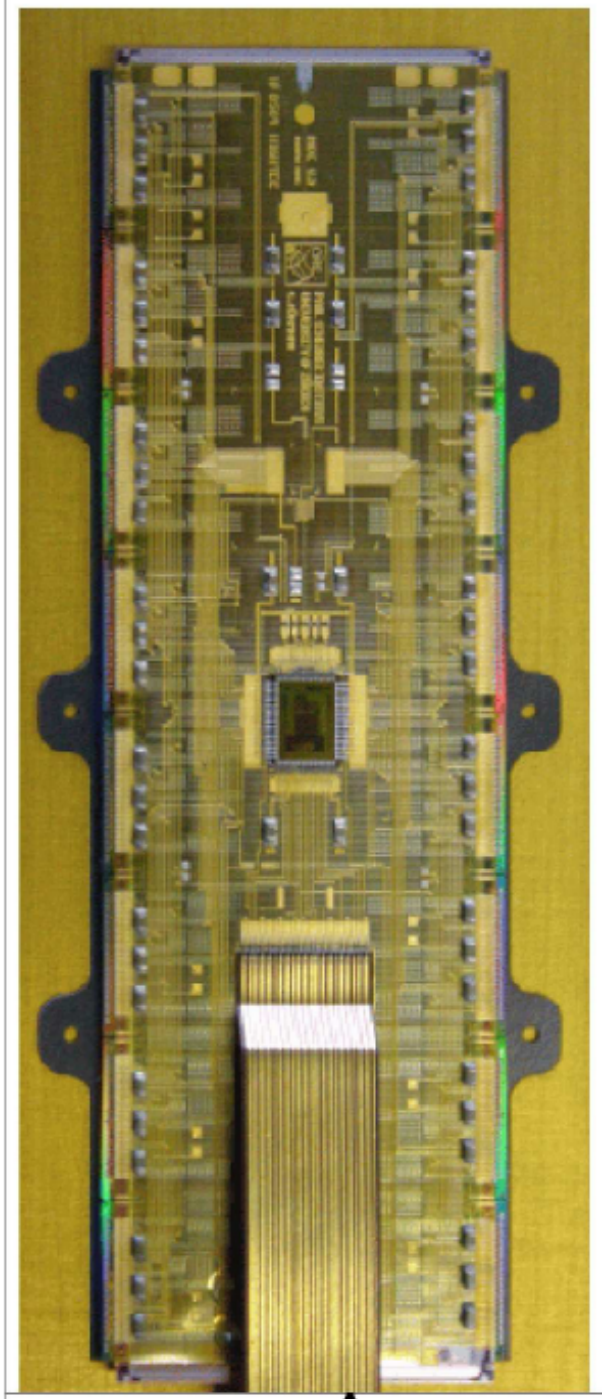
- Prepare for 3× higher luminosity than design: $3 \cdot 10^{34}/\mathrm{cm}/^{2}$:
  - Requires a new readout chip with more buffering.
- Less material:
  - Low mass supports, CO_2 cooling, optical converters outside the tracking volume.
- 4^{th} layer for better track seeding efficiency and improved stand-alone tracking:
  - Digital readout and DC-DC power converters (have to use the same outer power cables and optical fibers)
- Smaller beam pipe for improved impact parameter resolution:
  - Negotiate with LHC machine group.
- Add redundancy in the tracking system:
  - Be ready early, almost independent of the luminosity evolution.

CMS Pixel modules at DESY

- Deliver 352 good barrel pixel modules.
- Input:
  - Si sensors on wafers.
  - Readout chips on wafers, already tested at PSI.
  - High density interconnects and cables from external company.
- Tasks:
  - Test Si sensors, prepare bump bonds, cut.
  - Cut and select readout chips: 5632.
  - Bump bond chips to sensors.
  - Glue HDI to sensors.
  - Wire bond chips to HDI: 200k.
  - Test and calibrate at several temperatures.
  - Document.

CMS barrel pixel module





W. Erdmann

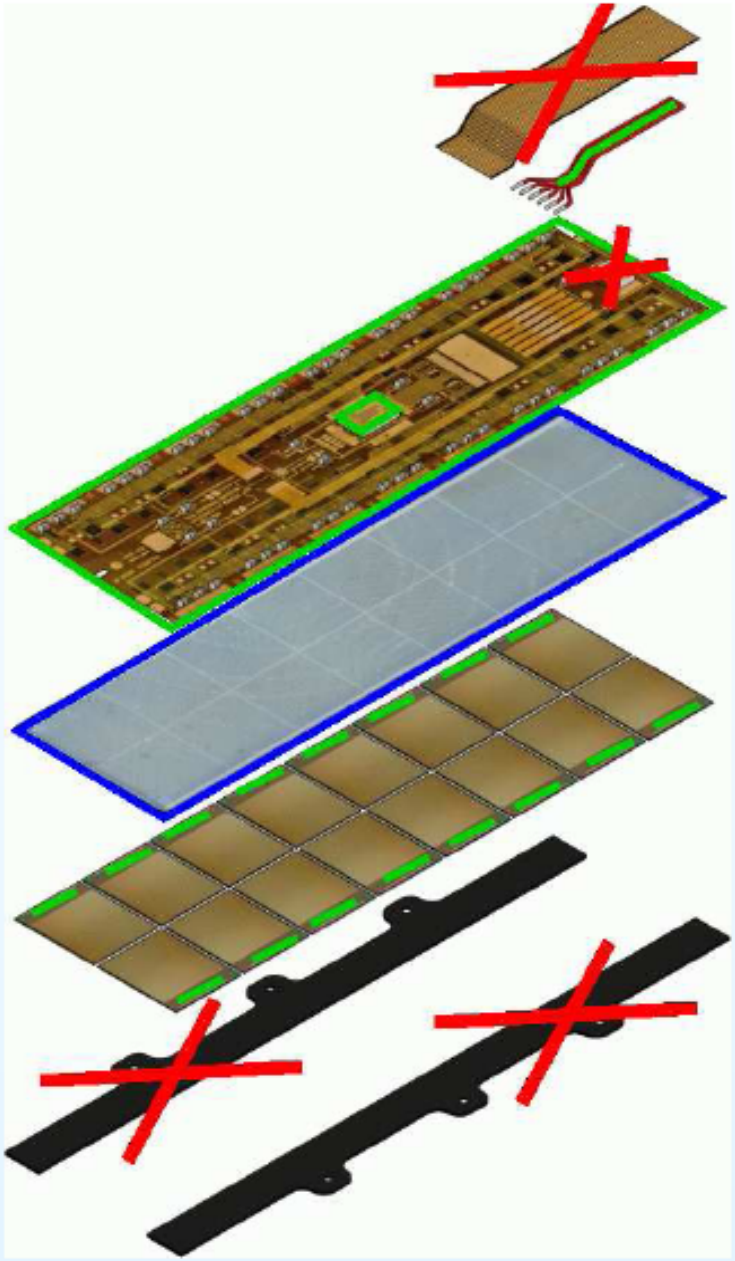
CMS pixel upgrade

Module: Design Changes I

one module design

- no basestrips
- ROC:
  - thickness 175 $\mu m \Rightarrow$ 75 μm
- HDI:
  - no HV-capacitor
  - miniaturise SMD - components

R. Horisberger
Jun '09

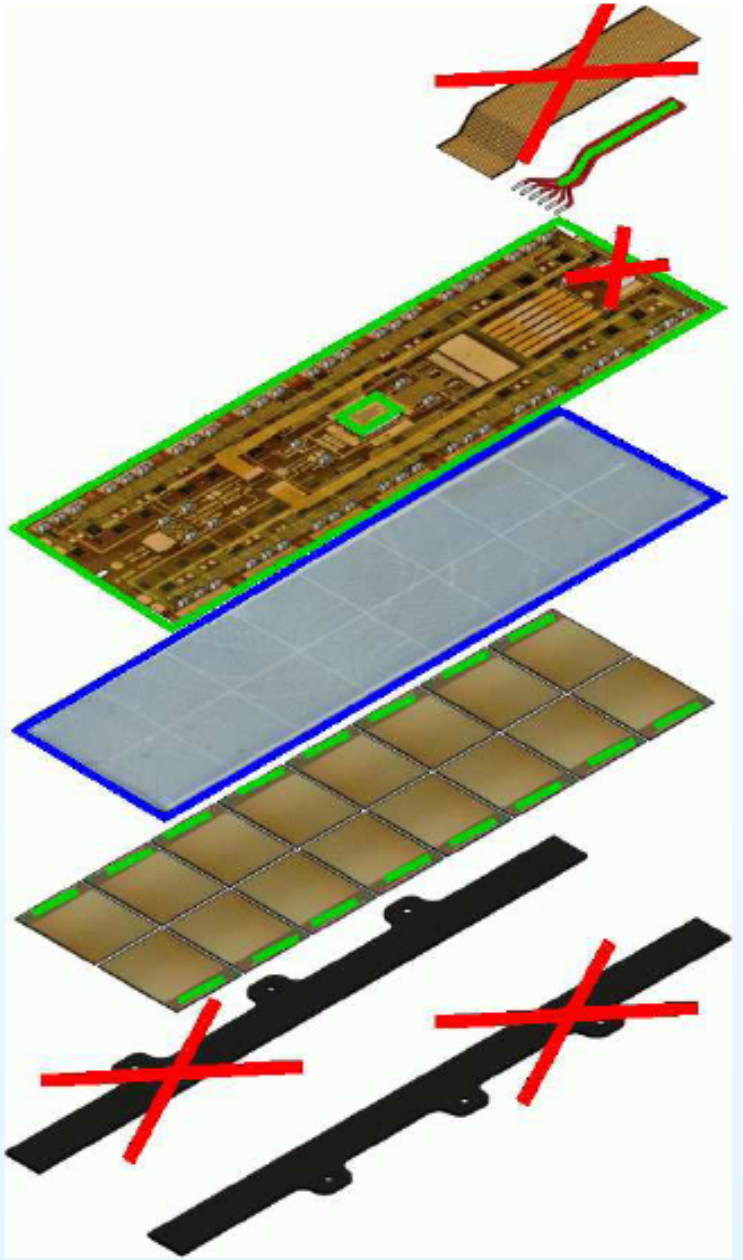


CMS pixel upgrade

Module: Design Changes II

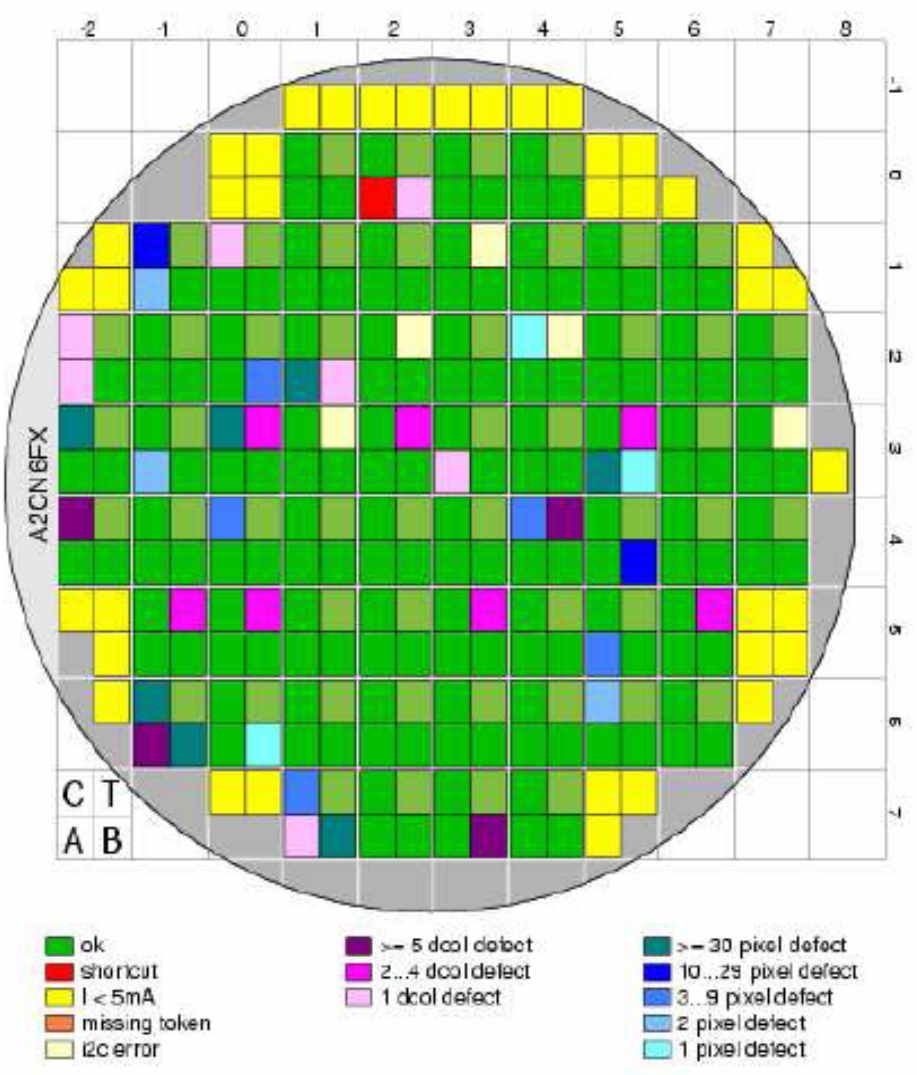
- cables:
  - one micro twisted pairs cable:
    - 6 x 250 μm Ø
    - 12 x 125 μm Ø
  - 50% of current connectors
  - long pigtails (~1.2 m)

$\Rightarrow$ no plugs/port-cards in active area



R. Horisberger
Jun '09

CMS Pixel Chip



- Automated Suss Prober (8"):
- Test procedure
  - Threshold scan for all pixels
  - Test all DACs
  - Check all trim bits & mask
  - Check all data buffers
  - Check all time stamp buffers
  - Check power consumption
- 400K I2C commands to ROC
- Time 70 sec/chip, 1 wafer/day
- Average yield 74%

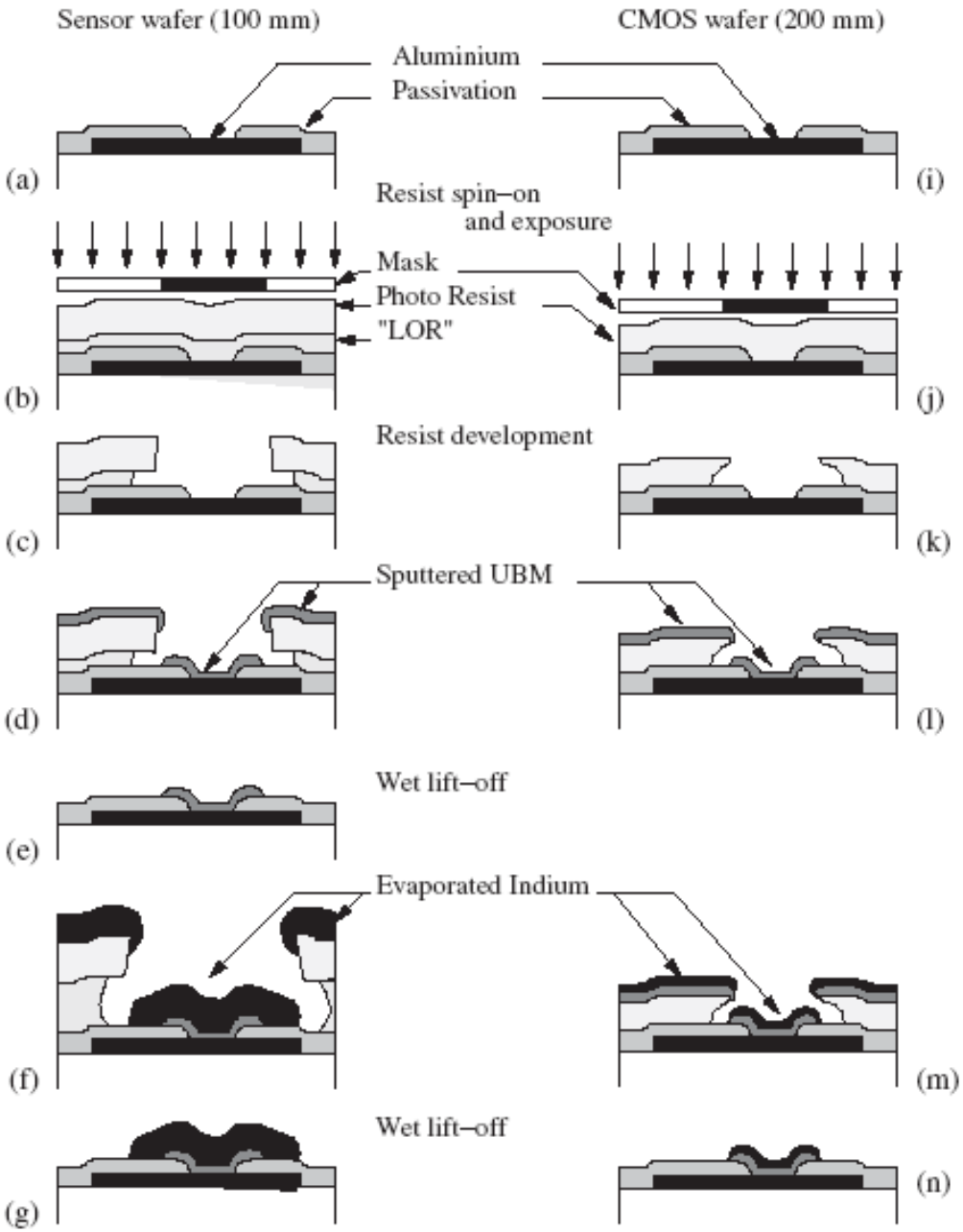
A. Starodumov

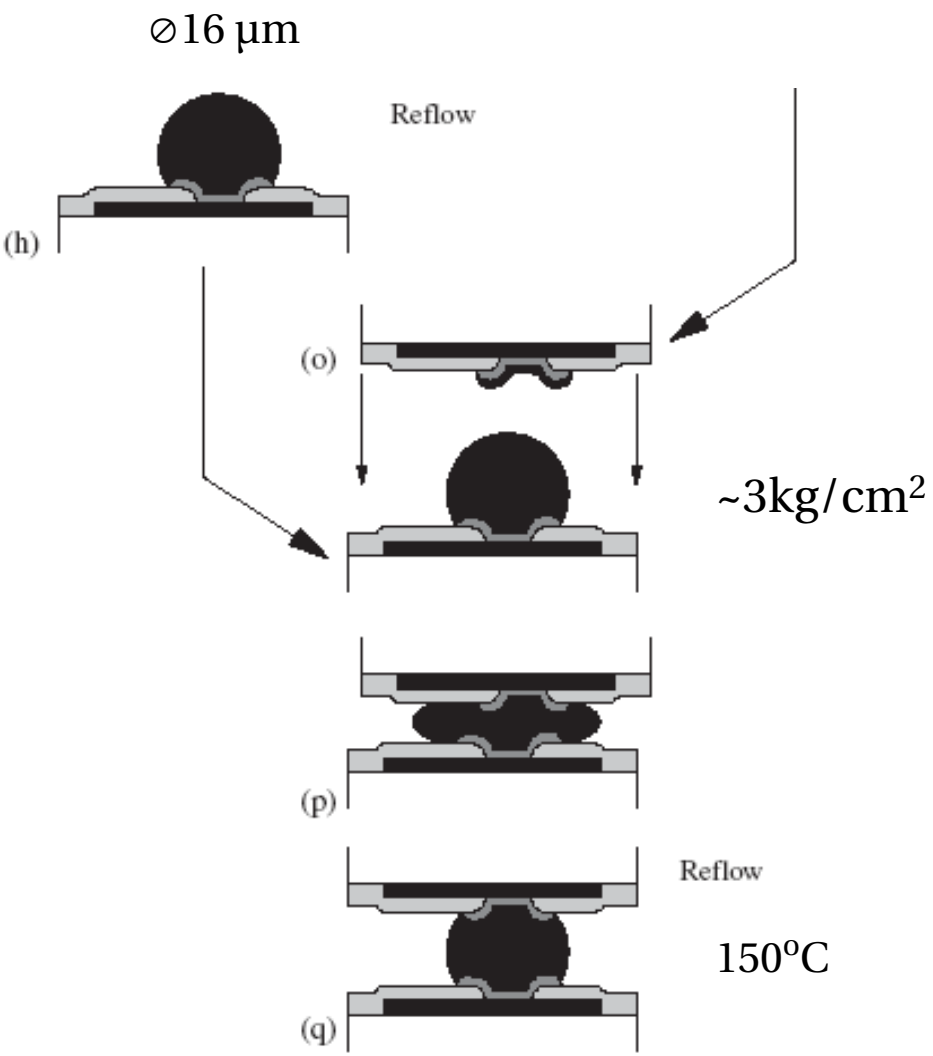
Assembly part I

- Si sensors come from CIS Erfurt, with under bump metal
  - Test 3 sensors on a 4” wafer: I-V, C-V.
  - Deposit bump bond material: at PSI? at IZM?
  - Cut at ?
  - Test sensors: I-V.
- Read out chips come wafer-probed from PSI, with UBM?
  - Thinned to 175 or even 75 µm ?
  - Cut and pick at ?
- Flip-chip bump bond 16 ROCs to sensors: at DESY? at IZM?
  - Re-flow sensors to form bump spheres,
  - Automated bump bonding,
  - Re-flow once more to fuse bonds.
  - Test ROCs and bonds using automated prober.
  - Re-work failed ROCs.

bare module

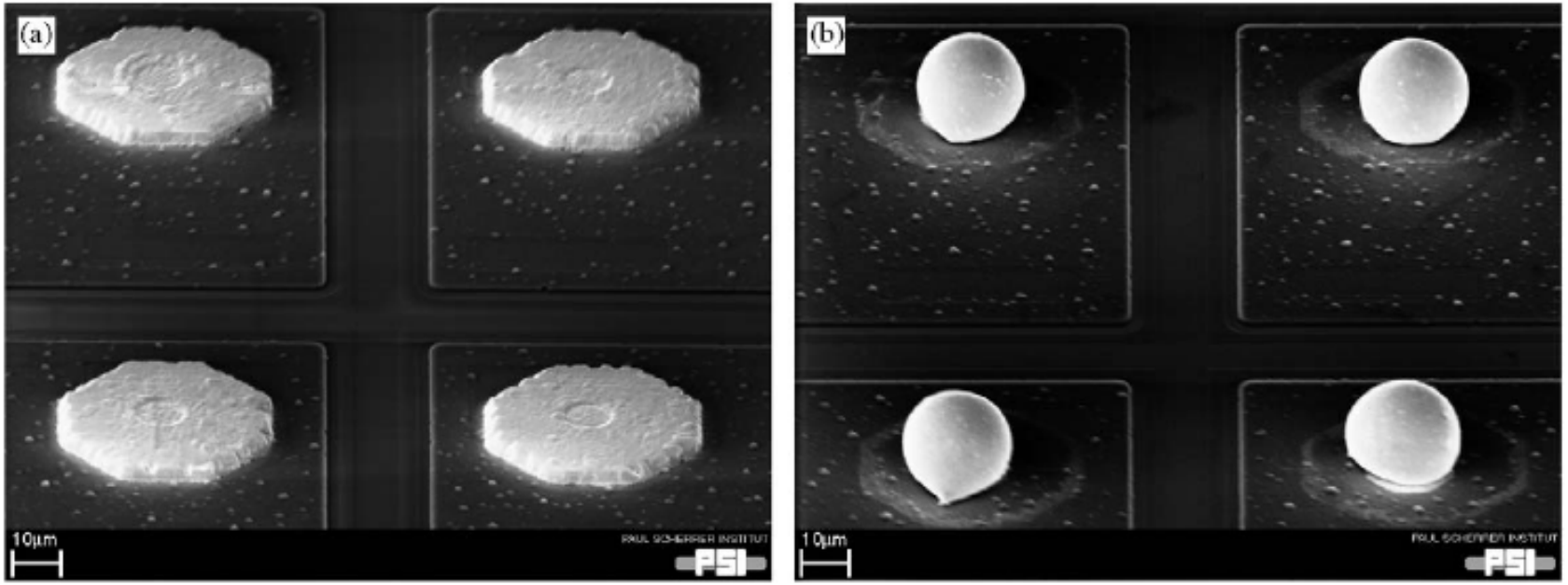
CMS Pixel bump bonding





Ch. Broennimann et al.: Development of an Indium bump bond process for silicon pixel detectors at PSI NIM A565(2006)303-8

CMS Pixel bump bonding

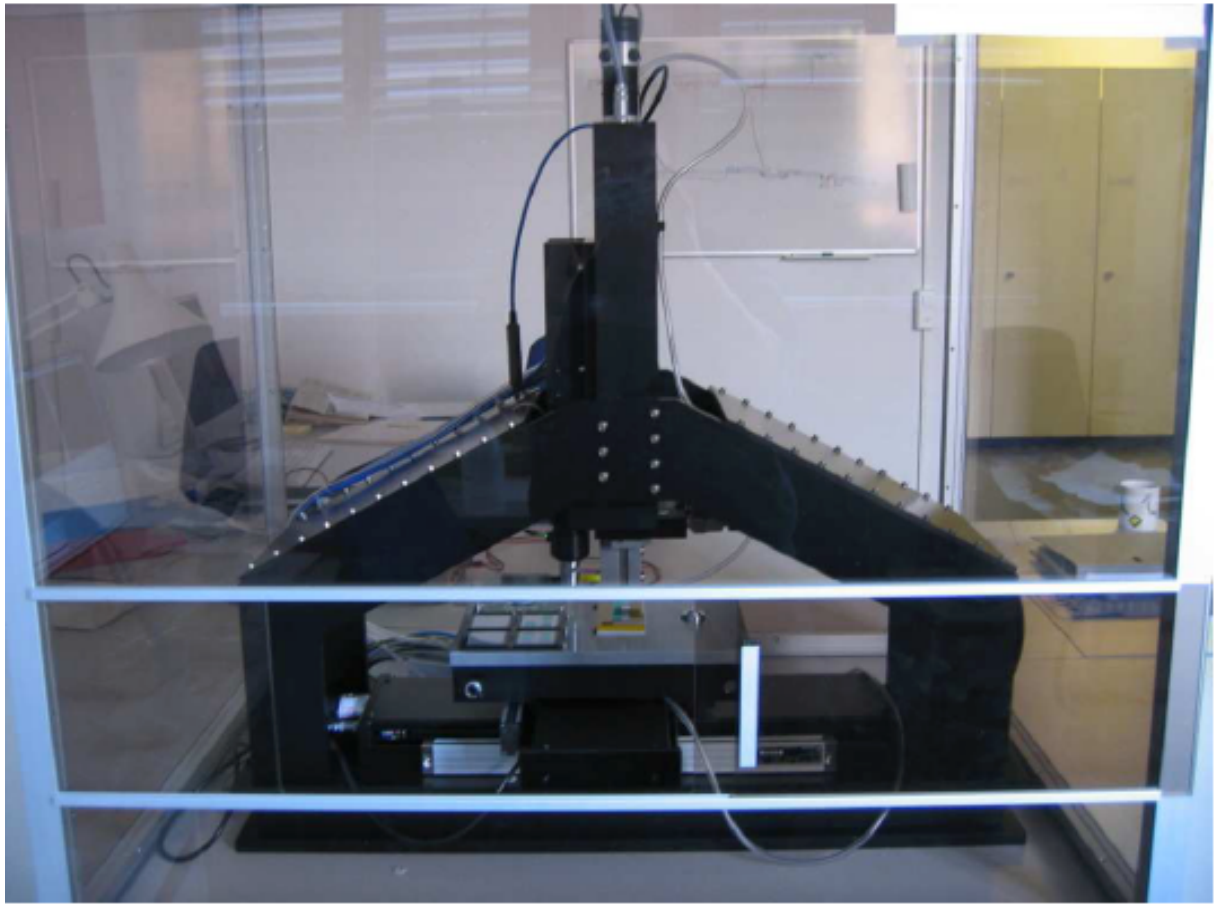


Indium pads from PSI.
150 µm pitch.

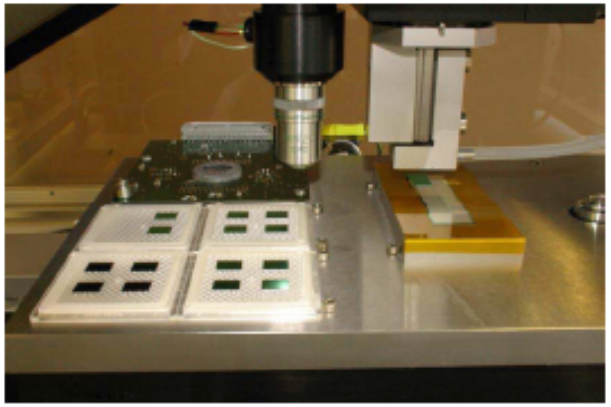
After re-flow at 150°C in
N_2 and CH_2O_2 atmosphere.
15 µm diameter.
Need oven at DESY.

Ch. Broennimann et al.: Development of an Indium bump bond process for silicon pixel detectors at PSI NIM A565(2006)303-8

CMS Pixel bump bonding

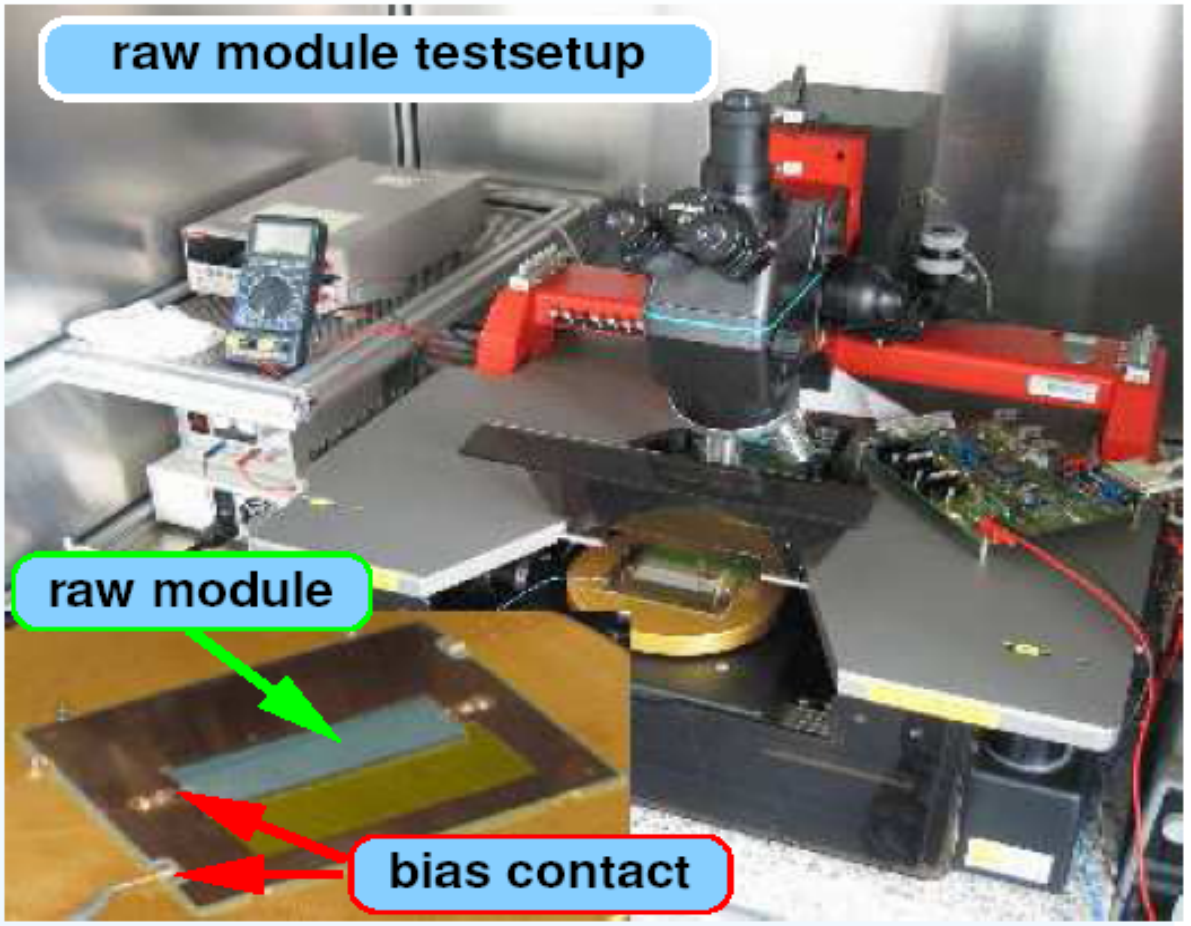


- Precision: $1 \div 2\,\mu\mathrm{m}$
- Production rate:
  - 6 modules / day + tests
  - automated: 1 hr/module
- Bare module test:
  - IV-curve
  - ROC functionality
  - bump yield
  - rework: 80% success



A. Starodumov

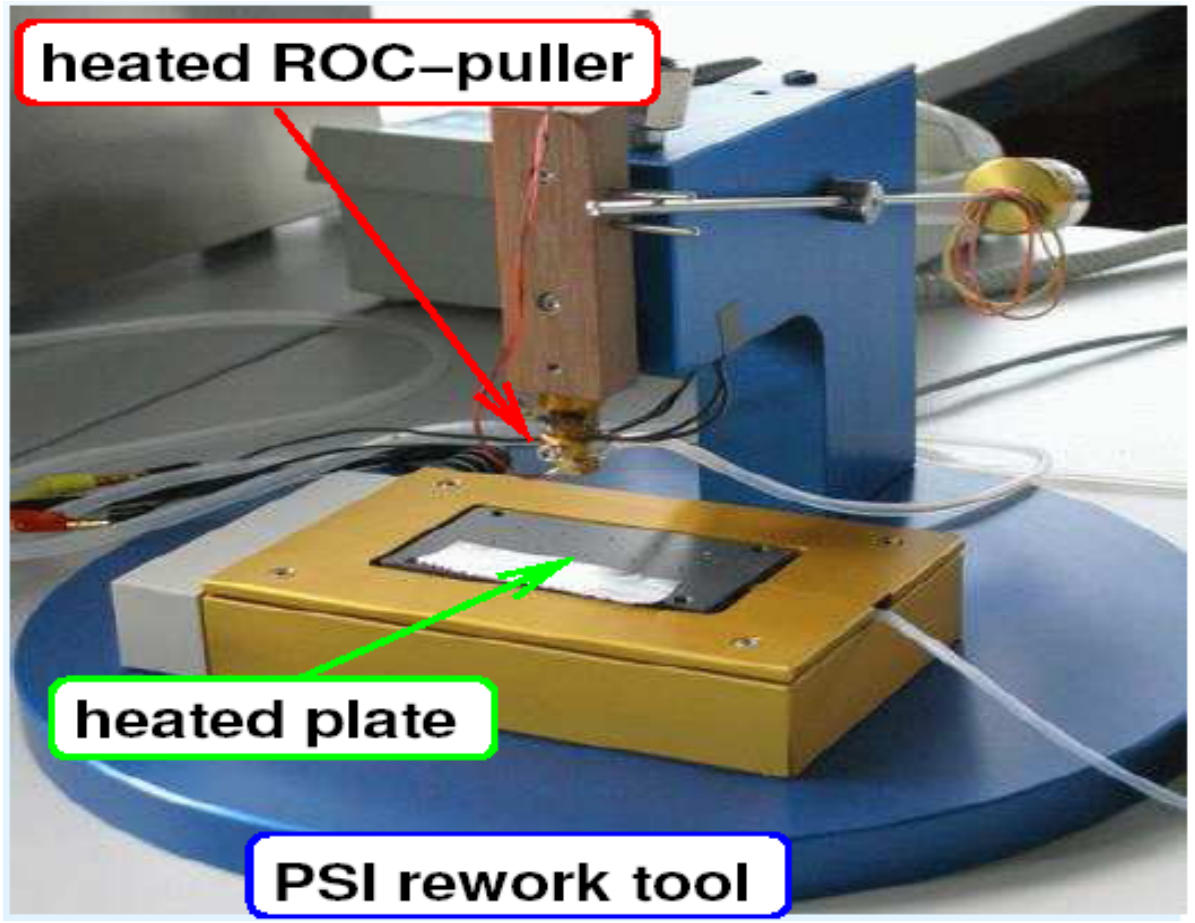
Bare module test



- Step-motor controlled probe station.
- Sensor I-V curve.
- Test each readout chip.
- Determine bump yield.

S. Koenig 2008

Re-work tool



- Removal of individual readout chips from a bare module is possible.
- Indium bumps remain on the sensor.
- Re-bonding of a new readout chip has 80% success rate.
- Improves module yield significantly.

S. Koenig 2008

Assembly part II

- TBM chip comes diced and tested from Fermilab.
- Micro twisted pair cable from PSI.
- HDI interconnect comes tested with 0.2×0.1 SMD components.
  - Glue and solder cable to HDI. Test bias line at 1000V.
  - Glue and wire bond TBM to HDI.
  - Test TBM on HDI.
- Glue HDI to back of sensor.
- Wire bond ROCs to HDI.
- Test and calibrate.

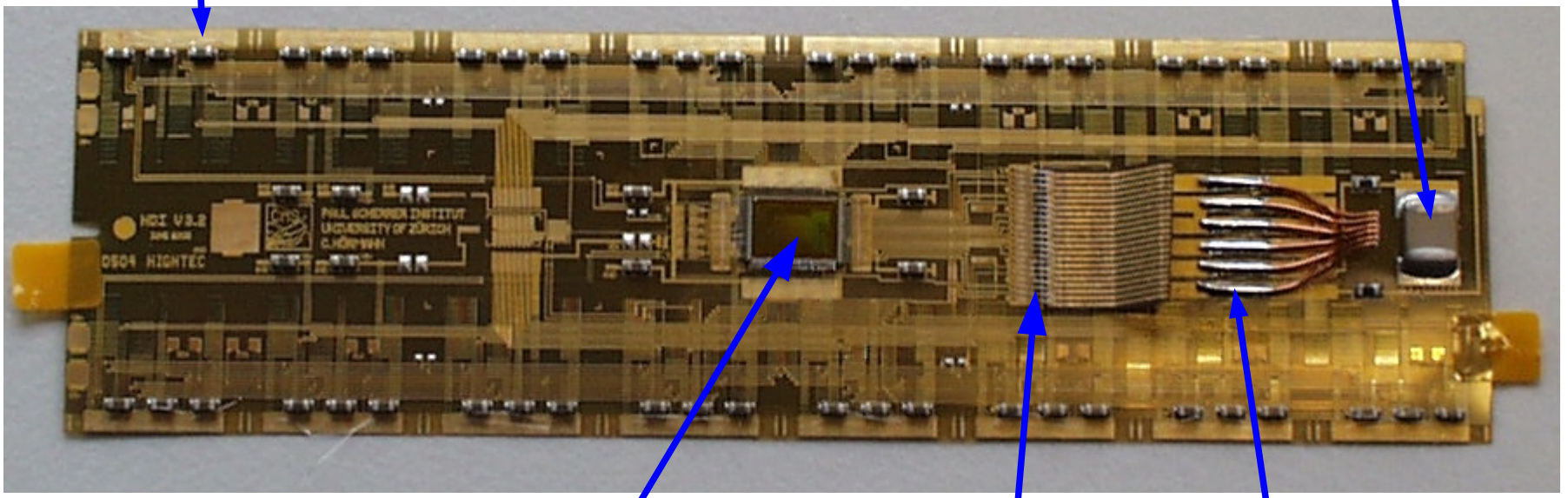
full module

High Density Interconnect

3 layer flex print
need new, common design
adapt to larger RO chip

0.2×0.1 SMD components

Bias capacitor
omit



TBM chip
wire bonded

signal cable
wire bonded

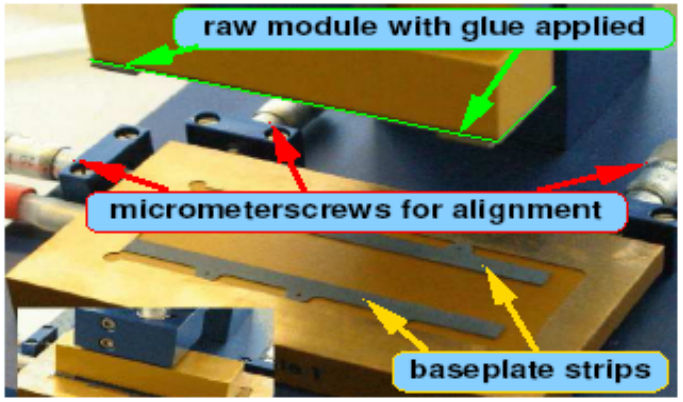
power cable
soldered

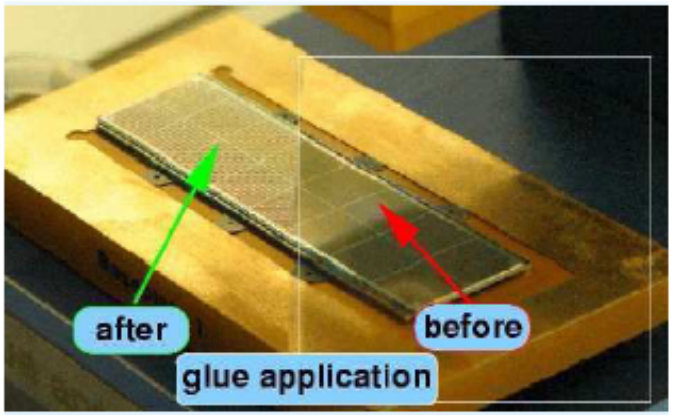
combine in micro
twisted-pair cable

pic65.jpg

CMS barrel pixel module assembly line

- Production rate:
  - 4 full + 2 half modules / day
  - or 6 full modules / day
- Three glueing steps:
  - glue basestrips to raw module
  - underfill sensor with glue
  - glue HDI to complete assembly
- Important: custom-made tools



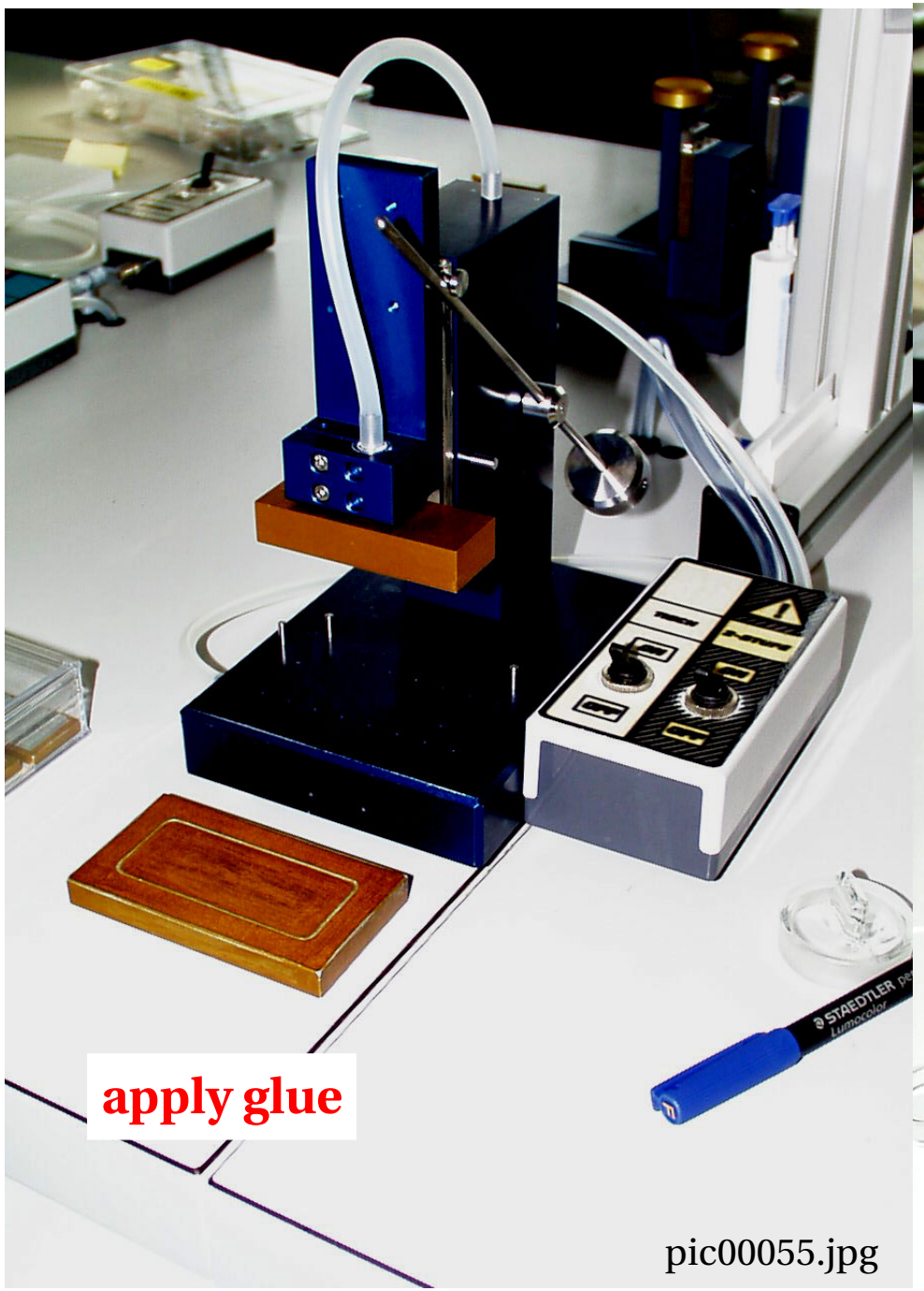


A. Starodumov

CMS barrel pixel module assembly line

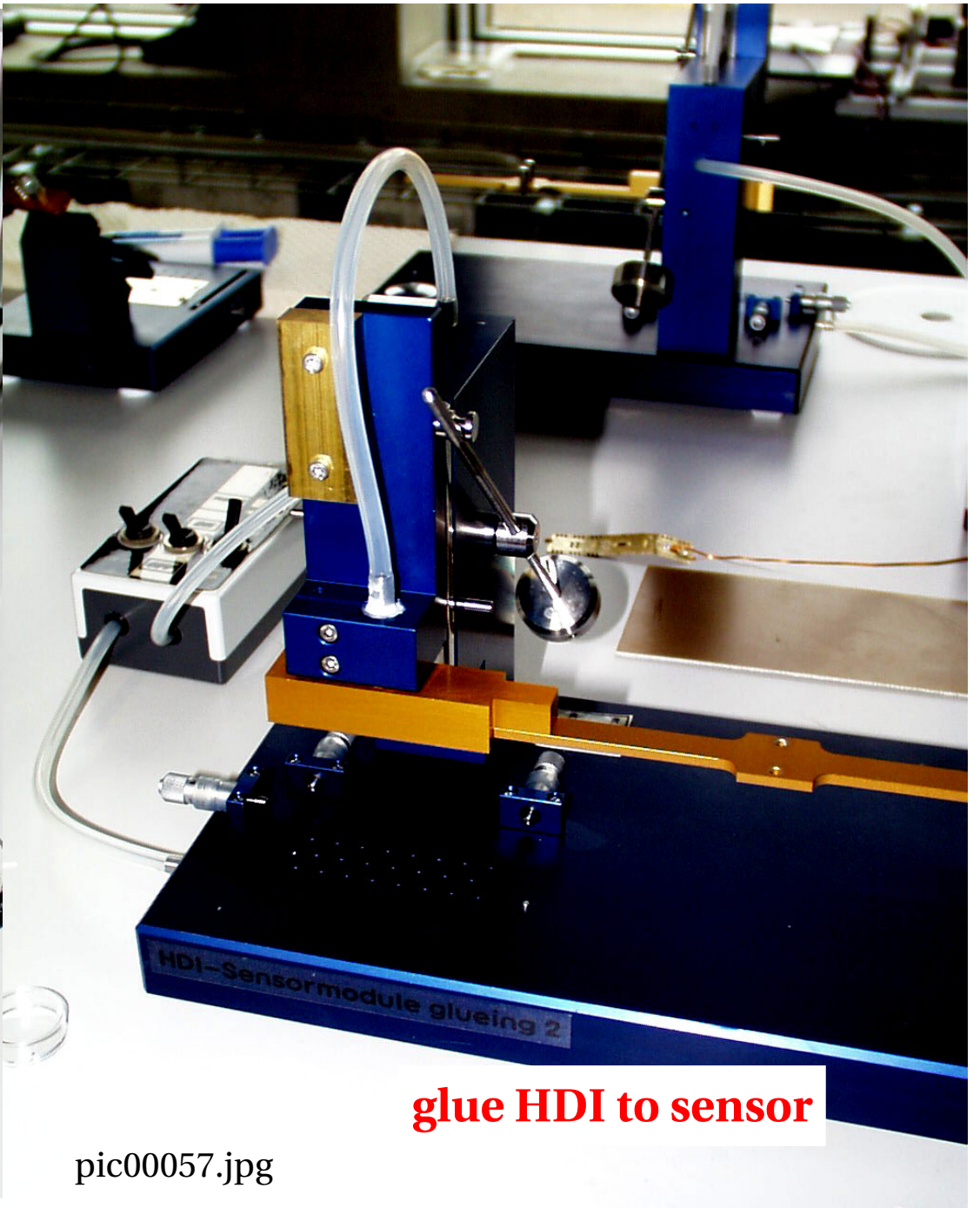
pic00058.jpg

CMS barrel pixel module assembly tools



apply glue

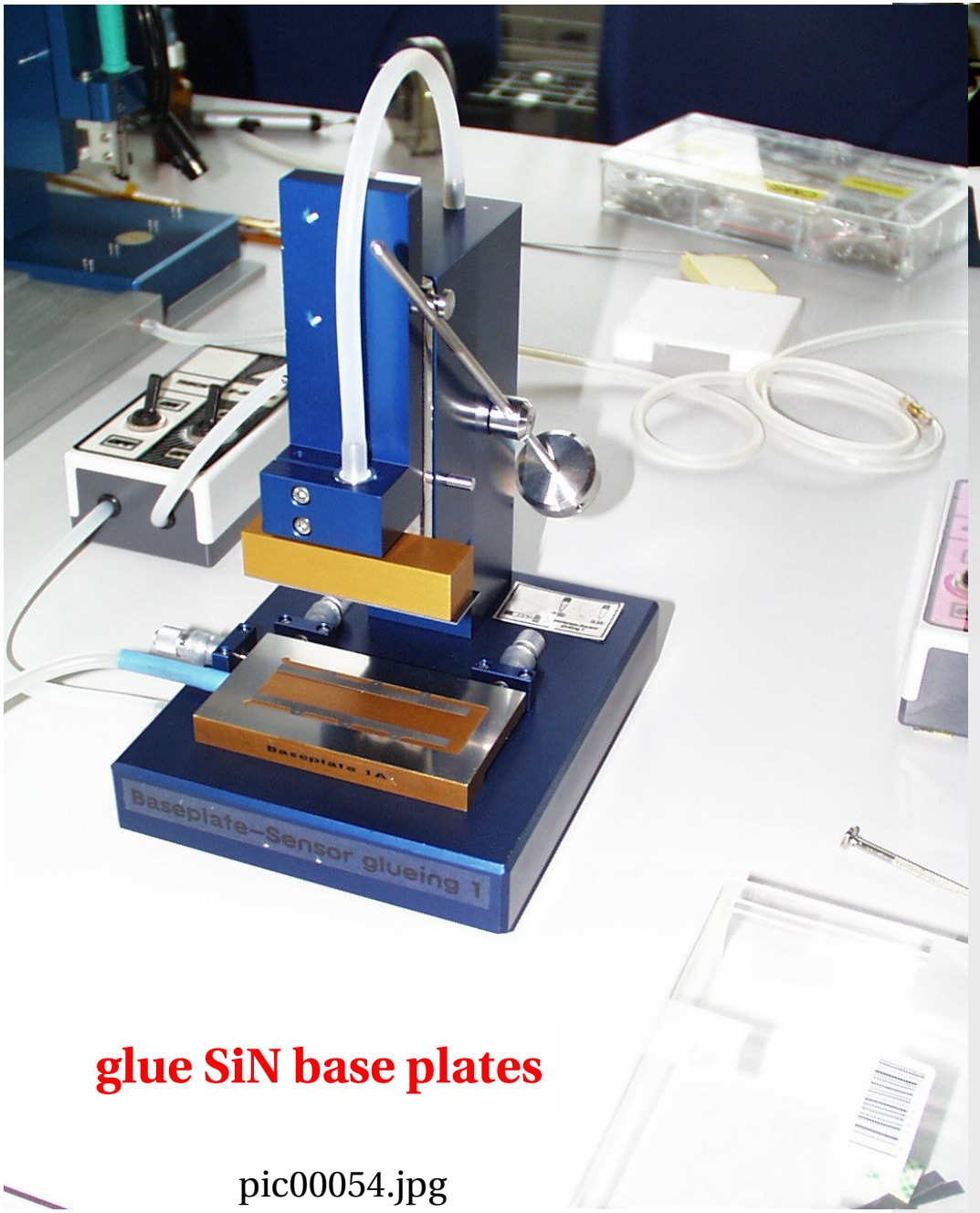
pic00055.jpg



glue HDI to sensor

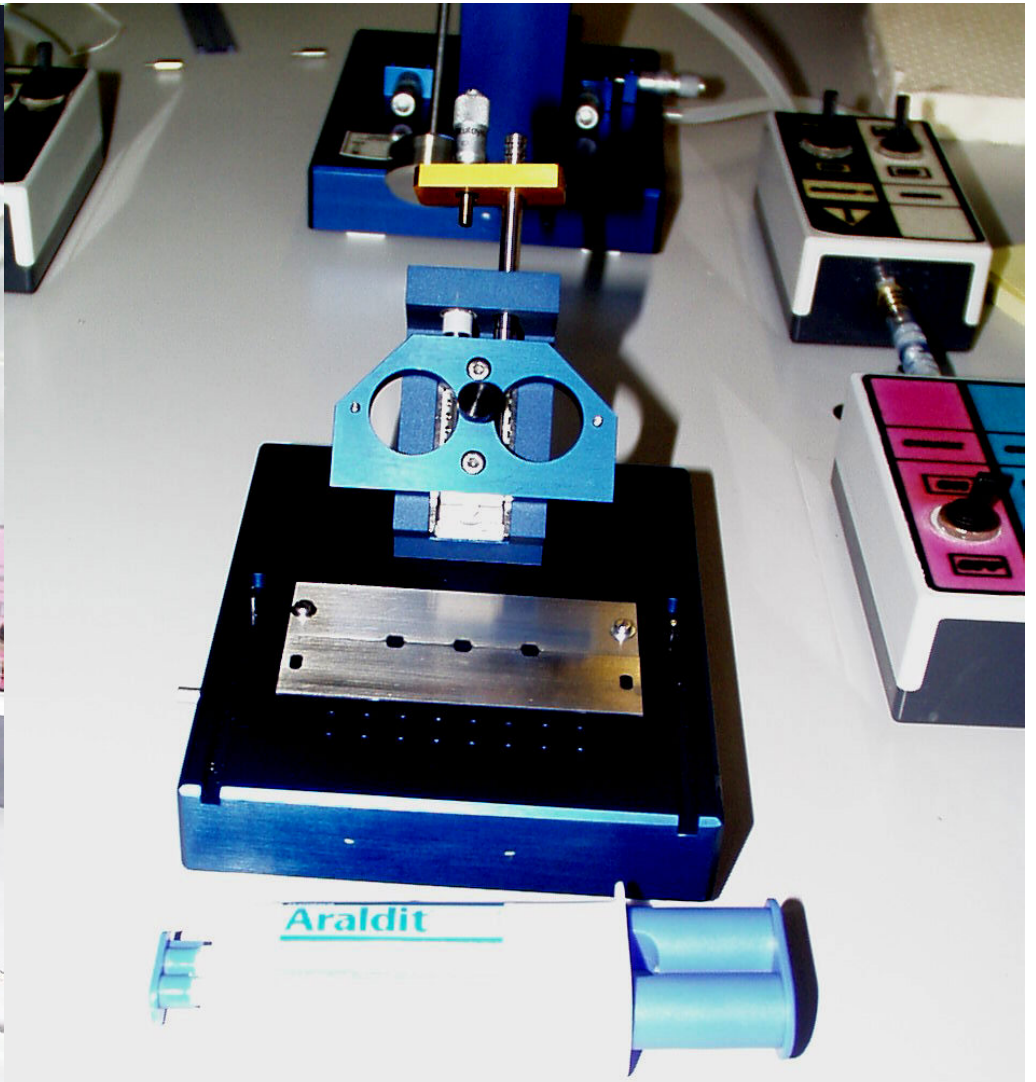
pic00057.jpg

CMS barrel pixel module assembly tools



glue SiN base plates

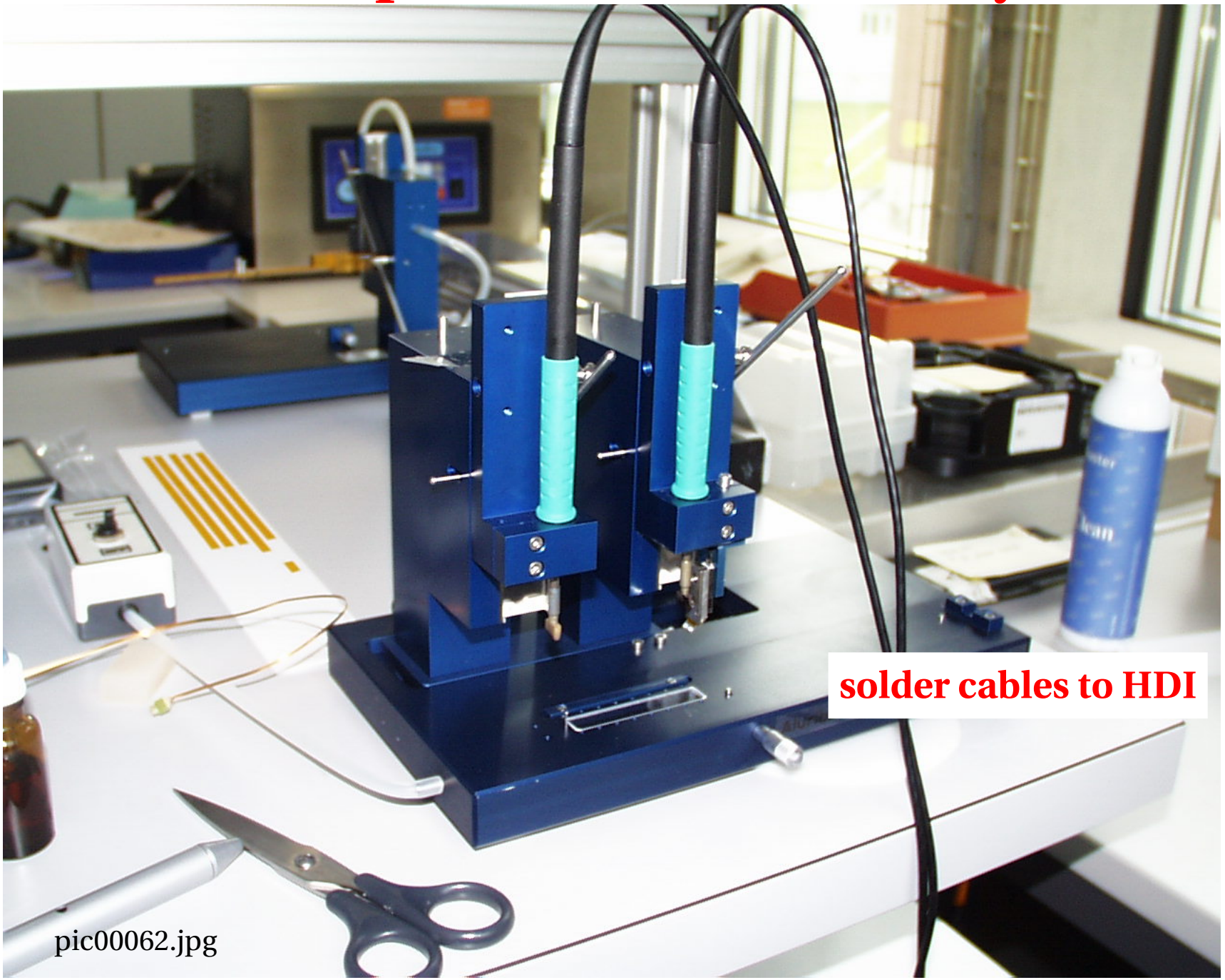
pic00054.jpg



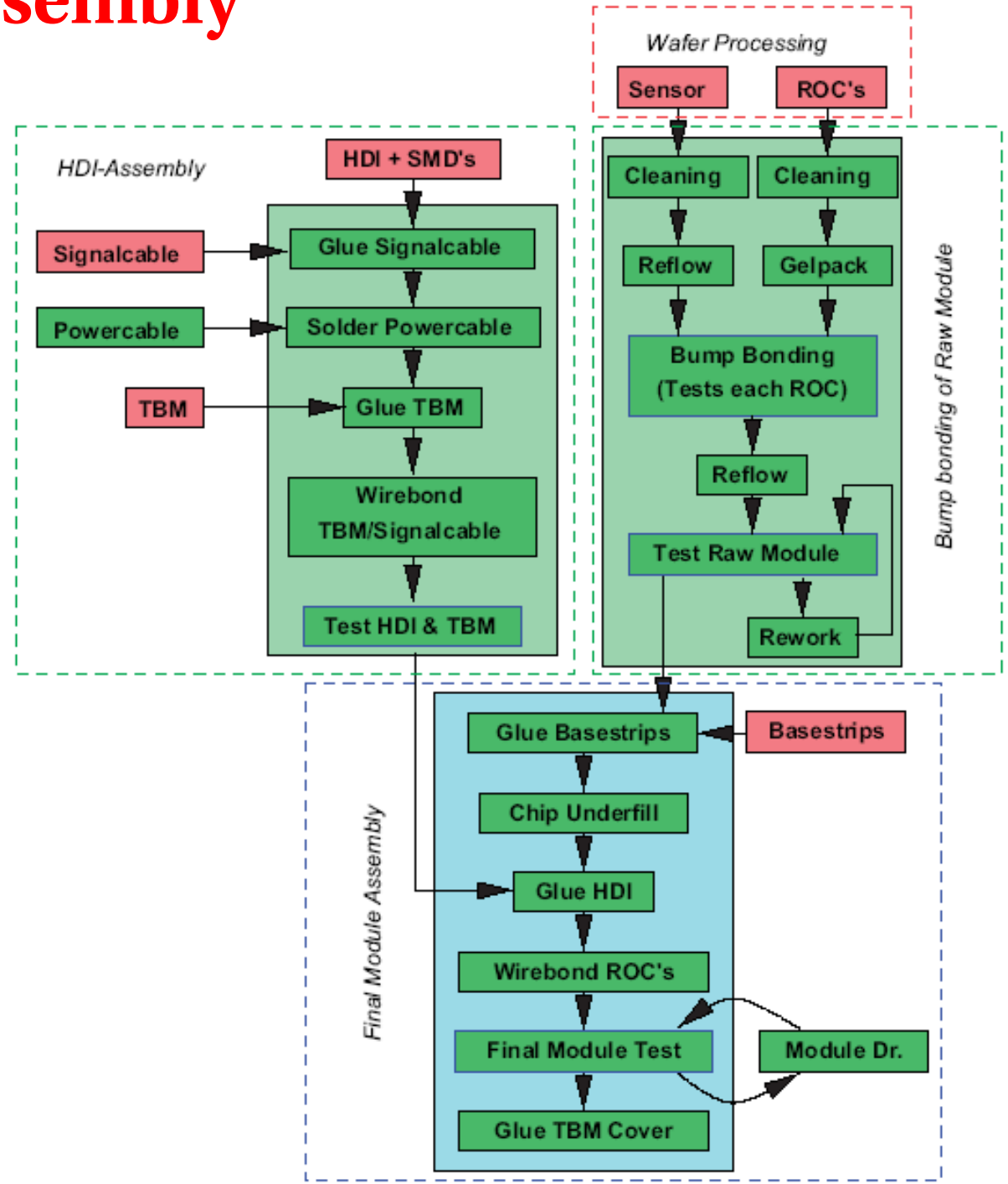
epoxy under-fill before wire bonding

pic00060.jpg

CMS barrel pixel module assembly tools



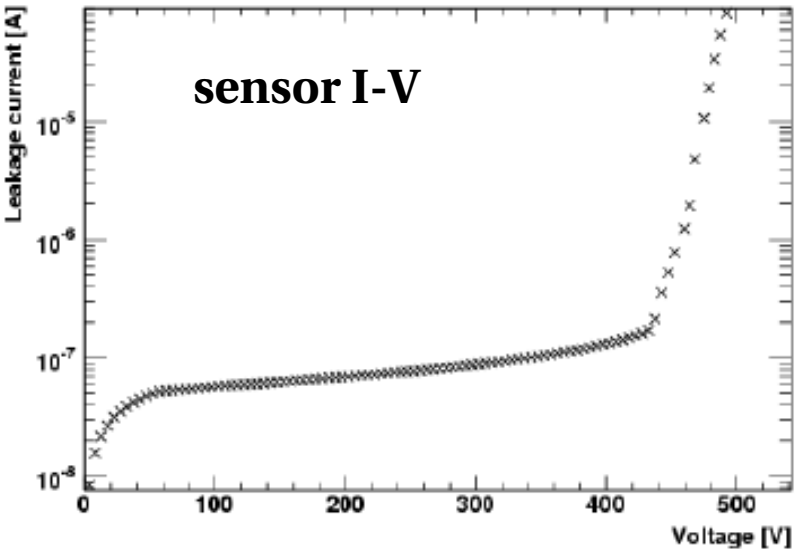
Module assembly



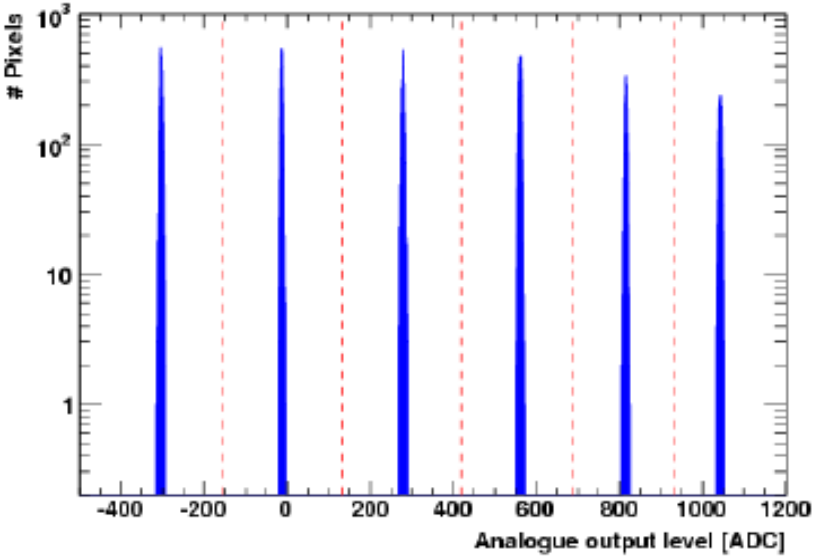
S. König et al.: Building CMS pixel barrel detector modules NIM A582(2007)776-80

Testing

- Start-up adjustments
  - Analog current setting
  - Threshold and delay settings
  - Analog levels setting
- Functionality tests
  - Verification of pixel readout
  - Check bump bonding quality
  - Functionality of 4 trim bits
- Performance tests
  - Pixel noise measurements
  - Si sensor IV curves
- Calibrations
  - Find separation between address levels
  - Calibration of pulse height
  - Threshold unification (trimming)
  - Internal signal calibration (with X-rays)

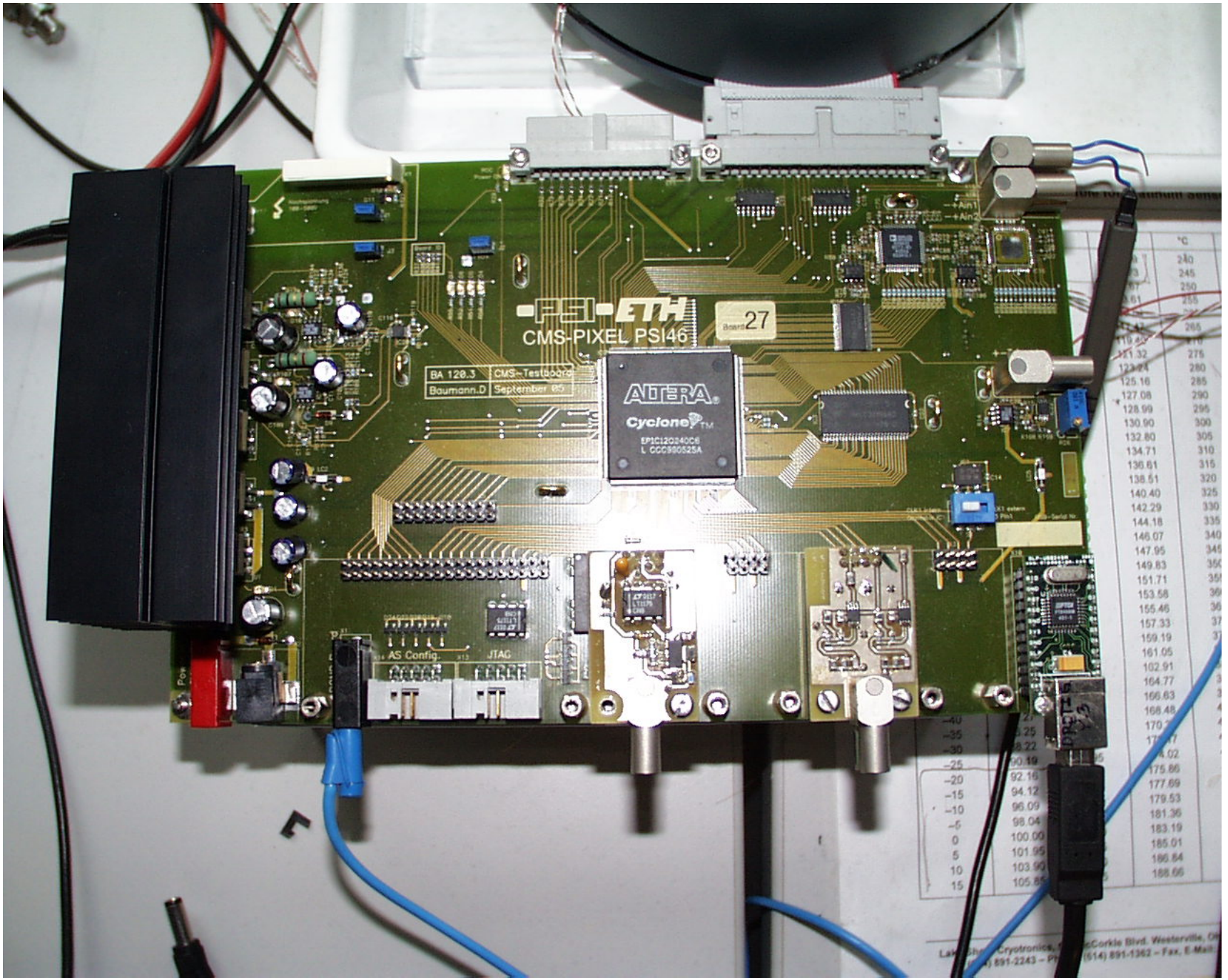


6 address levels



A. Starodumov

CMS pixel test board



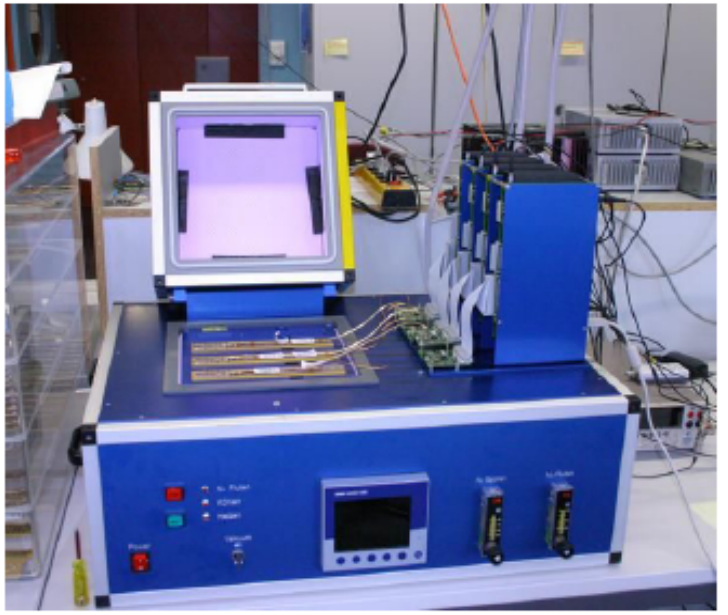
Connector to device under test

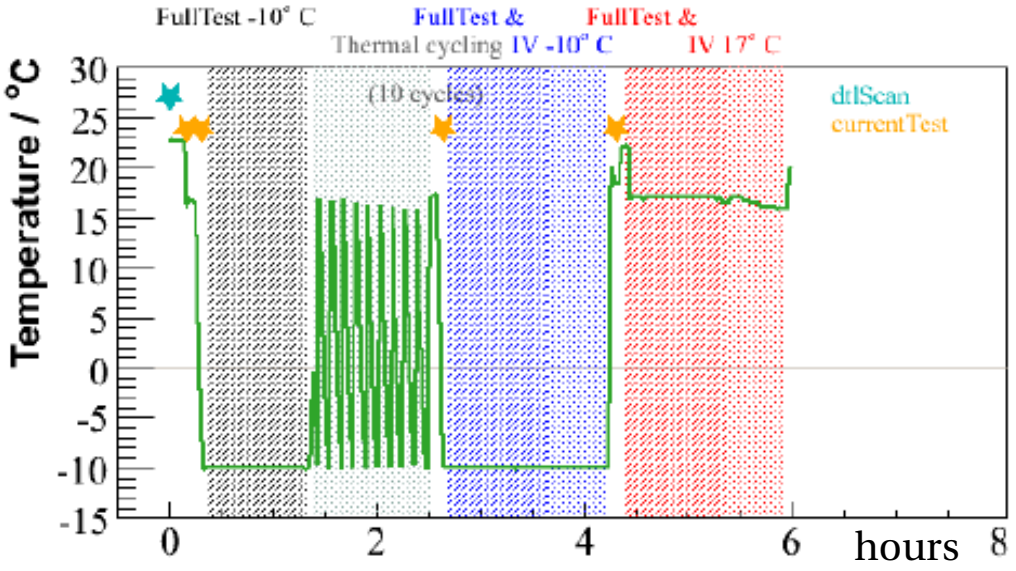
- Have one test board from PSI at DESY.

USB interface to PC

CMS pixel calibration and thermal cycling

- Challenges
  - Huge number of channels: $5 \div 6 \times 10^7$
  - Multy-dimensional parameter space: 29 DACs/ROC
  - Temperature dependence: tests done at -10°C and +17°C
- Test set up
  - Programmable cooling box
  - 4 modules at a time
  - Castom built test-boards with FPGA
- Procedure
  - Start-up adjustments
  - Full Test at -10°C
  - 10 thermal cycles
  - Full Tests and IV at -10°C and +17°C





A. Starodumov

2010

- Set up electronics test stand: PSI46 test board, software. Phys
- Set-up Suess PA300 prober, buy probe card for PSI46 chip. FE
- Write HGF application. Phys
- Buy fine place (Kadett K1?). Lexi?
- Build or buy re-flow oven. TechM
- Produce gluing tools Uni HH?
- Establish bump bonding on single-chip modules from PSI. at FE

2011

- Order silicon sensors from CIS Erfurt — Pitzl
  - I-V curve on 100mm wafers — Phys + TechE
  - Indium sputtering — at PSI
  - Cutting — at company
  - Clean — TechM
  - I-V curve on sensors — Phys + TechE
  - Seal and store in N_2 atmosphere — TechM
- Set up X-ray test stand — Phys + TechE
- Design and build box for module cold calibration — Eng + TechM
- Prepare series production — all

2012

- Set-up production lab:
  - Bonder and re-flow oven — at FE
  - Prober and tester — at FE
  - Klimatisierter Grauraum mit Personenschleuse — where?
  - Pump and low pressure distribution pipes
  - Gluing table — at FE?
  - Storage containers — at FE?
- Design and build assembly tool for 3rd layer. — Uni HH or Eng
- Receive tested and diced readout chips — from PSI
- Receive HDI with SMD components — from common supplier
- Receive micro twisted pair cables — from PSI
- Receive tested and diced TBM chips — from Fermilab
- Start series production mid 2012 — see next page

2013

- Series production: team
  - Bump bonding 2+1 TechM at FE
  - Bare module test and re-work Phys + PhD at FE
  - Glue and wire bond micro coax cable to HDI at ZE
  - Glue and wire bond TBM to HDI. Test. at ZE + 1 TechE
  - Glue HDI to bare module 2+1 TechM
  - Full module test and calibration Phys + PhD + TechE
  - Store.
- Assemble 3rd layer 2 TechM
- Group test 2 Phys + PhD
- Transport to PSI or CERN: mid 2013
- Ready for installation in CMS: end 2013

Summary

- DESY was asked by PSI whether we want to contribute to a 4-layer replacement of the CMS pixel detector for phase I: yes!
- Benefits:
  - Improved pixel stand-alone tracking: important for the High Level Trigger?
  - Improved track seeding efficiency.
  - Reduced material budget.
  - Readout chip adapted to increased luminosity.
  - Establish bump bonding technique at DESY.
  - Establish chip testing and calibration procedure at DESY.
- Need physics benefit study at DESY.
- Need extra funding from HGF: ~ 1.5MEUR for sensors and chips.
- Further opportunities for an even larger pixel system for phase II (SLHC):
  - ASIC design, radiation hard sensors, trigger, integration...

CMS Pixel history

1994 - CMS Technical Proposal, pixels included
1998 - Tracker Design Report
1994-2005 - R&D, mostly readout chip (ROC) and sensor.
9/2005 - discovered a serious problem the PSI-46V2.2 ROC
11/2005 - submit PSI-46V2.3
3/2006 - final ROC arrives

FPIX
6/2006-10/2007 -
plaquette & panel construction
2/2007-11/2007 -
disk assembly
4/2007-12/2007 -
delivery to from FNAL to CERN
1/2008-7/2008 - testing

BPIX
6/2006-12/2007 -
module production
1/2008-3/2008 -
module mounting on ladders
2/2008-4/2008 -
integration with the supply/service tubes
5/2008-6/2008 -
testing at PSI
7/2008 - delivery to CERN

July 23-24th 2008 BPix insertion
July 29-31st 2008 FPix insertion
August 7th 2008 loose all access to PP0 (our connection area)

D. Kotlinski