Verbund 05H2018
R&D Detektoren (Tracking)

KET Preparation Meeting
May 12, 2020

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What is “Verbund Tracking”

Consortium of BMBF funded R&D projects in the field of tracking detectors:

- “Integrierte Spannungsregler und Kontrolleinheiten für die Versorgung von hybriden Pixeldetektoren”
  - → ATLAS/CMS pixel readout chips (RD53 collaboration)
  - → controller chip for ATLAS ITk
  - Michael Karagounis (FH-Dortmund)

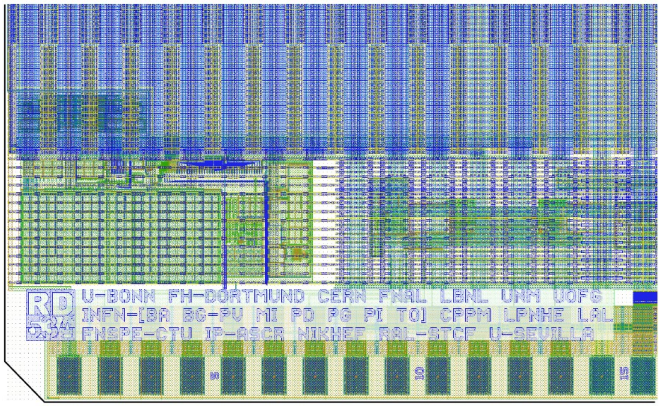
- “Entwicklung von HV-MAPS Detektoren für Teilchenphysik-experimente an Großbeschleunigeranlagen”
  - Miriam Fritsch (Uni Bochum)
  - Ivan Peric (KIT)
  - AS (Uni Heidelberg)

Disclaimer: “Verbund Tracking” is not a network of all R&D activities in the tracking area!

Integrierte Spannungsregler und Kontrolleinheiten für die Versorgung von hybriden Pixeldetektoren (FH-Do)

Project 1: RD53 Collaboration

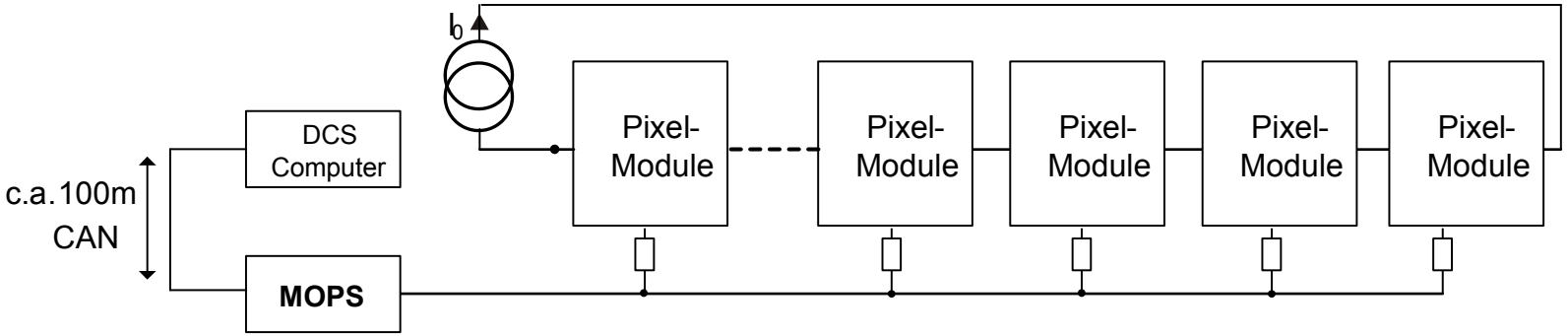
- “common” ATLAS/CMS readout chip for hybrid pixel sensors in context of High Luminosity LHC upgrade
- design of shunt-LDO power regulator



RD53A readout chip prototype

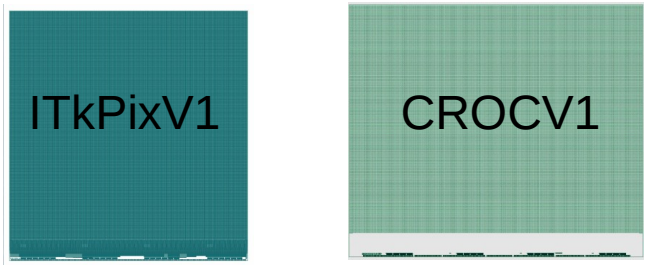
Project 2: MOPS Controller Chip (ATLAS upgrade)

- ATLAS pixel sensors will be serially powered
- MOPS (monitoring of pixel system, previous DCS) chip provides independent temperature and voltage monitoring of pixel modules



Milestones and Achievements (FH-Do)

- Integration of Shunt-LDO regulator with improved voltage references and safety features for
  - ATLAS ITkPix Pixel-RO-Chip (Q1/2020)
  - CMS CROC Pixel-RO-Chip (Q4/2020)



- Completion of the MOPS Controller Chips (Q4/2019)
- Design of a fully-integrated and radiation tolerant DC/DC-converter with conversion factor 4 (Q4/2020)
- Design of an radiation- and SEU-tolerant micro-controller (MOPS) (Q4/2020)

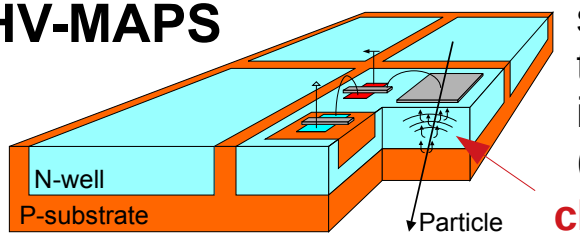
Plans for Funding Period 2021-24 (FH Do)

- Chip developments need to be completed in the coming funding period
- Funding options: BMBF Verbundforschung or Forschungsinfrastructure (FIS)

HV-MAPS R&D Project (BO, HD, KIT)

I.Peric, et al., NIM A 582 (2007) 876

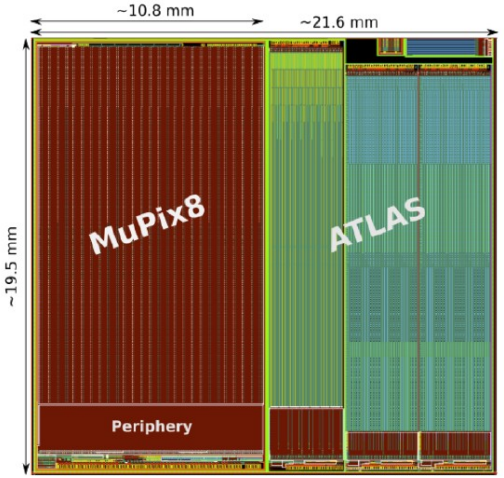
HV-MAPS



standard HV-CMOS process
transistor logic embedded
in N-well
("smart diode array")

charge collection by drift!

(aka depleted MAPS "Monolithic Active Pixel Sensor")



2018

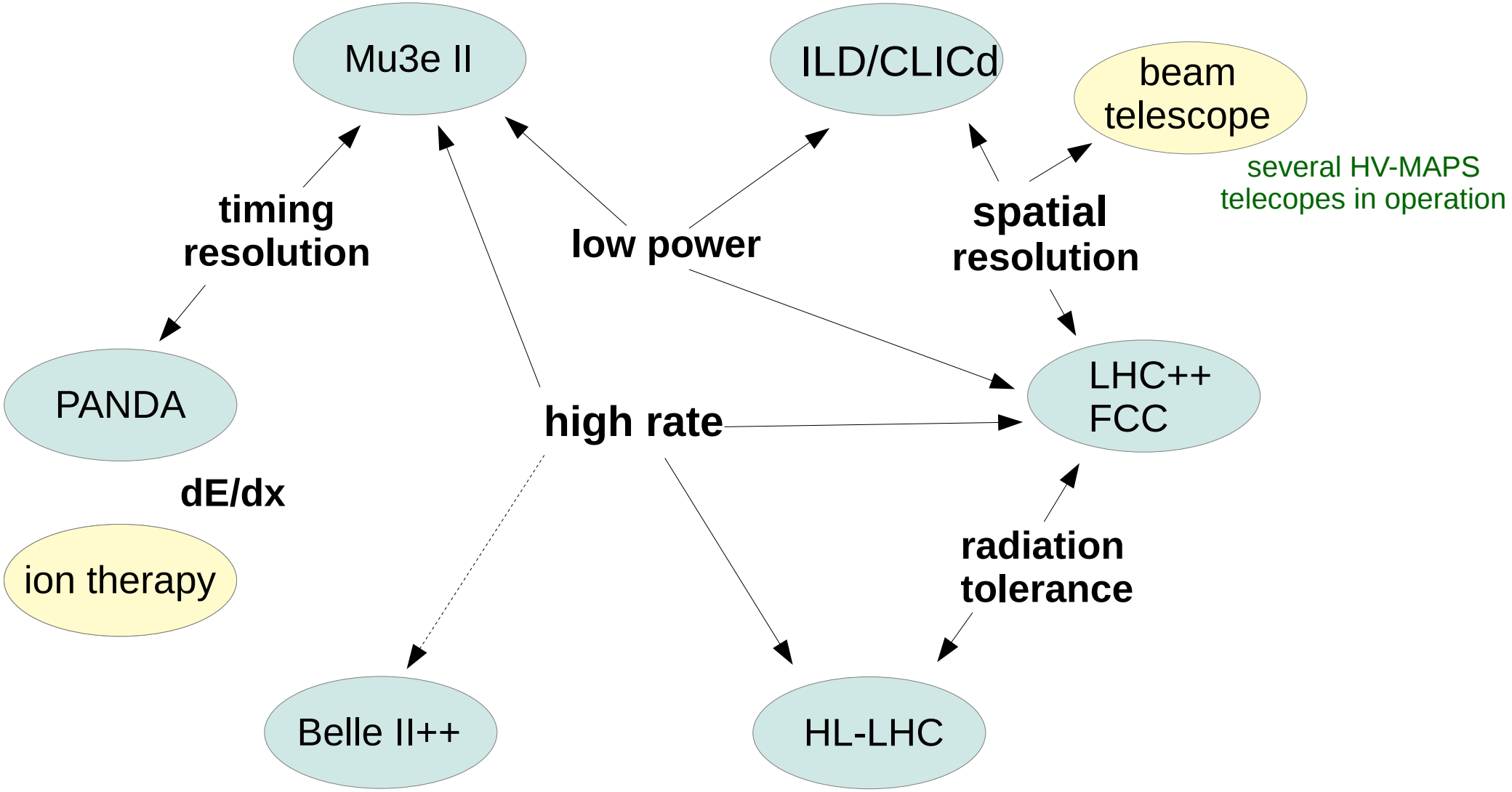
- Successful R&D program for many years for Mu3e, ATLAS and PANDA
  - based on a commercial 180nm HV-CMOS process (AMS,TSI)
  - high efficiency, low noise, high radiation tolerance (→ arXiv:2002.07253)
  - fast readout (untriggered, triggered)
- Technology foreseen to be used by various experiments:
  - Electron Ion collider (EIC @ BNL)
  - LHCb Mighty Tracker
  - P2 experiment @ Mainz
  - PANDA luminosity detector
- Technology option for other/future experiments

Goals of HV-MAPS Project
(BO, HD, KIT)

Based on the HV-MAPS concept perform generic detector R&D:

- Sensors suitable for the production of **multi-chip modules** providing **low power** consumption
- **High spatial resolution** and **radiation tolerance** for future vertex detectors
- High **time resolution** for pileup-suppression and time-of-flight (PID) in low energy experiments
- High **energy resolution** for dE/dx (PID) in low energy experiments
- Dedicated sensors allowing for **high-counting rates** (integration) for beam-monitoring and medical applications (e.g. ion-therapy)

Requirements & Experiments



- **Sensor requirements are application specific!**
- **What are the technological limits of monolithic HV-CMOS sensors?**

Milestone: Large Scale HV-MAPS

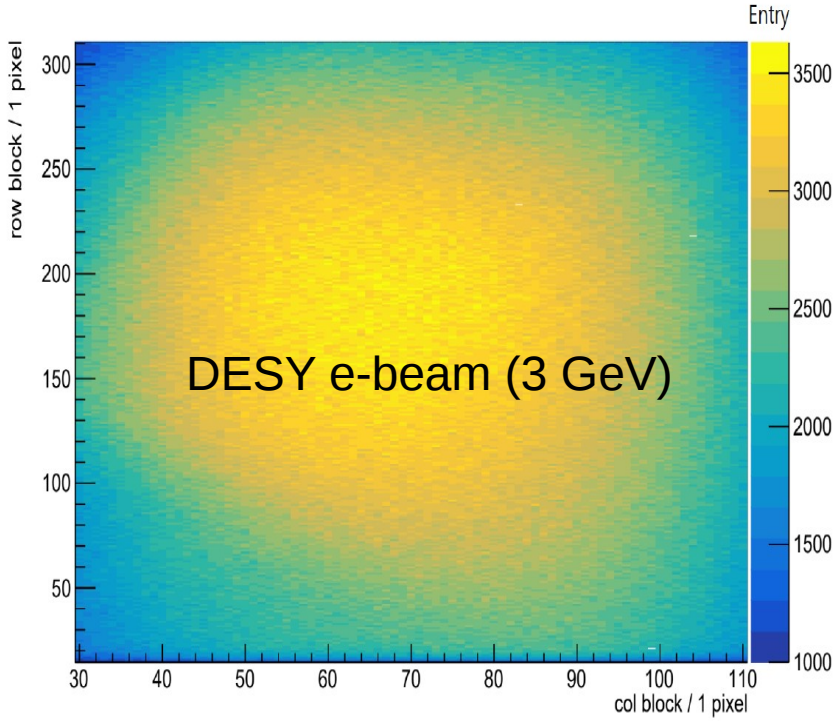
Timestamps: 10 bits, ToT: 7 bits

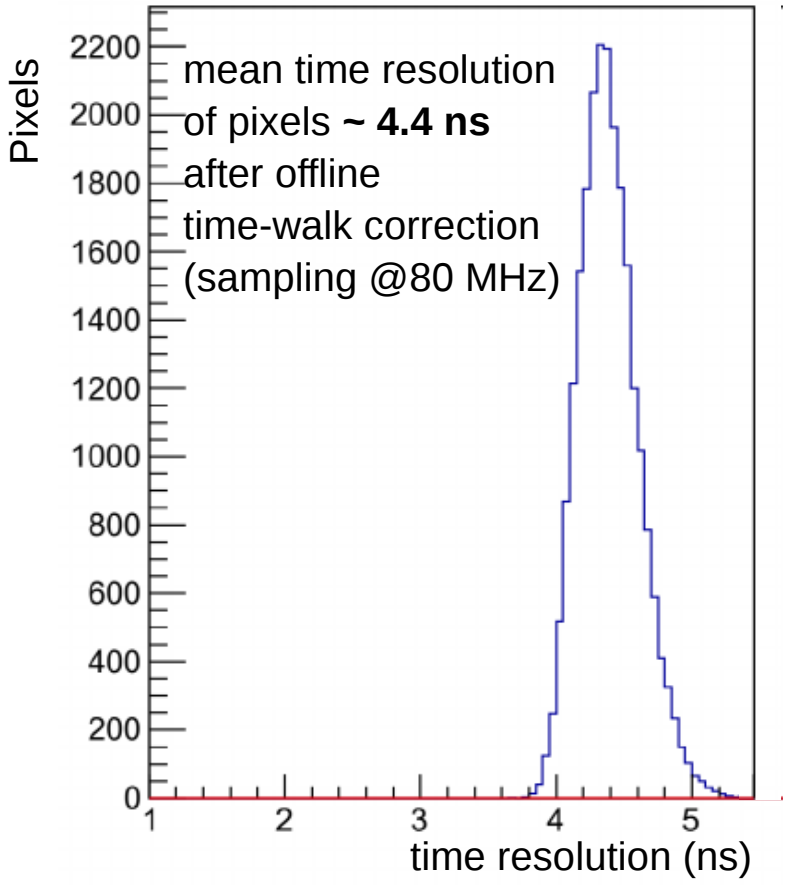
RO: triggered & continuous

pixel size: 50 x 150 µm²

Efficiency: 99.8%

Noise: ~0.1 Hz/pix

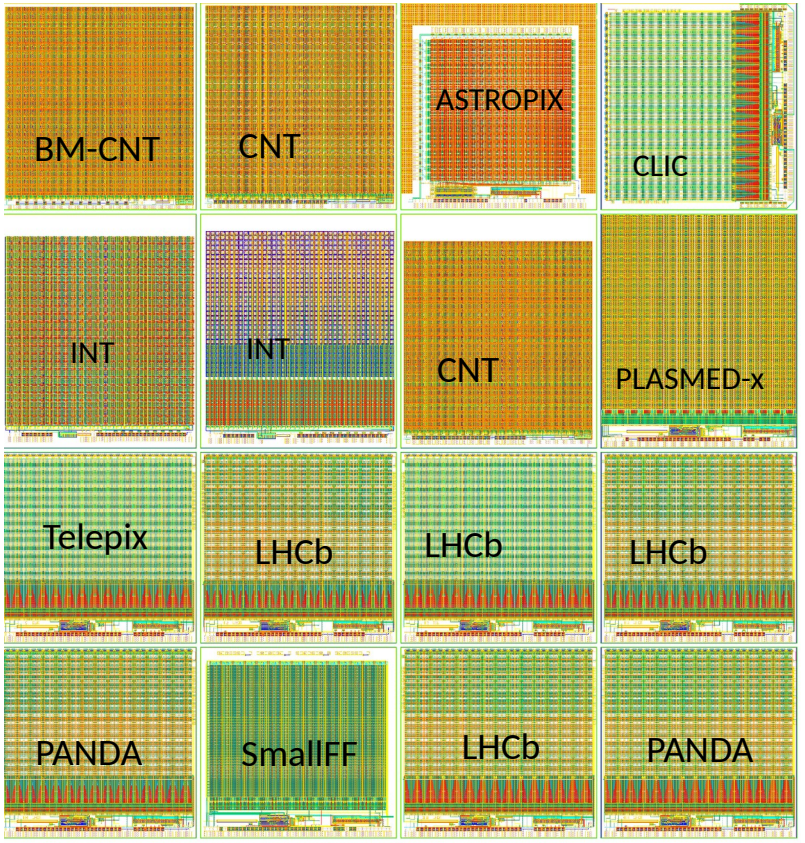




Milestone: Multi-Project Run2020

14/16 chips in context of the Verbund-project

- “PANDA”: large dynamic dE/dx range
- Telepix: high spatial resolution with trigger-output for new DESY beam telescope
- MightyPix: several lo power chips with large pixel sizes → LHCb
- Counting / Integrating Sensors for high rate applications (→beam monitor)
- “Small Fill Factor” design: pixel 25 x 35 µm



submitted last week to TSI (180nm)

- Common readout interface (→ synergies)
- Many different circuits (amplifiers, comparators, etc.) implemented

Another submission (engineering run) is planned for 2021

Plans for 2021-2024 (Bo, HD, KIT)

- Continue generic R&D on monolithic pixel sensor R&D, keeping in mind applications in different particle physics areas (→ community) and related fields
- Further improve performances (energy-, spatial-, time resolutions) and add more features (e.g. system requirements)

Technologies:

- TSI (AMS) 180 nm HV-CMOS
  - relatively “cheap” and good availability
  - very successful process
- 130 nm SiGe BiCMOS IHP (Frankfurt/Oder)
  - better signal to noise (bipolar transistors) and higher density
  - time resolution of 50 ps demonstrated by Geneva group (arXiv:1908.09709)
  - first design studies already started

Note: funding is required for **designers**, **chip submissions** as well as for **characterisation studies** (→ personal, → travel costs for test beams)