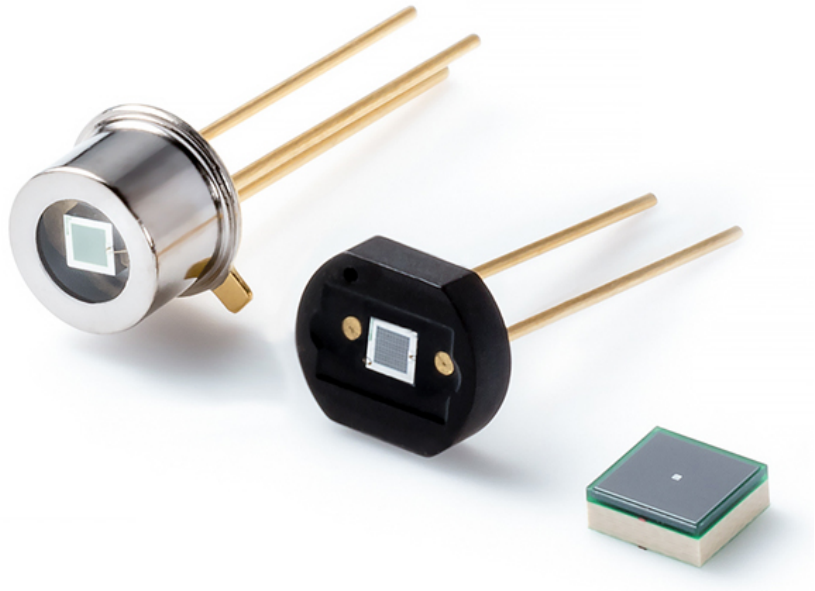
KLauS ASIC development in Heidelberg

Z. Youn, Y. Munwes, W. Shen, Hans-Christian Schultz-Coulon

KIP, Heidelberg University

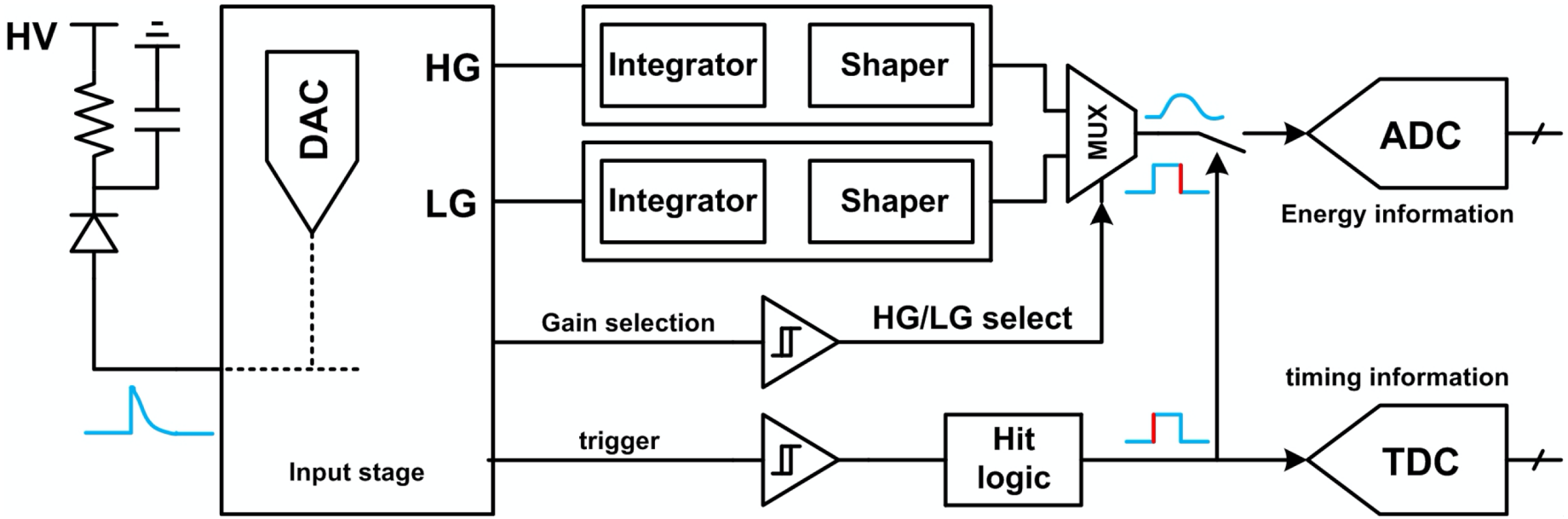
Application: imaging calorimeter

- **Requirements on the readout electronics**
  - **Auto-triggered, fully integrated: Front-end + Digitization**
  - **Low noise & high dynamic range charge measurement**
    - SiPM gain calibration for small pixel device
    - Up to 150 MIPs (~4000 ph.)
  - **Low power consumption**
    - No active cooling
    - 25 µW/Ch with **power-pulsing**
  - **Timing resolution better than 1ns**



- **KLauS: K**anäle für die **La**dungsauslese von **S**ilizium-Photomultipliern
  - Development started in 2010
  - KLauS-4 : mixed-mode version with ADC, received on 2016.12, successful beam test
  - **KLauS-5** : full 36-channel, BGA package available, integrated on the HBU
  - KLauS-6 : submitted in 2020.02

KLauS-5: 36-channel SiPM readout ASIC – analog part



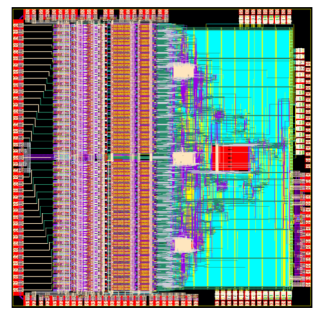
Can select:

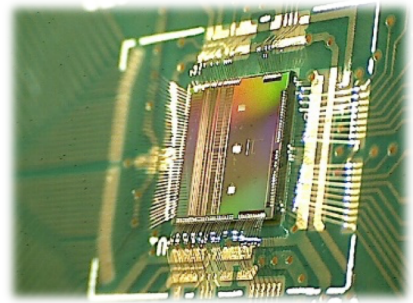
HG or MG

LG or ULG

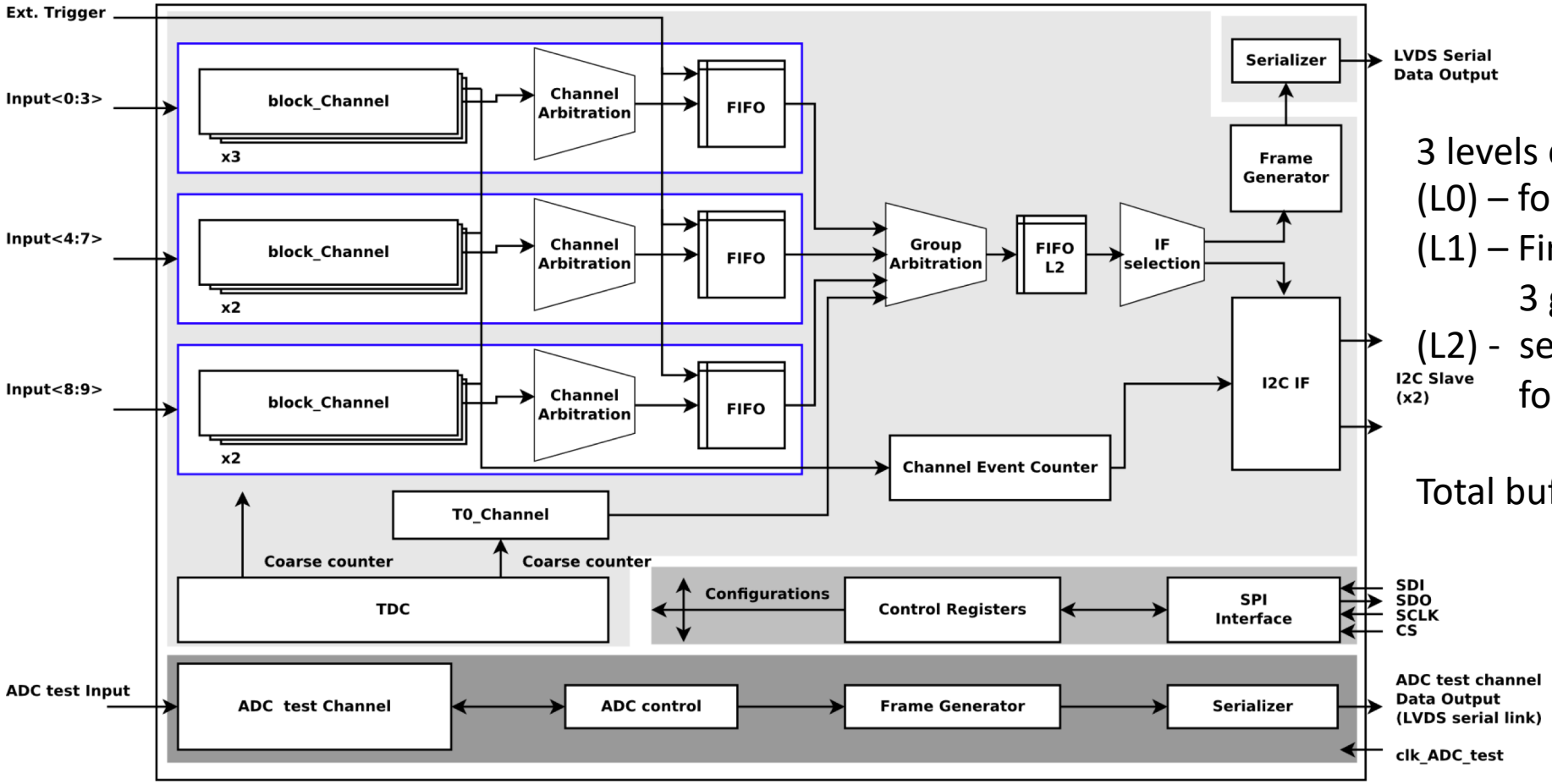
- **Two gain branches:**
  - **High gain branch: SiPM gain calibration for small pixel device**
  - **Low gain branch: Extend the input charge range**
- **ADC (channel-wise):**
  - **10-bit SAR: physics mode**
  - **12-bit Pipelined: SiPM gain calibration mode for small pixel device**

UMC 180nm CMOS





KLauS-5: 36-channel SiPM readout ASIC – digital part



3 levels data storage:

(L0) – for each ch 2 hits depth

(L1) – First level fifo buffer
3 groups of channels, 64 hits depth

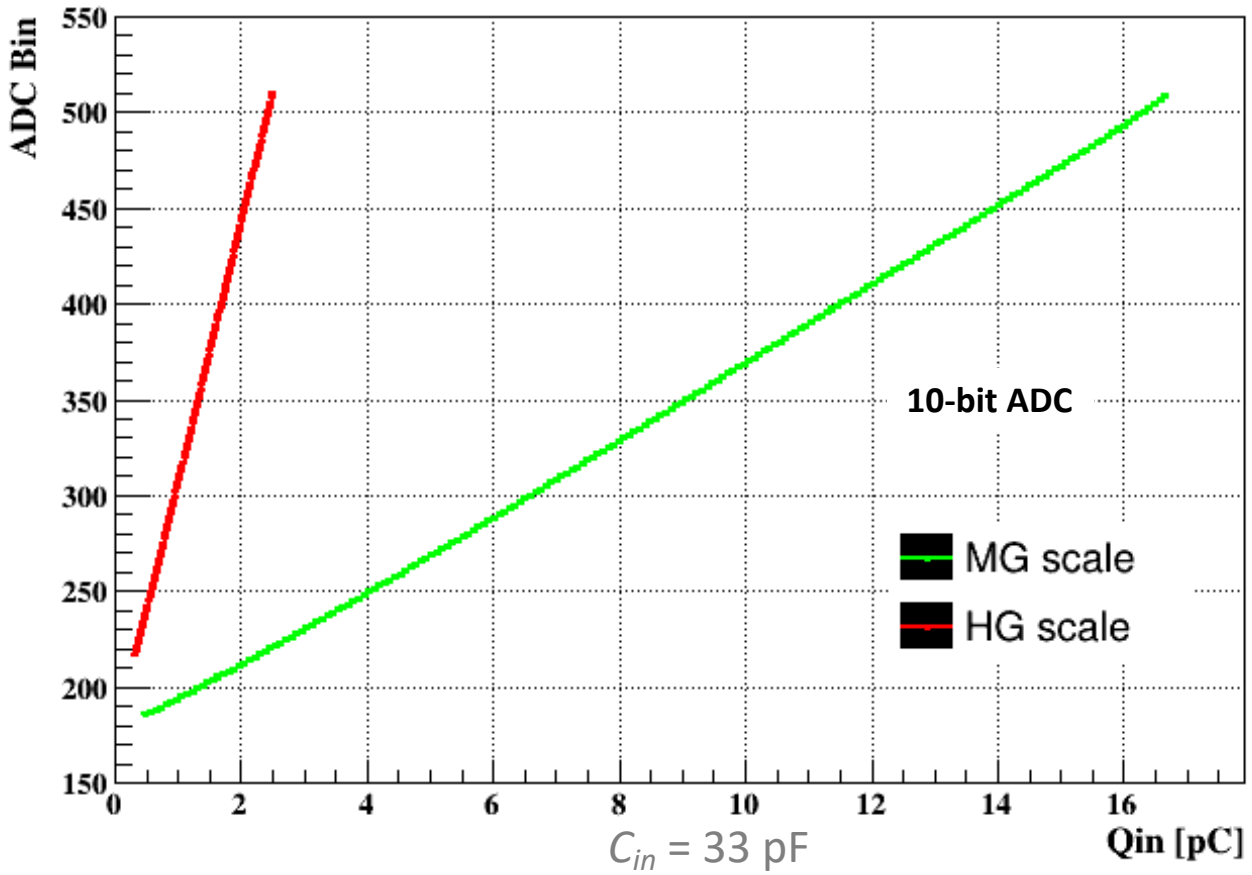
(L2) - second level fifo buffer
for all channel groups, 128 hits depth

Total buffer size 330 hits

Precise charge measurements

- **Equivalent Noise Charge (ENC) :**
  - **6fC @ C_{in}< 100 pF, HG scale**
- **Charge injection measurements**
- **Dynamic Range:**
  - **Limited by the ADC range**
  - **Within $\pm 1\%$ Full Scale Range Linearity**
  - **ULG scale extends to 460pC**
  - **Stable in working temperature range**

High gain branch



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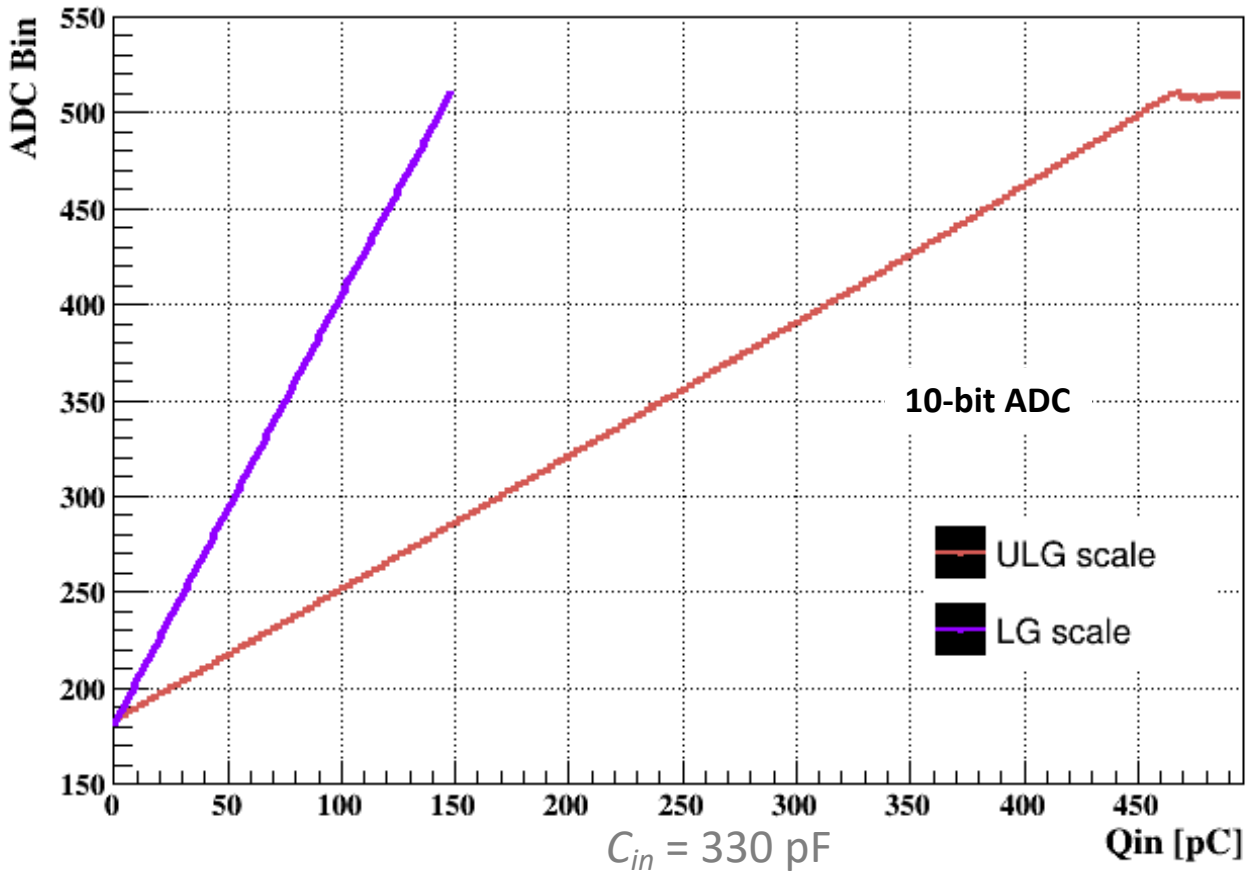
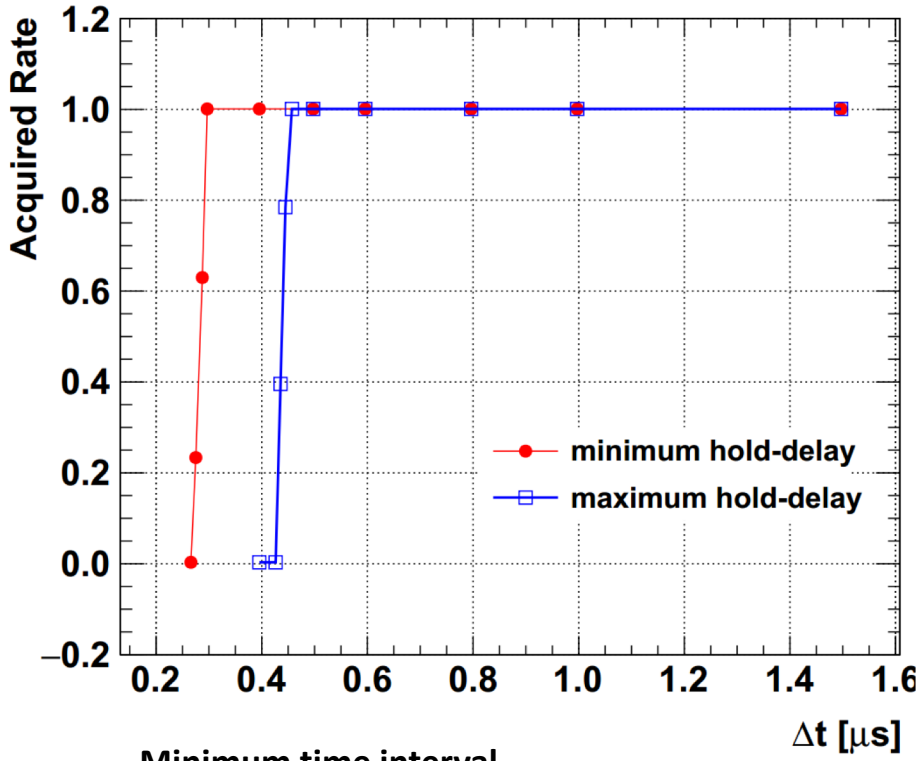
Low gain branch



C_{in} = 330 pF

Maximum event rate

- **Limiting factors:**
  - **Analog FE and ADC:**
    - hold-delay, sychronization, and ADC conversion time
    - Event with time interval smaller than around **500ns** to prevous hit may miss
  - **digital FIFOs throughput:** two level FIFOs to increase the averaged throughput
    - L1-FIFO limiting: minimum time interval is 900ns
    - L2-FIFO limiting: depending on readout speed

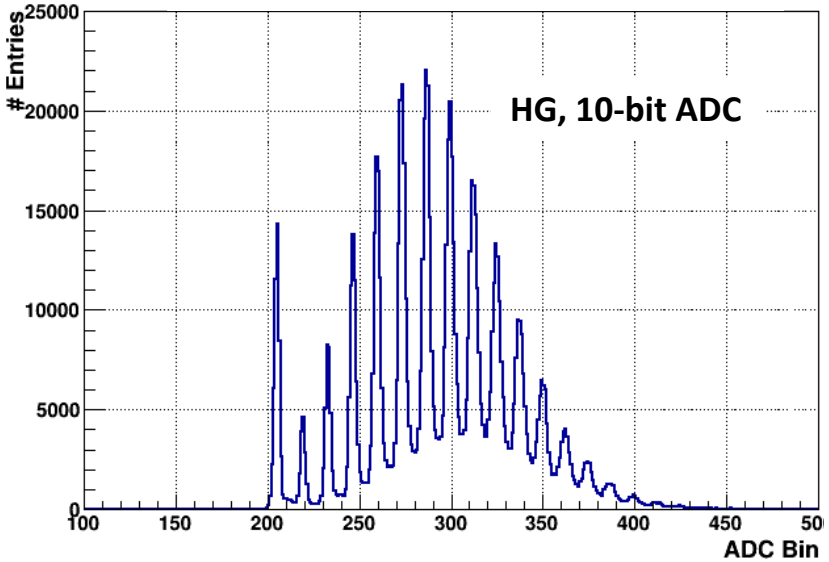


Minimum time interval
Only Analog FE and ADC considered

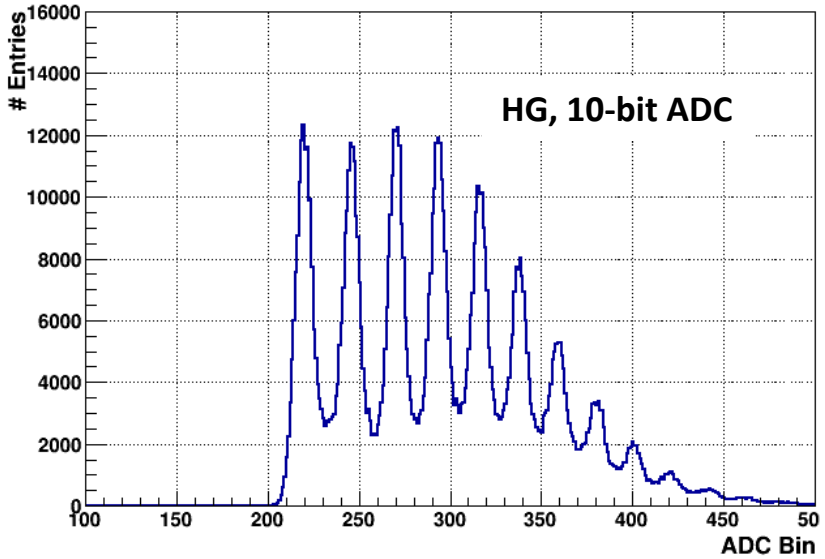
Single photon spectra

- **Sensor illuminated by a pulsed laser at 25°C, spectra recorded in auto-trigger mode**
  - **Pedestal and primary dark noise supressed**

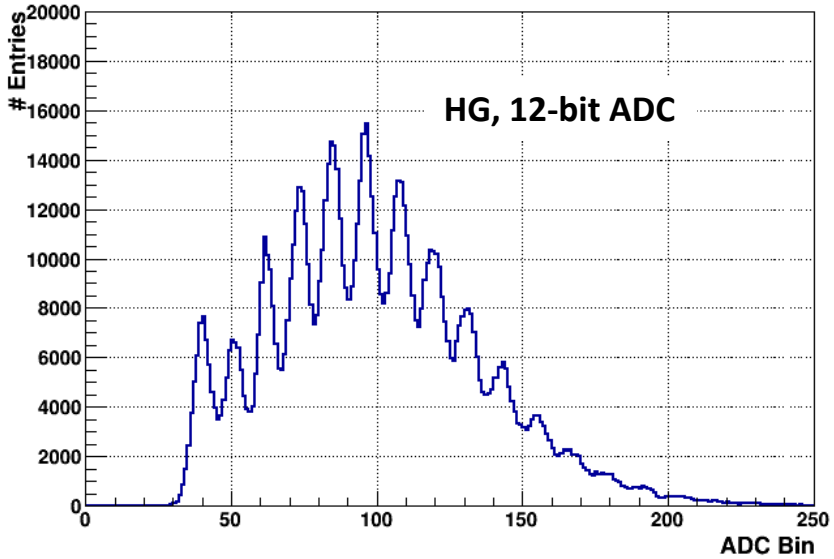
Hamamatsu S13360-1325CS
$1.3\times1.3 mm^2$, 25 µm pixel size
Gain = 7.0×10^5



Hamamatsu S13360-6050CS
$6\times6 mm^2$, 50 µm pixel size
Gain = 1.7×10^6



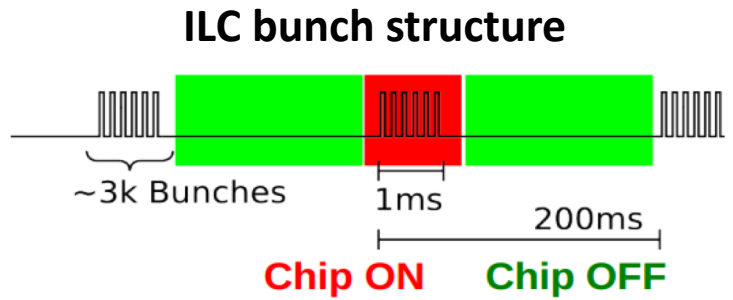
Hamamatsu S12571-010C
$1\times1 mm^2$, 10 µm pixel size
Gain = 1.35×10^5

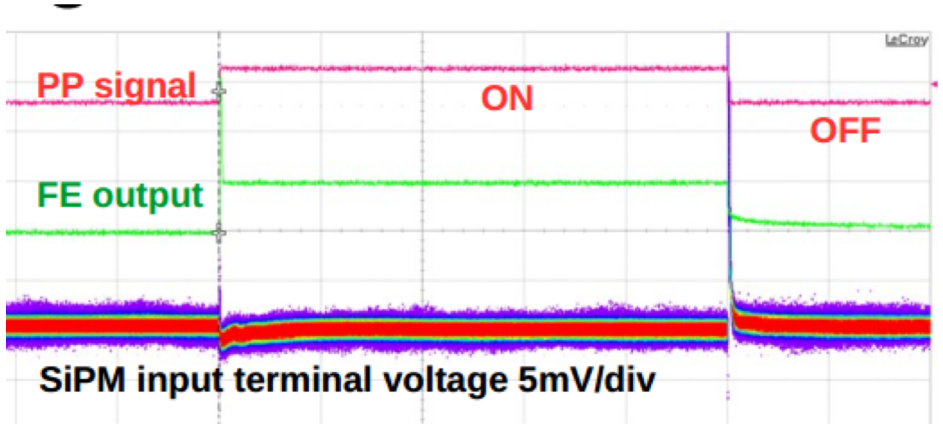


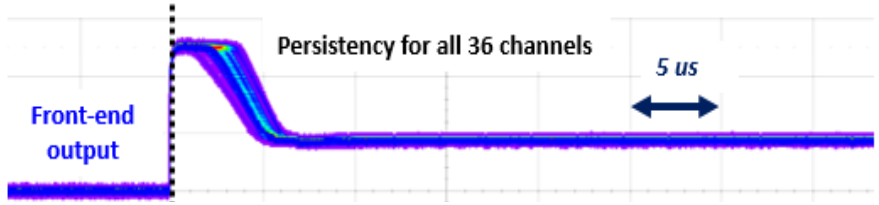
Power-pulsing functionality

- **Power-pulsing scheme**
  - **“ Turn off " ASICs when no beam (aquisition-off)**
  - **25 µW/Ch (>=0.5% duty cycle)**

- **Key design points:**
  - **Stable bias voltage at the SiPM input terminal**
    - Input stage works in sub-threshold region during the acquisition-off state
    - Changes smaller than 10mV max.
  - **Front-end fast setup**
    - Dedicated switching procedure
    - Stable 20us after acquisition-on (±0.5% error)







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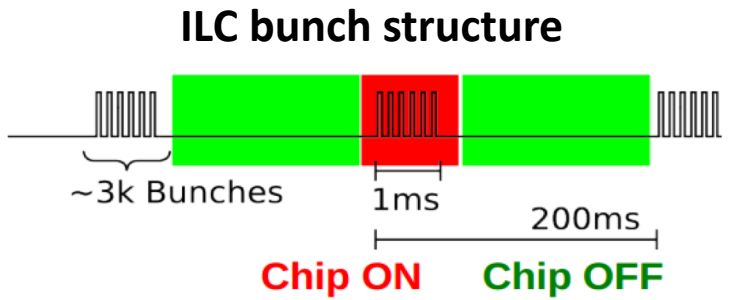
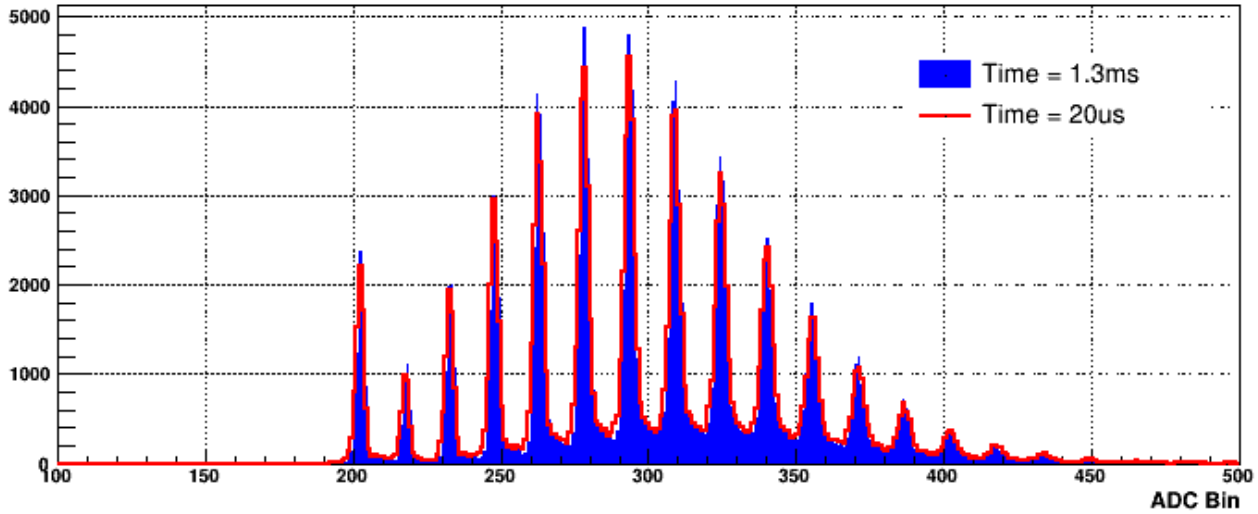


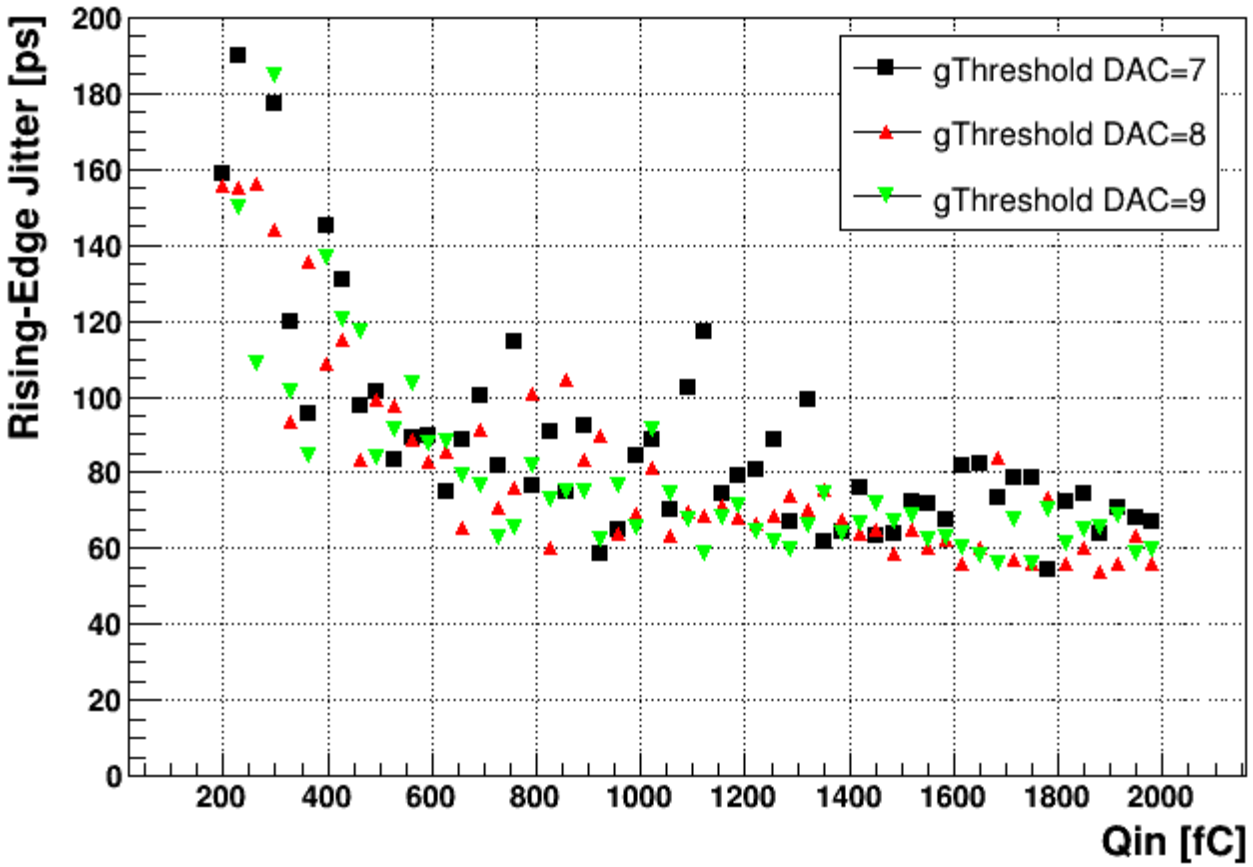
- **Single photon spectra at different time**
  - **No changes in the SiPM gain (input DC stable)**
  - **Small pedestal displacement at 10 ~20 µs**
    - From ~20 µs on, no visible pedestal shift



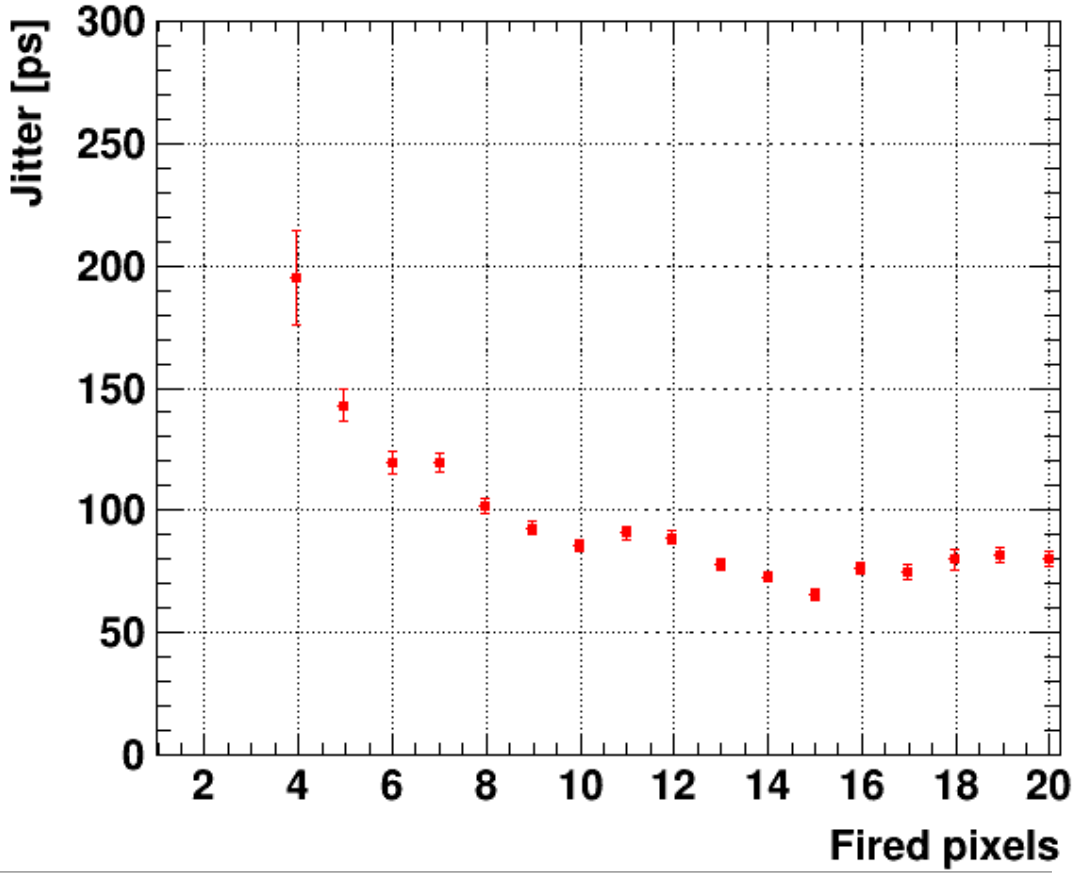
- **Power consumption:**
  - **20 µW/Ch for analog domian**
    - 2.5mW/Ch X 0.5% + 7.6µW/Ch
  - **Power-pulsing for digital parts will be implemented in next version**

Timing resolution

- **Front-end jitter ~ 60ps(sigma)**
  - Charge injection

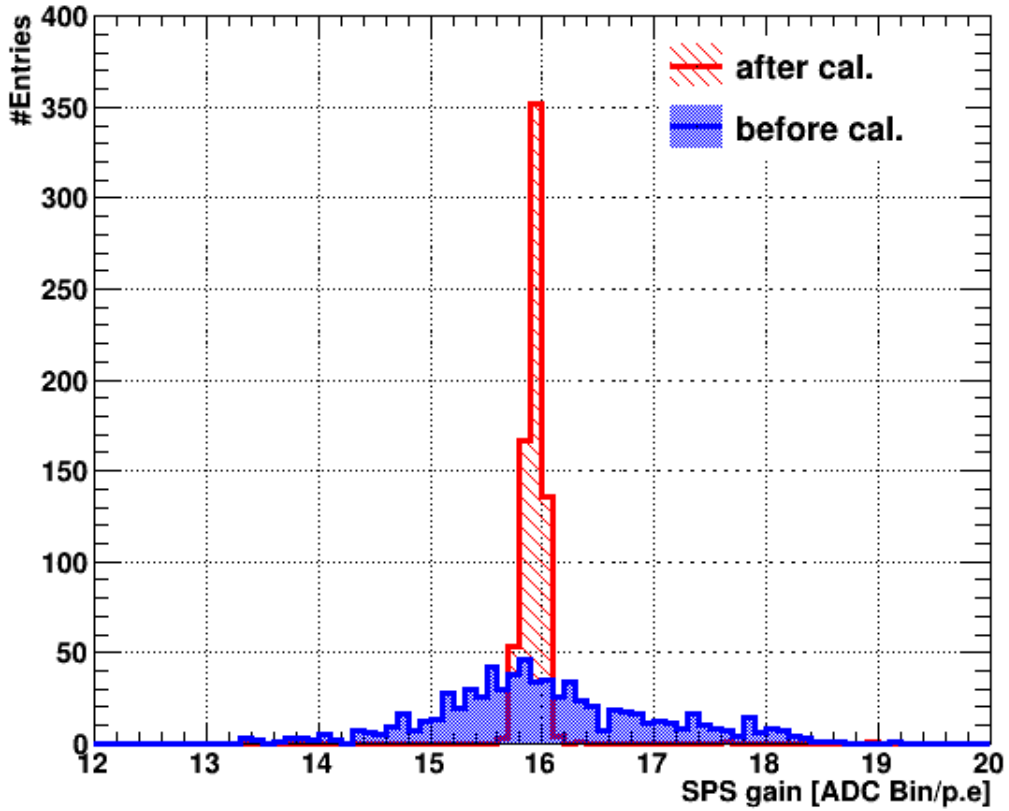


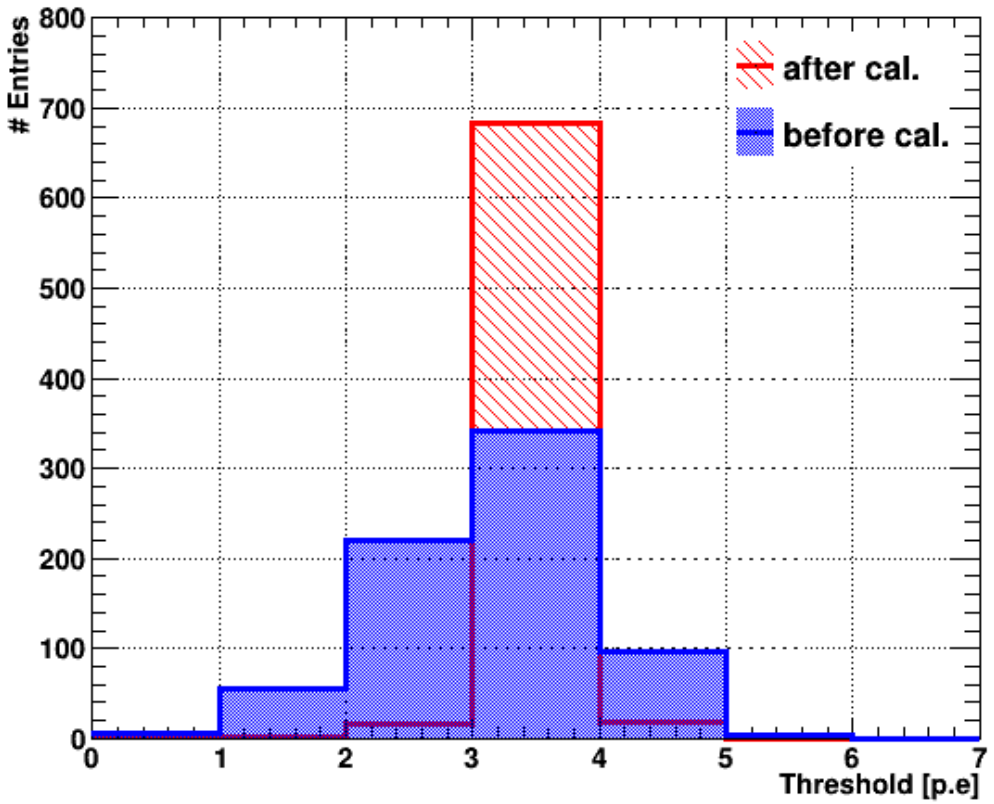
- **Front-end jitter ~ 80ps(sigma)**
  - With MPPC S13360-1325PE, laser



Automatic calibration test

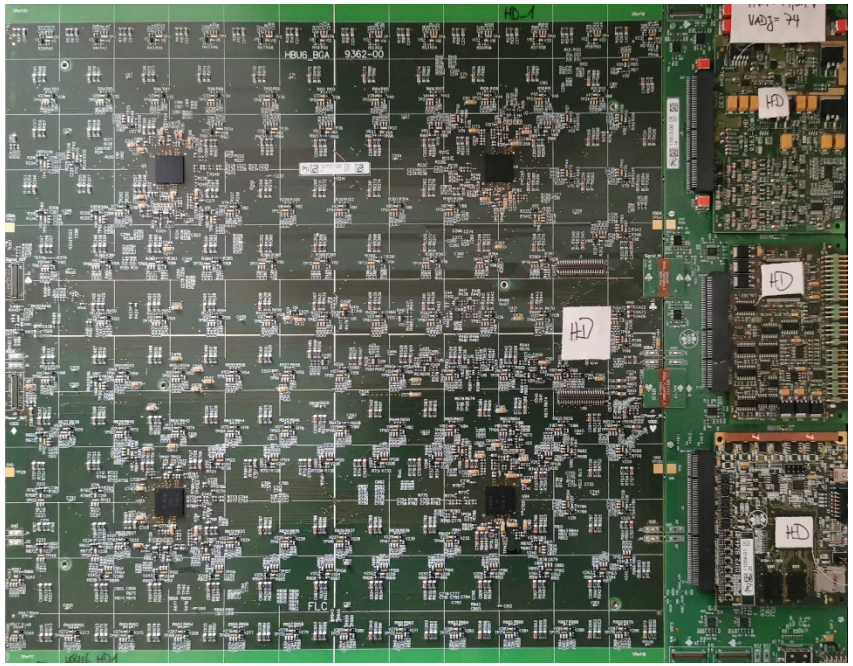
- **ASIC calibration procedure to deliver uniform SPS gain and threshold (2h per chip)**
  - **Config parameters: SiPM bias DAC, threshold DAC, hold-delay DAC**
  - **20 chips tested: SPS gain within +/-1.5%, 94% channels in target threshold level.**

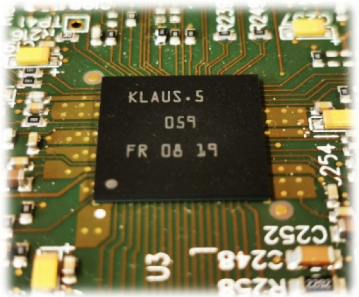


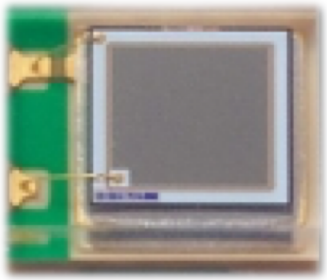


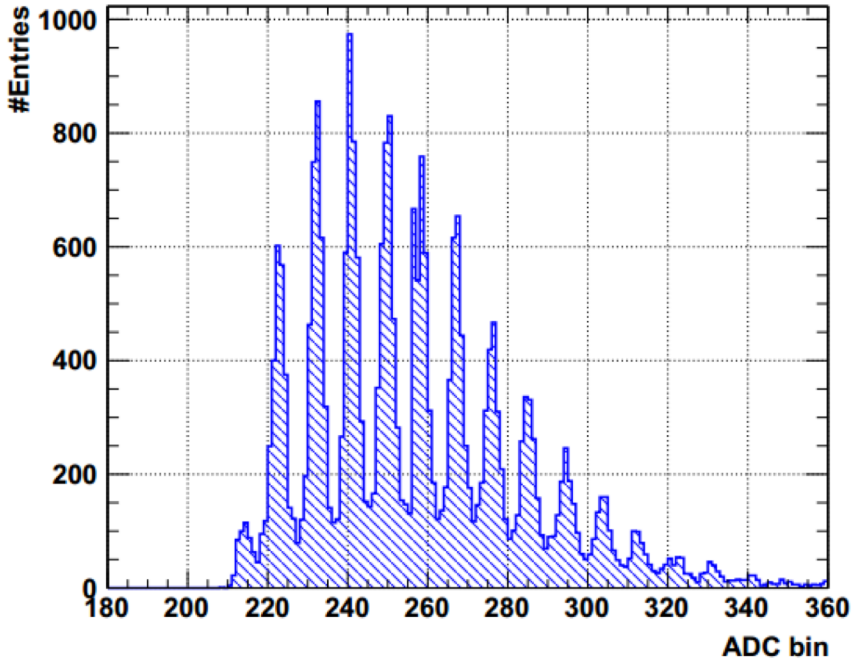
New AHCAL HBU with KLauS ASIC

- The KLauS-HBU with KLauS-5 (BGA package):
  - All HBU hardware and labview software are re-designed and prepared by DESY/FEB
  - USB readout scheme for the first debuging step
  - New SiPM sensor with smaller pitch, Hamamatsu S14160-1315PS
  - Scintillator tiles partially assemled, cosmic moun test on-going



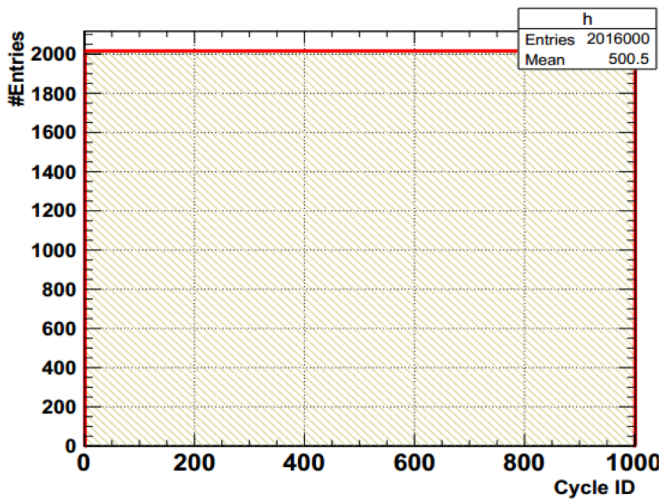




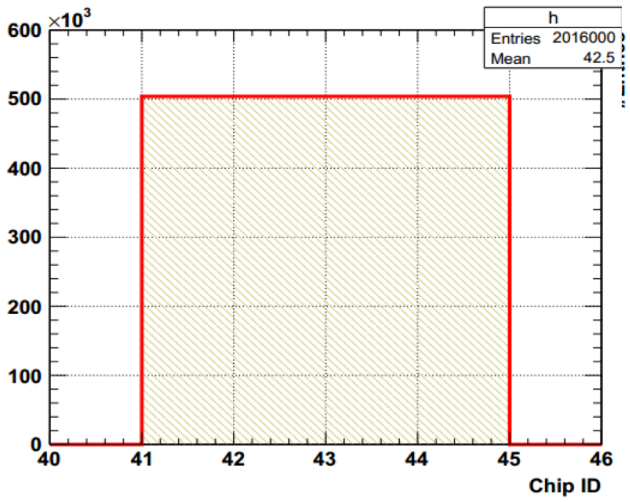


DAQ data integrity

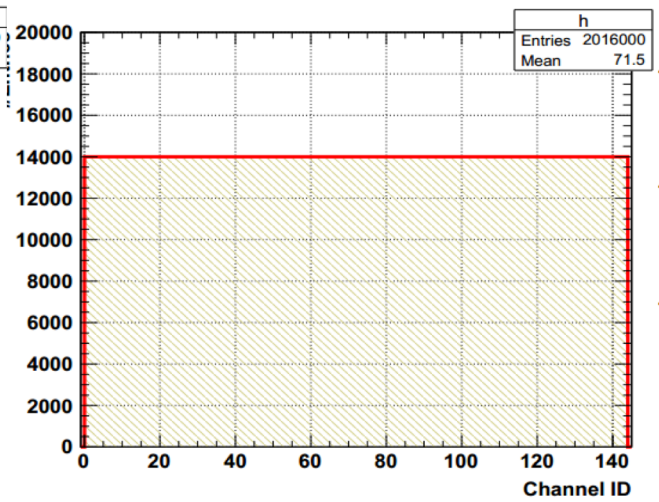
- One HBU, External-trigger model, 1000 cycles, 14 evts/cycle, 8us time interval
  - Data integrity confirmed!



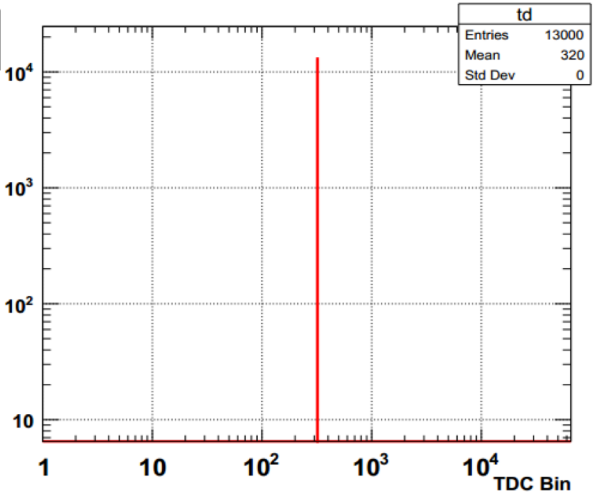
Events per cycle



Events per chip



Events per channel

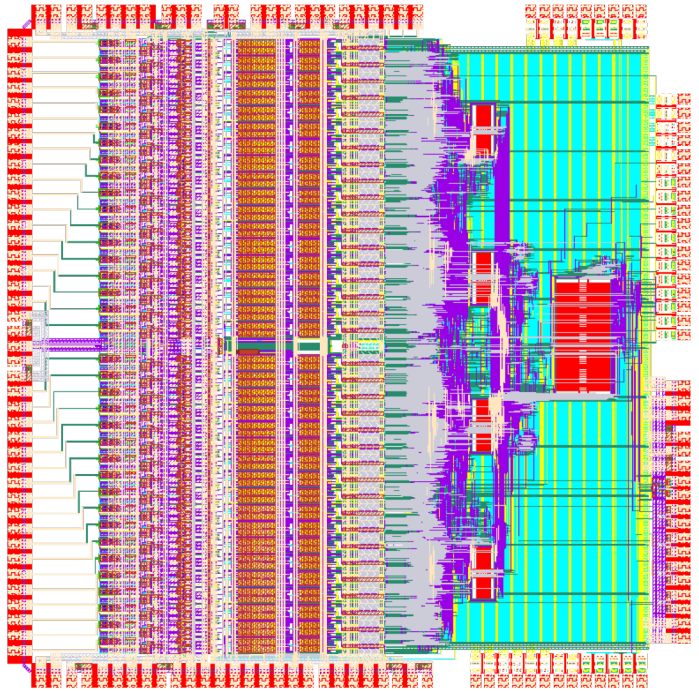


TDC value for events of the same cycle

Development of the KLauS-6

- **Main modifications:**
  - **Channel-wise PLL-based TDC with bin-size downto 200ps**
  - **Power-gating in the digital part to fullfil the power constraint**

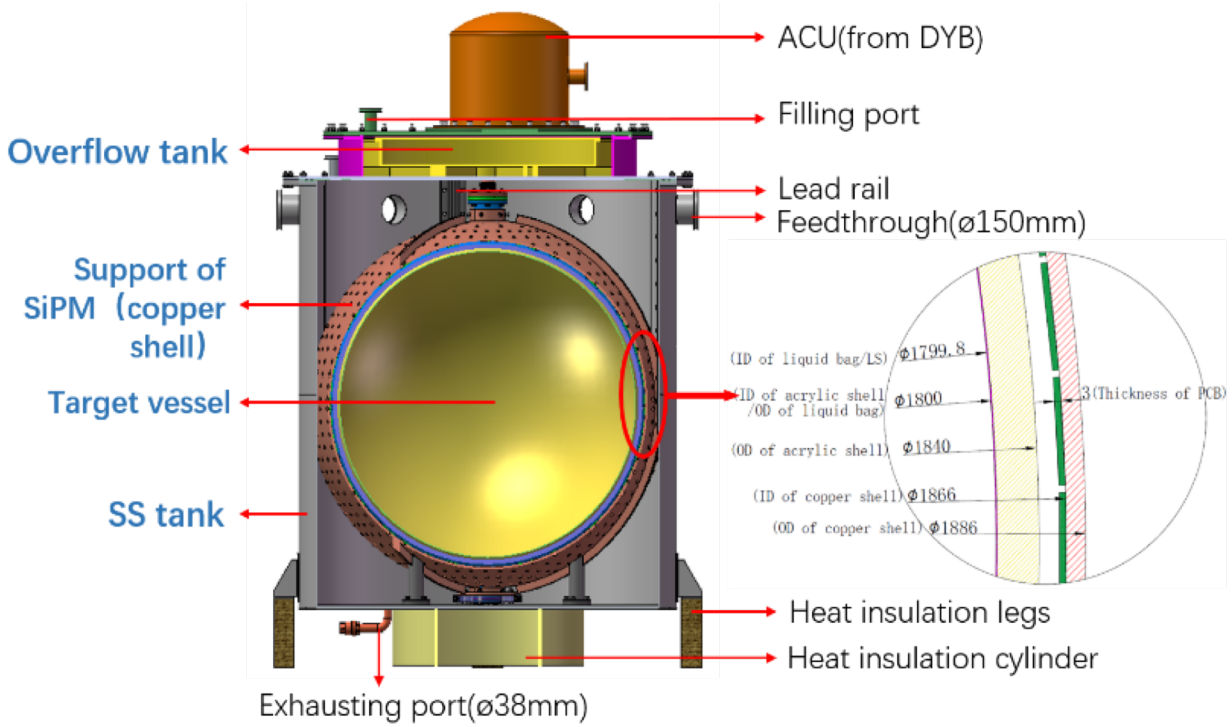
- **Status:**
  - **First submission on 2019.07 but with failure**
    - Misconduct the fabrication process from the Mixed-mode/RF process to the BCD process, no NMOS in the analog parts.
    - By the manufacturer
  - **Re-submitted on 2020.02, except on 2020.07 (next week?)**



Other activities (slides from Wei Shen)

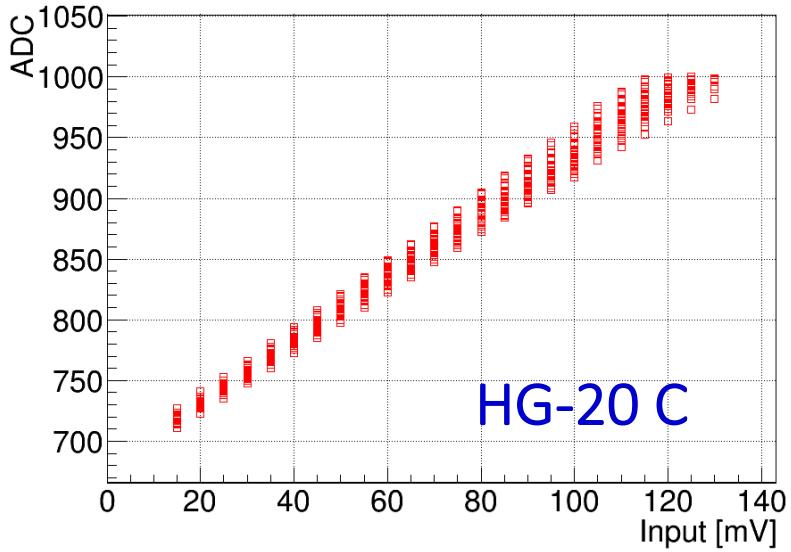
- **TAO** – Taishan antineutrino observatory, Reference Detector for JUNO neutrino experiment
- Main goal is determining neutrino mass hierarchy by precisely measuring the energy spectrum of reactor electron antineutrinos at a distanceof ~53 km from the reactors.

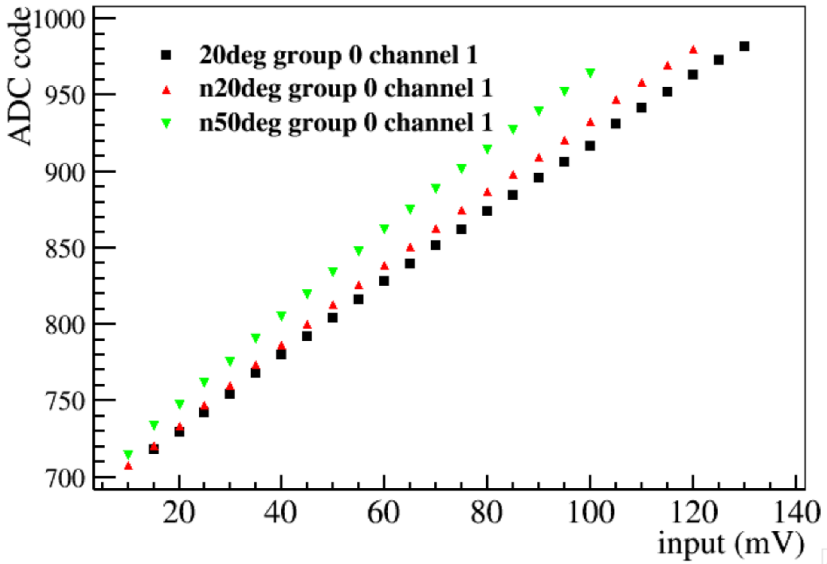
- SiPMs readout at -50 degrees, ~2m diameter liquid scintillator sphere



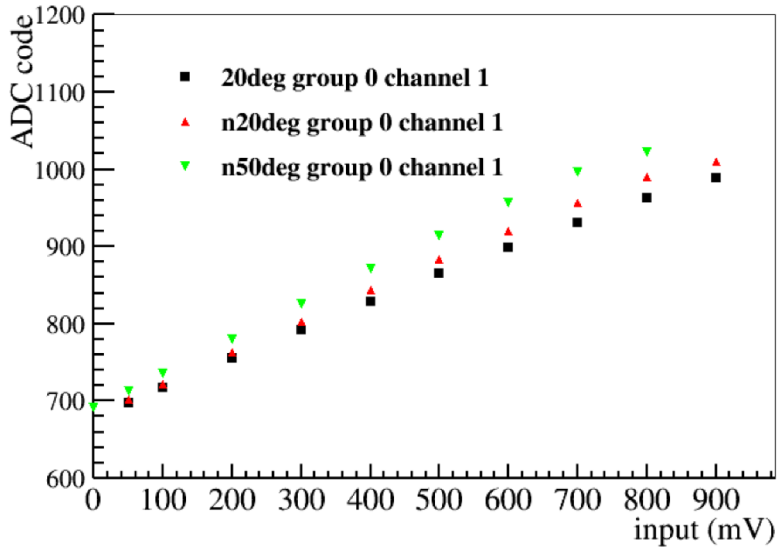
Charge injection test

- **HG and MHG with charge injection**
  - **Temperature: 20 C to -50 C**





HG-ch1

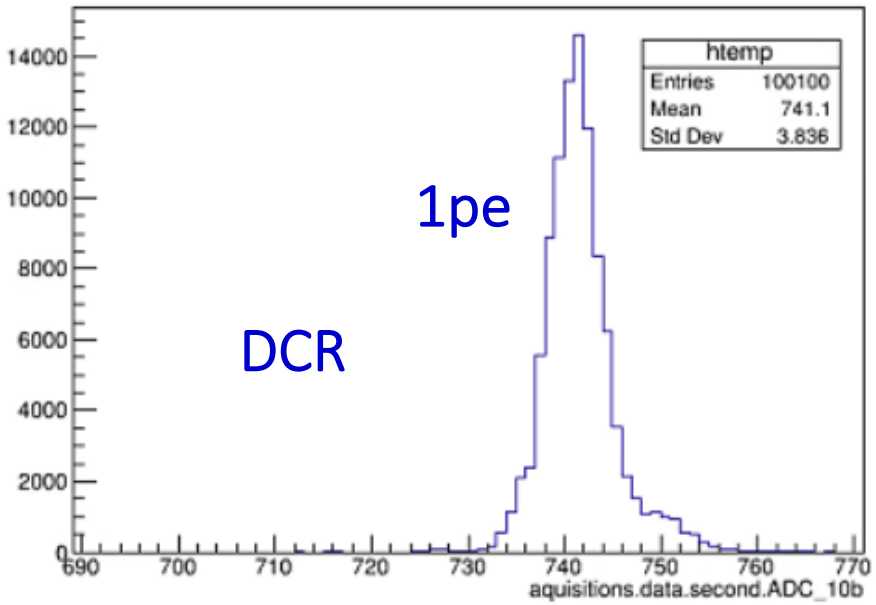


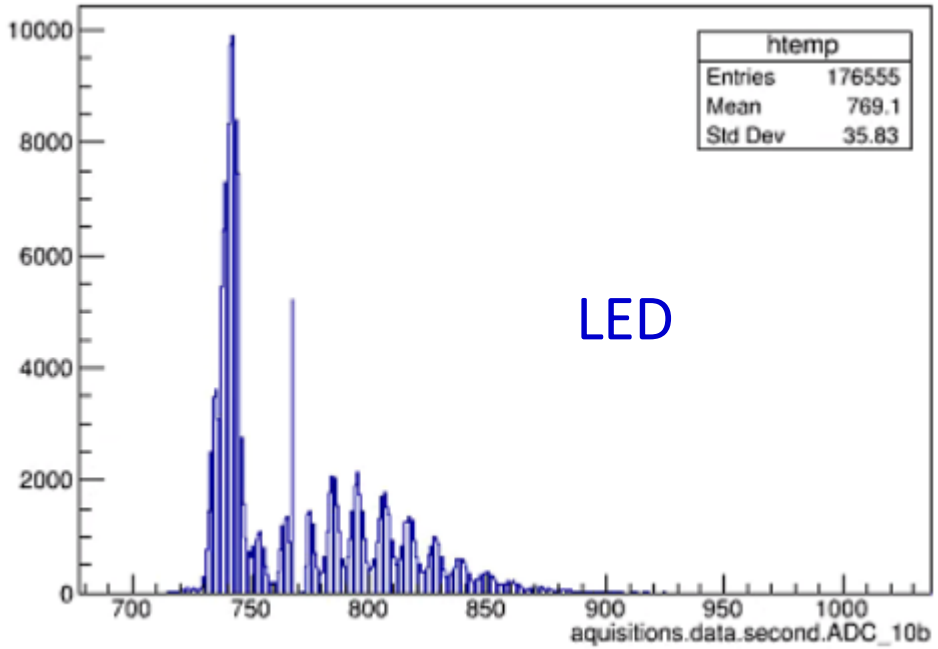
MHG-ch1

SiPM test

† **Hamamastu vuv4 array test, 2x 6mm x 6mm, with ch1**

- **Over voltage: 1V**
- **Temperature: ~-50 C**
- **Hold delay: 6-0**
- **Threshold: 7-5**





Conclusion and future plan

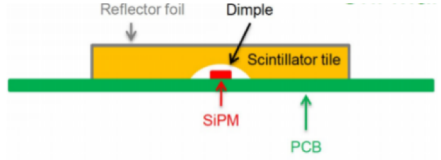
- **Current 36-channel KLauS5 ASIC**
  - **Working well and fulfilling the design requirements**
  - **High dynamic range up to 460pC(LG branch) and low ENC of 6fC(HG branch)**
  - **Single pixel spectra for SiPM down to 10µm pixel size, or large area device**
  - **Good timing resolution under low power consumption**
  - **BGA packaged KLauS5 ASIC ready**
  - **New HBU equipped with KLauS5 ASIC**

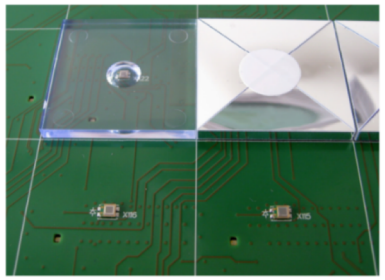
- **Next submission for KLauS6:**
  - **Power-gating for the digital parts**
  - **New 36-channel ASIC with TDC binsize down to 200ps**

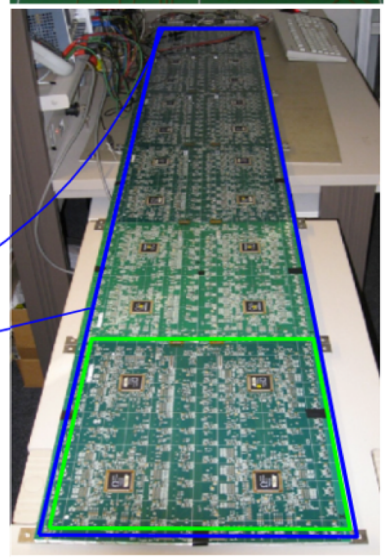
Back up

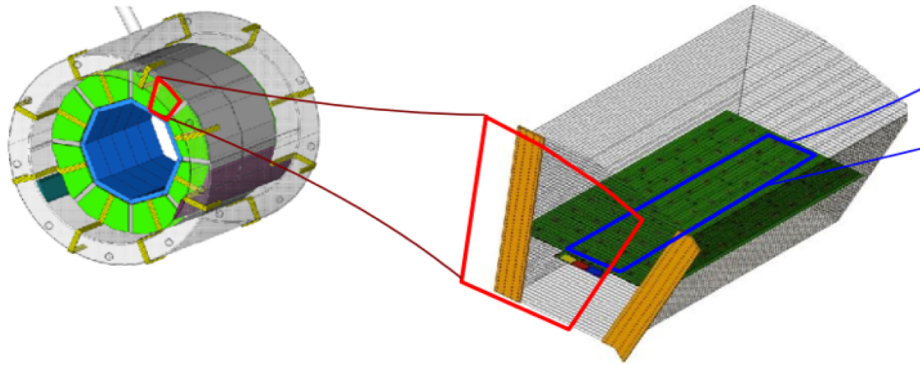
Application: imaging calorimeter

- **Analog Hadronic CALorimeter(AHCAL) (ILC, CALICE collaboration)**
  - **Sandwich structure: steal absorber, scintillator + SiPM readout**
  - **8M channels for AHCAL barrel**

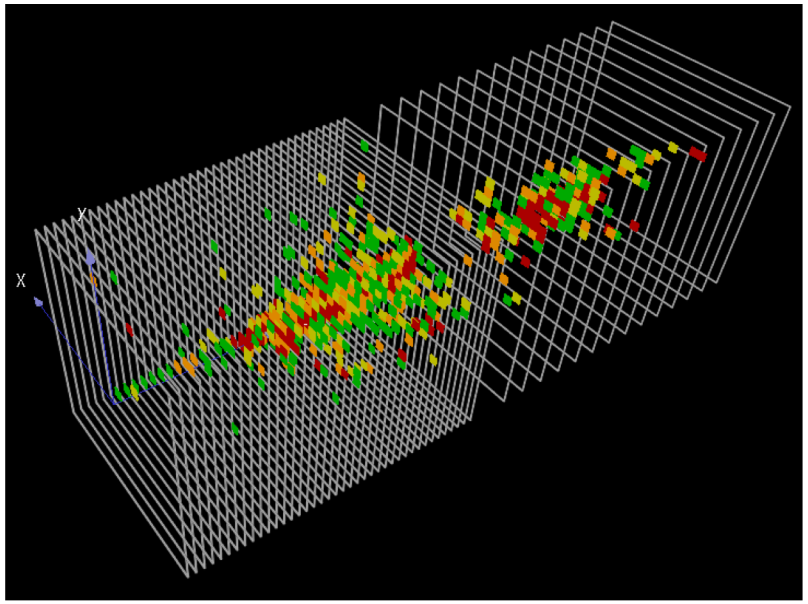






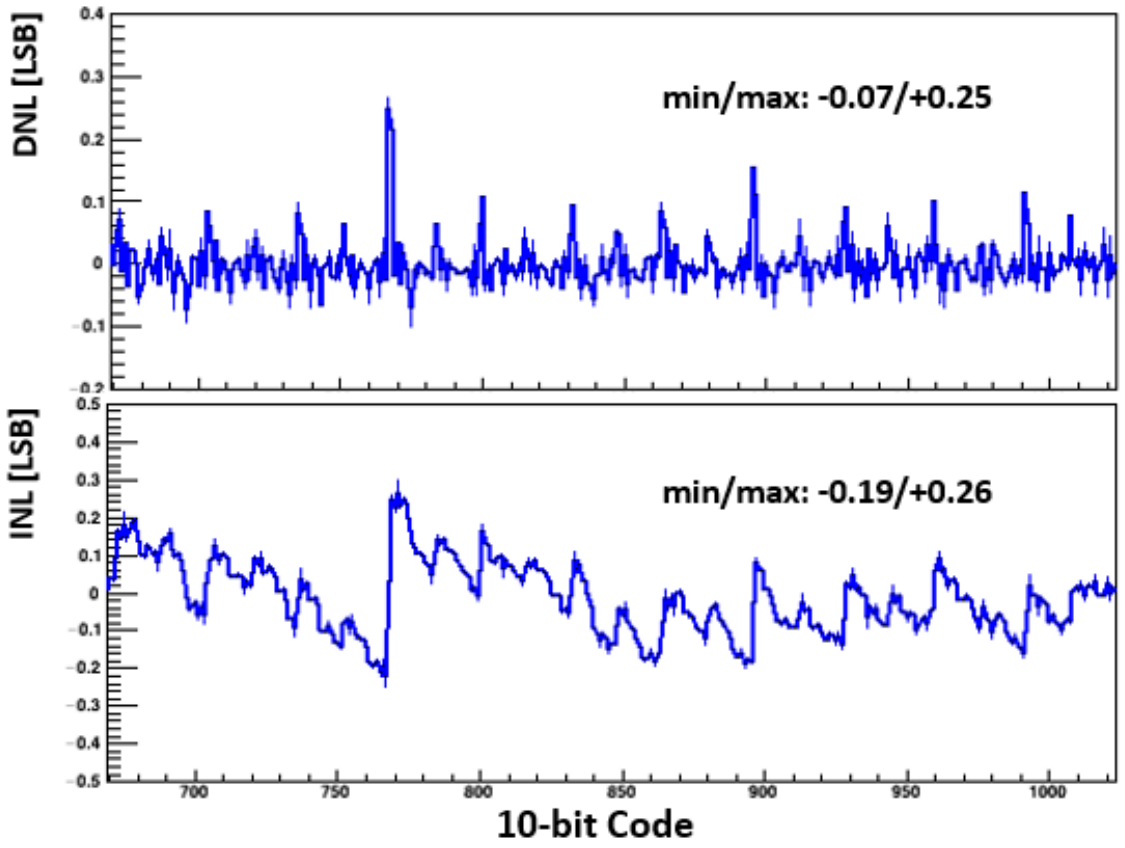


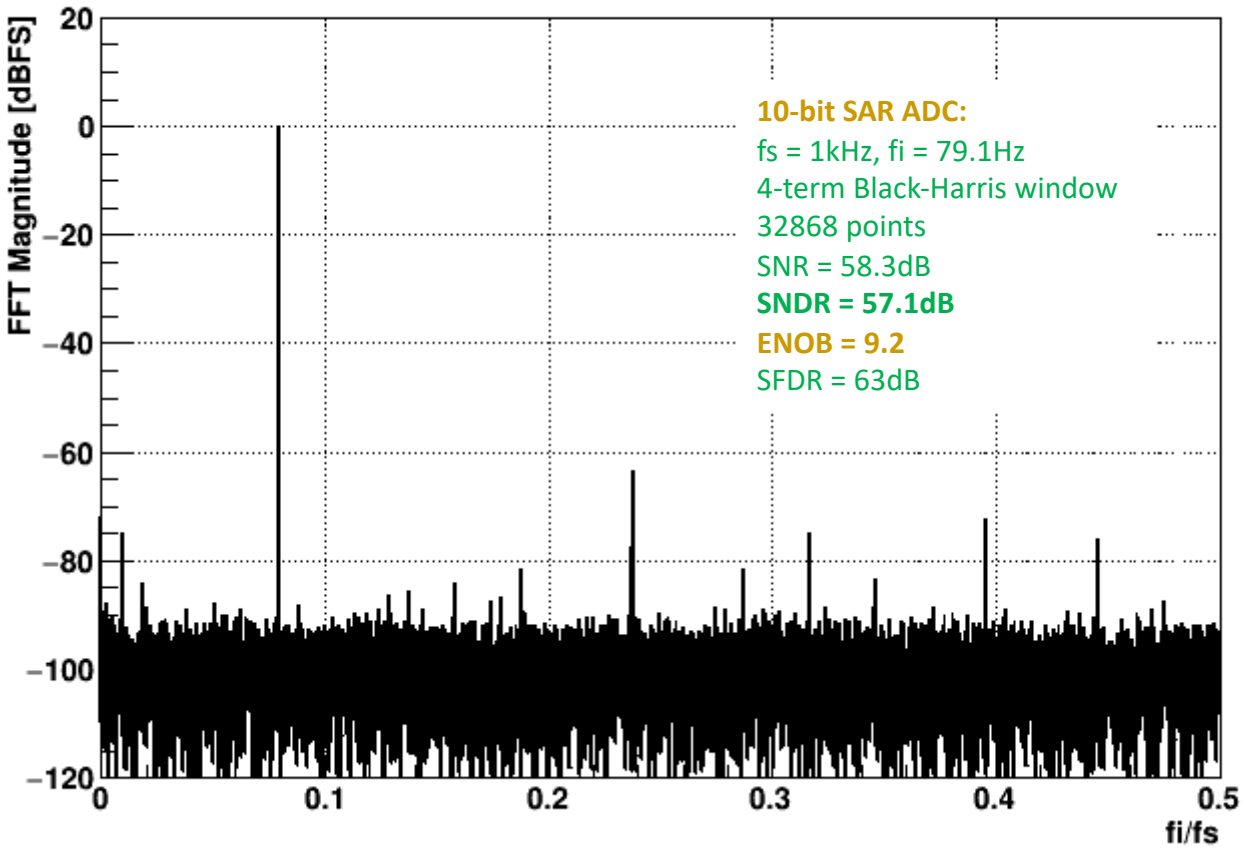
AHCAL technical prototype, 2018



ADC performance

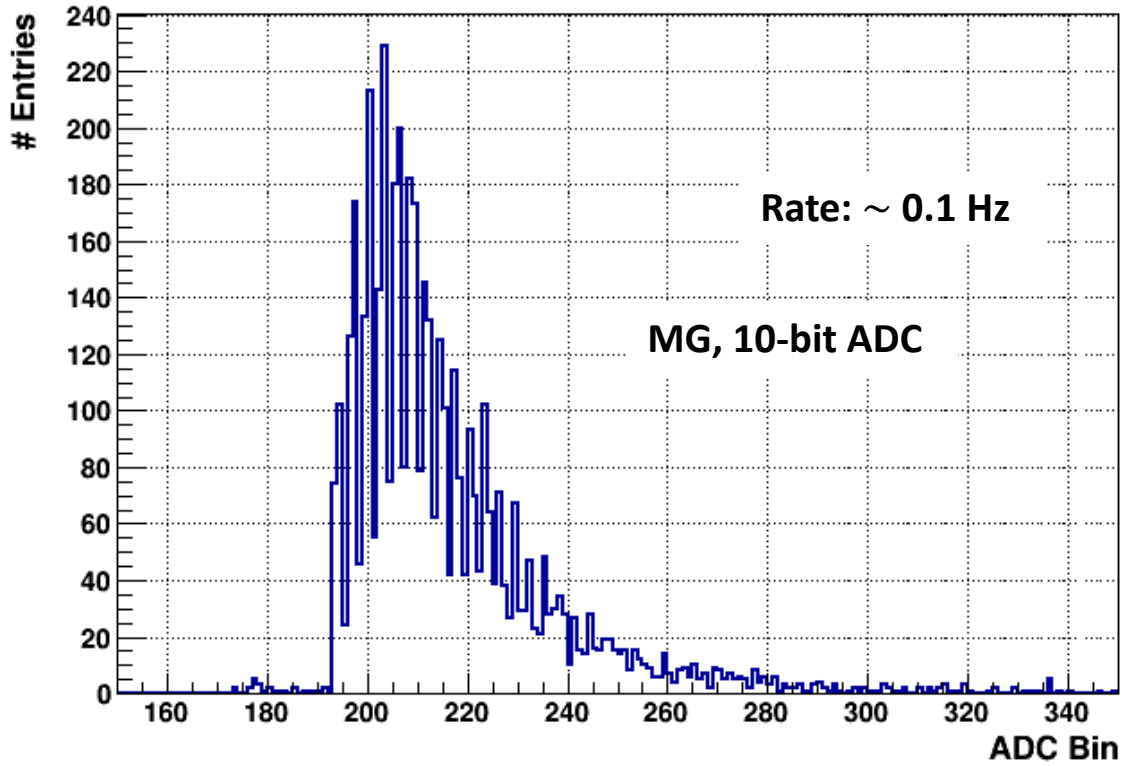
- **Linearity:** differential/integral non-linearity for the region of interest
- **Dynamic performance**: ENOB ~ 9.2bit





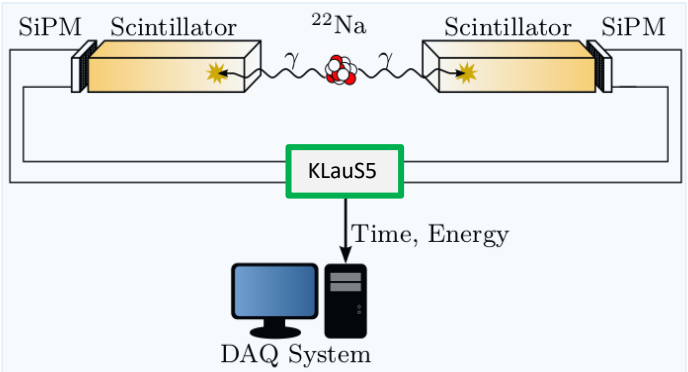
Cosmic ray test

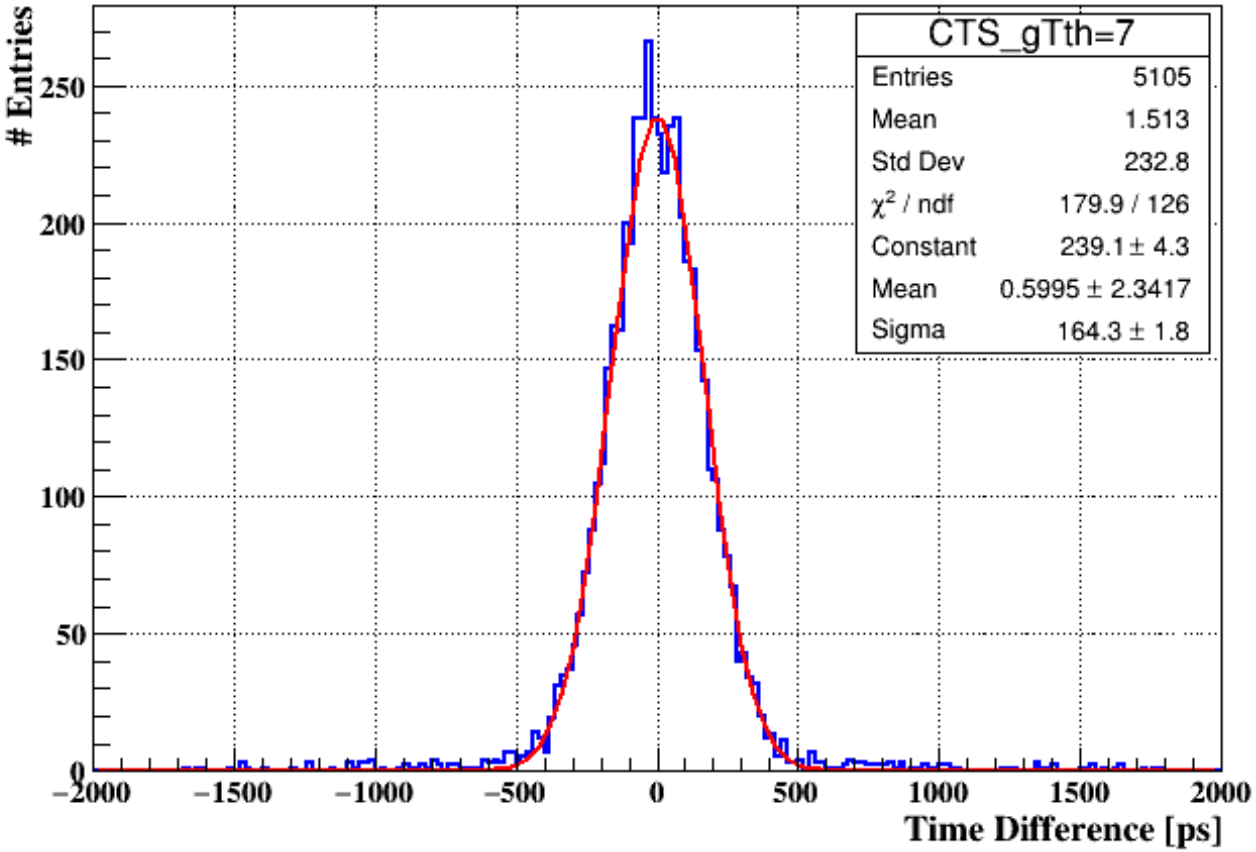
- **On-chip coincidence logic in KLauS ASIC**
  - **External validation**
  - **Internal validation: 12 channels in same group**
- **Cosmic ray test with scintillator + SiPM setup**
  - **Trigger threshold ≈ 5 ph., DCR of serveral Hz**
  - **Coincidence enable, window ≈ 75ns, internal**
  - **Old AHCAL detector setup**
    - **3×3 cm^2 scintillator**
    - **Large noise from the old sensor**



Timing resolution

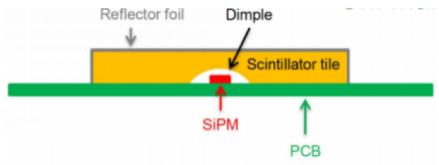
- **Front-end jitter ~ 60ps(sigma)**
- **CTR Measurements (T=15°C):**
  - **Scintillator: LYSO:Ce,** $3.1\times3.1\times15mm^3$
  - **SiPM: Hamamatsu MPPC S12643-050CN(X)**
  - **Energy resolution: ~11.5%**
  - **CTR(FWHM) = 387ps @ 2.5mW/Ch**
- **TDC binsize 200ps for next version**

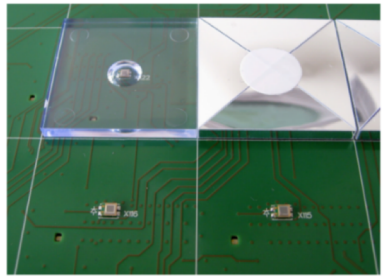




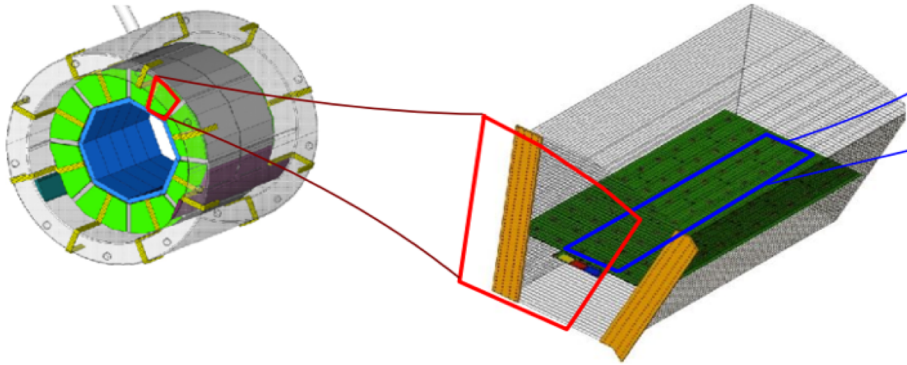
Application: imaging calorimeter

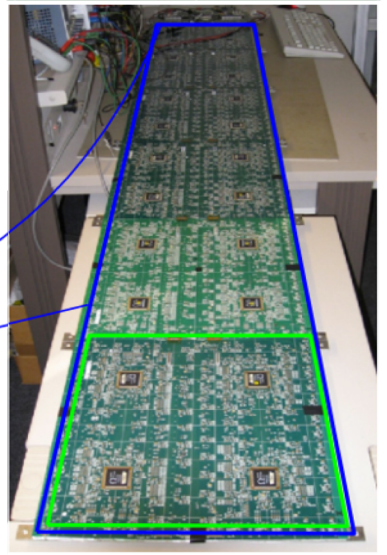
- **Analog Hadronic CALorimeter(AHCAL) (ILC, CALICE collaboration)**
  - **Sandwich structure: steal absorber, scintillator + SiPM readout**
  - **8M channels for AHCAL barrel**



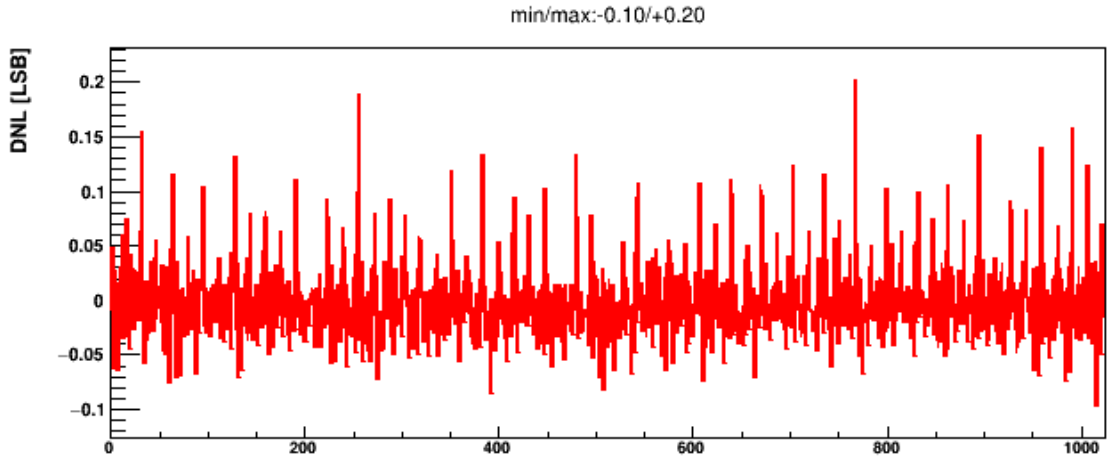


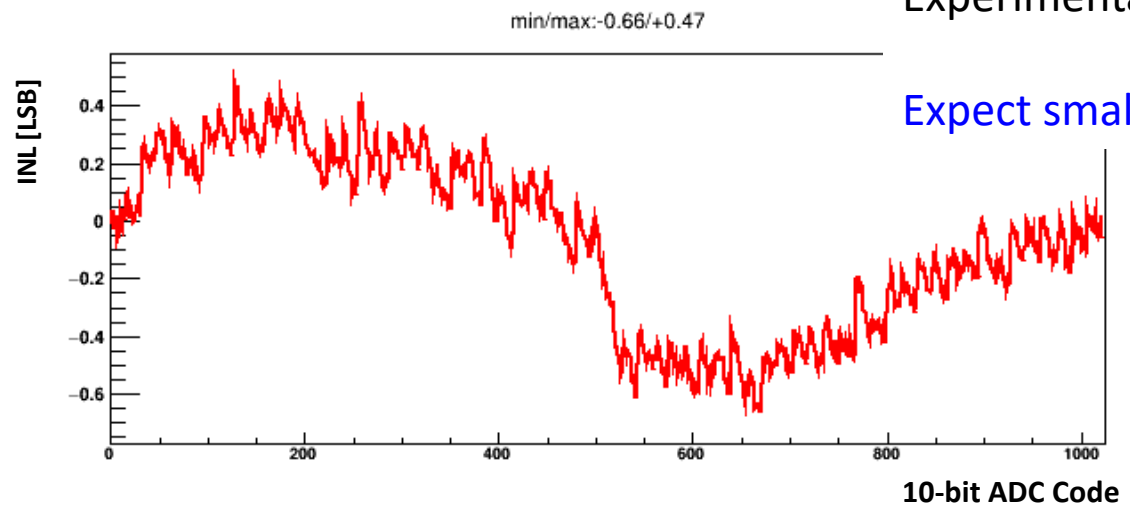
- **Requirements on the readout electronics**
  - **Auto-triggered, fully integrated: Front-end + Digitization**
  - **Low noise & high dynamic range charge measurement**
    - SiPM gain calibration for small pixel device
    - Up to 150 MIPs (~4000 ph.)
  - **Low power consumption**
    - No active cooling
    - 25 µW/Ch with power-pulsing
  - **Timing resolution better than 1ns**





ADC full range non-linearity





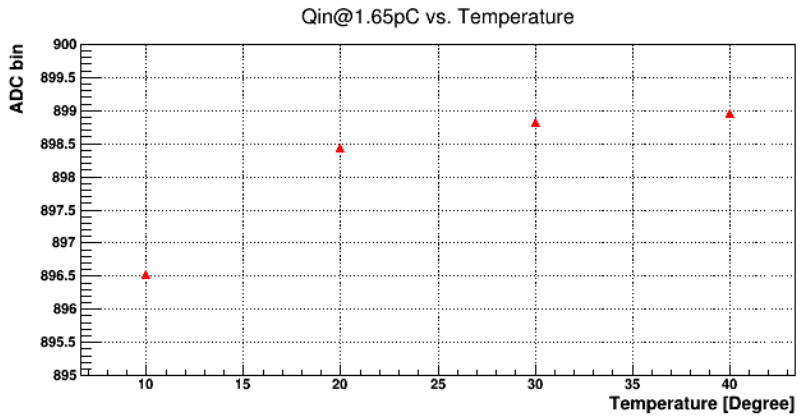
Experimental setup is not optimized.

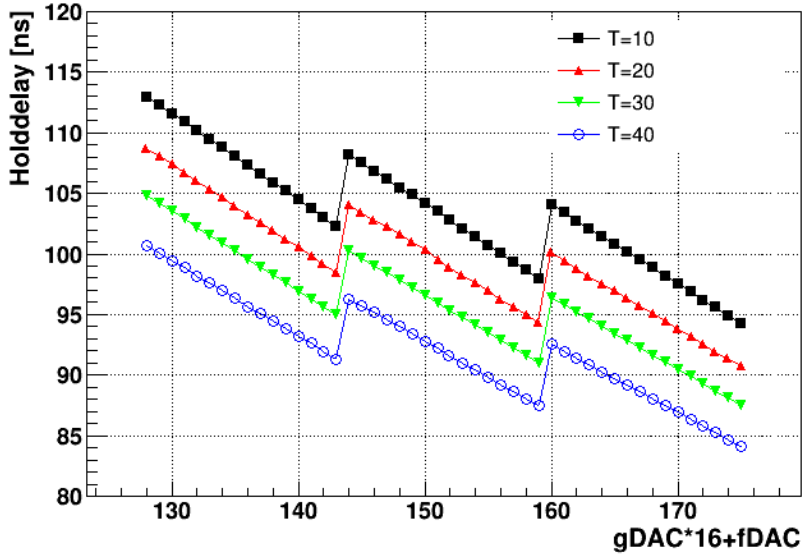
Expect smaller INL

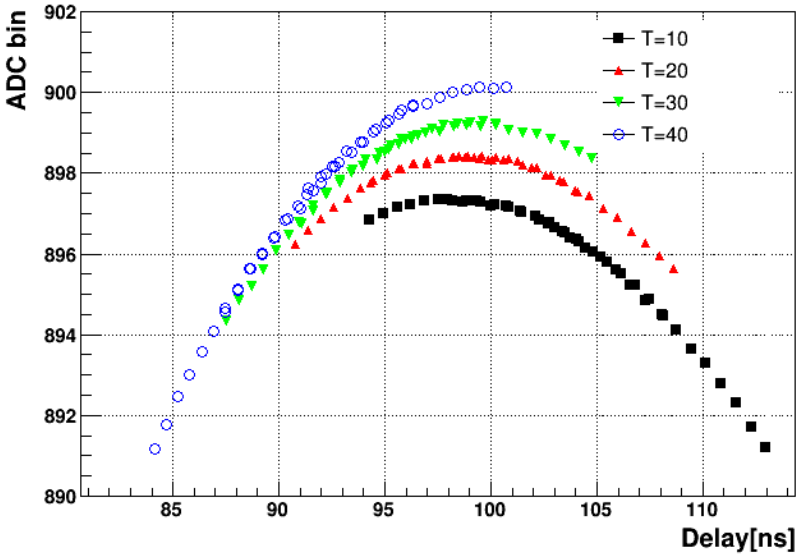
Full-chain @ different temperature

- **Charge injection tests under different Temp.**
  - **Changes smaller than 1% FSR range**

- **Possible sources for the changes:**
  - **Hold delay**
  - **peak time**
  - **Front-end output amplitude**



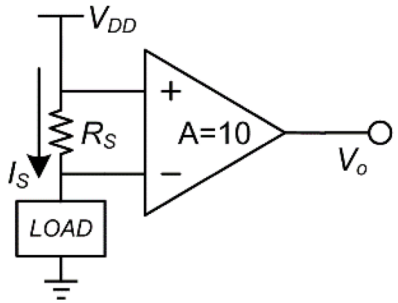




Power consumptions

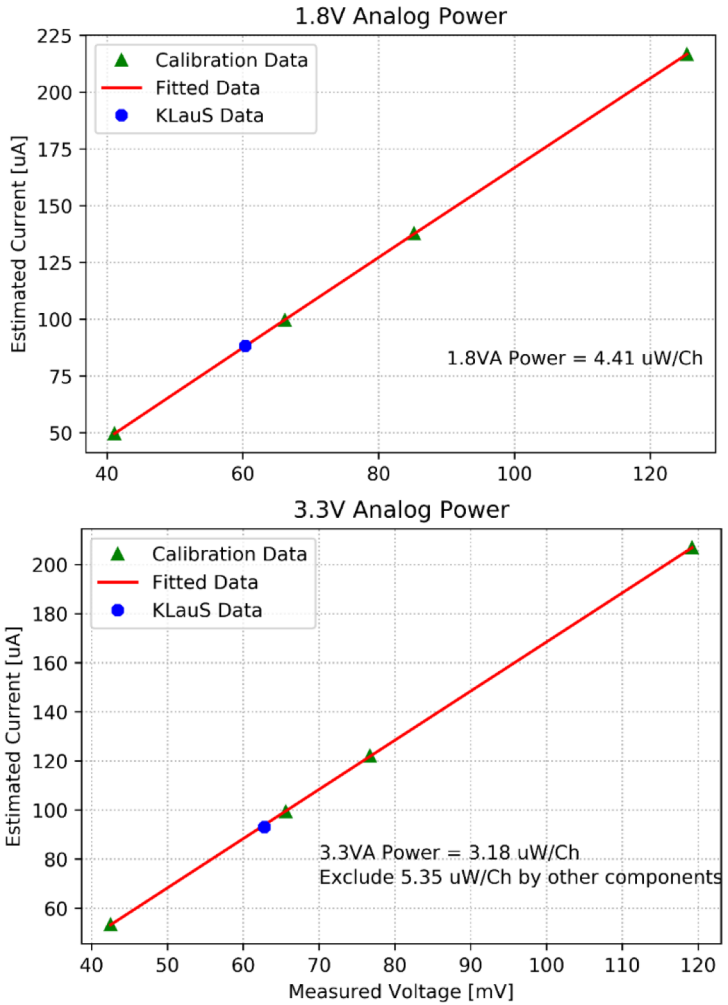
- **Measurements for the power of *acquisition-off* state**
  - **Setup calibrated: resistor, gain, offset**
  - **Exclude power from other active components**

- **Results:**
  - **Same for results under *acquisition-on* state**
    - **2.5 mW/Ch** (VA3.3 → 0.93, VA1.8 → 1.53)
  - **New results for acquisition-off state**



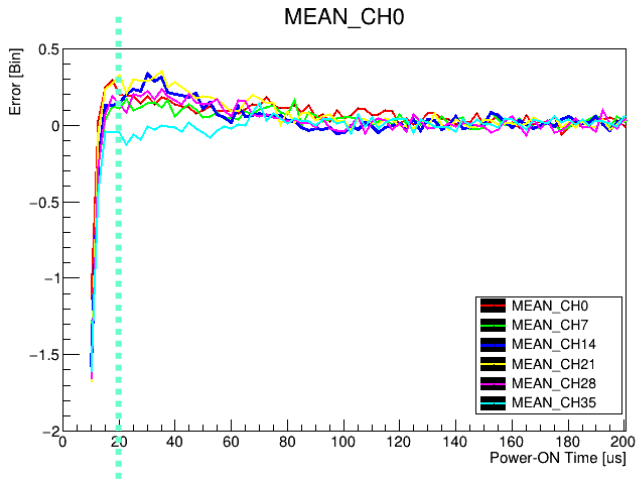
Name	Simulation	Measurement
3.3 V VA	3.78	3.18
1.8 V VA	3.63	4.41

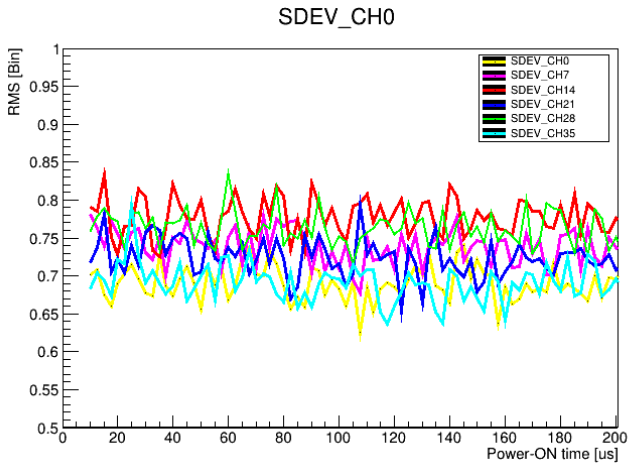
  - **Power-consumption under 0.5% power-pulsing duty-cycle:**
    - **20 uW/Ch** (for analog power only)
    - **5 uW/Ch budget left for TDC and digital parts (challenging)**



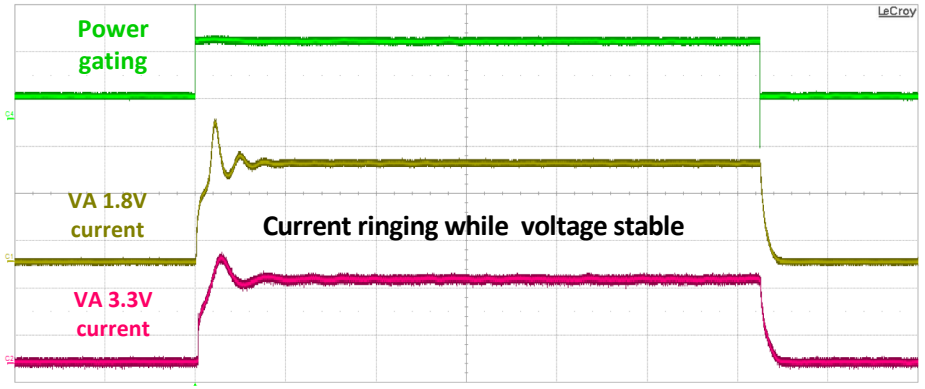
Power-pulsing

- **Pedestal stable 20us after power-on(error<±0.5%), 0.5% duty cycle reserved**

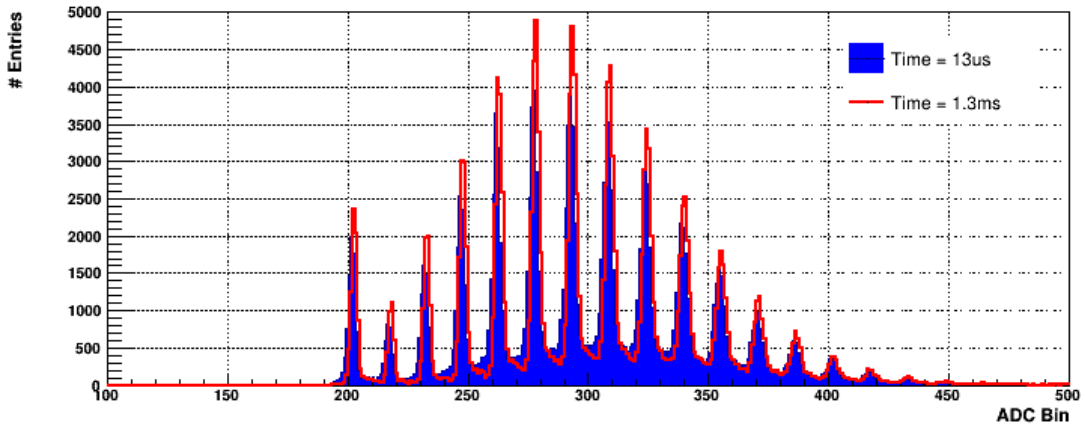




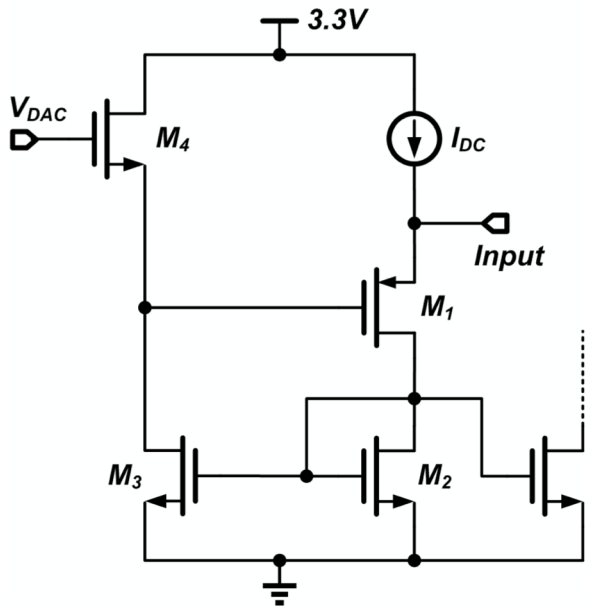
Analog Power supplies

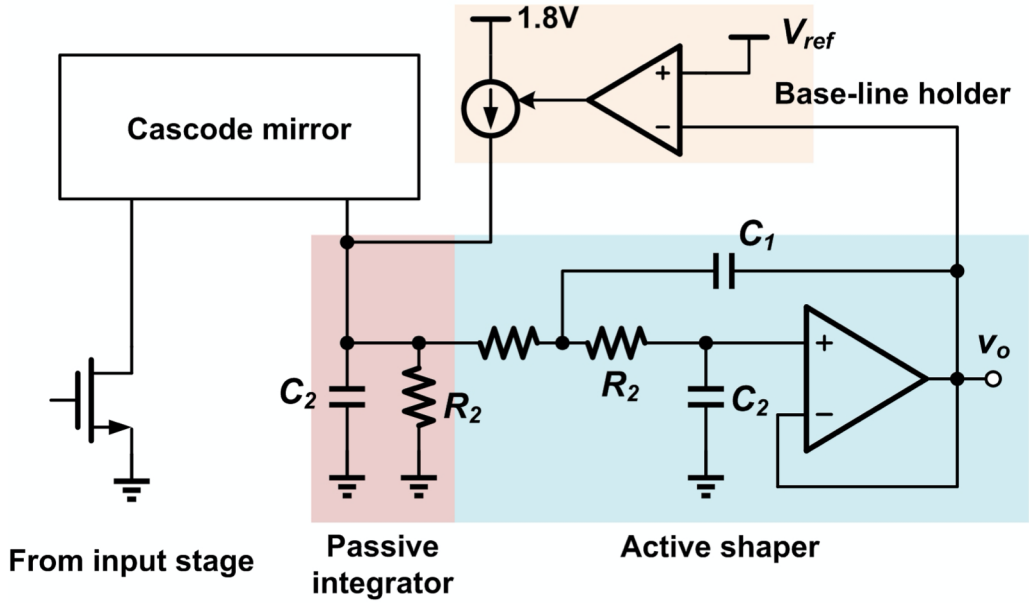


SPS_T2

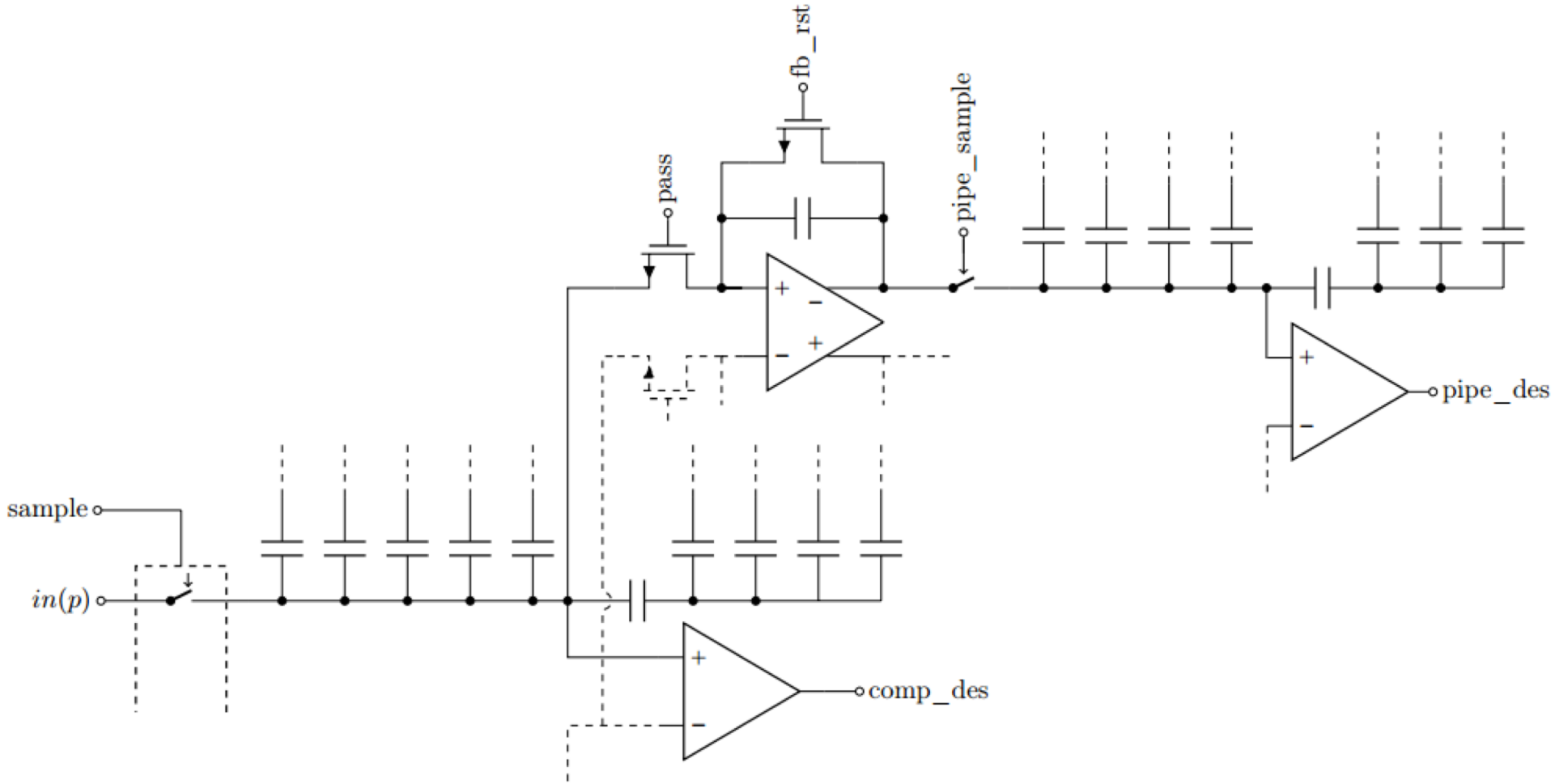


Design details

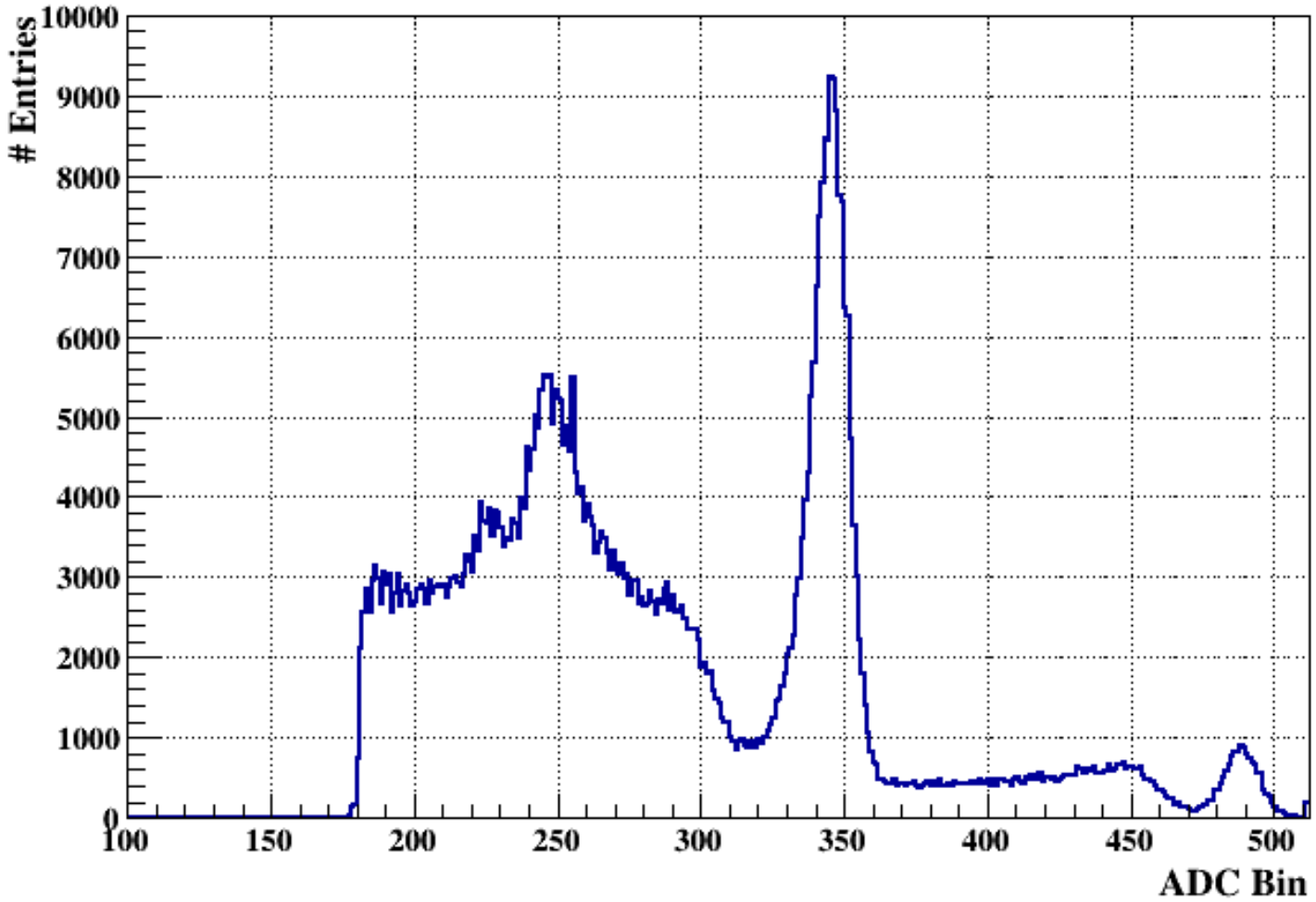




Design details



Energy spectrum of ^{22}Na source

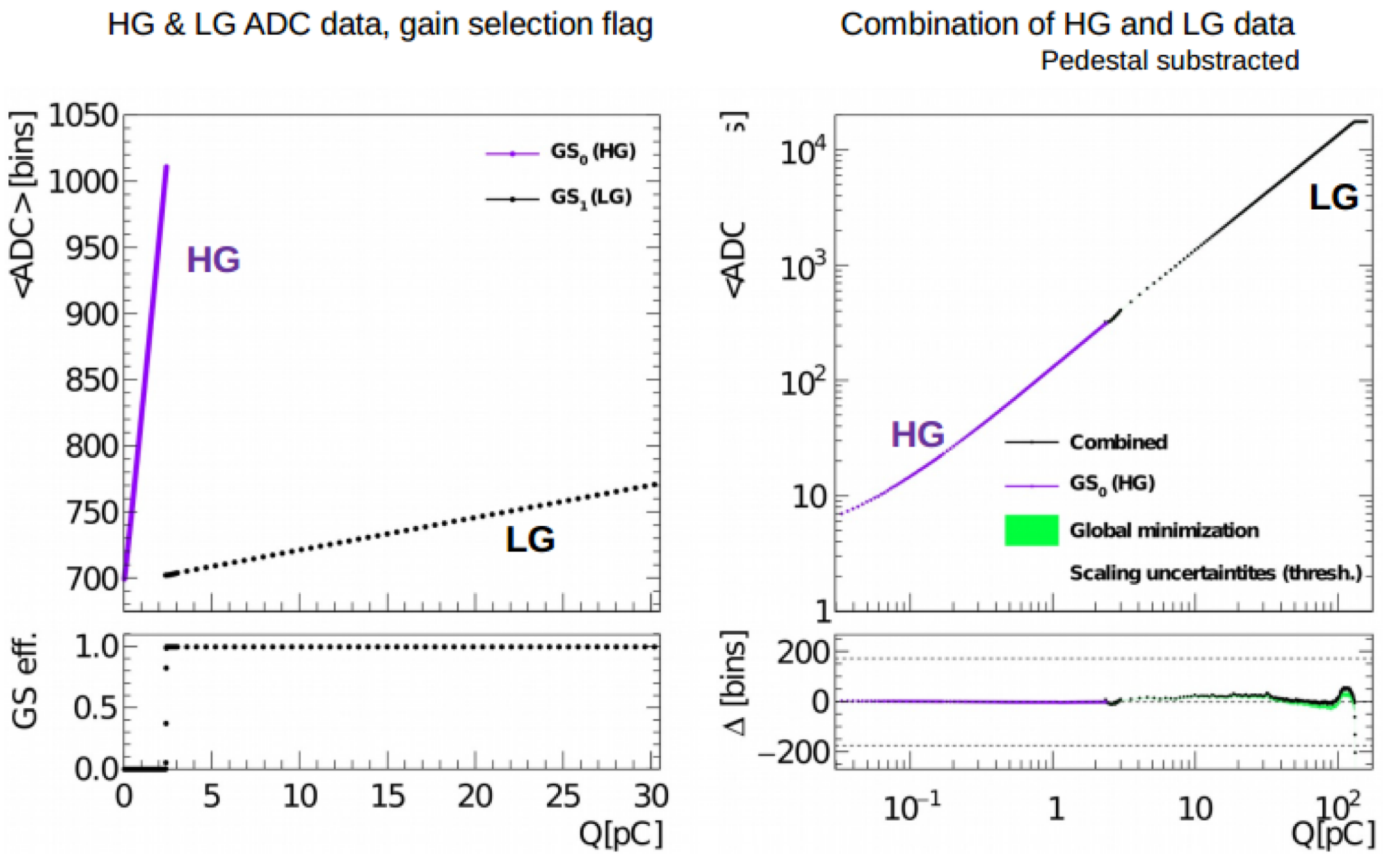


Auto-gain selection

Combine data from HG and LG branches
- HG: small dynamic range, high resolution
- LG: large dynamic range, lower resolution

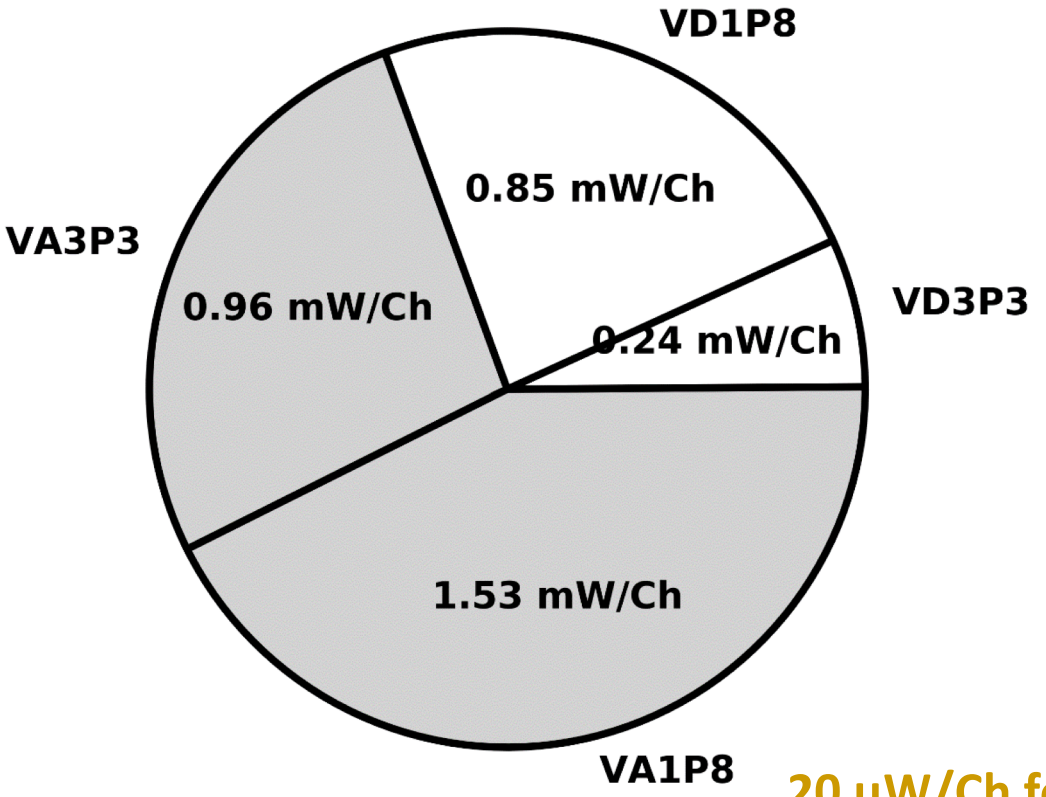
Merge using gain selection flag & ADC data
Analysis not inferring linearity

INL deviations << 1% FSR

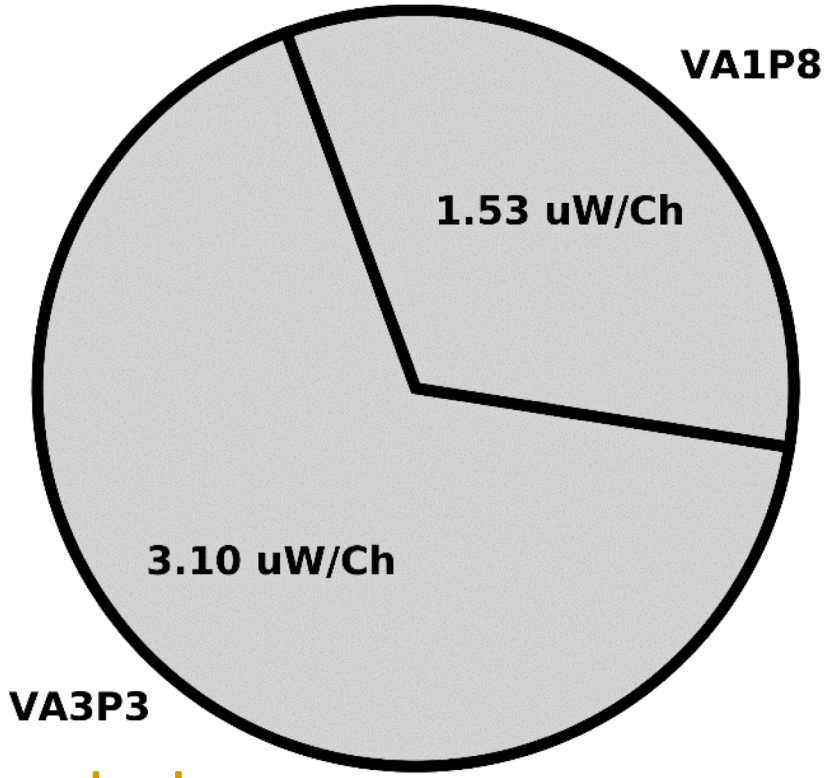


Power consumption

Acquistion-on



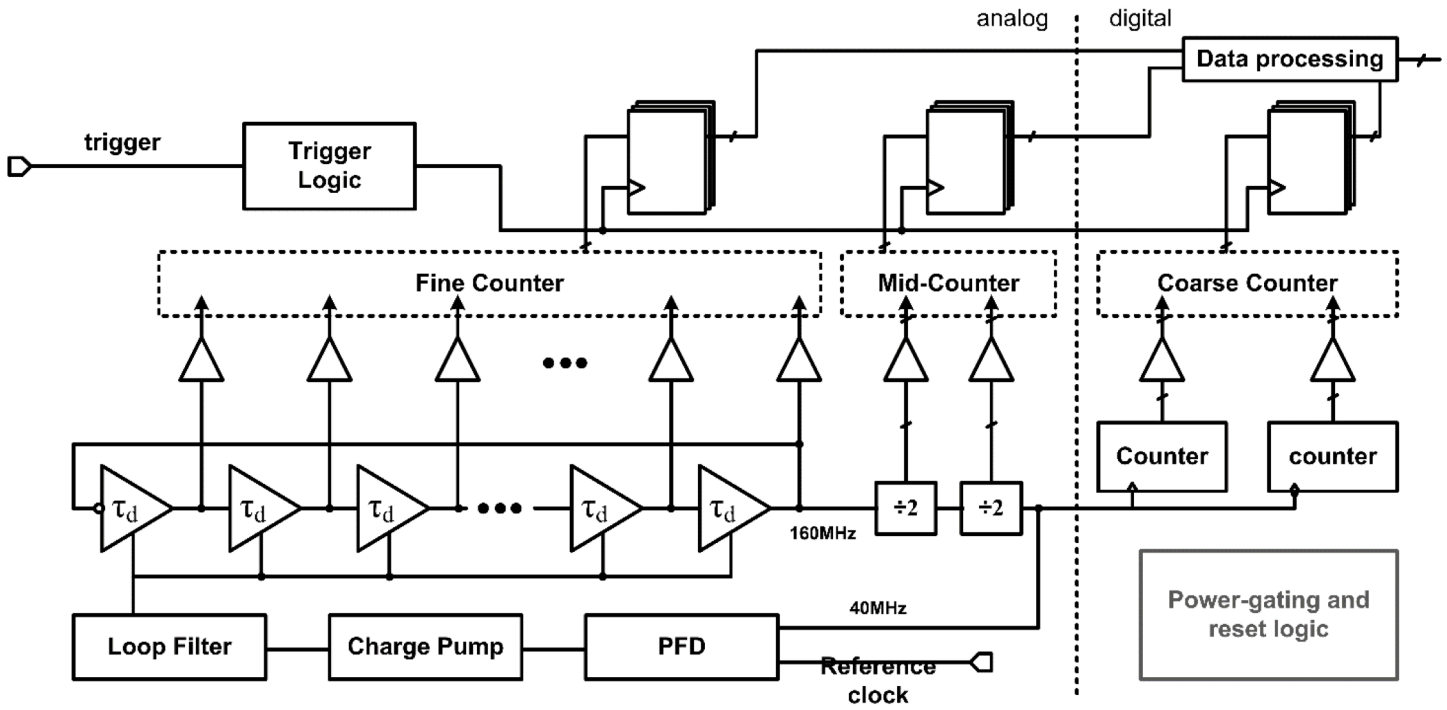
Acquistion-off



20 µW/Ch for analog front-end only

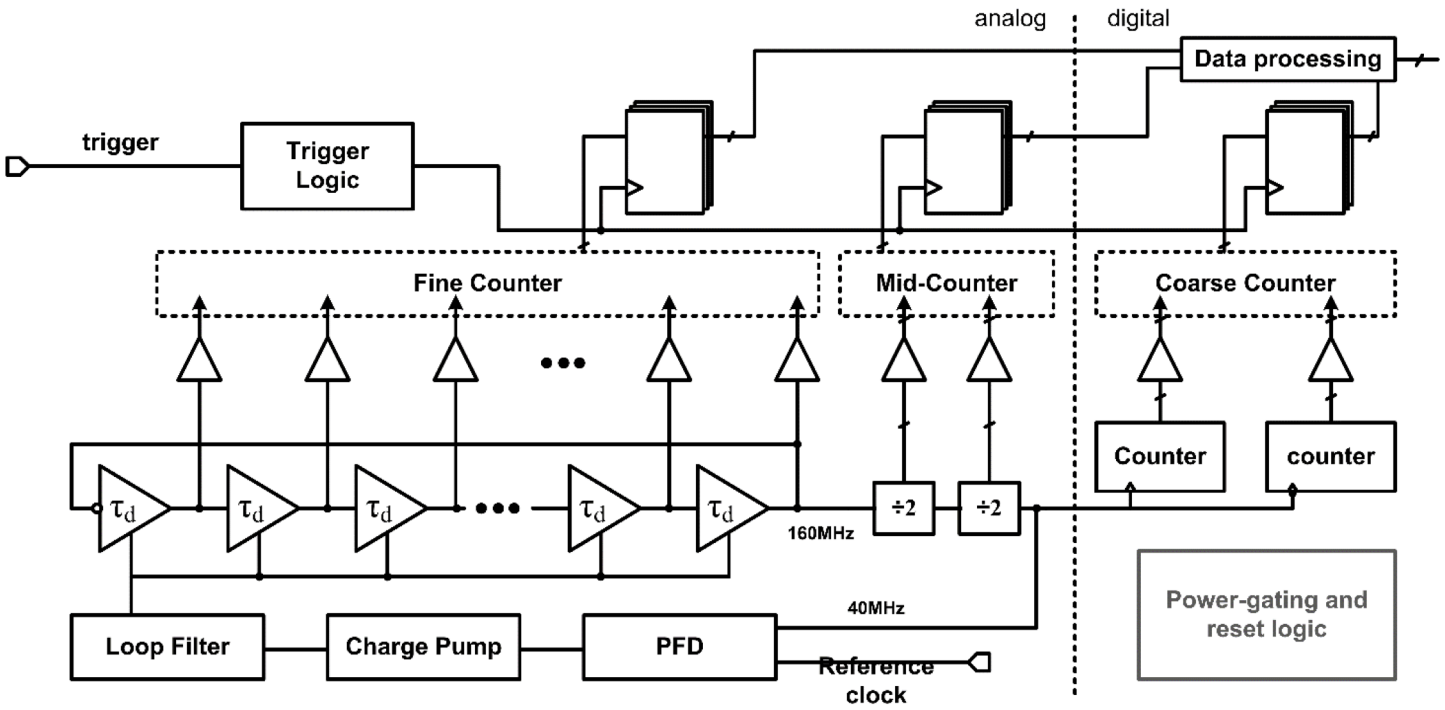
(2.5mW/Ch×0.5%+7.6 µW/Ch)

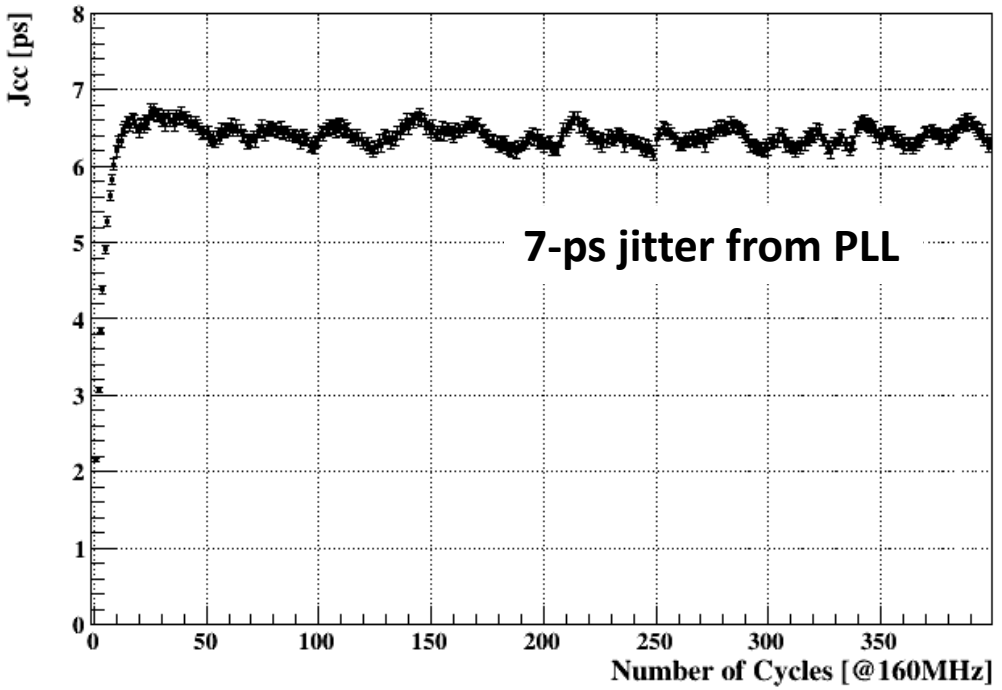
PLL-based TDC for next version



- **Stable, 200ps binsize**
- Power consumption:
  - VCO: 2.3mA
  - Buffers: 3.6mA
  - Latches: no DC power
  - Others: 0.6mA
  - Total: 6.5mA
  - 0.35mW/Ch
- **< 2µW/Ch (0.5%PP)**

PLL-based TDC for next version

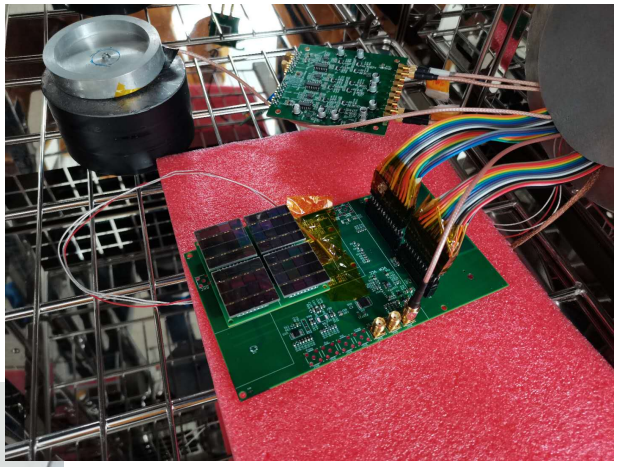


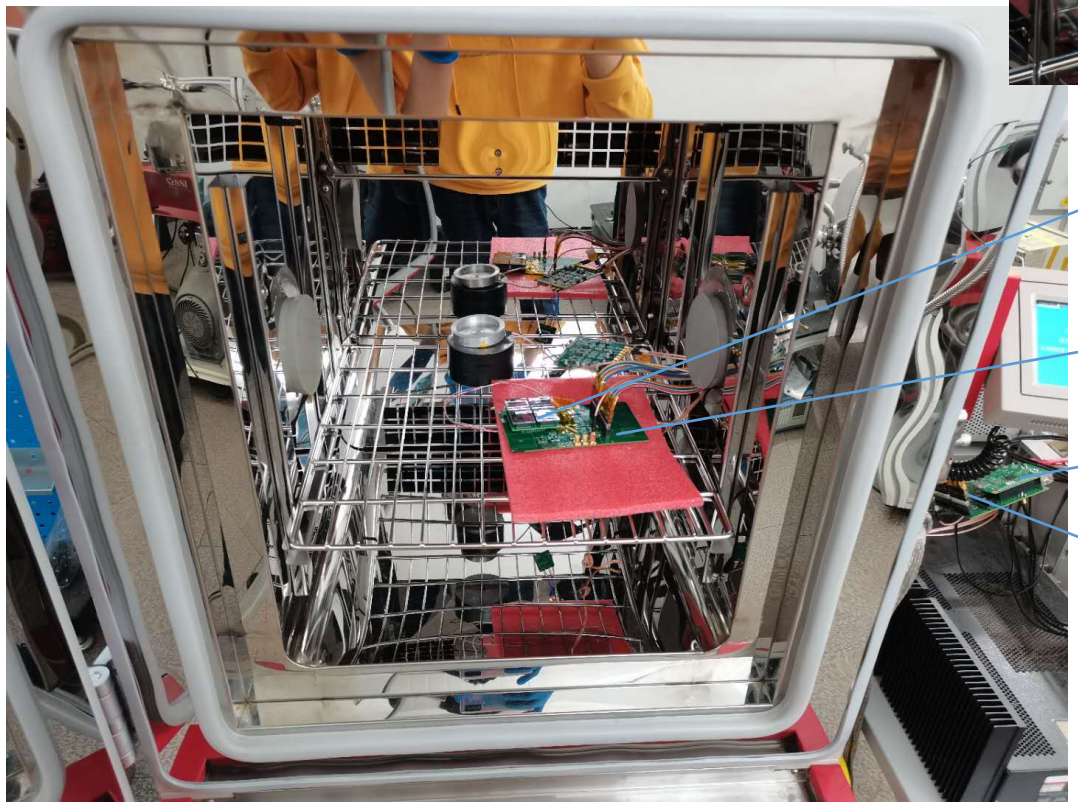


Experiment set-up

† Low temperature box
- Working region: -120 C to 150 C
- From room-T to -50 C, ~10 min

† charge injection board: 33pF+50Ω





SiPM array of FBK

ASIC board

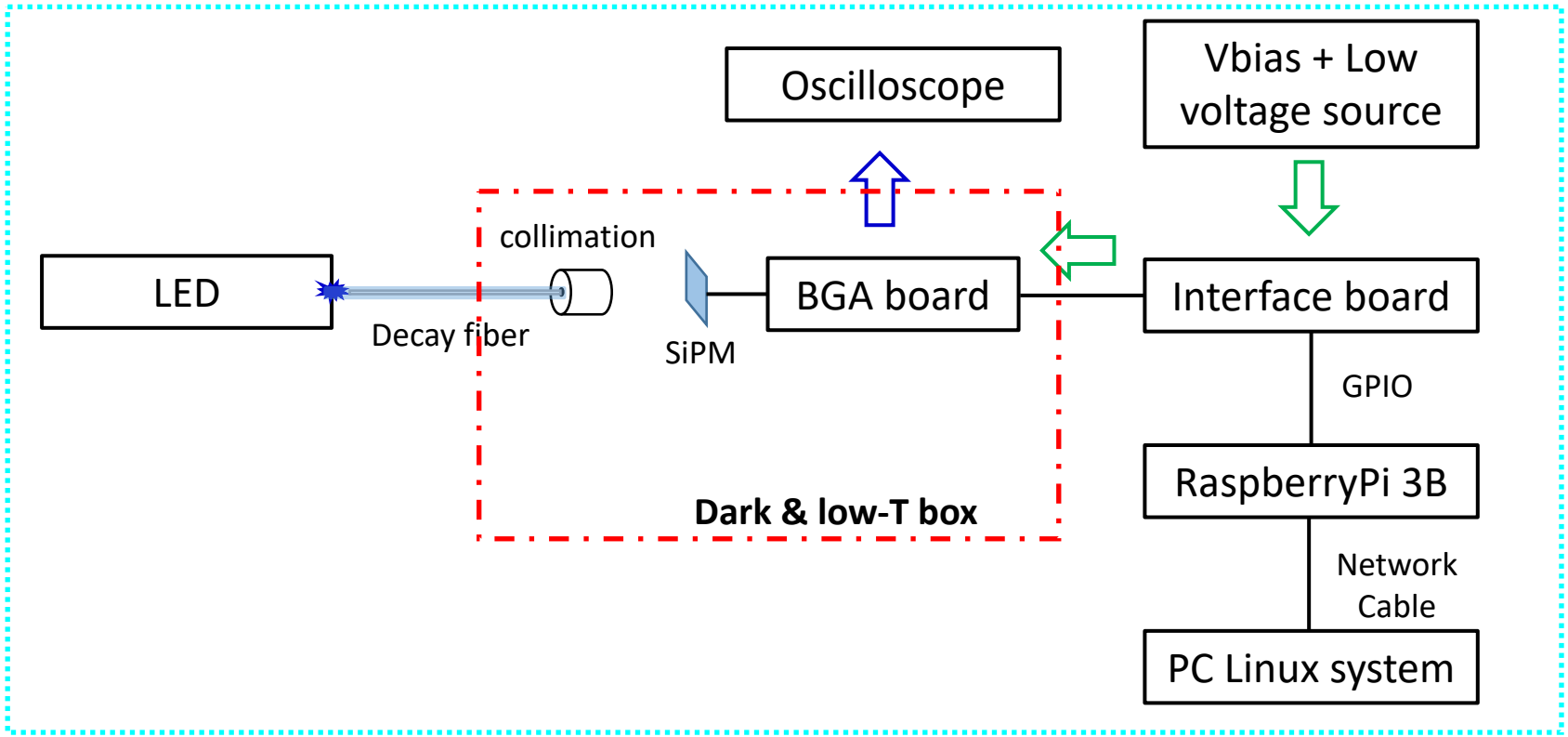
Raspberry pi

Interface board

Experiment set-up

Configuration:

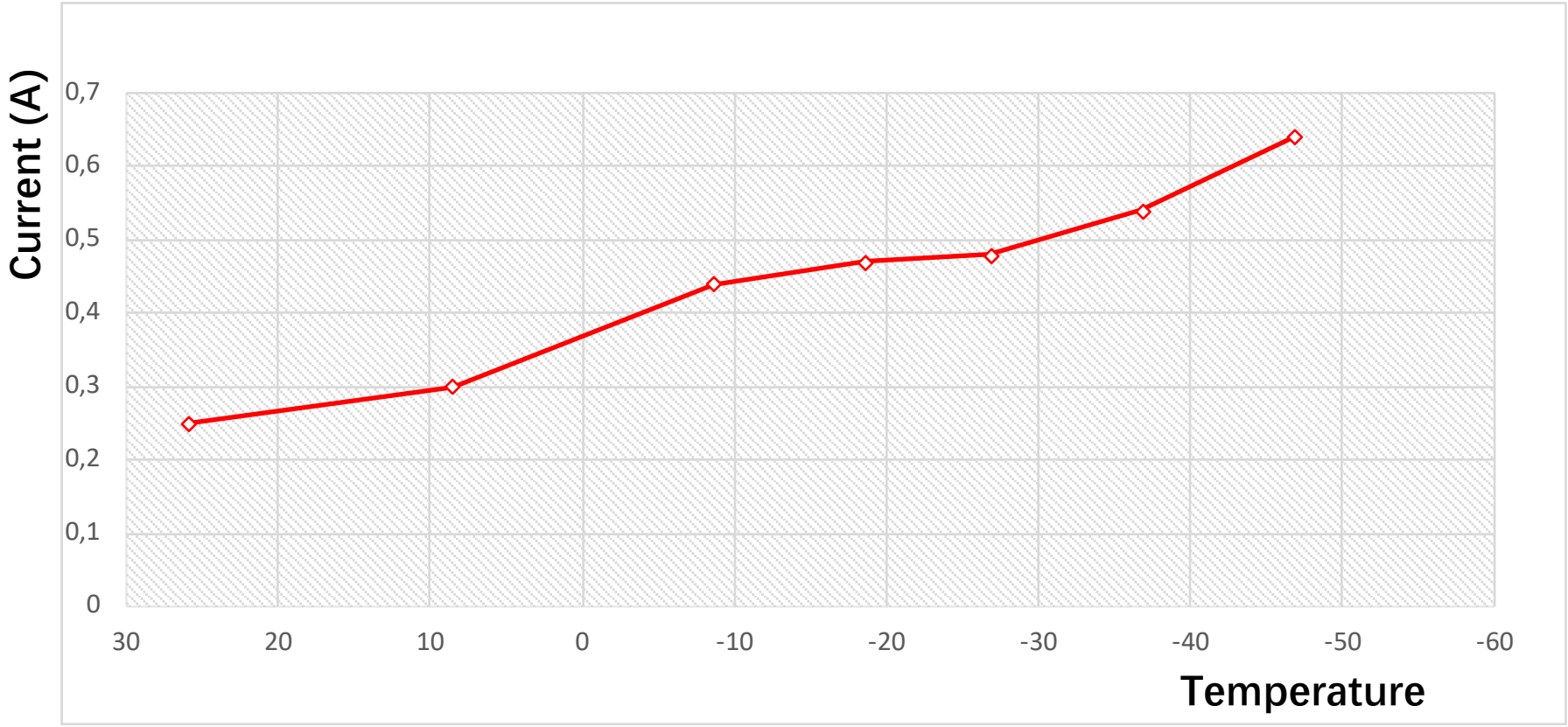
- Pi 3B: root_v5.34 and the same local network with PC are required
- PC: Ubuntu 18.04 with root_v6



Board performance

† Working current

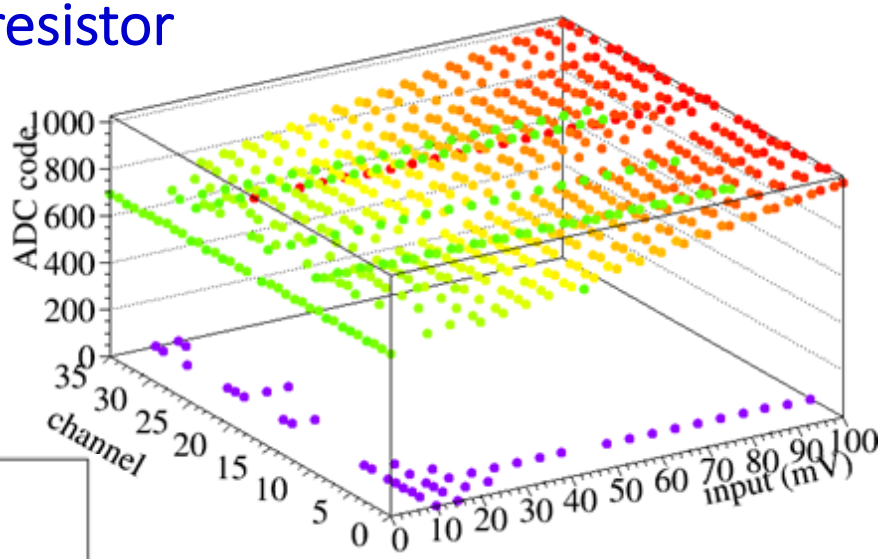
- Temperature: 30 C to -50 C

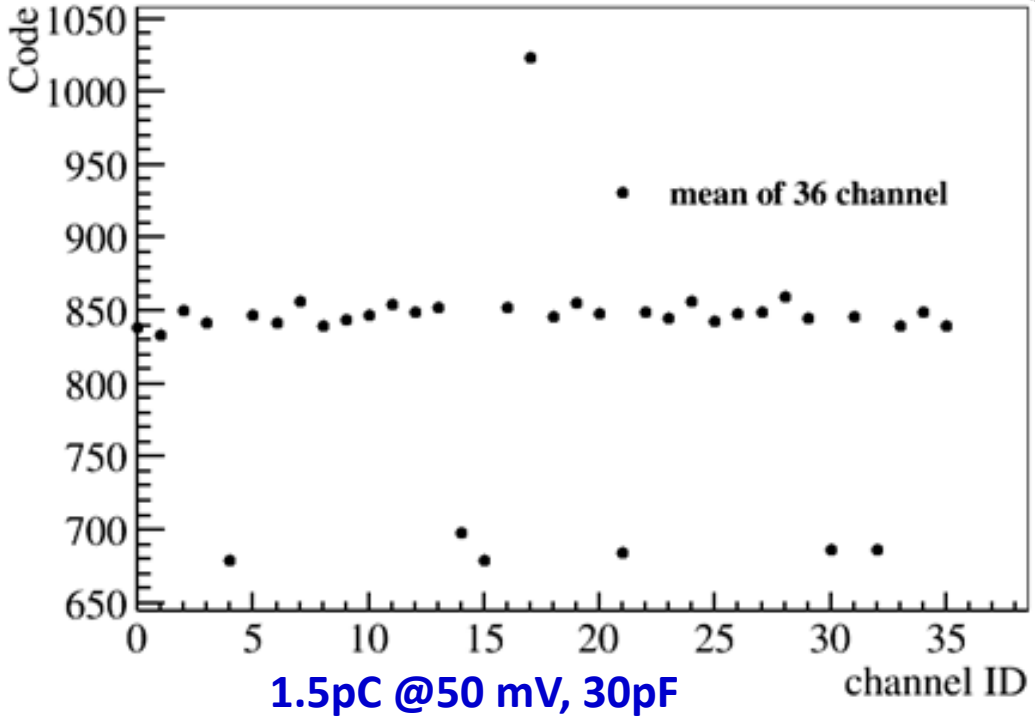


Charge injection test

† Several channels work abnormal, T: -50 C, HG model

1. Ch17: forget welding HV filter resistor
2. Other: baseline w/o signal





1.5pC @50 mV, 30pF

7个channel和个别点有问题。

group 0，channel 4；

group 1，channel 2；

group 1，channel 3；

group 1，channel 5；

group 1，channel 9；

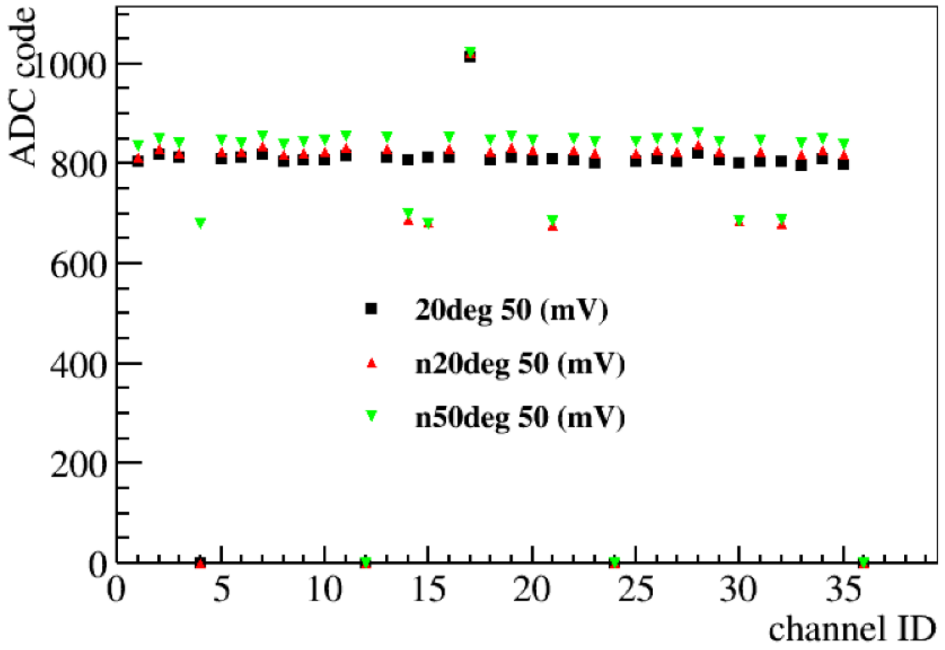
group 2，channel 6；

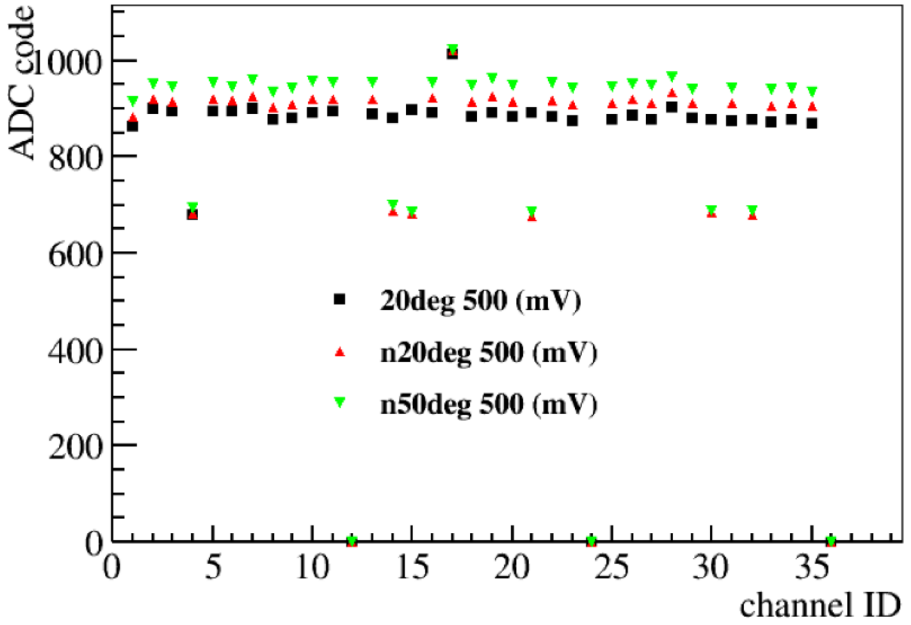
group 2，channel 8；

Charge injection test

† Several channels work abnormal, T: -50 C
- Left: 1.5pC input, HG model
- Right: 15pC input, MHG model

† Baseline drifts with T

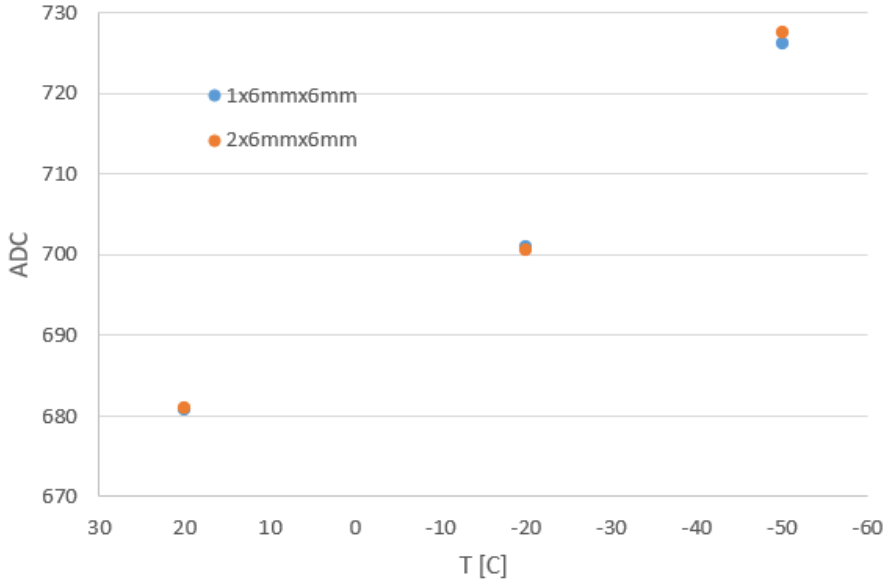


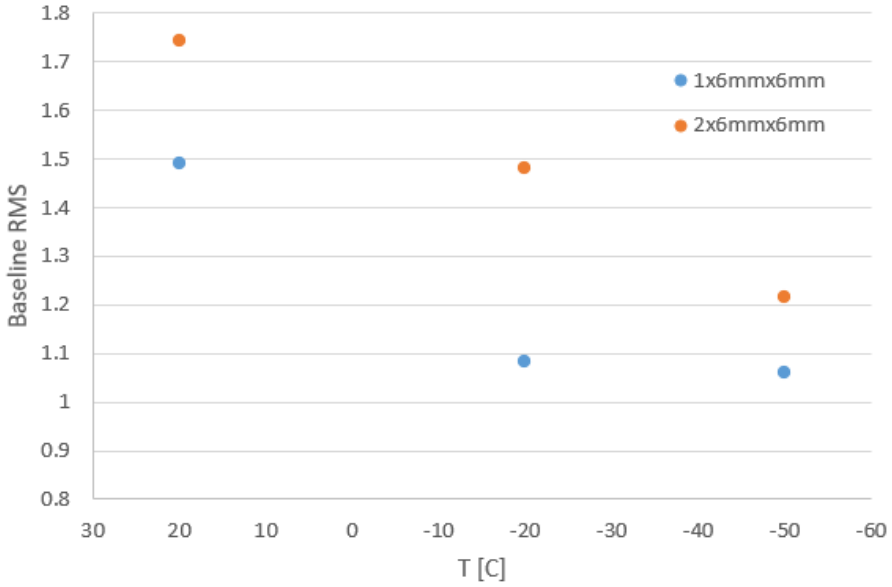


SiPM test

† Hamamastu vuv4 array test

- Pedestal





SiPM test

† Hamamastu vuv4 array test, 2x 6mm x 6mm, with ch1