

# MicroTCA.4 for the ESO Astronomical Detector Controller (9th MTCAWS)

Public





#### **Abstract**

The Extremely Large Telescope (ELT) is under construction on Cerro Armazones in Chile. MicroTCA.4 will be used as a basis for the new modular ESO detector controller for all future visible and IR scientific detectors. The presentation gives an overview over current MTCA.4 related developments at ESO and how the new controller can continue the legacy of the previous ESO detector controller, NGC, that has enabled groundbreaking astronomical discoveries on the Very Large Telescope (VLT) over many years of operation.





## **European Southern Observatory**



European Organization for Astronomical Research in the Southern Hemisphere

- Intergovernmental Organization
- Founded: 1962
- 16 Member States
  - + Chile (Host Country)
  - + Australia



## **ESO Telescope Sites**





#### La Silla Observatory



#### Santiago de Chile



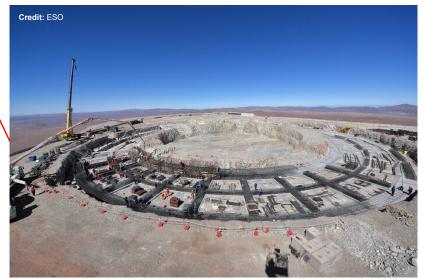


Credit: NASA, TerraMetrics, Google

Paranal Observatory



#### ELT Building Site



#### ALMA/APEX Observatory

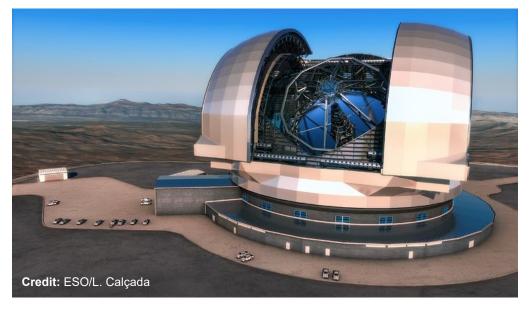


9<sup>th</sup> MTCAWS, 2<sup>nd</sup> – 4<sup>th</sup> Dec 2020, Public



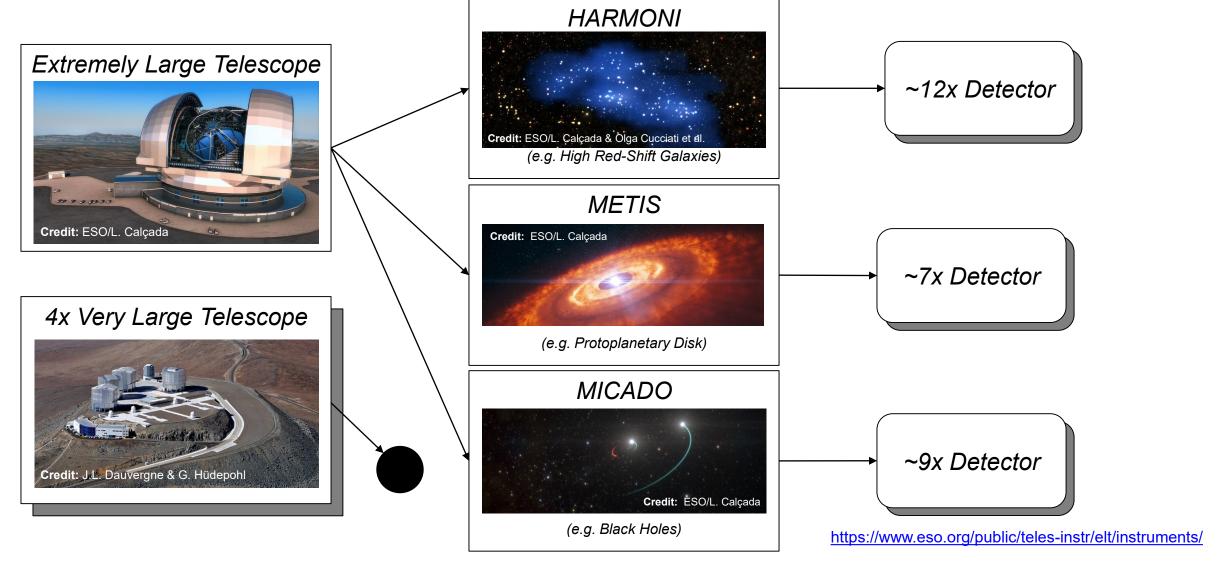
## **Extremely Large Telescope**

First Light: 2025 (planned)
 Primary Mirror: 39.3m
 Primary Mirror Area: 978m<sup>2</sup>





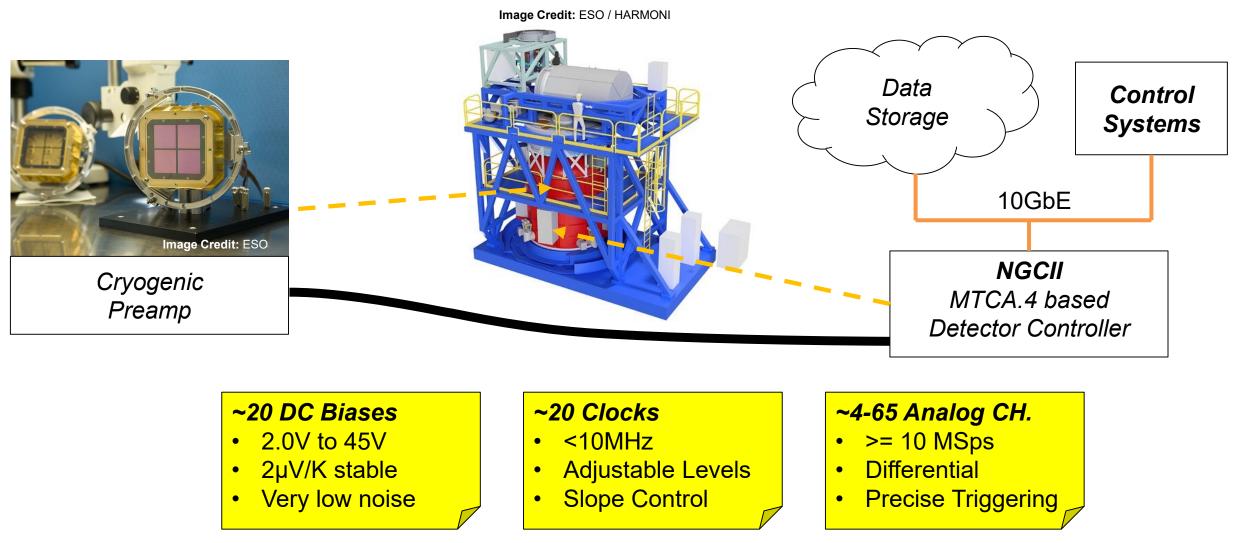
### **Instruments and Detectors**



6

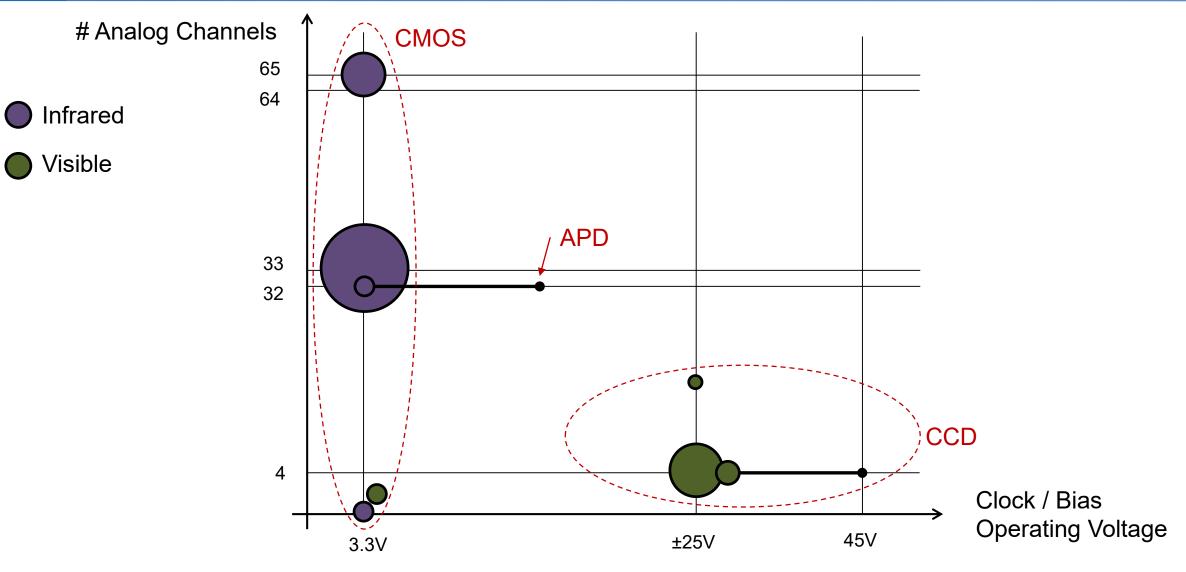


### **Detector Interfacing**





## **Detector Technology**





## **MTCA Adoption**

#### Fully Adopt MTCA.4

> No plans to implement MTCA.4.1

Shelf:

- Chosen not to go for standard 12 Slot (low module density)
- > Baseline will be 6 slots in 2U for highest RTM/HU density.

MCH:

- Standard MCH using PCIe
- Support for x8 PCIe on some slots appreciated

PSU:

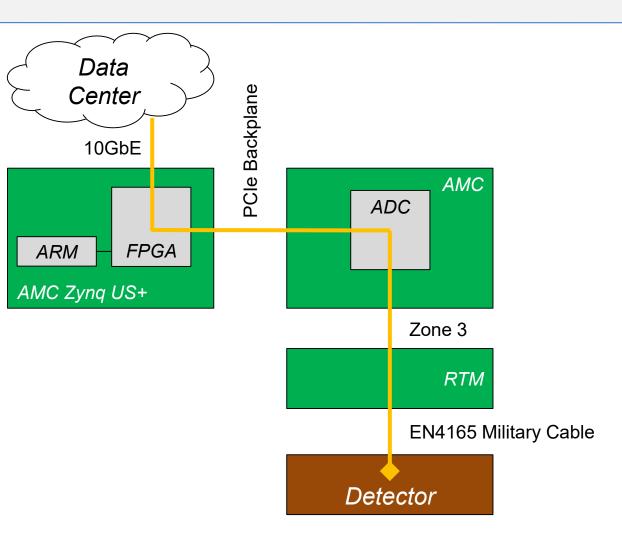
Standard 600W AC PSU



## **MTCA.4 Modules (Commercial)**

- Zynq US+ AMC
  FMC Carrier (10GbE)
  White Rabbit Support
  D1.x Profile Zone 3
- Artix 7 AMC
  - FMC Carrier
  - D1.X Profile Zone 3

#### No CPU





# MTCA.4 Modules (In House)

#### CMOS Clock/Bias RTM

- ➢ 20 CMOS Bias Channels
  - <2µV/K Drift</li>
  - 0..5V
- > 20 CMOS Clock Channels
  - 2.0V to 5V CMOS Clock into 5m cable

#### CCD Clock RTM

- > 24 CCD Clock Channels
  - Tri-Level  $\pm 15V$
  - Optional Slope Control

#### CCD Bias RTM

- > 24 CCD Bias Channels
  - $\pm 25V$ , low drift







## MTCA.4 Modules (In House)

#### 22 Channel ADC AMC

- > 22 ADC Channels
- SAR ADCs
- ➢ 10Msps
- > 16 bit / 18 bit
- Custom Sequencing and Triggering
- 22 Channel Analog RTM
  - Companion to AMC
  - > 22 Analog Frontend Channels





## **Conduction Cooling**

- Some systems cannot use air cooling
- Water assisted conduction cooling required.
- Approach
  - > Make hybrid MTCA.4 and MTCA.3 rack
  - > Copy electrical topology from existing 5/6 slot rack.
- Challenges:
  - Clamshell for Double-Mid-Size RTMs/AMCs
  - > MTCA.3 PCIe MCH supporting MTCA.4 Clocks
- Setting up cooperation with Australian National University