



# Application of MTCA.4 with RF Backplane to LLRF and BPM Electronics at SPring-8

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#### Introduction

- SPring-8
  - Beam Energy: 8 GeV
  - Lattice: Double-bend acromat (DBA)
  - Natural Emittance: 2.4 nm rad
  - # of cells: 44
  - User service since 1997.
  - Electronics are based on NIM and VME.
- SPring-8 Upgrade Project (SPring-8-II)
  - Beam Energy: 6 GeV
  - Lattice: 5-bend achromat (5BA)
  - Natural Emittance: ~100 pm rad
  - MTCA.4 for high-speed electronics.
    - Low-level RF (LLRF), Beam position monitor (BPM), etc.
  - We started R&D of MTCA.4 ~5 years ago and we are already upgrading these electronics.
- New 3 GeV light source in Japan will also use MTCA.4 for LLRF and beam diagnostic systems.



## **Design Concept**

- LLRF and BPM electronics must detect acceleration RF signals precisely.
  - Acceleration RF frequency: 508.58 MHz
- Under-sampling scheme was chosen for RF detection.
  - The circuit is simpler than down-conversion scheme.
  - Drifts of active RF components can be reduced.
    - Mixers, LO generators, etc.
  - Sampling frequency ( $f_S$ ): 363.3 MHz = 508.58 x 5 / 7
  - Intermediate frequency ( $f_{IF}$ ): 145.3 MHz = 508.58 x 2 / 7
  - Digital down-conversion from IF to IQ baseband in the FPGA on the digitizer.
  - Required resolution (10 MHz BW):
    - Amplitude:  $60 \text{ dBc} = 1 \times 10^{-3}$
    - Phase: 0.1 degree
- MTCA.4 can be one of the best choices for the new system.
  - A common digitizer AMC can be used.
  - The individual RF front-end circuit for each system can be incorporated into a  $\mu$ RTM.
- The RF backplane provides rigid transmission lines and reduces wiring.



# **Digitizer AMC**

- ADC x 10 ch.
  - 370 MSPS max., 16-bit
  - ADC16DX370
- DAC x 2 ch.
  - 500 MSPS max., 16-bit
  - AD9783
- FPGA: Kintex7 (XC7K480T)
- On-board RAM: DDR3-SDRAM 1 GiB
- ADC performance
  - Noise level (182 MHz BW):
    –69.9 dBFS (No input)
    - -51.7 dBc (508.6 MHz input)
      - Larger noise than ADC datasheet for 509 MHz input due to clock jitter.
  - Amplitude resolution (10 MHz BW):
    -64.9 dBc ~ 5.6 x 10<sup>-4</sup> (508.6 MHz)
  - Phase resolution (10 MHz BW):
    0.058 deg. (508.6 MHz)



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### **RF/Clock eRTM** (extended RTM)

- The primary clock and LO signal are generated by direct digital synthesizer (DDS).
  - AD9914
  - Up to 500 MHz.
- The two clocks and three RF signals (LO, REF, and CAL) are distributed to  $\mu RTMs$  through the RF backplane.
  - Clock: 11-way fan out
  - RF: 9-way power divider
- All the outputs can be turned on and off.
- The DDS frequency and output switches are controlled by using UART through LVDS data lines of the RF backplane.
  - Operability confirmed with NAT-MCH-RTM-BM-FPGA.
- The MMC (IPMI) also works well with NAT-MCH-PHYS80 and NAT-RPM-AC600.





Made by Candox Systems

## **LLRF System**

- An acceleration RF signal is generated by an IQ vector modulator on a  $\mu RTM.$ 
  - Baseband signals are given by DACs on the digitizer.
- RF signals from high-power components are directly digitized by ADCs after level adjustment by step attenuators on the µRTM.
- IF data from ADCs are digitally down-converted in the FPGA.
- The klystron forward signal and the vector sum of the cavity pickup signals are fed back to DAC for the stabilization of the amplitude and phase.
- The RF switch is turned off when a machine protection interlock signal is detected.
  - Waveforms at such an event can be recorded.
- We have replaced the electronics for all the four RF stations with the MTCA.4 system.





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### **LLRF Performance**

- Stability of the vector sum data
  - 1-week data
  - Amplitude: 1.4 x 10<sup>-4</sup>
  - Phase: 0.017 deg.
  - (within the feedback loop)



- Waveform data in case of a breakdown in a cavity.
  - The backward power from the cavity began to increase about 6 µs before SW off.
  - This interlock was triggered by over-voltage of the cavity backward signal.
  - These waveforms are quite useful for postmortem analysis.



#### **BPM Electronics**

- Two BPM inputs per board.
  - (4-ch. BPM) x 2 + (2 ref. inputs) = 10 inputs
- 508.58 MHz signals are extracted by SAW band-pass filters (~10 MHz BW).
- The signal level is adjusted by step att. and amplifiers.
  - Attenuation: 0 63 dB, Gain > 40 dB
  - Input signal level
    - 100 mA uniform filling: -6 dBm
    - 0.1 nC single bunch: -53 dBm
- Pilot tone generators for gain calibrations.
- FPGA Firmware
  - Digital down-conversion
  - Beam position calculation

$$X = \sum_{i=0}^{7} \sum_{j=0}^{7-i} k_x^{ij} \Delta_x^i \Delta_y^j, \qquad Y = \sum_{i=0}^{7} \sum_{j=0}^{7-i} k_y^{ij} \Delta_x^i \Delta_y^j$$
  
$$\Delta_x = (V_1 - V_2 - V_3 + V_4) / (V_1 + V_2 + V_3 + V_4)$$
  
$$\Delta_y = (V_1 + V_2 - V_3 - V_4) / (V_1 + V_2 + V_3 + V_4)$$

- Four kinds of data.
  - COD mode, 10 Hz slow data
  - COD mode, 10 kHz fast data
  - COD mode, Turn-by-turn data (209 kHz for SPring-8)
  - Single-pass mode (turn-by-turn)
- We are testing the new BPM electronics with 4 BPMs in the present SPring-8 storage ring.
- The present BPM electronics will be gradually Dec. 2nd, 2020 replaced with the MTCA.4 system.

**BPM RTM Digitizer AMC** 10 ch.,16-bit, 370 MSPS ADC BPF Step Att. Step Att. BALUN ADC Step Att. BALUN -> Step Att. ADC ADC BPF Step Att. Step Att. BALUN ADC BALUN BPF Step Att. Step Att. ADC ADC Step Att. Step Att. BALUN ADC Clock Ext. Clock BPF BALUN Step Att. Step Att. < ADC Distribution ADC Step Att. Step Att. BALUN ADC BPF Step Att. Step Att. BALUN RTM Cloc 2 ch.,16-bit, 500 MSPS DAC Ext. R BALUN DAC BALUN < DAC Digital I/O **}**€ Clock Ext. CLK Backpl Digital I/O Digital I/O Pilot Tone FPGA  $\langle \rightarrow \rangle$ SDRAM 







### **BPM Performance**



#### **BPM** Resolution

- Single pass: 22 µm (0.13 nC)
- COD (fast data): 0.39 µm (30 mA, 2 kHz BW)

Beam orbit was intentionally shaken for these measurements.

0.55 µm std.

 $20 \,\mu\text{m/div}$ .



#### Long-term stability

- The beam orbit was stabilized by the present BPM system.
- Beam position data from the MTCA.4 system was stable within 10 µm for more than 1 month.



### Summary

- We have developed MTCA.4 LLRF and BPM electronics for the SPring-8 upgrade project.
   RF backplane is used for RF and clock distribution.
- High-speed digitizer AMC
  - 370 MSPS, 16-bit, 10-ch. ADCs and 2-ch. DACs
  - Under-sampling scheme to detect 508.58 MHz RF signals.
- RF/Clock distribution eRTM
  - DDCs for primary clock and LO generation.
  - This eRTM can distribute three RF signals (LO, REF, CAL) and two clock signals.
- RF Frontend µRTMs
  - LLRF: 9 RF inputs with step attenuators and 1 vector modulator output.
  - BPM: 2 BPM inputs with SAW filters, step attenuators, and 40 dB amplifiers.
- LLRF system
  - RF detection, RF generation, ALC and PLL feedbacks, etc. are working well.
  - We completed the replacement of the LLRF system for all the four RF stations.
- BPM electronics
  - BPM calculations for single-pass and COD modes are successfully implemented.
  - Sufficient position resolutions and long-term stability were confirmed.