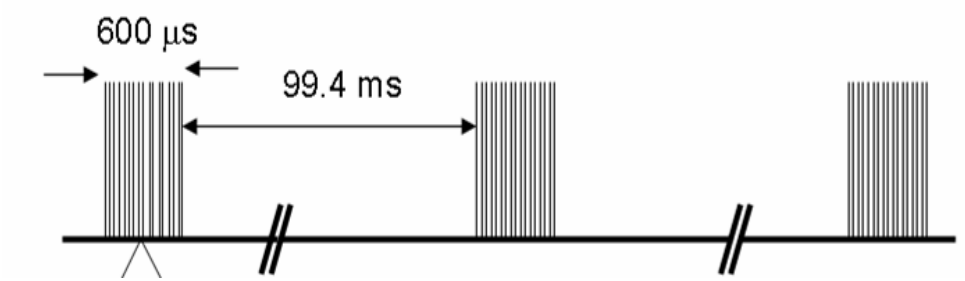
MicroTCA applications at the European XFEL Experiments - Experience and outlook

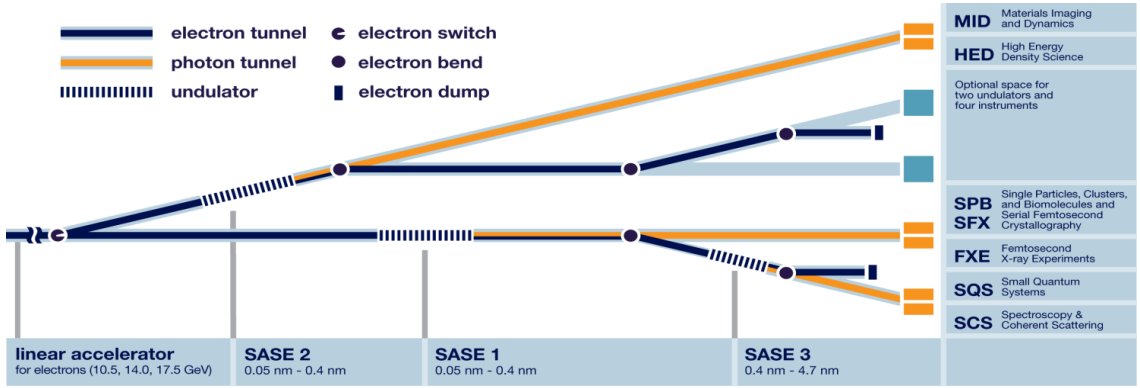
Bruno Fernandes
Fast Electronics Team Leader
EEE Group

Hamburg, 2 December 2020
9th MicroTCA Workshop for Industry & Research

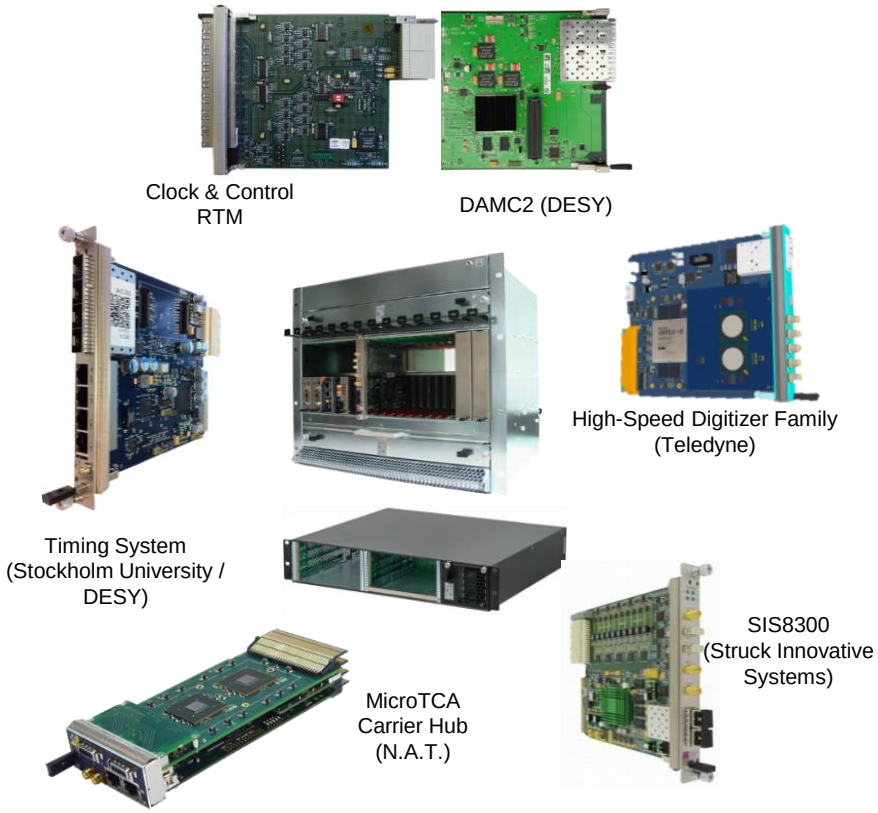
XFEL Overview



- The European XFEL generates up to 2700 X-Ray pulses
  - Inter pulse separation of 220 ns
  - Train repetition of 10 Hz
- First user operation started in September 2017

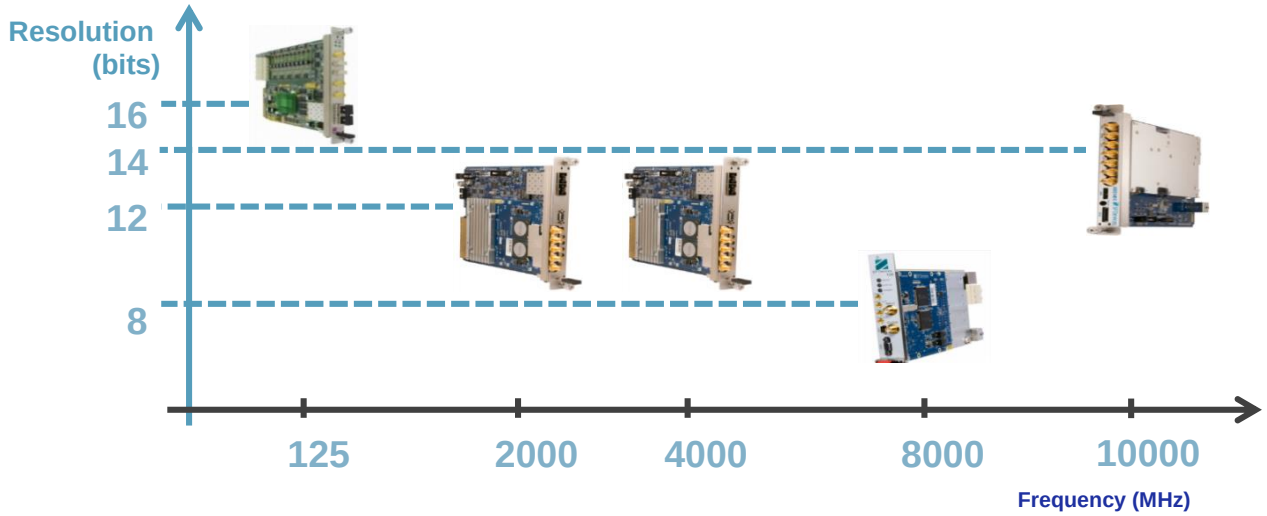


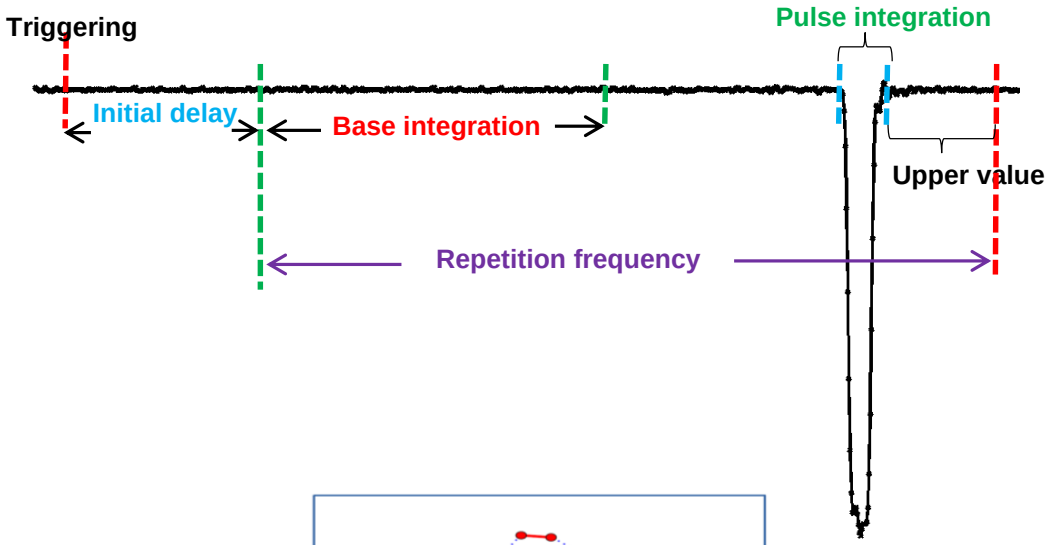
MicroTCA in XFEL

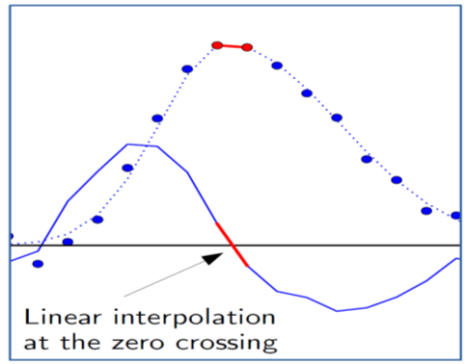


- MicroTCA platform is **the key component** for
  - Timing distribution (both in and outside the crate)
  - Digitizer raw and process data
  - Detector triggering and synchronization
- At photon beam lines, experiments and related laboratories at XFEL are **42 MicroTCA crates (more already planned)**
  - 65 Timing Systems
  - 170 fast data channels (SIS8300, 16 bit @ 125MHz)
  - 68 high speed data channels (ADQ412, 12 bit @ 2 GHz)
  - XFEL will continue to grow (SASE4 and 5, new instruments)
- On Call Duty has significant **low activity** when compared to other groups
  - **Of 16 calls, 10 were not hardware related**
  - Stability of MicroTCA and XFEL's FPGA solutions

FPGA Signal processing







- Most MicroTCA are used for hosting **Digitizers**
  - Raw data acquisition is the primary usage of these devices
  - Hardware algorithms such as **Peak Integration**, **Peak Detection , Zero Surpression** are being used more commonly

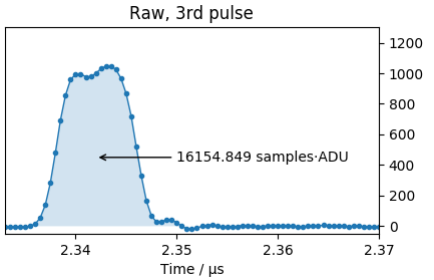
CPU installation/maintenance with Foreman and Puppet

- OS installation + Puppet **via network**
  - New CPU shows up on Network
    - ► Foreman install OS and configures target Puppet Manifest
  - Puppet guarantees that CPUs have the same environment
  - Monitor Host resources
- This solution as proven **very successful** for maintenance, testing and migration of our MicroTCA CPUs
  - **Ubuntu 20.04 transition**
  - Roll out of updates/bug fixes
  - Management of hosts groups
- This process is now **nearly 100% done automatically**
  - Next step is FPGA/MCH management

XFEL MicroTCA in 2020

- The COVID pandemic allowed us to focus in **review and development**
  - Integration of new Digitizers
  - Review of current hardware (FPGA/MicroTCA) based solutions
  - Review of digitizer usage by the Instruments
  - Digitizer Integration Effort

DAQ



FET – FPGA Firmware

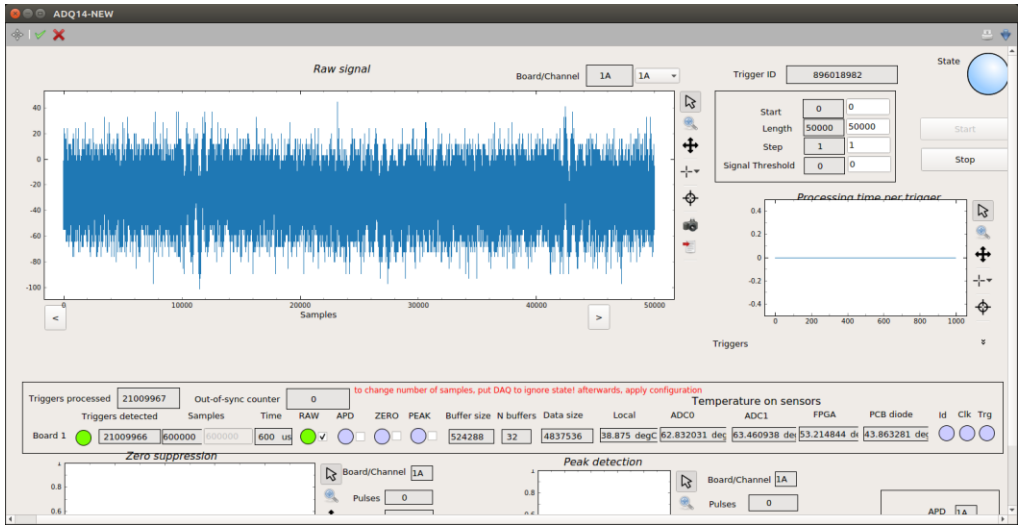
ICI – Karabo Integration

ITDM

Data Analysis

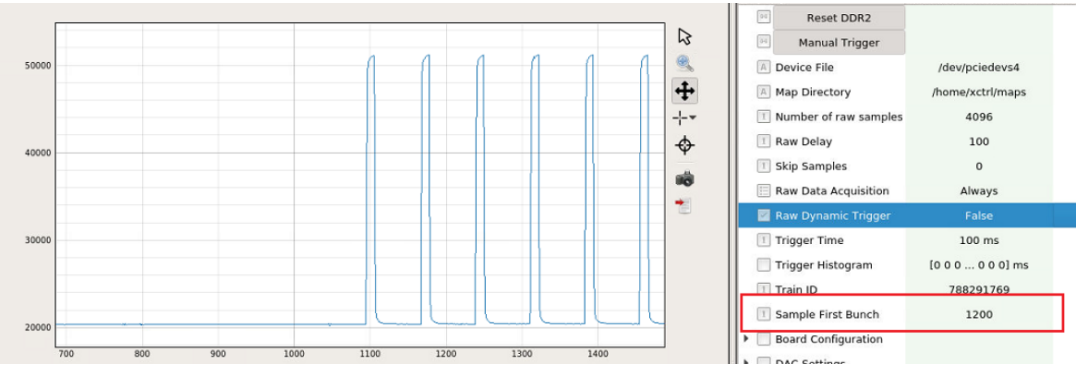
Integration of new ADC cards

- ADQ7
  - 1 channel @ 10GSPS or
    2 channels @ 5 GPSP
- ADQ14
  - 4 channel @ 1GSPS
- Review of current ADC cards
  - Integration of newer versions - SIS8300 KU
  - Interested in new ADC cards



Hardware Bunch Pattern Decoder

Bunch Pattern Settings		
Enable	True	True
Light Source	SASE1	SASE1
Decode PPL	False	False
Pulse Probe Source	None	None
Bunch pattern logic	Or	Or
First Bunch	50	
Number of Bunches	7	
Bunch Pattern Period	24	24



- Integration of **Bunch Pattern Decoder**
  - Decoding of pulses present in the Train according to **FEL and PPL parameters**
    ► OR/AND operation between SASE and PPL
  - Also accepts **User Bunches**
- Provides **number of bunches, First bunch and Bunch IDs** as well as the sample position of the first Bunch
  - Adjusting the timing trigger so that these two coincide effectively **aligns the digitizer with the Machine Pulse Pattern**

Hardware Bunch Pattern Decoder

- **How the Digitizers use the Bunch Pattern Decoder**
  - Number of pulses → if 0, no interesting bunches → **disable Trigger = Conditional Trigger**
  - Sample of First Bunch → delay the trigger by this value→ s**ampling of raw data at first Bunch** = **Dynamic Trigger**
  - Digitizer align with Machine → **Automatic integration of Bunches with recorded Bunch IDs**
    ► Only need to configure number of samples per Integration
    ► Use samples before the First Pulse for baseline calculation → **Dynamic Baseline Calculation**
- **Also used in AMC Boards interfacing 2D Detectors**
  - VETO information updated according to Bunch Pattern Table

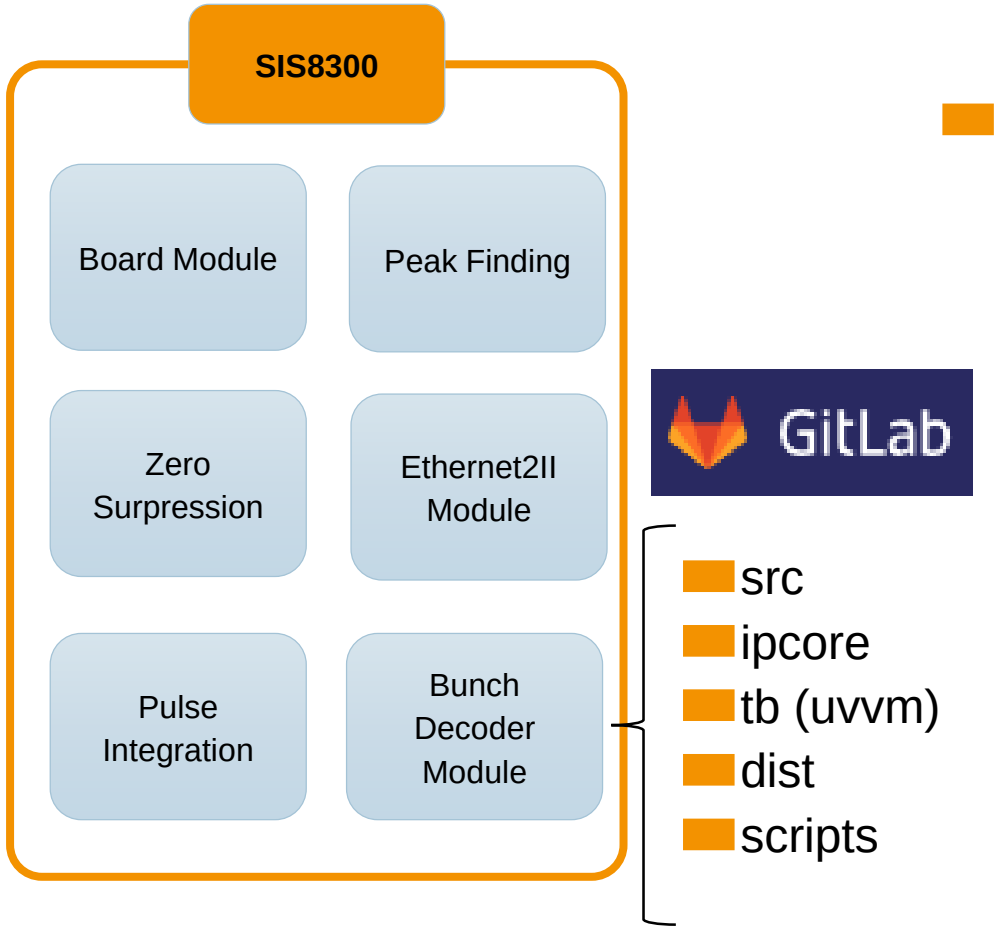
Ethernet communication

- Ethernet connection for FPGA configuration, monitoring and raw/process data
  - Updated design
  - Integrated ARP protocol
    - ► ARP request & announcement
    - ► Assign/Update MAC address on the fly
  - Supports IPv4/UDP
    - ► Data transfer in XFEL is based on UDP
    - ► TCP being implemented for configuration
  - 10Gb Interfaces for Raw data

Ethernet XFEL Data Module

Ethernet 2 II Module

FPGA Continuous Integration



- FPGA Projects are usually Board driven
  - Each module is treated as **a separate Git project**
  - Board project use modules as **Git submodules**
  - **Continuous integration** with Verification Methodology
    - ► Currently testing with **UVVM**, OSVVM and **VUnit**
    - ► Using real data in testbenches/simulink enviroments
  - Scripts available for
    - ► FPGA Project generation/tests
    - ► Testing module in hardware

FPGA Software Integration

Bunch Decoder Module

XML register description

Direct software initialization

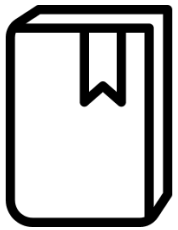
Standard Module Interface

Set of Registers

Standard (SHAPI) and Module specific

```
<II_Item>
  <name>WORD_CLK_RST</name>
  <itemType>WORD</itemType>
  <address>44</address>
  <numElements>1</numElements>
  <access>RW</access>
  <dataType>BOOL</dataType>
  <width>1</width>
  <fractionalBits>0</fractionalBits>
  <defaultValue>0</defaultValue>
  <displayedName>Clock Reset</displayedName>
  <description>Reset divider chips circuits</description>
</II_Item>
```

Full Board/Module Interface



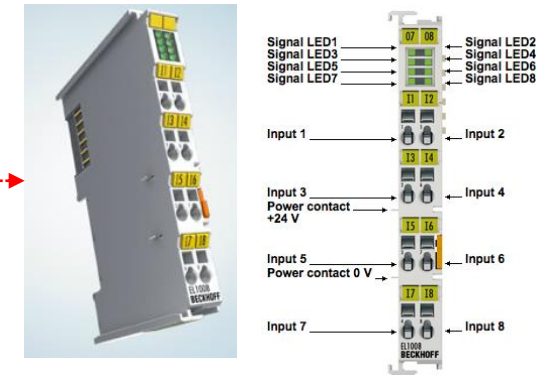
Common Library that defines

- W/R register
- State machines
- Module dependency
- DDR transfer
- Independent of device driver

Programmable Logic Controllers (PLC) systems – simplified overview

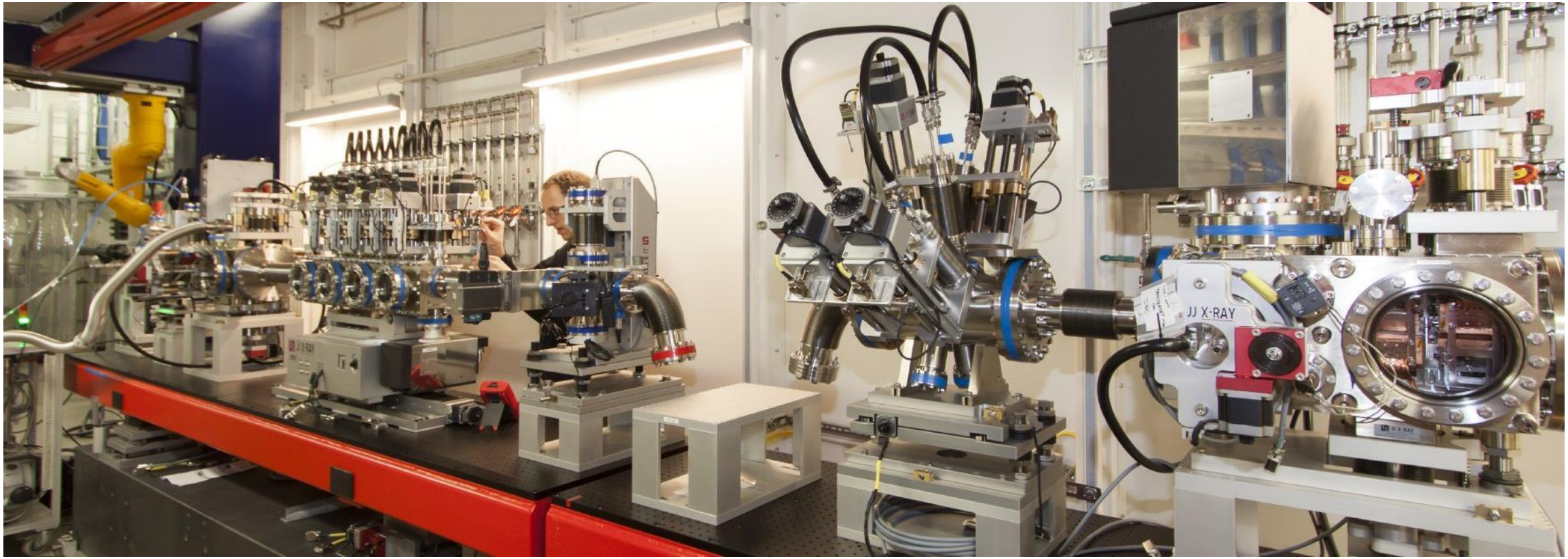
- Terminals as interface to h/w
- PLC CPU
  - Connects via cables to Terminals
  - Implements programs for control
- Computer
  - connects to PLC CPU
  - Implements Control System
- XFEL PLC numbers
  - PLC CPUs: 120
  - PLC Modules / crates: >580

PLC Terminals (i.e. digital input)



PLC Crate

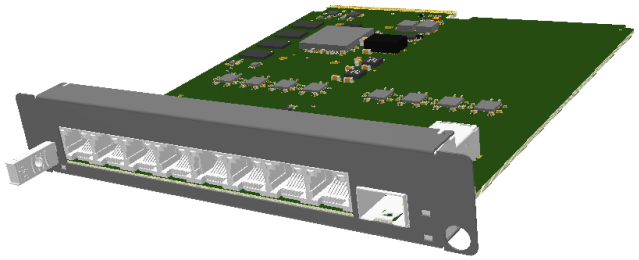
PLC controls motion, vacuum, temperature, power, protection,…

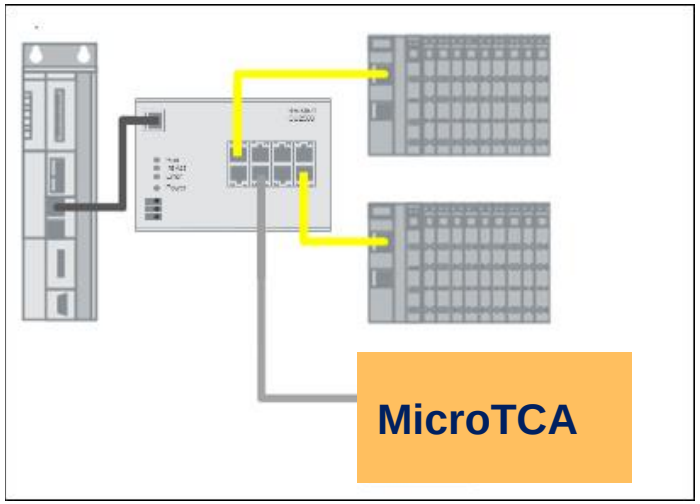


MicroTCA ⇔ PLC Communication

- Some current examples at XFEL include
  - TrainID via RS232 for Unique ID / Time-stamping
  - Alarms from PLC connected to MPS AMC module
  - More and more Instrument setups want to use PLC together with MicroTCA signals
    - ► Open shutters if…, forward trigger when..., start after “OK” from this device, etc.

- NAT Ethercat AMC solution - **NAT-AMC-ZYNQUP-ECAT**
  - Up to **8 ECAT networks**
  - Direct communication of Information (TrainID, Beam Modes…)
  - Use of FPGA processing to communicate PLC actions
    - ► **Bunch Pattern decoder information**
  - Distributed Clocks and synchronisation
  - Setup automation based on other AMC information
    - ► P2P/Ethernet communication



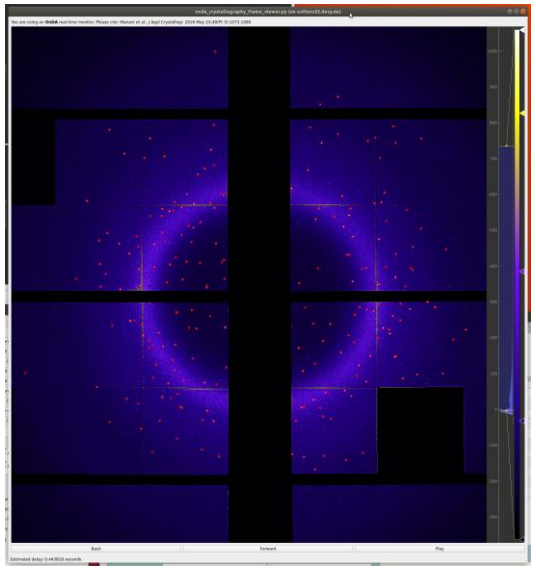


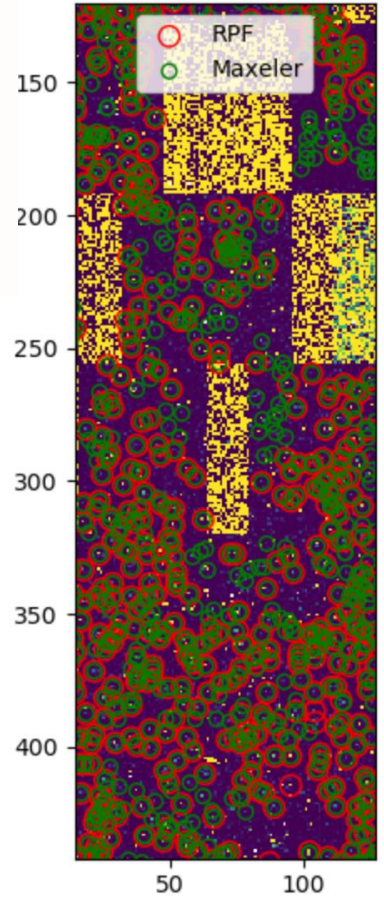
- See presentation by Herbert Erd
  Tomorrow @ 15:30
  Synchronization several EtherCAT networks through mTCA

Outside of MicroTCA…

- FPGA based online calibration and image processing
  - Project for processing of data from 2D Detectors
  - Using platform from Maxeler Technologies
    - ► Dell Server System w/ 4 Alveo 250 Cards
  - Calibration and Peak Finding algorithms implemented
  - **Latency reduced from 2min to ~100ms**
- FPGA for Machine Learning Applications
- Collaboration with other facilities **<u>is more than welcome</u>**
  - FPGA standardization
  - MicroTCA Setups/Applications
  - Brain storming, knowledge transfer…

MAXELER Technologies
MAXIMUM PERFORMANCE COMPUTING





Thanks for the attention

Questions, ideas, experience, advice?



bruno.fernandes@xfel.eu

hamed.sotoudi.namin@xfel.eu

frank.babies@xfel.eu

Fast Electronic Team