

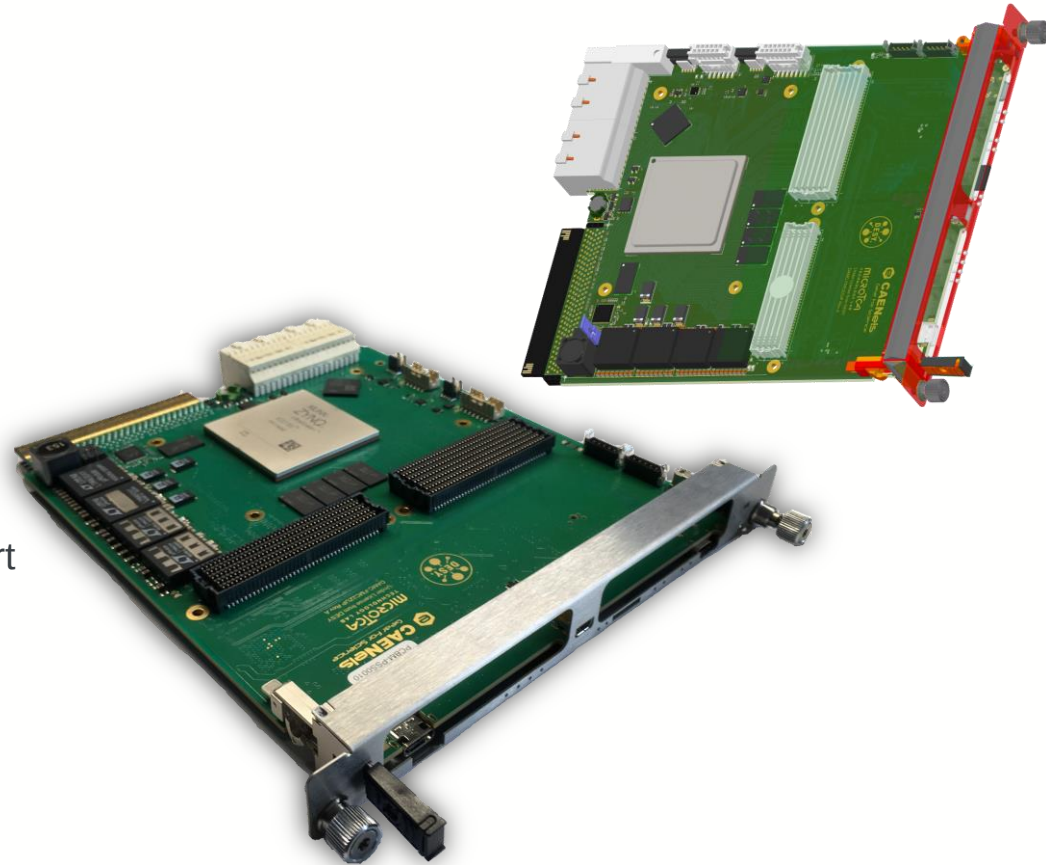


Next Generation SoC-based AMC Developments at DESY

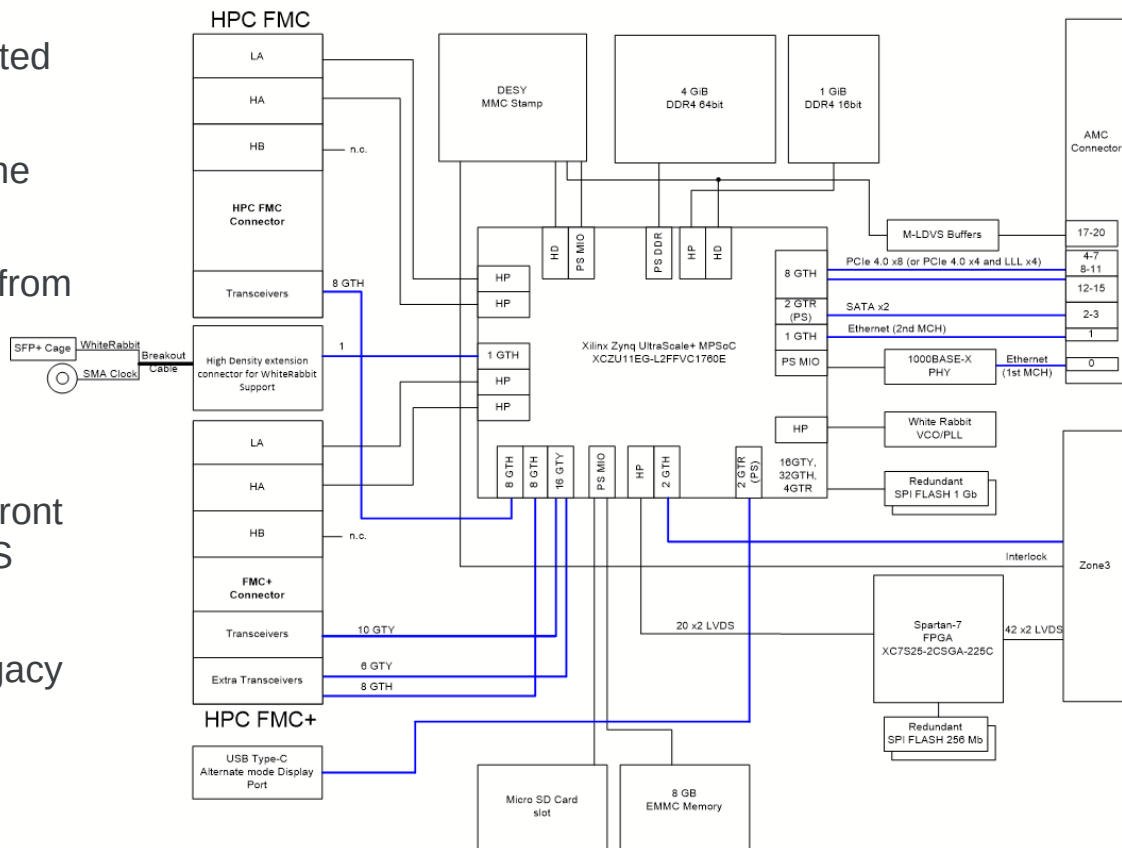
Michael Fenner, Simone Farina et al.
MTCA Workshop, DESY Hamburg, 02.12.2020

- DAMC-FMC2ZUP : ZYNQ Ultrascale+ MPSoC FMC+ carrier
- DAMC-DS5G14ZUP : ZYNQ Ultrascale+ RFSoc Digitizer
- DAMC-DS812ZUP : 8 channel 800MSPS 12-bit Digitizer ZYNQ Ultrascale+ MPSoC
- DMMC-Stamp : Turnkey SoM Module Management Controller
- DAMC-FMC1Z7IO : ZYNQ-7000 GPIO extension board and FMC carrier
- DRTM-MXC : Mobile eXpress Module Carrier - Graphics carrier RTM module

- Double-width mid-size AMC board
- 1 FMC+ slot (VITA 57.4)
- 1 FMC HPC slot (VITA 57.1)
- ZU11EG Zynq Ultrascale+ MPSoC (653k logic cells, 2928 DSP) or ZU19EG (1143k logic cells, 1968 DSP) available on request
- Works as “CPU module”: front panel USB type-C provides DisplayPort and USB 3 & 2 host capabilities.
- Front-panel clock input
- Zone 3 connector compliant to Class D1.1
- White Rabbit endpoint capability



- Both FMC connectors are fully populated up to the HA section
- Transceiver set is fully populated on the FMC+ module
- 8 XCVR connected on the FMC HPC from the PL
- 4GB DDR4 connected to PS and 1GB DDR4 16bit bus to PL
- Embedded 8GB eMMC memory and front panel accessible SD card for Linux OS rootfs and user data
- Voltage level translation to support legacy RTM with Zone3 @ 2.5V

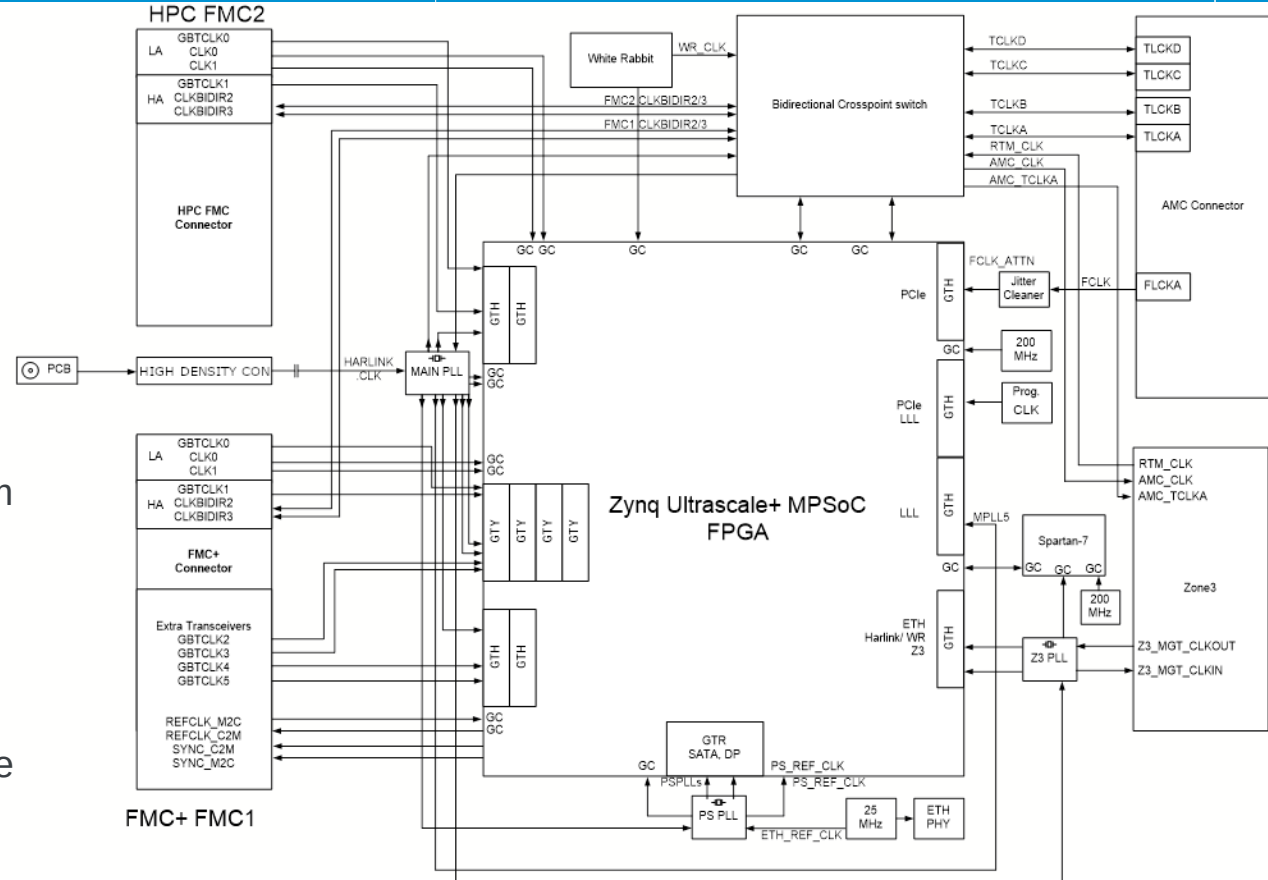


Clock Tree:

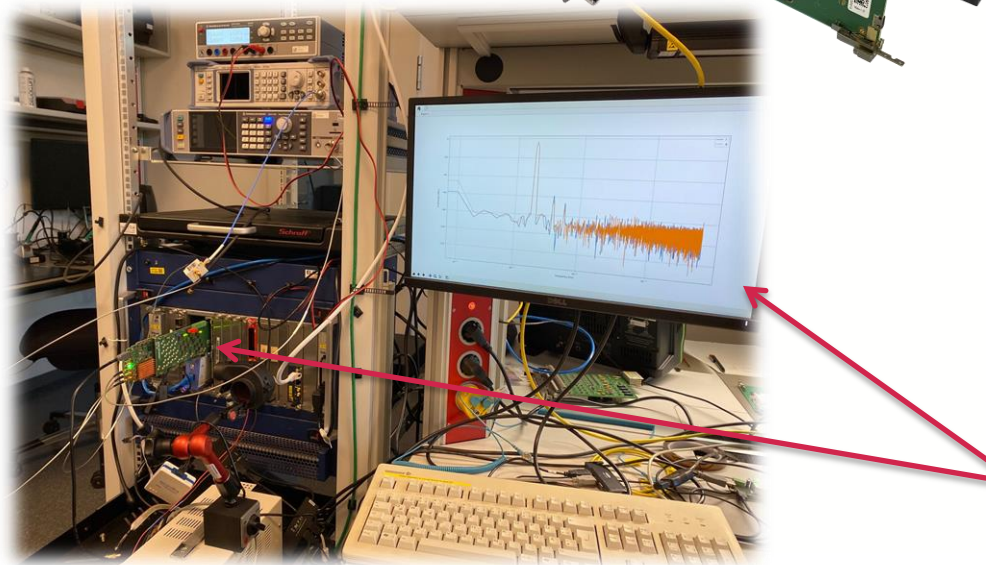
Clock tree chain configured by MMC Stamp before PS boot sequence

Key features:

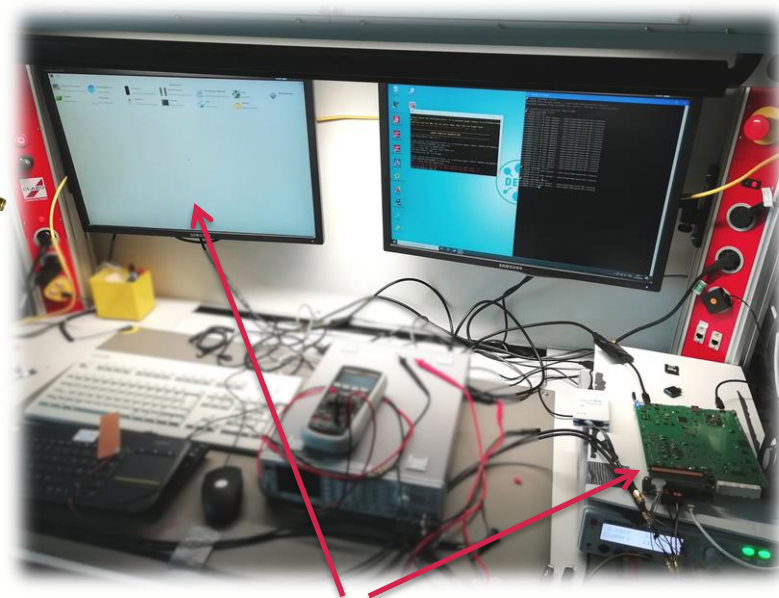
- A cross point switch collects/distributes clocks from backplane, mezzanine connectors and PLLs.
- Dedicated clock ICs for Ethernet and PL reference
- VCXO and VCTCXO for White Rabbit endpoint support



- Typical use case with fast digitizer FMCs



Courtesy of J. Marjanovic



- DAMC-FMC2ZUP operating on bench with graphical Linux OS and display output
- DAMC-FMC2ZUP collecting data from FMC-DS500 and plotting on Display using Python Matplotlib

- Double-width mid-size AMC board
- ZU47DR Zynq Ultrascale+ RFSoc 3rd generation (930k logic cells, 4272 DSP),
ADC 8ch 14-bit 5GSPS,
DAC 8ch 14-bit 10GSPS
- Zone 3 connector compliant to new Class RF1.0
- Works as “CPU module”:
front panel USB type-C provides DisplayPort and USB 3 & USB 2 host capabilities.
- Configurable Front-Panel and/or RTM ADC Inputs
- DAC Outputs : 4 to Front-Panel & 4 to RTM
- RTM, Front Panel and Backplane Clock Inputs
- White Rabbit endpoint capability

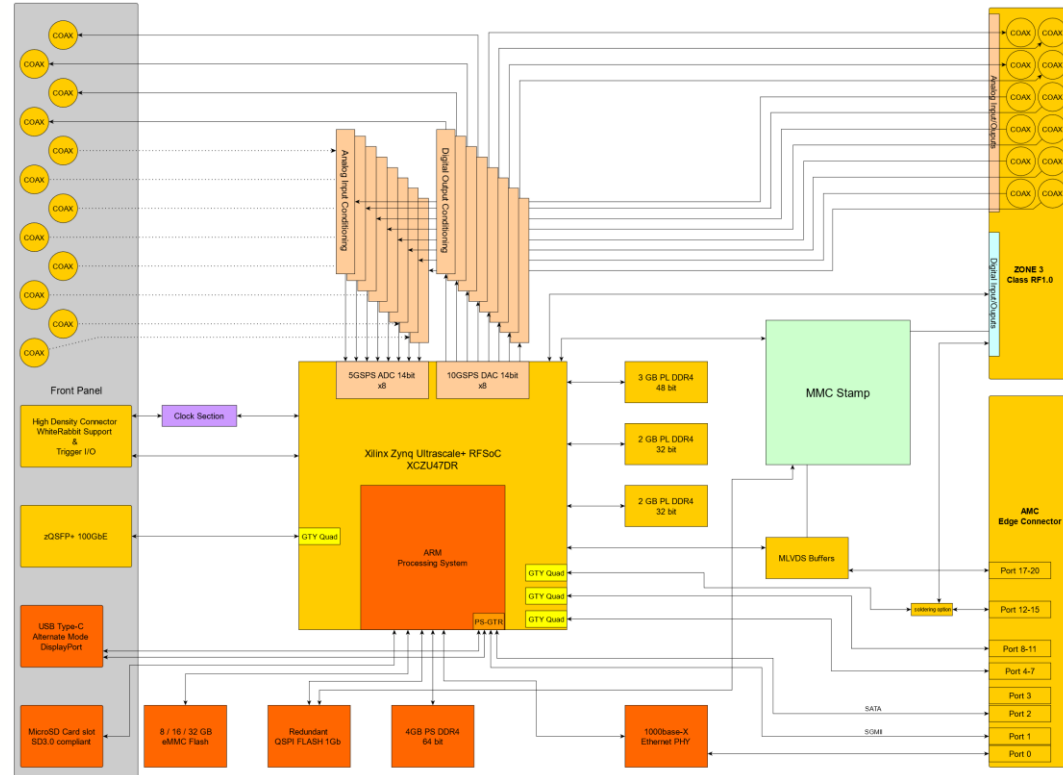


Processing System Features:

- Quad-core ARM A53 + Dual-core R5
- 4GB 64-bit wide dedicated DDR4
- Booting and storage devices:
 1. Dual redundant QSPI flash memory
 2. 8GB eMMC
 3. Front panel uSD card
- 1000base-X ETH PHY to AMC port 0
- USB type-C with DisplayPort, USB3 & USB2

Programmable Logic connections:

- DDR4 memories :
3GB 48-bit wide & 2x 2GB 32-bit wide
- AMC ports 4-11 (redundant or single PCIe/GbE)
- Backplane MLVDS
- 100GbE zQSFP+ on front panel
- Zone3 RF1.0 digital interfaces

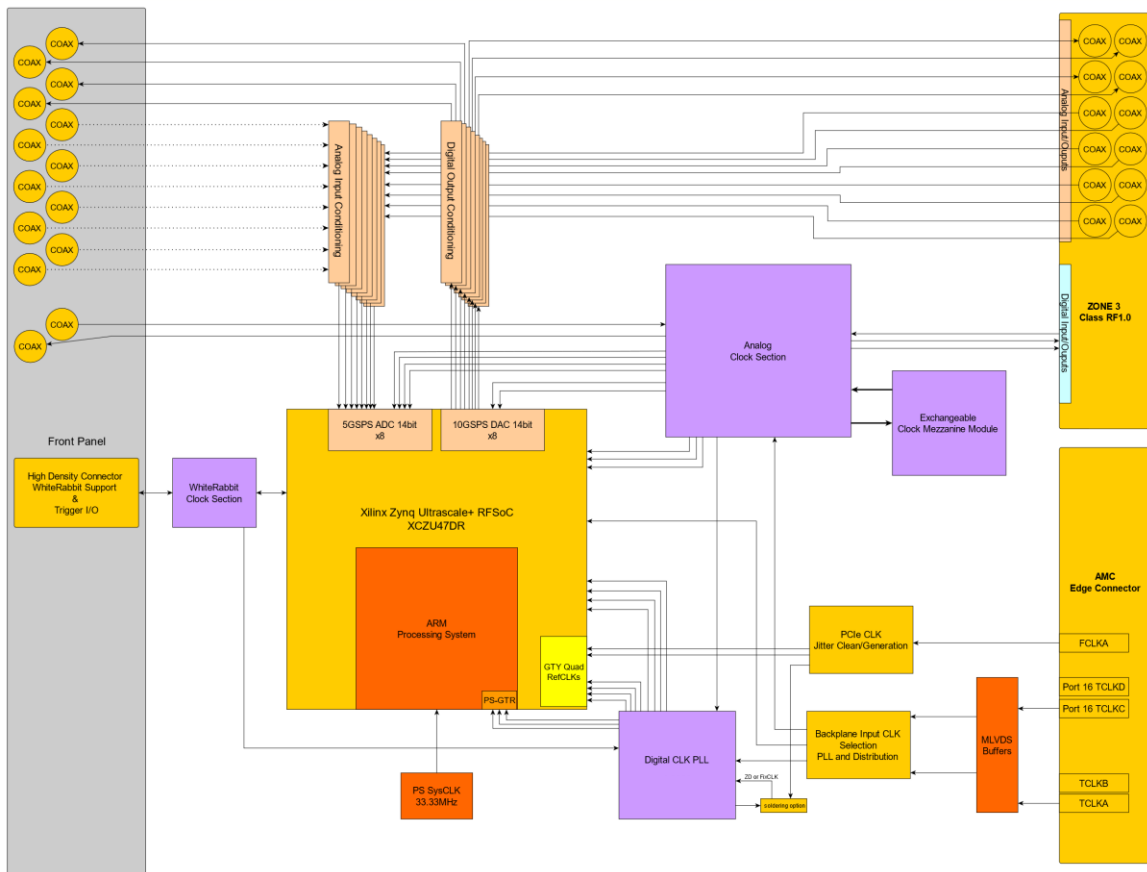


Clock Tree:

Clock tree chain configurable by MMC Stamp and Processing System

Key features:

- Analog Clock section with external dual VCO and filters. Configurable for Deterministic Latency ADC/DAC data. Inputs from Front Panel, RTM and TCLKA/C. Clock Mezzanine Module can bypass the Analog Clock Section for fully flexible ADC/DAC clocks
- Digital Clocks can be derived from either TCLKA/C, Analog Clock and WR with additional option for FCLKA
- VCXO and VCTCXO for White Rabbit endpoint support



Benefits:

- Highly integrated AD and DA sections together with FPGA logic reduce interconnection / MGT pin count
- No MGT related latency

ADC	Boards	Interface	Resolution [bits]	Sampling rate [MSPS]
AD9268	SIS8300-KU	LVDS	16	125
ADC12D800RF	DAMC-FMC2ZUP + DPMC-DS800	LVDS	12	800
ADS54J60	DAMC-FMC2ZUP + ADS54J60EVM	JESD204B	16	1000
XCZU28DR	ZCU111	RFSoc int.	12	4096

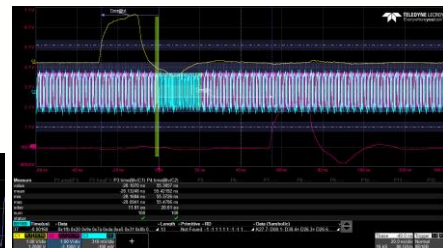
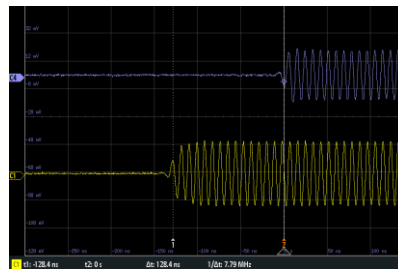


GTYE4 MGT latency (@6.25Gbps)

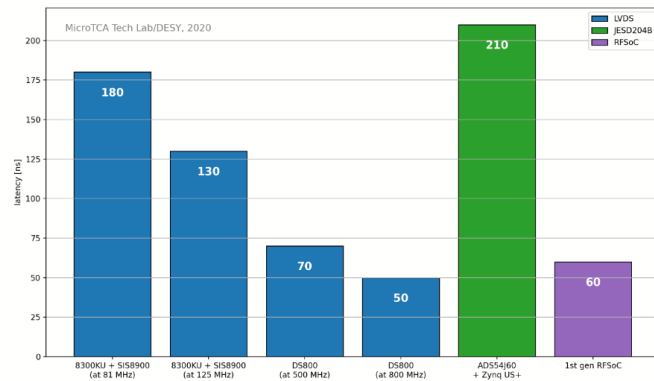
83ns (28ns TX, 55ns RX) →

RFSoc ADC + DAC loopback

128ns ↓



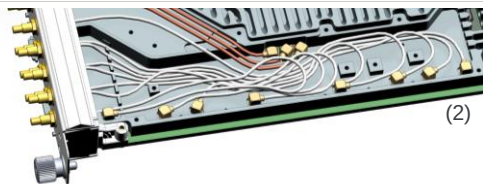
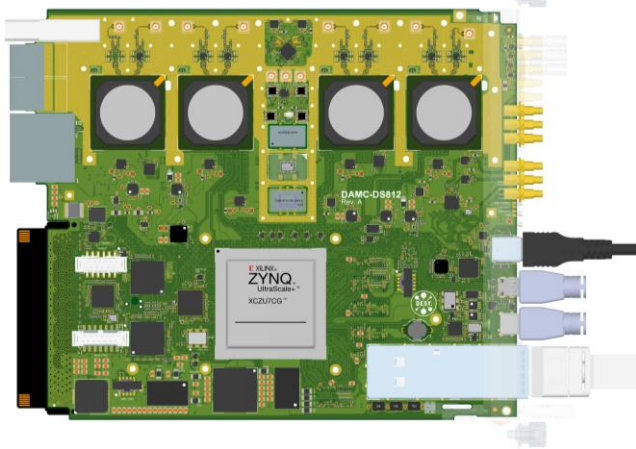
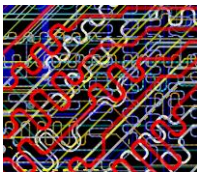
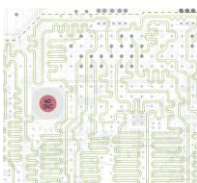
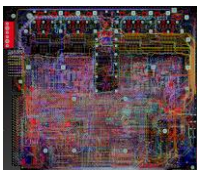
AFE+ADC+interface latency



Courtesy of J. Marjanovic, U. Mavric

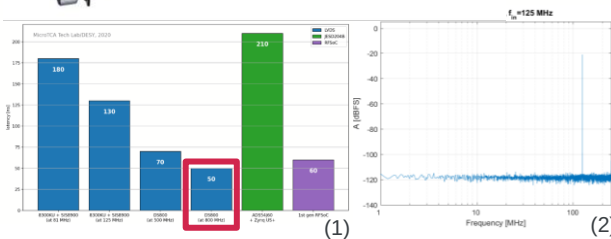


(2)

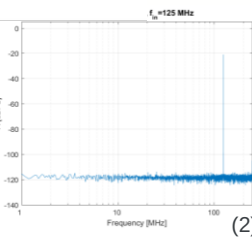


(2)

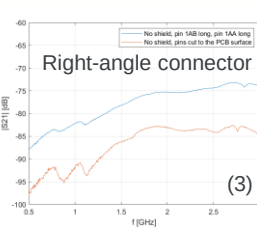
- Low-latency 8-channel 12 bit ADC board
- Xilinx Ultrascale Plus SoC: Stand-alone mode (“Scope“)
- Based on new coaxial analog Zone 3 Class RF1
- AC and DC inputs: Front and RTM 3 RF inputs
- 800 MSPS / 1600 MSPS, 4GBytes data memory
- 2.7 GHz input bandwidth (amplifiers: 4.8 GHz)
- Synchronous operation: exactly length-matched paths
- Excellent performance expected (measured on FMC)
- Dedicated per-chip clock inputs
- Low-noise PLL with on-board VCXO and TXCO
- Trigger inputs and White Rabbit support
- PCIe Gen.3 x 8 and zQSFP+ support
- Support for JESD DACs via Zone 3



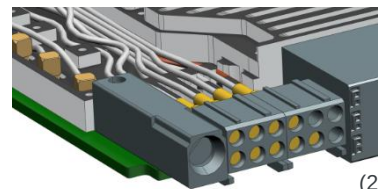
(1)



(2)



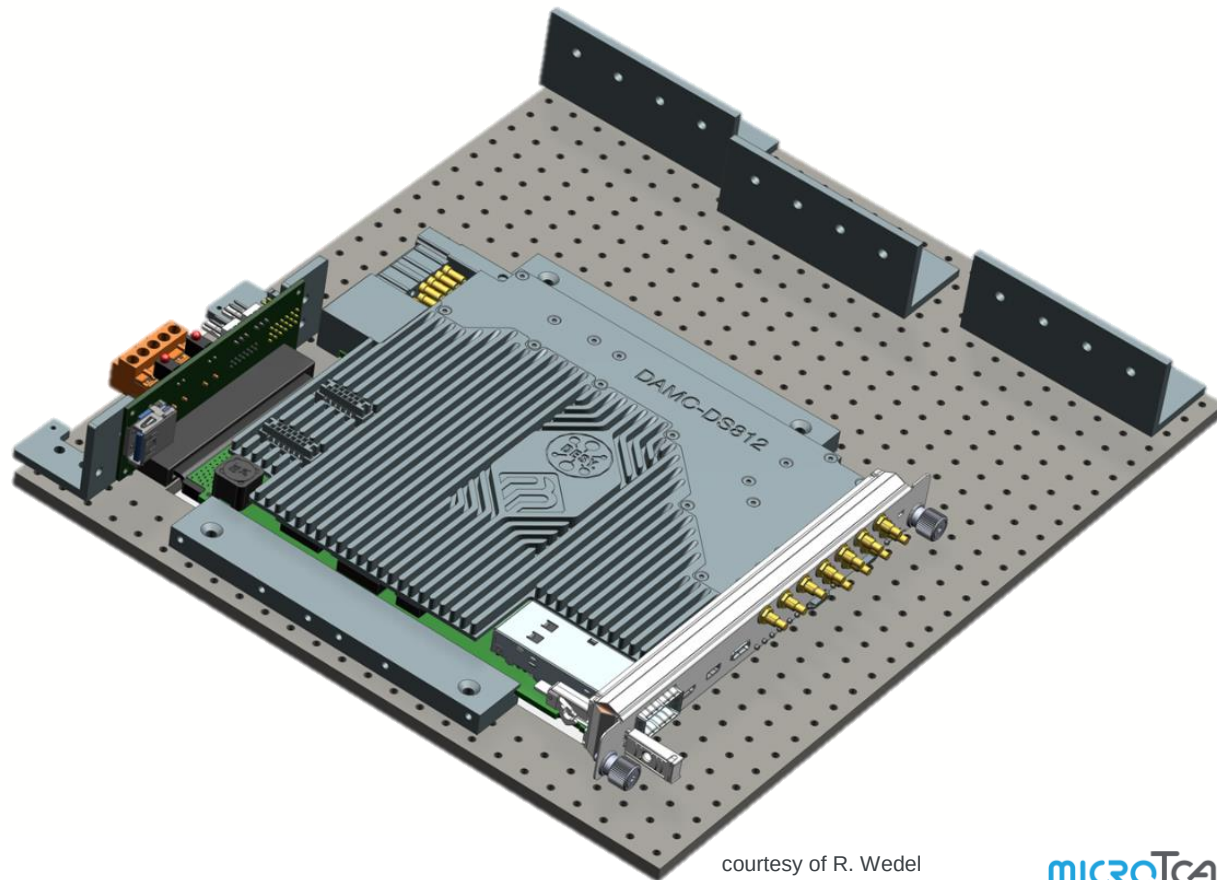
(3)



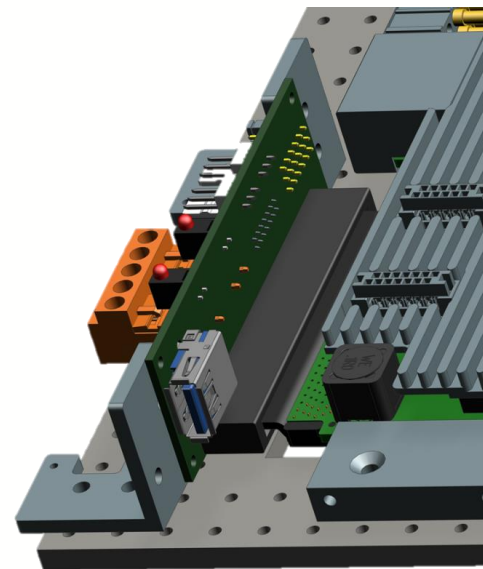
(2)

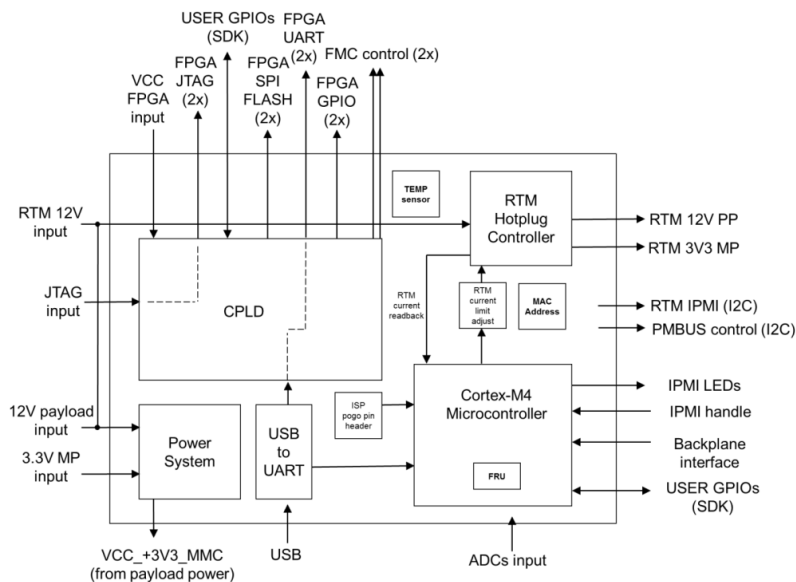


- (1) courtesy of J.Marjanovic
 (2) courtesy of J.Zink
 (3) courtesy of S.Jablonski

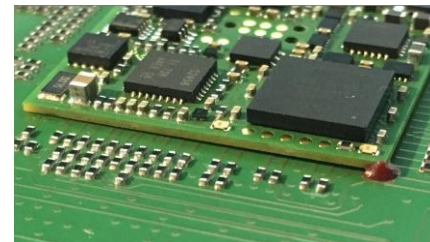
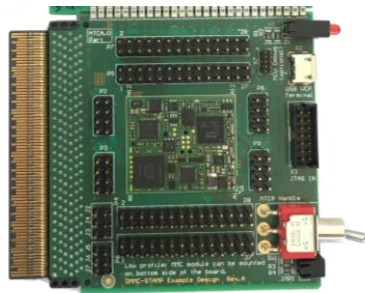
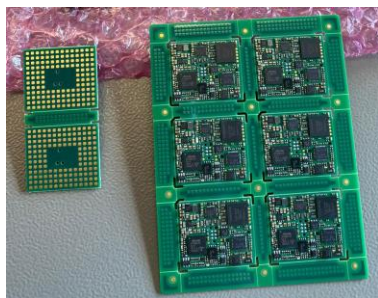


courtesy of R. Wedel

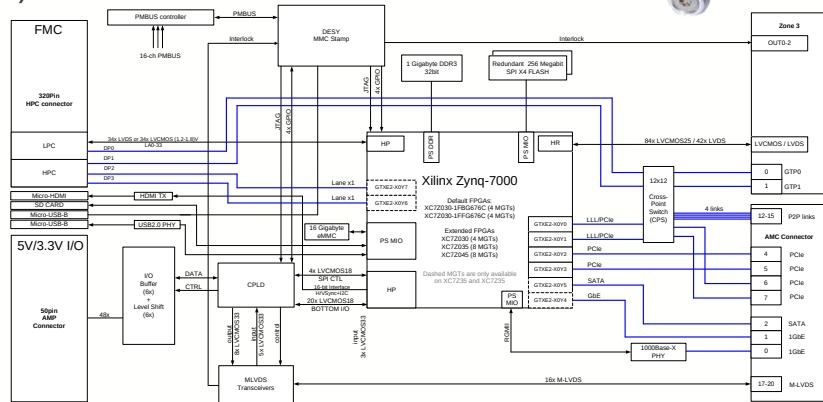


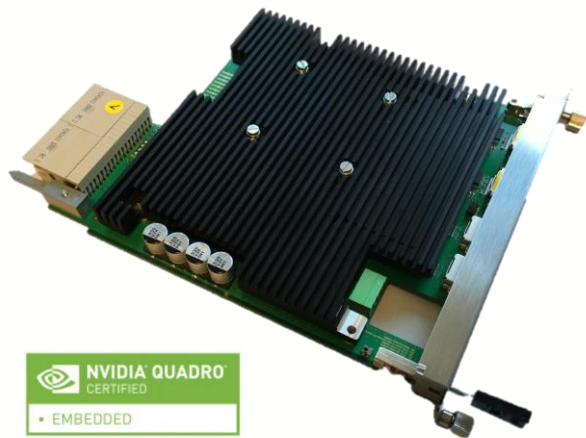


- MMC is integrated: System-on-Module
- Highest integration: Power, USB, MCU, RTM, Translators
- Shipped as a pre-programmed LGA module
- Handles MCH Communication, RTM, FPGAs, JTAG, FMCs
- Simplest drop-in solution: no code, components, schematics
- High-density PCB with chip-scale components
- Code is maintained by DESY, SDK will be available
- In-system update via HPM (also for FPGA memories)
- Effort was put into code maintenance and compatibility



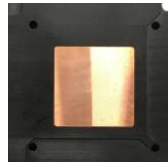
-





NVIDIA Quadro RTX 3000

- Idea: contribute to MicroTCA ecosystem
- Solution for GPU processing in MTCA
- Machine learning (CUDA, TensorFlow)
- Designed for concurrent AM900 CPUs
- Space available in typical installations
- Host standard MXM graphics cards
- Internal or external power input (12V-19V)
- 2x Display Port, 2x USB on rear panel
- MXM module can be installed by user
- Cooler: copper core, backplate + bushing



Vielen Dank für Ihre Aufmerksamkeit

Thank you for your attention