### IRIO-OpenCL: Applications of OpenCL to instrumentation use cases for the MTCA platform

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- Context
- MTCA System Architecture
- IRIO-OpenCL applications
- Conclusions









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### One research group on instrumentation

- 1 Full Professor
- 7 Asociate professors

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ACÚSTICA APLICADA

- Tens of researchers
- 10 years of work relations with ITER
- Work related to EPICS, FPGAs, interlocks...
- Working with CIEMAT, JET, ITER, F4E, RFX, IFMIF, Indra, Sgenia, Imperial College, Airbus,....









### Context

Previous work with diagnostics/intrumentation

- High speed DAQ with flexRIO, cRIO.
- Integration into EPICS?

**IRIO.** No more driver compilations for FPGA changes in NI platform.

New ITER drivers based in Nominal Device Support v3

- MTCA and NI hardware drivers
- MTCA supports multiple vendors....

**IRIO-OpenCL.** Standard and high level programing in FPGA... standard, modular and maintainable drivers with NDS.

# IRIO-OpenCL is <

Vendor agnostic (OpenCL)
Muti Control System (NDS) core-interface
Modern, modular, standard (C++11)









# OpenCL before...

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#### OPEN STANDARD FOR PARALLEL PROGRAMMING OF HETEROGENEOUS SYSTEMS



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# OpenCL v3 specc today

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### Neutron diagnostics

Experienced in the developed examples of high speed acquisition in PXI platforms for neutron diagnostics





**Neutron Flux Measurements** 

- Low intensity  $\rightarrow$  Pulse Detection
- High intensity → Campbelling



Neutron/Gamma discrimination in fusion enviroments

- Pulse Detection
- Examples based in BC-501 liquid scintillator

ML!

Classification of Gama-Neutron suing SVM Reproduced from [Gelfusa]. JET Pulse no. 90653



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# System Architecture Example

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PC + PCle + MTCA + AMC + (PROCESSING) + (I/O)



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# **OpenCL FPGA application**

- The part of OPENCL that goes into the C++ drivers.
- Host sends commands and can set Global Memory (DDR) (SLOW!)
- Critical processes can be organized with a chain of pipes (HDL=AXI ST)
- Data can be gathered from I/O pins, but kernels are launched from host.



# IRIO-OpenCL

- Many new cards in PCIe form factor.
- Evaluation of the algorithms
- The processing kernels are easily ported





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# IRIO-OpenCL integration

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- The test application is introduced into a generic Processing node.
- State Machines control execution.
- Automatically connected to the CS.
- Basic DAQ functionality is covered with IRIO-OpenCL kernels.
- Explore devices and connect to them.



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### 14 bit 1 GS/s



- 1ms window
- 170MHz kernel clock
- Lots of room for more processing <40% FPGA resources.</li>
- BSP is around 15% resources.







### Use case 2: Simple MLP classifier

**OpenCL** 

optimization

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#### Poster presentation at SOFT2020

- >6k weights MLP 32bit float.
- ARRIA10 FPGA. Hardened 32b FP DSPs.
- ~200MHz kernel clock frequency.
- 0,5 to 14 GFLOPS

#### Adjustable parallelization:

- 30% area usage.
- Over 30 kEvents/s
- 32%
- Over 300 kEvents/s
- OR 70% area usage
- <u>Adjustable parallelization to 1300 kEvents/s</u>

### OPENCL



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### Use case 3: Full CNN development

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#### **Oral presentation RT2020 + Student Paper Award**

- 2532 weights CNN 32bit float.
- ~190MHz kernel clock frequency.
- 50% area usage.
- Preliminary latency results ~50 us.
- Pipelined design 79,8 kevent/s  $\rightarrow$  ~14 GFLOPs
- Maximum error in the classification with the test signals of 0.8% (gamma), 0.9% (neutron), 2.5% (close pileup), and 1.1% for each class.
- Collaboration with JET.



1 x 100 x 1
data
20 x20
weights tanh
40 <u>x 1 x </u> 20 (local mem)
STREAM
PE 20
data
weights tanh
15 x 1 x 8 (local mem)
Flatten
120(local mem)
STREAM
data 💛
×4
weights softmax
STREAM
Global Memory (external DDR)



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- DAQ combined with OpenCL reduces development of highperformance processing. OpenCL enables C-like development !!
- We are increasing the features of IRIO-OpenCL by developing example applications.
- We have a generic model for processing applications that is well suited for ML applications.







# Future Work

### • Future work:

- Expand IRIO-OpenCL functionalities.
- Test possibility of using SYCL.
- Prepare to open the framework to users.
- Look into the integration of HDL components.
- Looking for more use cases (possible collaborations) using IRIO-OpenCL -> Contact us!







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# Thank You! Questions?



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