Update on MicroTCA developments at SOLEIL

On behalf of SOLEIL digital electronic designers working group

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Outline

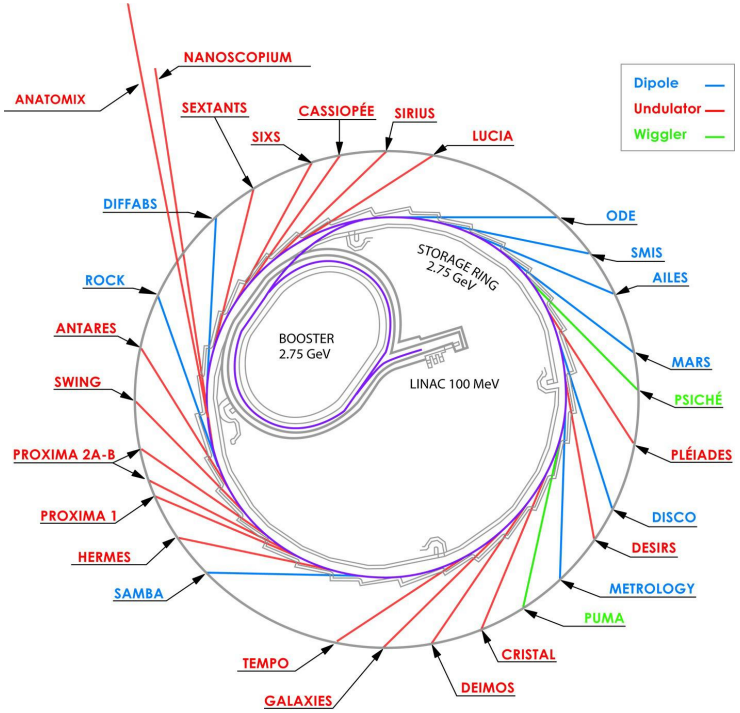
- SOLEIL overview
- MicroTCA experience
- Ongoing projects
- Roadmap

SOLEIL in a nutshell

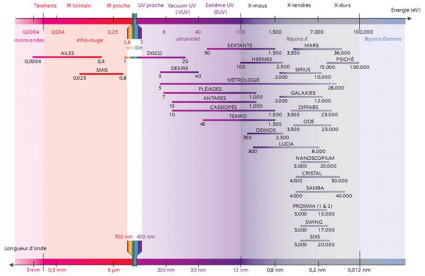
Synchrotron SOLEIL company : created in 2002 to operate & build SOLEIL

CNRS 72% - CEA 28% ; ~450 people (350 permanent)

- Emittance = **4nm.rad;** Circumference = **354 m and** Energy = **2.75 GeV.**



- **29 Beamlines** :
  - ✓26 built in 2 phases; then 3 on project funding.
  - ✓24 on insertion devices; 5 on bending magnets.
- **9 orders of magnitude in energy from far IR to hard X-rays:**



- **Support laboratories in 5 areas:** Biology (2), Chemistry (2), Surface Science, High pressure, Microfluidics.

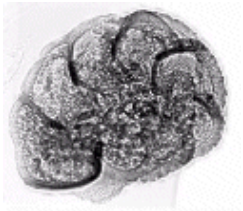
~1200 proposals per year : ~500 accepted ;

2391 unique users in 2017 from 880 laboratories (~ 10000 users from 2200 laboratories since 2008); ~ 1/3 foreign users

New Imaging and Tomography Beamlines

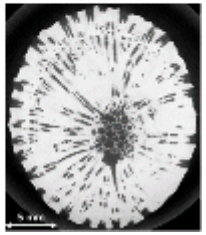
2017 NANOSCOPIUM

Fast multimodal 3D imaging, ptychography
High spatial resolution and analytical sensitivity

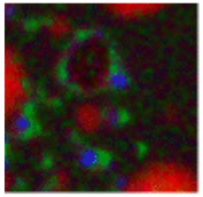


2018 anatomix

Parallel beam microtomography
TXM



2017 HERMES

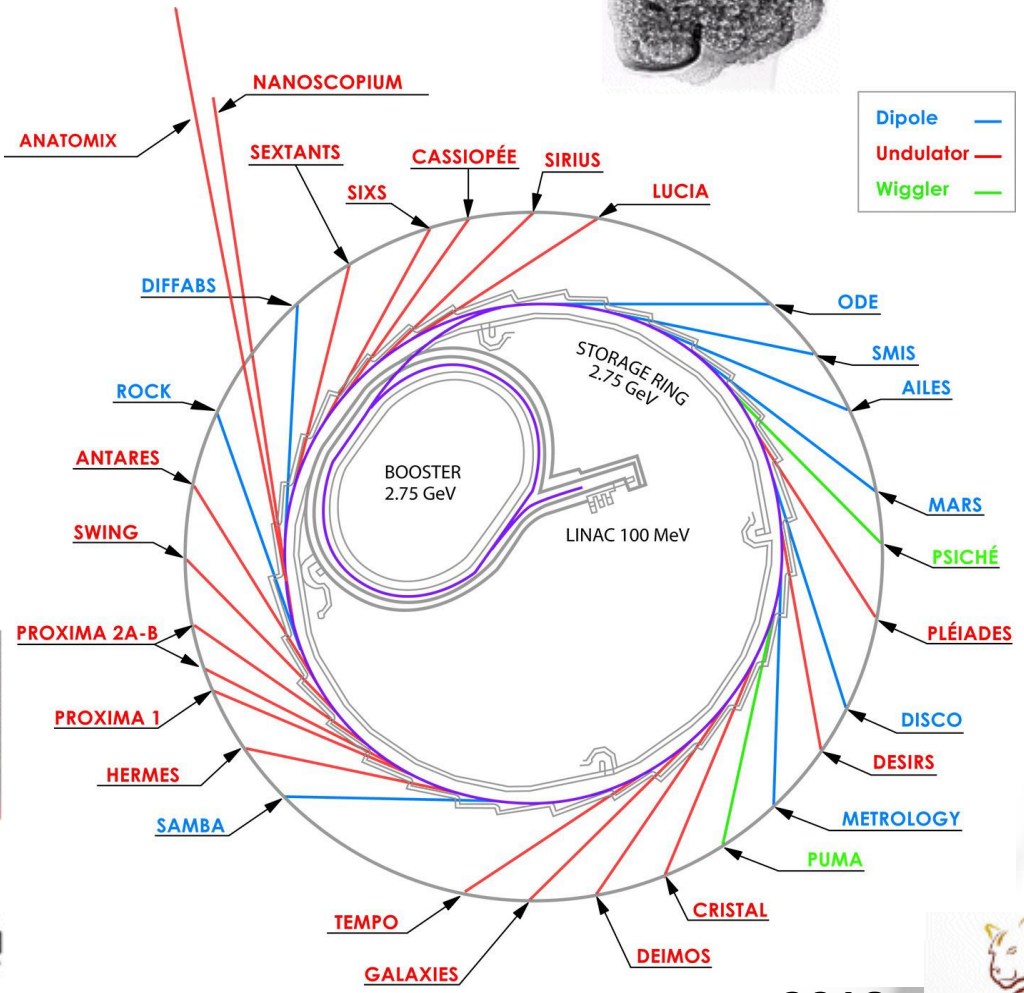


STXM + PEEM
14 x 3.5 µm²
10^{12}-10^{13} Phs/s
Resolving power > 10^4

Sub-10nm resolution
(C. David)

PAUL SCHERRER INSTITUT PSI

nffa.eu



2018 PUMA

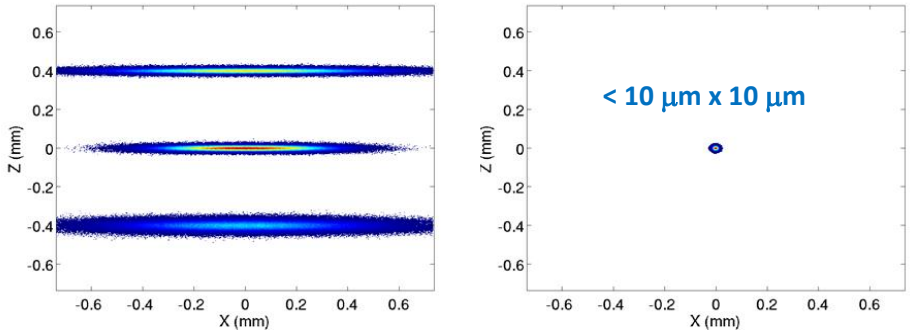
SOLEIL UPGRADE: Boundary Conditions and Constraints

- Reaching an emittance **< 100 pm.rad.**
- Keeping the same electron beam energy : **2.75 GeV**
- Preserving a maximum current of **500 mA** in the multibunch mode.

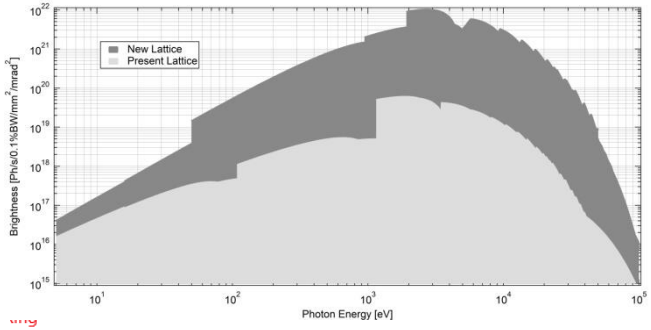
- The impact on the current positions of the beamlines should be minimized as **much as possible.**
- At least 4 beamlines on "**superbend**" (B ≥ 3T).
- Two extractions for IR photon beam considered, including one towards the largest wavelength possible.
- The period without beam for users, including the dismantling of the current machine, installation and commissioning of the new machine is expected to be between **18 and 24 months.**

Performances

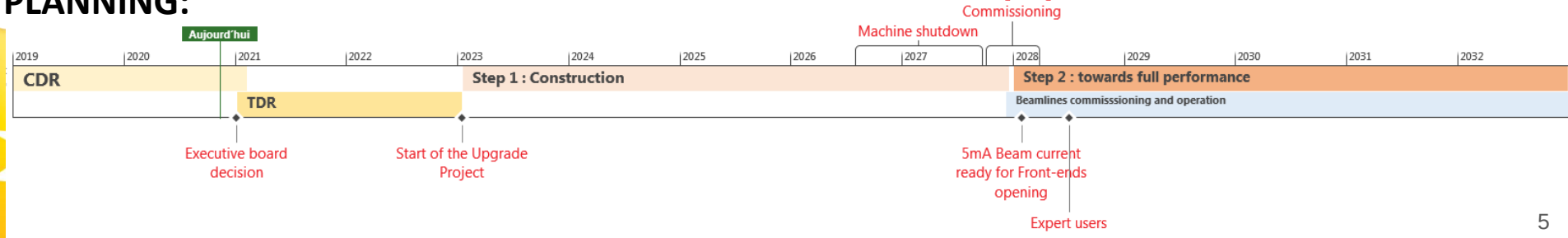
Beam SIZES:



Brilliance:



PLANNING:



MicroTCA experience

SOLEIL context

Transition from 15 years of operation toward an Upgrade (accelerators and beamlines)

- Managing obsolescence
- Identifying adapted new technologies
- Building architecture for the next decades

Transverse working group

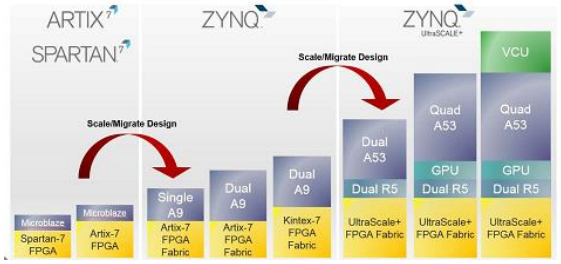
- ~10 digital electronic designers across SOLEIL
- Sharing experience, expertise and developments

Obsolescence

- Large installed base of cPCI systems
- Libera electronics for Machine BPM and Feedback
- Analog LLRF

New technology based on SoC (System-On-Chip) or FPGA with large range of scalabilities

- Custom electronics based on SOM (System-On-Module)
- MicroTCA
- PCIe board
- Others



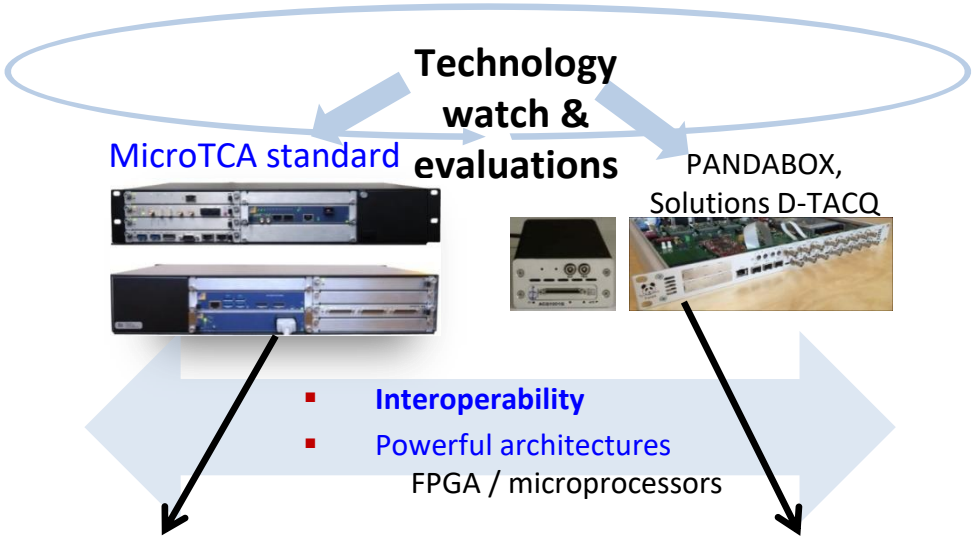
Architectures

- Hardware
- Firmware
- Software

Guidelines: systems flexible & easy to maintain, development shared inside SOLEIL and open collaboration with big physics partner facilities or industries.

Requirements

SCALABILITY **INTEROPERABILITY** **FLEXIBILITY**

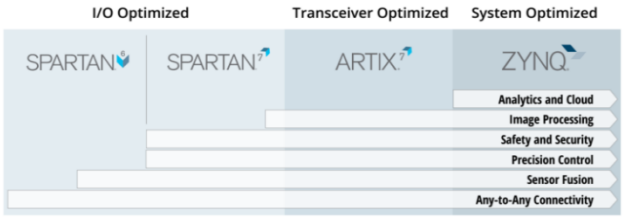


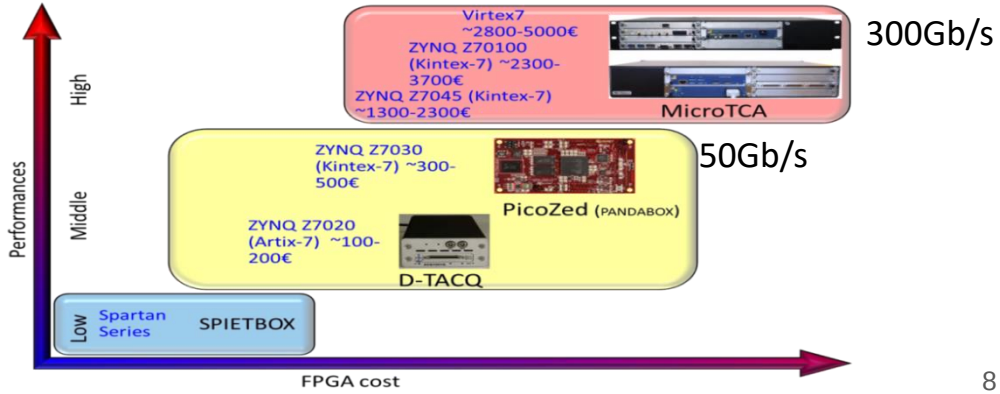
Well adapted for **demanding applications;** Technology intended for medium – long term

Well dimensioned for short term requirements

DAQ and data processing platform

- Improve **performances** (reduce dead time for DAQ, higher throughput…)
- Improve **embedded processing capability** and **flexibility**
- Improve **data processing** for **triggering and feedback** (FPGA processing, image processing…)
- Embed preprocessing **close to the sensors** in order to facilitate soft-processing





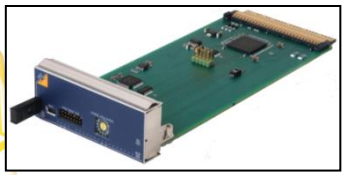
First step with MicroTCA

- Follow up MicroTCA development in the community over the MicroTCA workshop
- Contact with MicroTCA technology lab about the standardization PICMG
- Discussions with others facilities: ESS, Diamond …
- Evaluation of electronics from various vendors and their interoperabilities

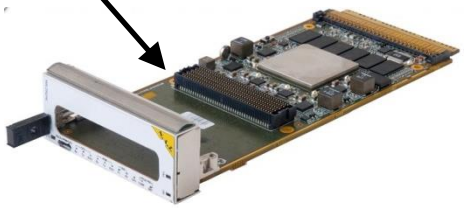
NAT-MCH-PHYS80 MTCA Carrier Hub for MTCA.4 and MTCA.4.1 applications supports GbE and PCIe Gen 3 switching and optical & copper PCIe x8/x16 uplinks

NAT NATIVE-mini
Smallest (1U) MicroTCA-chassis for industrial applications

Integrated MCH



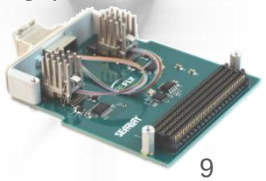
NAT-JSM
JTAG Switch Module



NAMC-ZYNQ-FMC: FMC Carrier AMC with Xilinx ZYNQ-7000 FPGA
AMC for data acquisition & signal processing applications and computing nodes based on MicroTCA and AdvancedTCA

+

FMC SFP (1Gbps)/SFP+ (10Gbps)
High throughput Interface



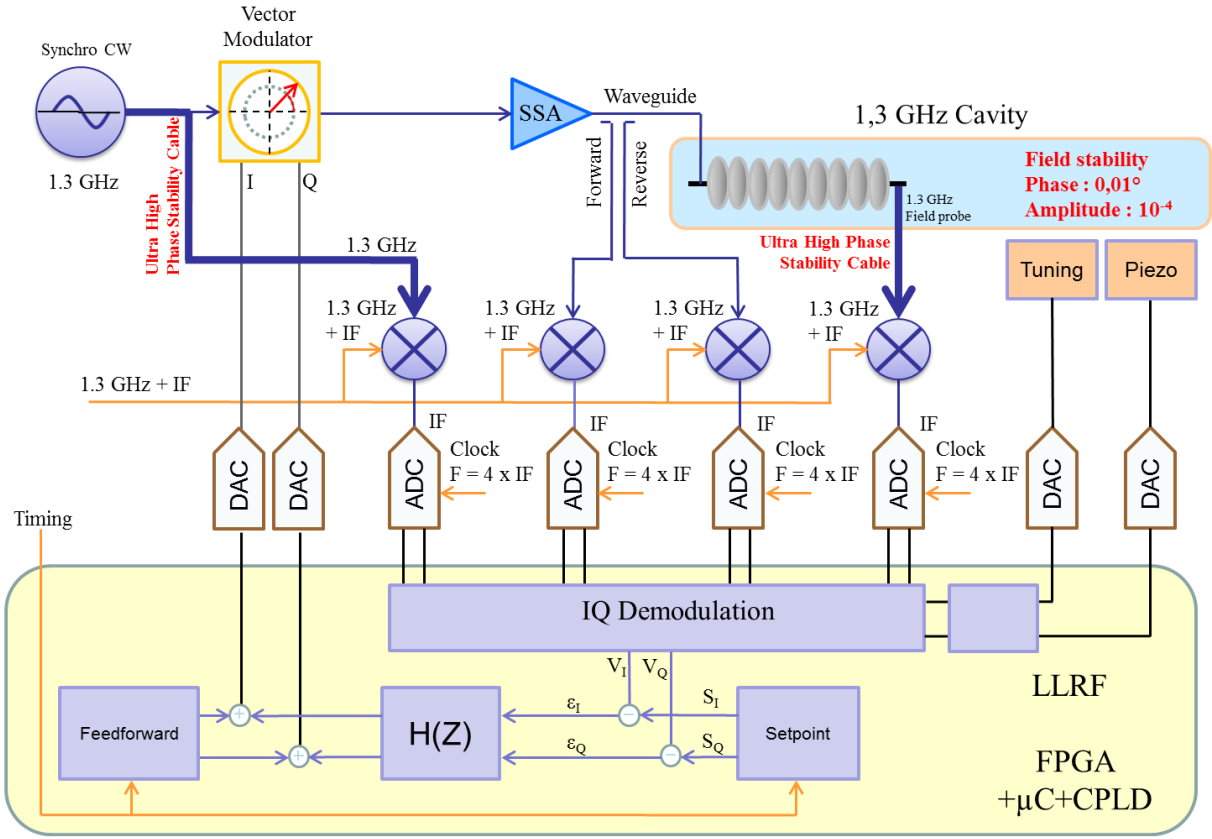
FMC firefly module (14Gbps x 10)

Ongoing projects

LUCRECE DLLRF for LUNEX 5 project

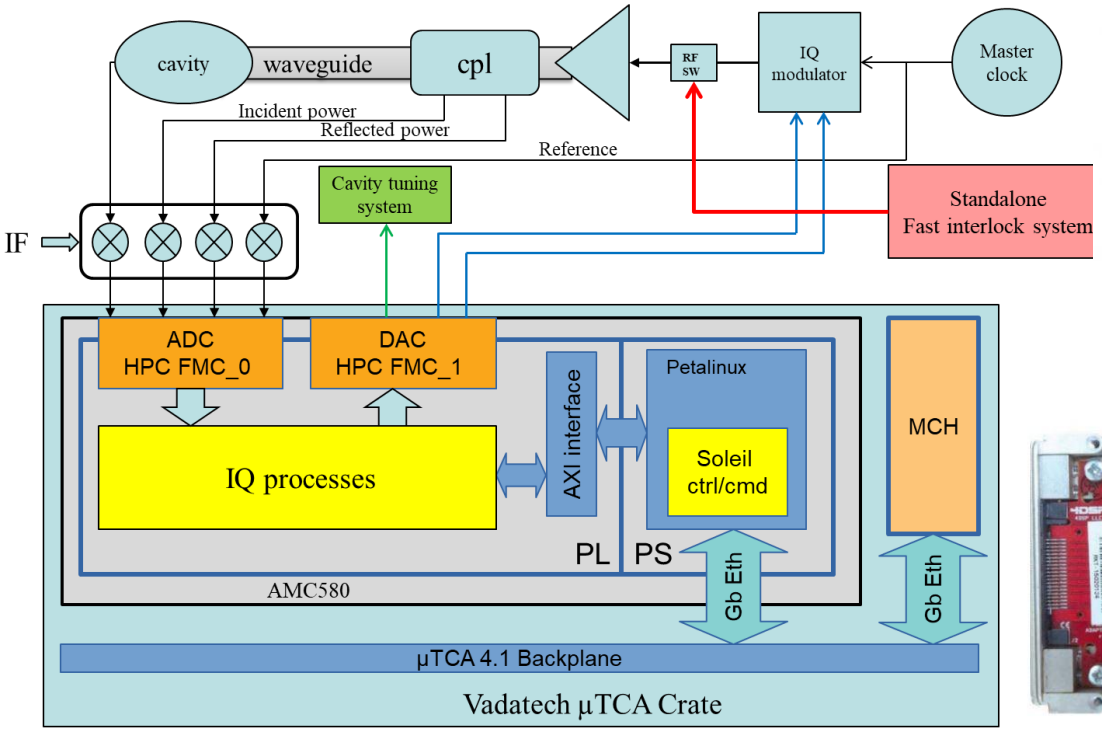
- **LUCRECE :** R&D program about RF technology for CW Linacs, with the aim to LUNEX5

Coordinated by SOLEIL, involves the CEA and CNRS labs as well as industrial partners, Thales, Alsyom and SigmaPhi Electronics (SPE) ; partly financed by the Region of Ile-de-France.

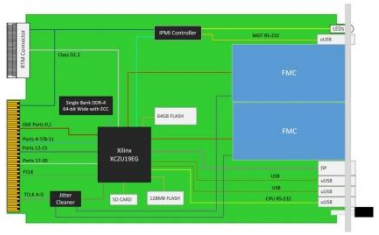


Contacts M.Diop, R.Sreedharan in RF group

The progress of the DLLRF on MicroTCA



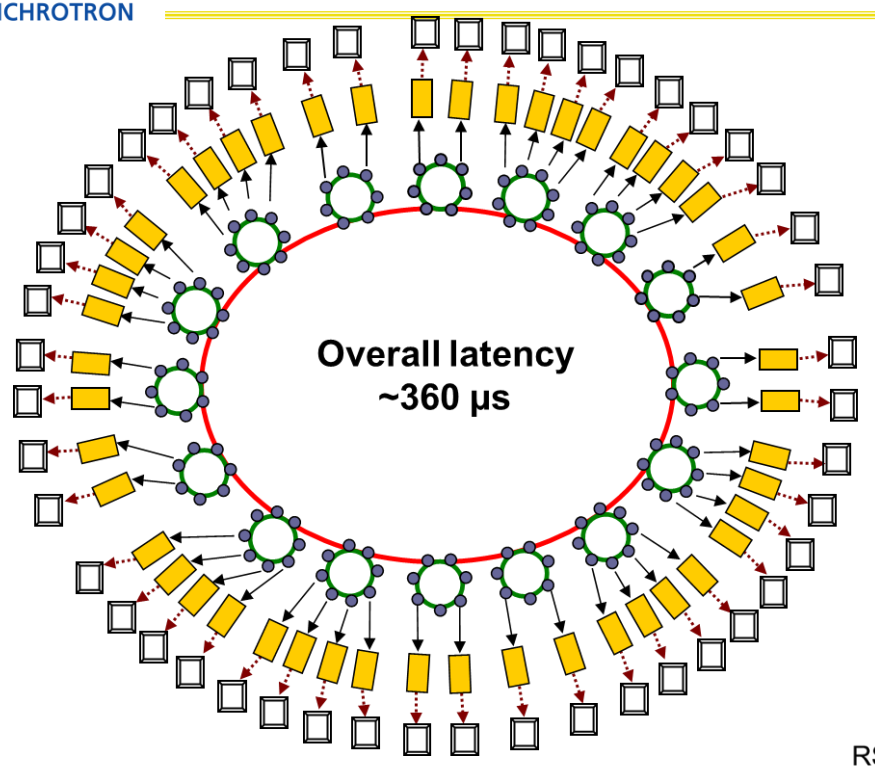
Block Diagram



- 4 channels ADC FMC board (TECHWAY) successfully interfaced into the Zynq of the ZC706 evaluation board, IQ process tested and validated
- Configuration and setup of Vadatech MicroTCA: done
- Migration of the previous development to the AMC580 (Vadatech) board is successful
- Development of python socket server on PS side for communication is done
- Interfacing of DAC FMC board (FMC224) is ongoing
- Interoperability difficulties during development: Vadatech AMC580 seems not working on NAT MicroTCA rack
- After repairing of the power supply of AMC580, we never tried it again and AMC580 is working fine on Vadatech rack

Today status: The main deal is to interface the DAC FMC.
Then all IQ process are ready to be implemented.

Fast Orbit FeedBack (FOFB) system



Existing architecture

Libera rack
(7 or 8 units)

Power supply
rack (2 planes)

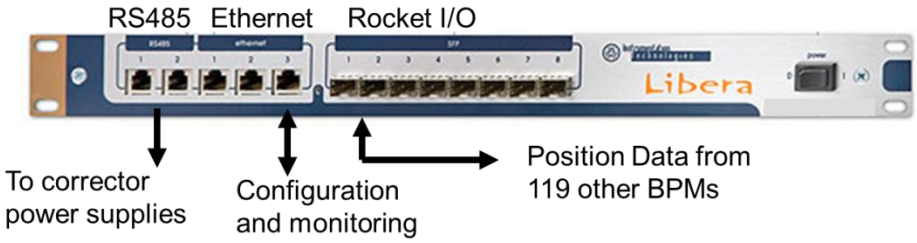
Air-coil magnet
(2 planes)

Copper link

Optic link

RS 485 link

2 conductor
copper cable



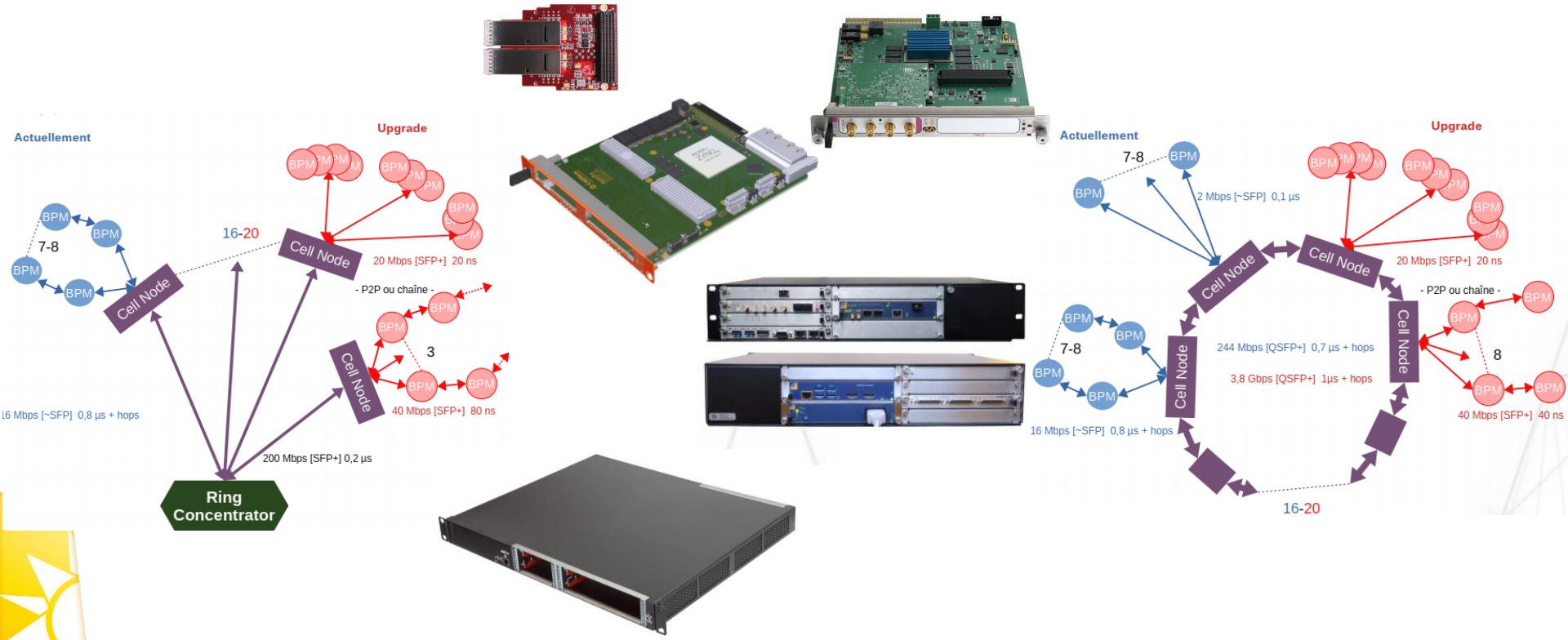
Libera electronics

- BPM (Beam Position Monitoring) and FOFB (Fast Orbit FeedBack) currently embedded in a single electronics
- The electronics Libera from Instrument Technologies integrated around the storage ring is obsolete

Contacts M.Hubert, R.Broucquart in diagnostic group

FOFB upgrade project

- Splitting BPM and FOFB is the first step for SOLEIL Upgrade
- Requirement for modularity : should work with actual/next BPM electronics and actual/next storage ring
- Two topologies analysed: « Single point processing» or « Ring »
- MicroTCA option identified to address requirements with AMC, FMC cards from various vendors
- Electronics are being purchased for evaluation and prototyping



- NAT, Vadatech, Struck, CAENels… depending on the topology

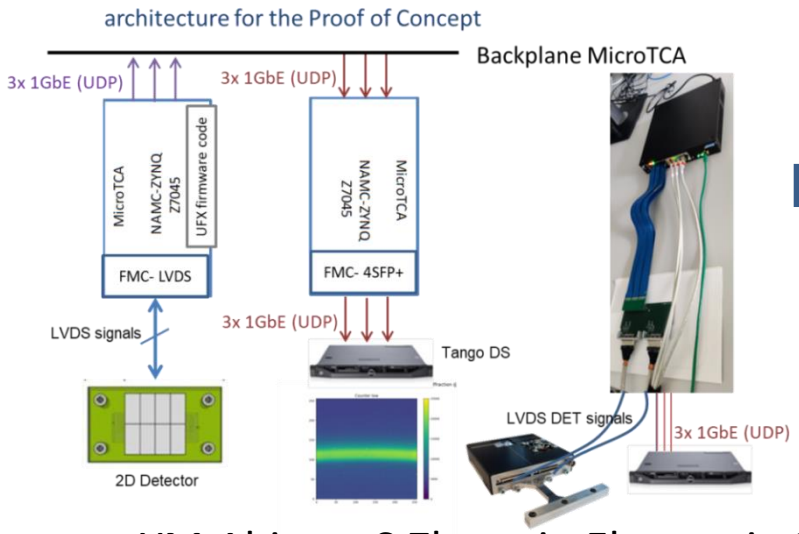
Evaluation for 2D hybride pixel detector readout

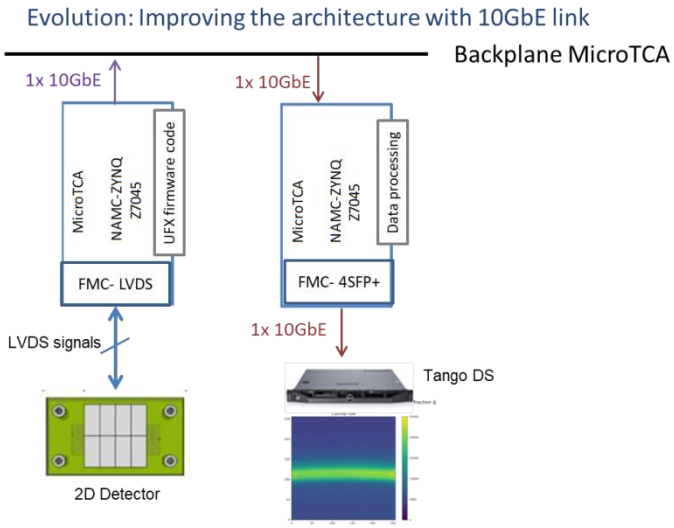
Current architecture for 2D X-ray detector acquisition

Hardware & Firmware adapted from PandABox* (based on Zynq 7030)

* https://ohwr.org/project/pandabox/wikis/home

- Detector firmware porting to a MicroTCA AMC card (NAT NAMC Zynq7045): done and compatible with same software
  - Demonstration with the detector to prove the whole chain functionality after the code porting
- Adding 10GbE to improve performance: not working for the moment, probably due to the card performance limitation





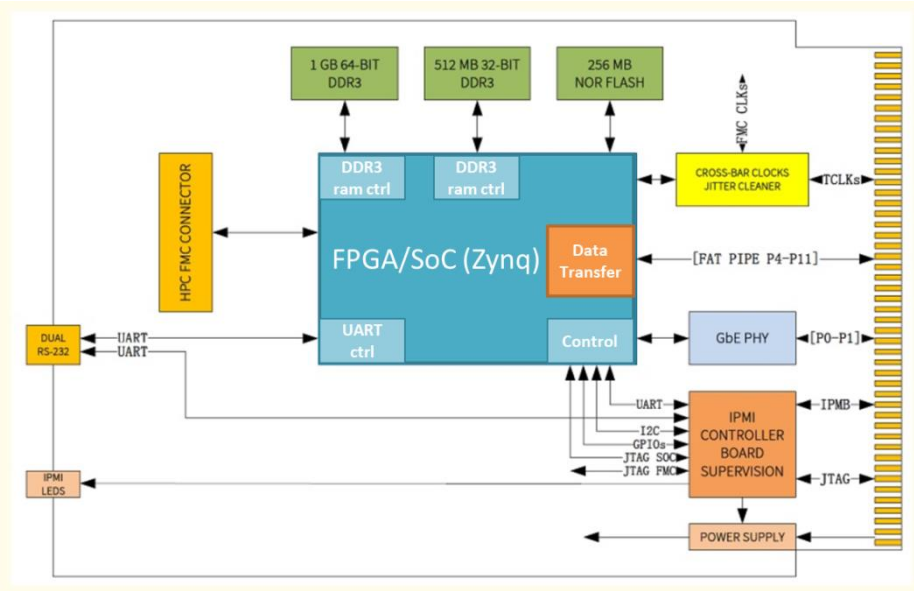
Contacts YM.Abiven, S.Zhang in Electronic Control and Acquisition group

Contact D. Arkadiusz in Detector Group

Roadmap

Build a generic framework on MicroTCA

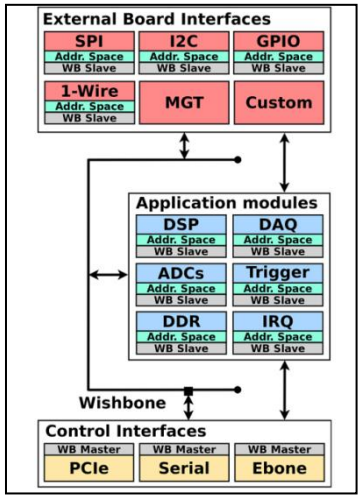
- Approach
  - Similar to PandABox
  - Common concepts for MTCA framework
    - **Flexibility**, **reuse** of component IPs,
    - **follow standards** as possible, scripted workflow
    - **easy integration** of new modules
  - Industrial support: Companies and MTCA TechLab (DESY)



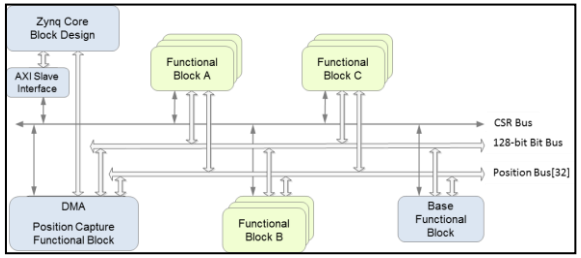
- Specification to be defined
  - Architecture (HW, FW, SW)
  - Interface for Control (PCIe, GbE …) and Data streaming & sharing (FAT PIPE)
  - FPGA internal modules communication interface
  - Reusable functions (DDR3 control, PCIe interface, register bank, …)
  - Auto-generation tools for custom module integration
  - Driver and library for remote clients (TANGO/EPICS…)
- Evaluation of existing platforms and solutions
  - ESS BI AXI4, IOxOS TOSCA, CERN IFDAQ, LNLS BPM etc.

Expected approach: generic framework

Modular Interfacing & Processing

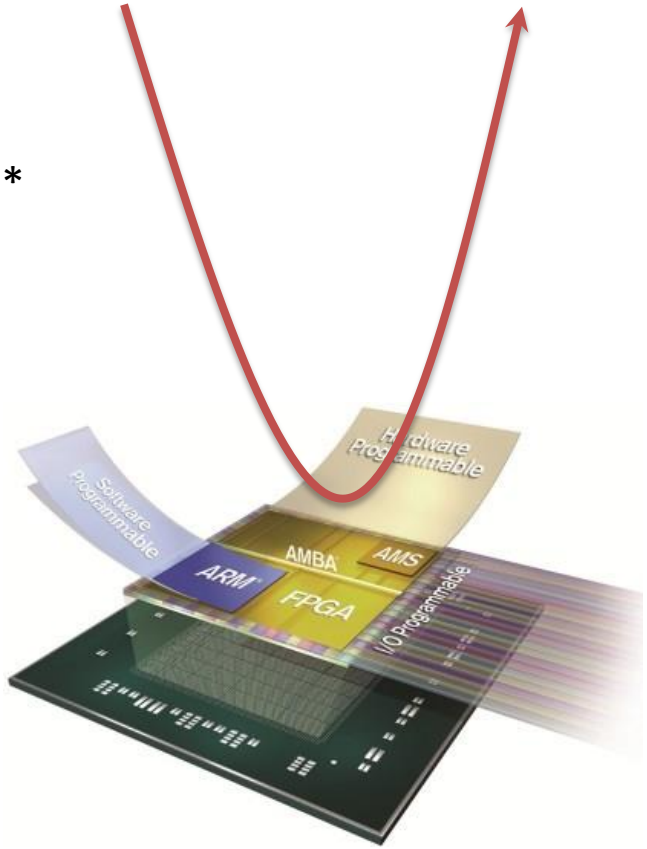


LNLS, Sirius*

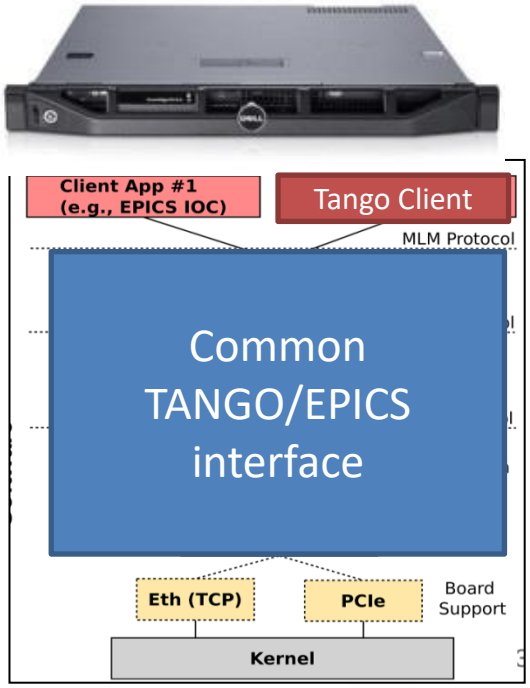


PandABlocks (SOLEIL & Diamond)

Data flow



Control Framework Ready



Gateware

Software

Modular Powerful Connectable

Flexible Framework architecture

for embedded processing and connectivity for Control and DAQ

* See Lucas Russo (LNLS, Sirius) presentation : ICALEPCS-2019-FPGA-Workshop

SOLEIL challenges

- Managing obsolescence

- Improving automation and feedback for machine and beamlines between DAQ, Robot, motion systems, IoT…

  (Interested in EtherCAT interface)

- Sharing development inside SOLEIL FPGA developers

  Interested in CI/CD for SOC/FPGA dev similar to LBL approach (Vamsi Vytla, ICALEPCS-2019-FPGA-Workshop)

- Creating MTCA network with other institutes and SMEs (Small Medium Entreprise) in France.

  Following techlab initiatives

- Interested in sharing development in a collaborative manner

  Please contact us if you have common interests


THANK
YOU
GRACIAS
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BOLZIN
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SHUKRIA
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