Digitizers
for Big Physics

Kacper Matuszynski
Sales Engineer Europe

TELEDYNE SP DEVICES
Everywhere**you**look™

The 9th MicroTCA Workshop
for Industry and Research

AGENDA

- ❖ About Us
- ❖ Technology
- ❖ Products in MTCA.4
- ❖ Developments

About Teledyne Signal Processing Devices

- **Innovative supplier**
    - Spin-off from Linköping University, Sweden (2004)
    - Research since 1998 with 65 active patents

- **Skilled team**
    - More than 80% are holding a PhD or MSc engineering degree
    - 60% of our employees work in R&D

- **Production capacity with the highest standards**
    - ISO 9001:2015, ISO 14001:2004, IPC-A-610
    - High-volume capacity

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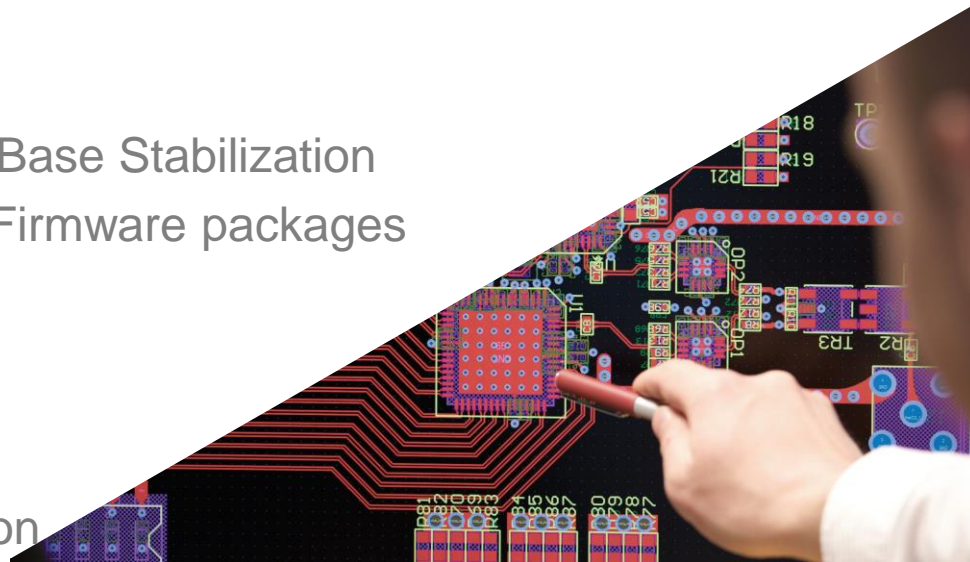
Technology

- **High-Speed Digitizers**
  - Portfolio reaching 10GSPS at 14bit
  - High-precision trigger (resolution:50ps; jitter:25ps)
  - Multi-channel synchronization support
  - 52ns re-arm time

- **Signal Processing**
  - Core IP: Interleaving and Digital Base Stabilization
  - Selection of application-specific Firmware packages
  - Open FPGA

- **Software Development Kit**
  - Digitizer Studio
  - Rich example code documentation
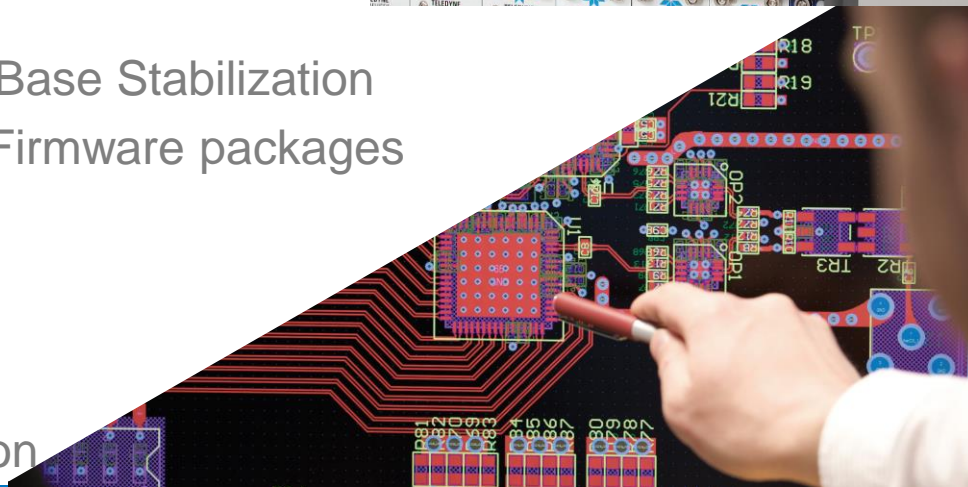
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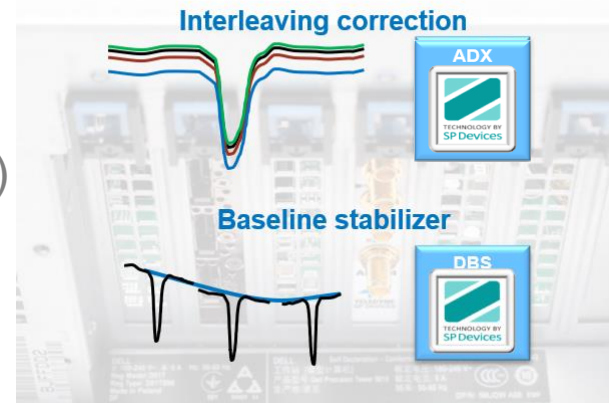
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Interleaving correction

ADX
TECHNOLOGY BY
SP Devices

Baseline stabilizer

DBS
TECHNOLOGY BY
SP Devices

Technology

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Product Portfolio in MTCA.4

- **ADQ412**
  - 2 / 4 channels
  - 4 / 2 GSPS
  - 12-bit resolution

- **ADQ14**
  - 2 / 4 channels
  - 2 / 1 GSPS
  - 14-bit resolution

- **ADQ7**
  - 2 / 1 channels
  - 5 / 10 GSPS
  - 14-bit resolution

- **ADQ8**
  - 8 channels
  - 1 GSPS
  - 10-bit resolution

Product Portfolio in MTCA.4

- **ADQ412**
  - 2 / 4 channels
  - 4 / 2 GSPS
  - **AC-coupled**
  - **BW 1.3 GHz**

- **ADQ14**
  - 2 / 4 channels
  - 2 / 1 GSPS
  - **DC-coupled**
  - **BW 1.2 GHz**

- **ADQ7**
  - 2 / 1 channels
  - 5 / 10 GSPS
  - **DC-coupled**
  - **BW 3 GHz**

- **ADQ8**
  - 8 channels
  - 1 GSPS
  - **DC-coupled**
  - **BW 500 MHz**

Product Portfolio in MTCA.4

ADQ412
- 2 / 4 channels
- 4 / 2 GSPS
- **1 GByte DRAM**
- **Xilinx Virtex-6**

ADQ7
- 2 / 1 channels
- 5 / 10 GSPS
- **4 GByte DRAM**
- **Kintex Ultrascale XCKU085**

ADQ14
- 2 / 4 channels
- 2 / 1 GSPS
- **2 GByte DRAM**
- **Xilinx Kintex7 325T**

ADQ8
- 8 channels
- 1 GSPS
- **1 GByte DRAM**
- **Xilinx Kintex7 325T**

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Product Portfolio in MTCA.4

ADQ412
- 2 / 4 channels
- 4 / 2 GSPS
- AC-coupled
- **Flexible configuration**

ADQ7
- 5 / 10 GSPS
- 4 GByte DRAM
- Kintex Ultrascale XCKU085
- **Maximum performance on few channels**

ADQ14
- 2 / 1 GSPS
- 2 GByte DRAM
- Xilinx Kintex7 325T
- **Large arrays of high-performance measurement**

ADQ8
- 8 channels
- 1 GSPS
- **Multi-board synchronization targeting single shot installations**

Product Portfolio in MTCA.4

- **ADQ412**
  - 12-bit resolution
  - 2 / 4 channels
  - 4 / 2 GSPS

- **ADQ14**
  - 14-bit resolution
  - 2 / 4 channels
  - 2 / 1 GSPS

- **ADQ7**
  - 14-bit resolution
  - 2 / 1 channels
  - 5 / 10 GSPS

- **ADQ8**
  - 14-bit resolution
  - 8 channels
  - 1 GSPS

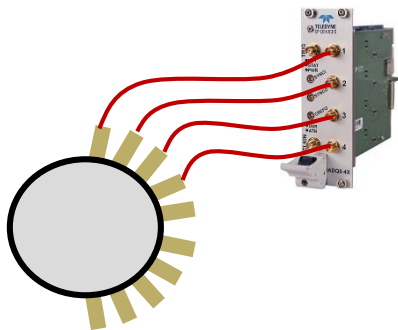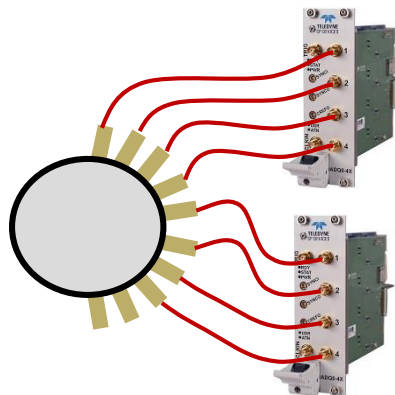**NEW DEVELOPMENT
WAS REMOVED
FROM THIS PUBLIC PRESENTATION**
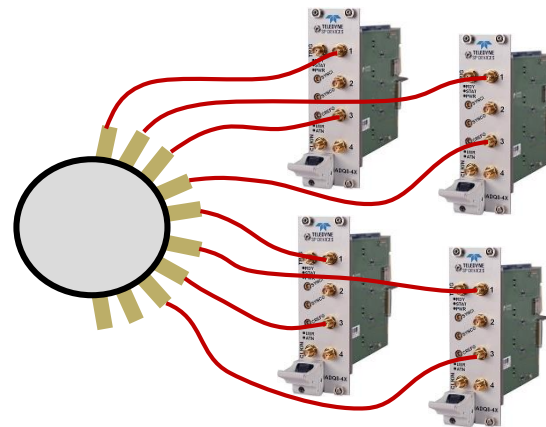
Developments – Sampling Switching

- The benefit of switchable sampling rate – **re-use of existing equipment**
- Adapted to phases of the project/experiment
  - proof of concept, prototype, final experiment)
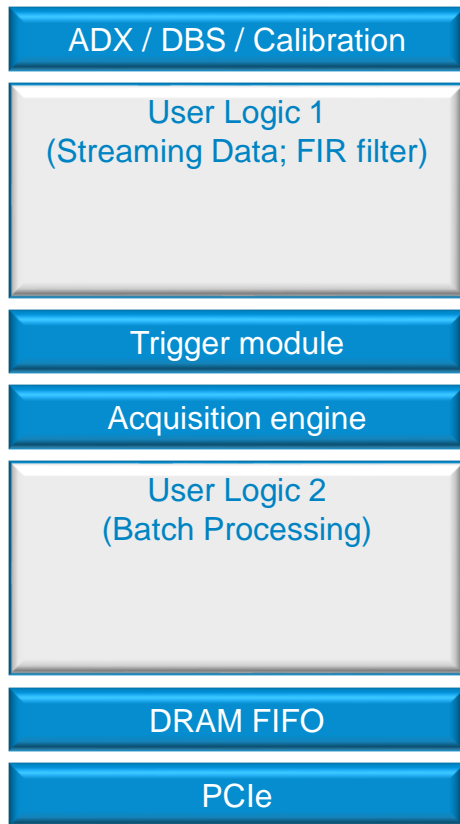

Initial tests
4 channels @ 2.5GSPS

More channels
8 channels @ 2.5GSPS

Upgrade of performance
8 channels @ 5 GSPS

Developments – Open FPGA

ADX / DBS / Calibration
User Logic 1 (Streaming Data; FIR filter)
Trigger module
Acquisition engine
User Logic 2 (Batch Processing)
DRAM FIFO
PCIe

Standard Functionality
- FWDAQ

Firmware Packages
- FWPD
- FWATD
- FWSDR

Design Services
- Many projects completed successfully

Developments – Open FPGA - New Trigger Logic

ADX / DBS / Calibration

User Logic 1
(Streaming Data; FIR filter)

User Logic 0: Trigger

Trigger module

Acquisition engine

User Logic 2
(Batch Processing)

DRAM FIFO

PCIe

NEW
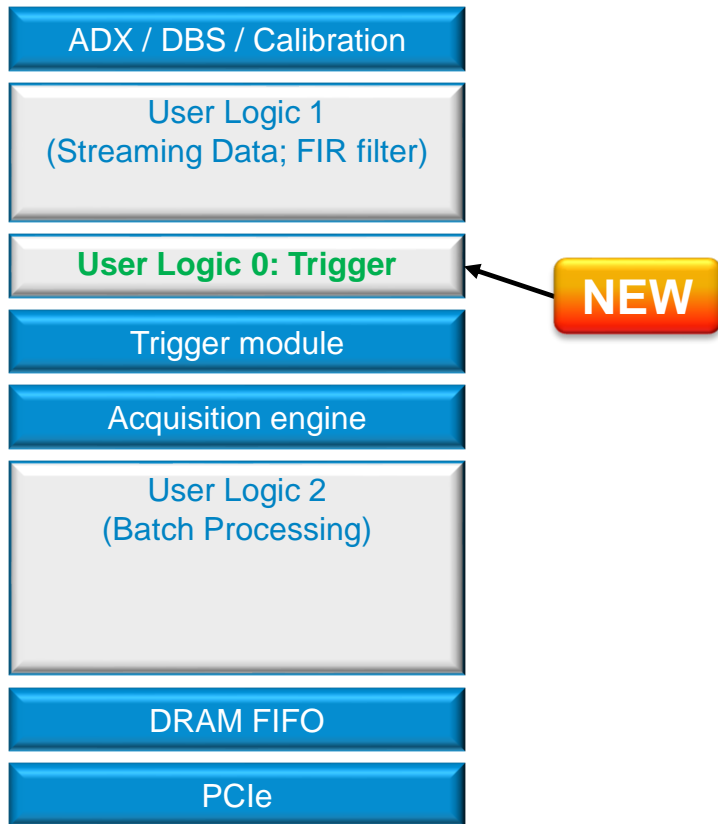
- Trigger Logic
- Intended for advanced conditions
- New applications still to be explored
- i.e. coincidence detection

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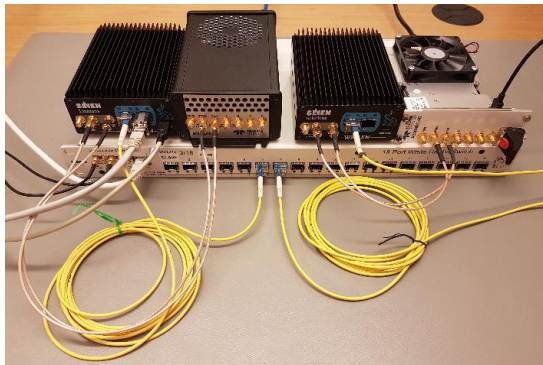# Developments – Support for industry standards

White Rabbit

- Ethernet-based time distribution network with picosecond precision

Supported features (on example of ADQ7)

- Clock reference distribution
- Time stamp distribution
- Software Support for 3rd Party WR devices

EPICS

- Experimental Physics and Industrial Control System – standardized control interface
- Abstracts away device specific protocols
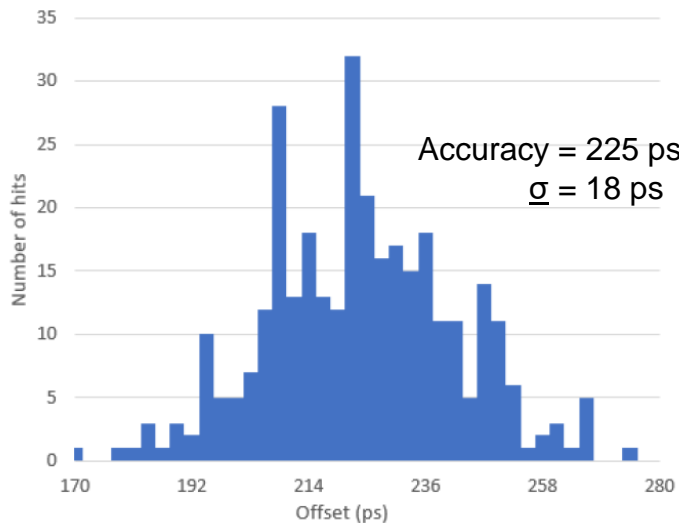- Supports initially EPICS CODAC Installation
- In collaboration with Cosylab

Developments – Support for industry standards

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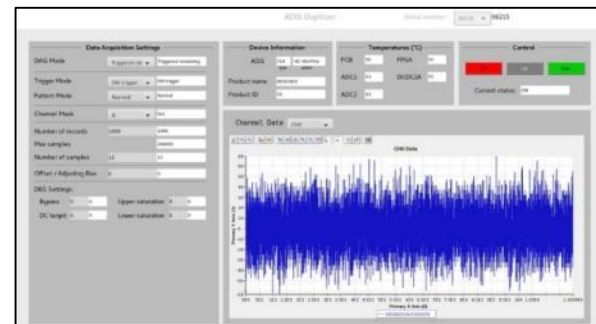Accuracy = 225 ps
$\underline{\sigma}$ = 18 ps
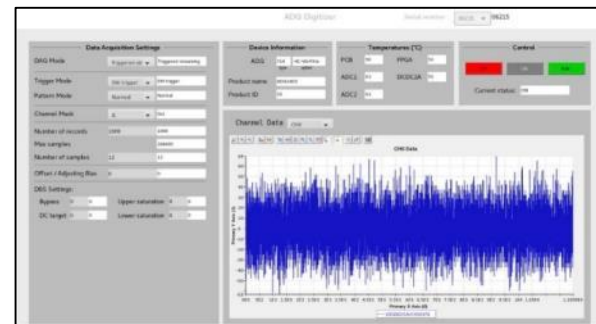
Histogram of offset between digitizers

EPICS

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Developments – Support for Vivado HLS

- Developing algorithm in high level programming language
  - C, C++, SystemC, OpenCL kernel
- Support for Vivado's High Level Synthesis
  - Synthesis to Verilog & VHDL
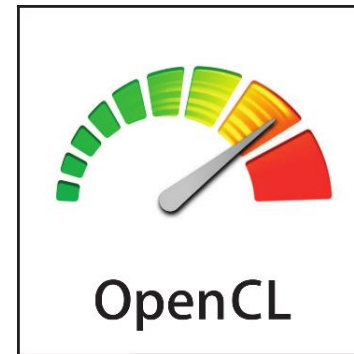
THANK YOU

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TECHNOLOGY LAB
A HELMHOLTZ INNOVATION LAB

DESY.