

# The MicroTCA.4 based LLRF system and other applications at NSRL

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## The introduction of NSRL

## **HLS II** brief introduction

linear segment (8 sections)

- electron energy 0.8GeV
- repetition frequency 1Hz
- working frequency 2856MHz

### storage ring

• perimeter 66.13m

400mA

- frequency 204MHz
- current



a 800 MeV synchrotron light source at the National Synchrotron Radiation Laboratory (NSRL) in university of science and technology,Hefei,China



9th MicroTCA workshop for Industry and Research



## The introduction of NSRL

### **IRFEL brief introduction**

Parameters	Specification
Covering spectrum	2.5 ~ 200 µm
MIR FEL oscillators	2.5 ~ 50 µm
FIR FEL oscillators	40 ~ 200 µm
Macro-pulse length(FW)	5~ 10 µs
Repetition of macro-pulse	20 Hz
Macro-pulse energy	~100 mJ
Micro-pulse length (RMS)	$5 \sim 10 \text{ ps}$
Micro-pulse energy	$1 \sim 50 \ \mu J$
Bandwidth	0.3 ~ 3 %
Continuous tunability	200 ~ 300 %



The linac drives two FEL oscillators to generate mid-infrared and far-infrared free electron lasers. Two accelerating tubes (A1, A2) are used to accelerate the electron beam to the maximum energy of 60 MeV. After the first accelerating tube the beam was extracted into the FIR oscillator, to leave enough space between the two oscillators. And it is under commissioning now.



## Pre-R&D of Hefei Advanced Light Facility (HALF)



2020-12-3

9th MicroTCA workshop for Industry and Research



## MTCA based LLRF

## **MTCA based LLRF application at NSRL**



#### Hardware

- MTCA Architecture
- 1 LLRF system per cavity
- AMC SIS8300L2 IQ demodulate and data process
  - RTM DWC8VM1 down/up conversion

#### Software

- VHDL /Verilog developments
- EPICS developments

used on normal conducting linac(include HLS II and IRFEL)





## MTCA based LLRF

### running status of LLRF



the digital LLRF system upgrade was completed in 2018

1.MicroTCA.4 crate

- 2.power amplifier
- 3.frequency synthesis system
- 4.signal source





## **MTCA** based LLRF

### our schematic of LLRF



- ADC sample signals
- upper computer calculate the amplitude and phase and transmit PI parameters via ethernet
- set flat length, amplitude, phase and delay of the output pulse by feed-forward(FF) table
- FPGA complete rotation and offset compensation
- the IQ data are transmitted to DAC and modulate to 2856MHz

### in-out amplitude predistortion model



g(x) is the predistortion function



use 4-order polyfit fit the input amplitude and output amplitude model the right picture shows the simulation result of linearization(red curve is the desired one,blue curve is the actual curve )

### **FPGA** implementation



1. use cordic algorithm convert IQ to amplitude and phase and then back to IQ

2. use LUT to convert the amplitude

(the LUT is nonlinear to improve the precision)

3. send the converted amplitude to multiplier and generate new IQ data

#### advantages:

make LUT is easy

#### disadvantages:

the phase conversion error and delay depends on the order of cordic the effect of input amplitude on output phase is not considered



### **FPGA** implementation



### result

clock delay=34(0.32us), clock period=105.76MHz, for repetition frequency 20Hz is negligible

the amplitude control have been tested and effects

higher order cordic can improve the conversion precision

### phase control on saturation area:

compute the phase error and rotate the feed-forward table to get the proper angle

$$I = I \_ feedforward * corr \_ I - Q \_ feedward * corr \_ Q$$
$$Q = I \_ feedforward * corr \_ Q + Q \_ feedforward * corr \_ I$$



 $corr_I, corr_Q$  determined by klystron output

JSR



### phase control on saturation area:

- 10 degrees ripples
- pulse to pulse fluctuation over 3 degrees

though the simulation prove the effectiveness, it cannot simulate the fluctuation pulse to pulse, the algorithm need to keep optimizing







## Next plan:

1. establish the input-to-output model of klystron in both amplitude and phase

- 2. find the reason of waveform fluctuation
- 3. continue to optimize phase control algorithm



### **MTCA-based BPM**







#### courtesy by Yu Liang of NSRL



### **MTCA-based Timing System**





mTCA-EVM-300

mTCA-EVR-300U

MTCA-based Event Master(mTCA-EVM-300) and Event Receiver(mTCA-EVR-300U) from MRF, will be tested and estimated for HALF.

courtesy by Prof. Chuan Li of NSRL





1.MicroTCA.4 based LLRF control system completed in 2018.2.LLRF is in operation and continue to optimize.3.designed BPM electronics based on MTCA.4.estimation about timing for HALF will be made.

## Thank you for your attention !