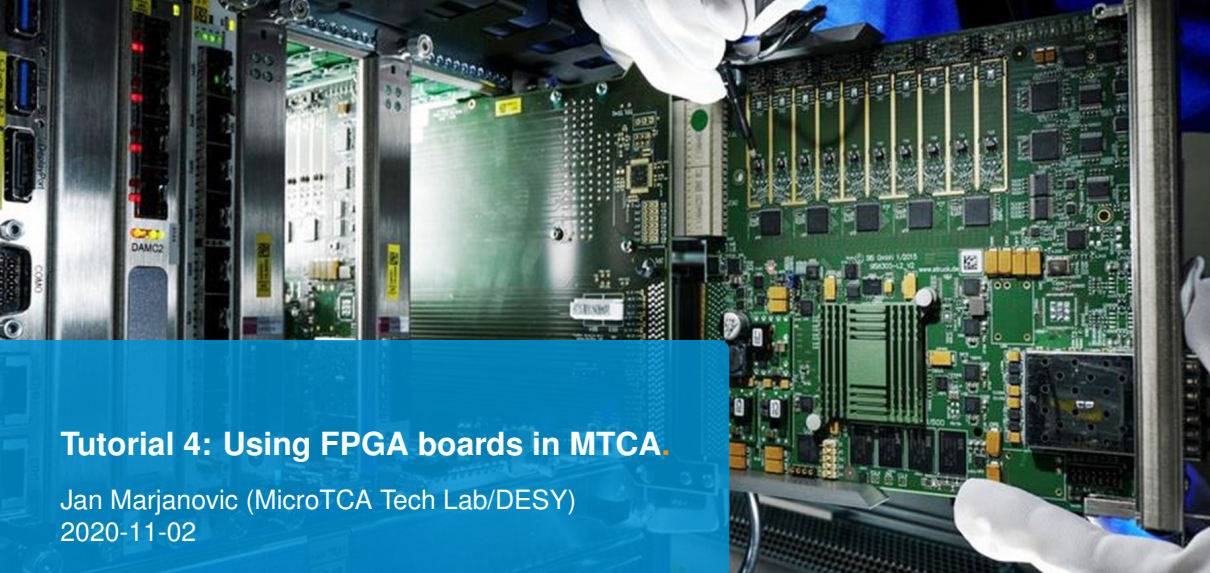




Tutorial 4: Using FPGA boards in MTCA.

Jan Marjanovic (MicroTCA Tech Lab/DESY)
2020-11-02

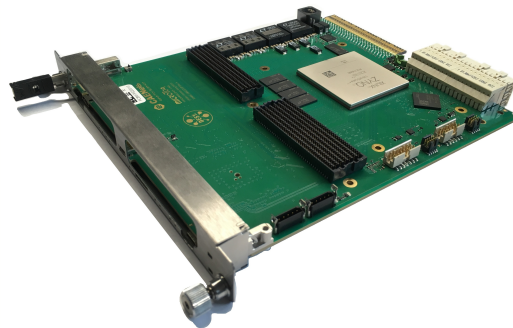
- ▶ Hardware
 - ▶ DAMC-FMC2ZUP - Zynq UltraScale+ MPSoC FMC/FMC+ carrier
 - ▶ DAMC-FMC1Z7IO - Zynq 7000 FMC carrier with GPIO
- ▶ Backplane connections - overview
- ▶ Backplane connections in FPGA
 - ▶ Ethernet
 - ▶ PCI Express
 - ▶ Point-to-point links
 - ▶ MLVDS
 - ▶ Clocking
 - ▶ JTAG
- ▶ Rear Transition Module



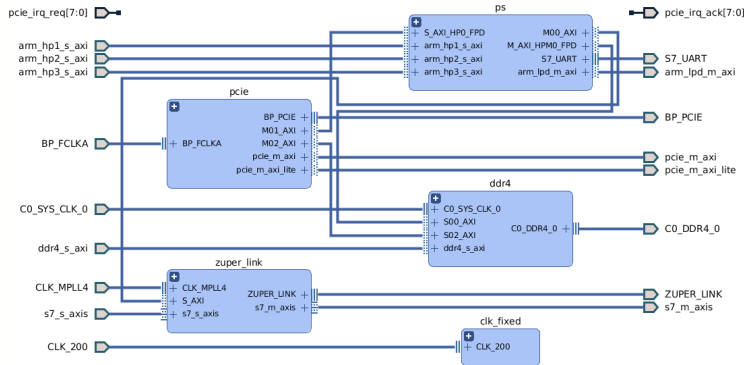
Hardware

- ▶ Advanced Mezzanine Card (AMC.0), compatible with MicroTCA.4
- ▶ Xilinx [Zynq UltraScale+ MPSoC](#) XCZU11EG: 653k logic cells, 2928 DSP
- ▶ 52 transceivers (32 GTH, 16 GTY, 4 GTR)
- ▶ Quad-core ARM® Cortex-A53 and dual-core ARM® Cortex-R5
- ▶ 4GB DDR4 (PS) + 1GB DDR4 (PL)
- ▶ White Rabbit support
- ▶ PCIe Gen3 x4, x8 in supported systems, can be used as a PCIe root complex
- ▶ DisplayPort and USB to front panel
- ▶ Variant with XCZU19EG

https://techlab.desy.de/products/amc/damc_fmc2zup/
<https://www.caenels.com/products/damc-fmc2zup/>

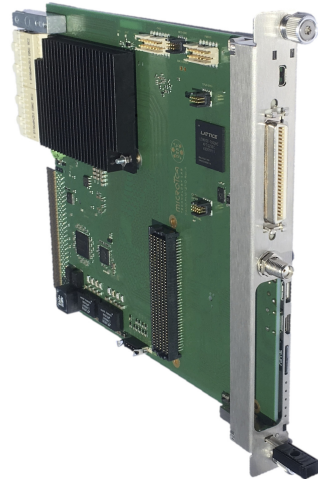


Board Support Package



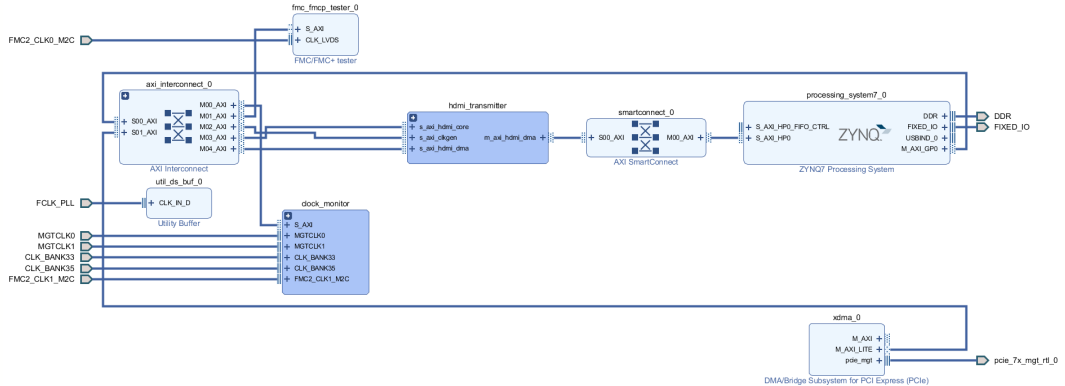
Includes FPGA part (Vivado project) and Yocto Linux.
Contact us for more information/access: mtca-techlab@desy.de

- ▶ Advanced Mezzanine Card, compatible with MicroTCA.4
- ▶ Xilinx Zynq-7000 SoC (XC7Z030, XC7Z035 and XC7Z045)
- ▶ 48 bidirectional IOs: 3.3V and true 5V
- ▶ FMC slot (full LA bank, 2/4 MGTs)
- ▶ PCIe x2 Gen2 (x4 optional)
- ▶ Dual core ARM processor
- ▶ HDMI and USB to front panel
- ▶ Zone 3 Class D1.1



https://techlab.desy.de/products/amc/damc_fmc1z7io/

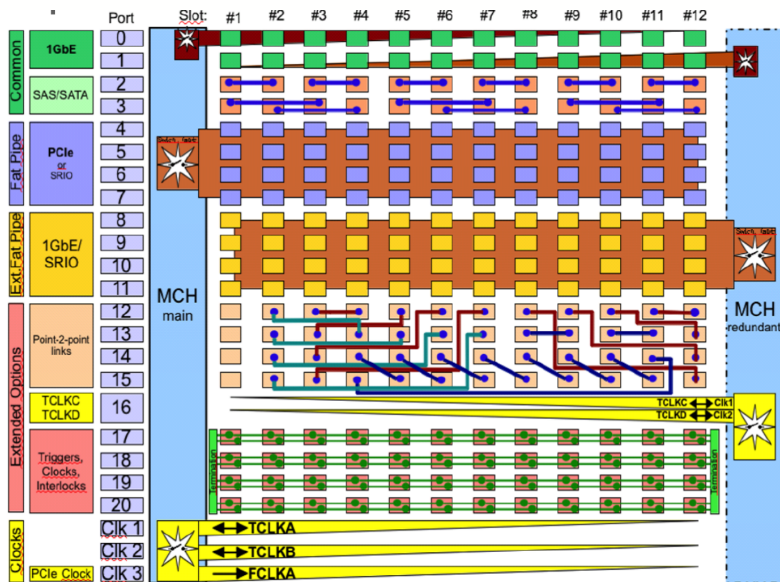
Board Support Package



In development, contact us for early access: mtca-techlab@desy.de

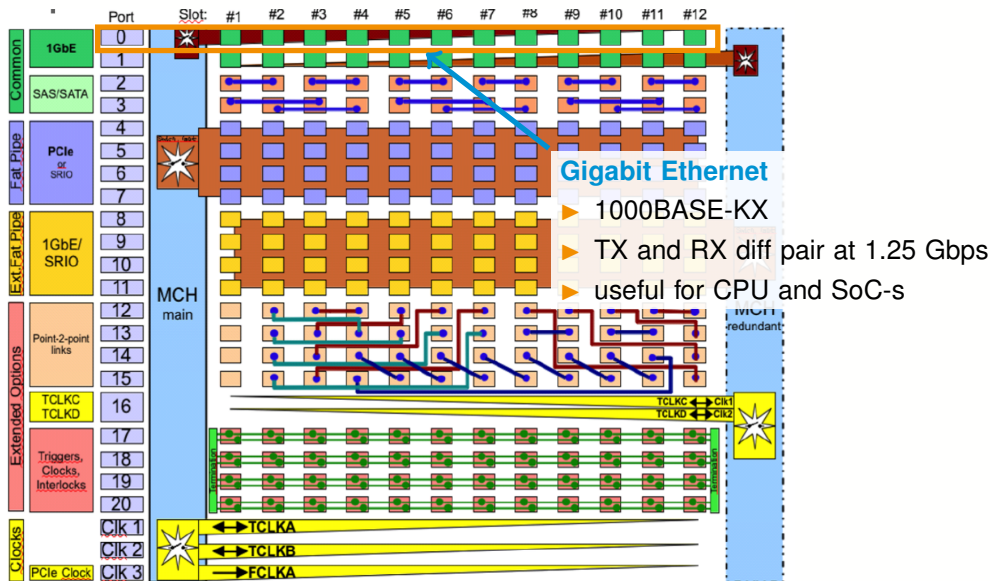
Backplane connections

Backplane connections



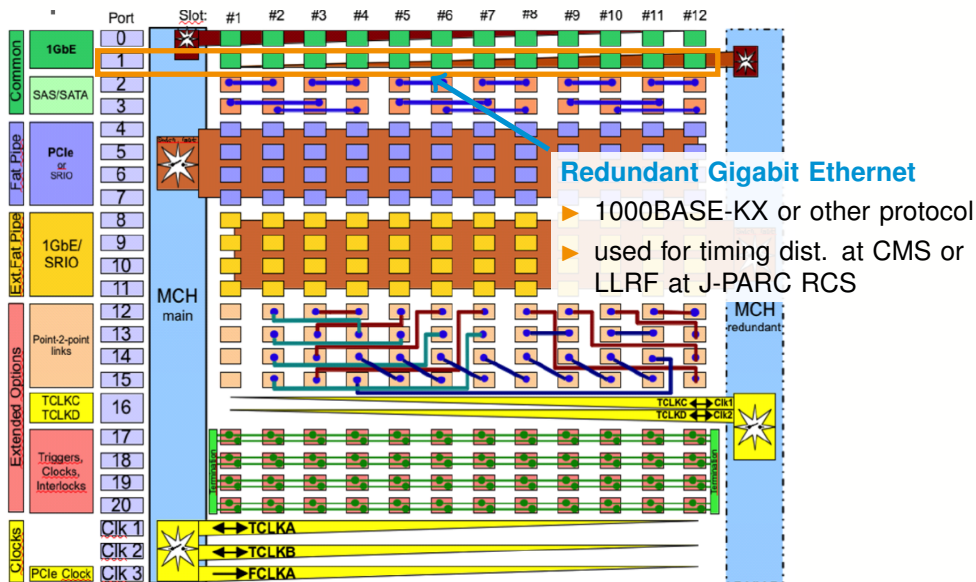
Backplane image from: PICMG® MicroTCA.4
Enhancements for Rear I/O and Timing R1.0

Backplane connections



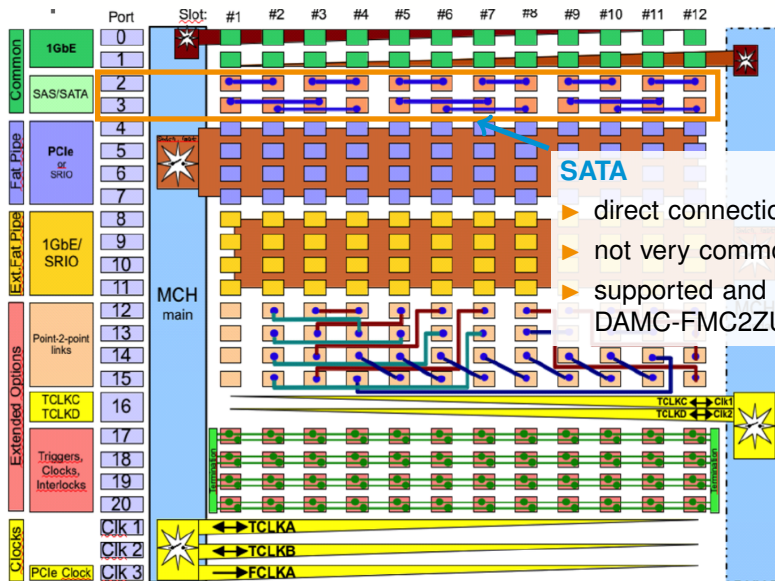
Backplane image from: PICMG® MicroTCA.4
Enhancements for Rear I/O and Timing R1.0

Backplane connections



Backplane image from: PICMG® MicroTCA.4
Enhancements for Rear I/O and Timing R1.0

Backplane connections

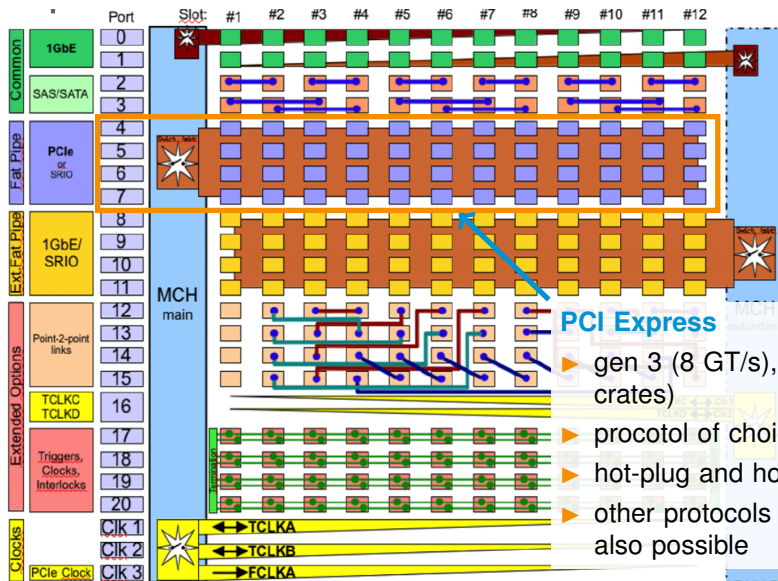


SATA

- ▶ direct connections between slots
- ▶ not very common
- ▶ supported and tested on DAMC-FMC2ZUP (Vivado 2019.1)

Backplane image from: PICMG® MicroTCA.4
Enhancements for Rear I/O and Timing R1.0

Backplane connections

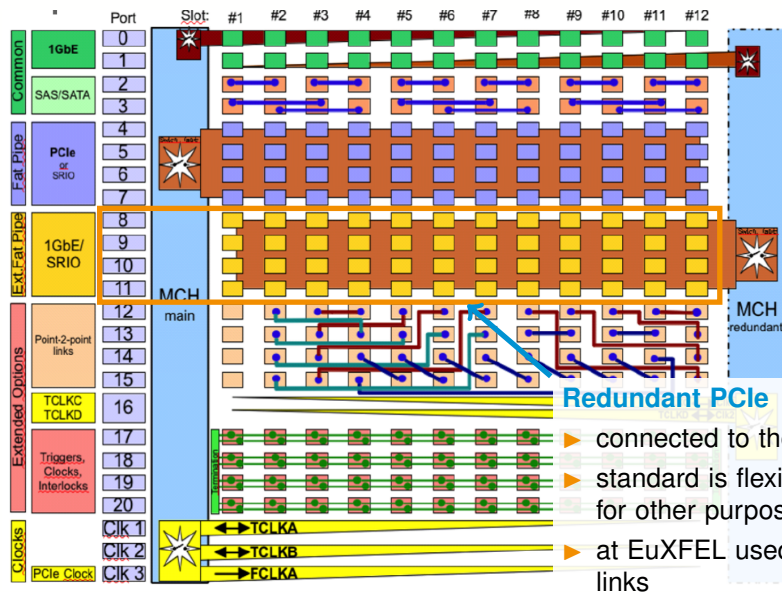


PCI Express

- ▶ gen 3 (8 GT/s), x4 (x8 in special crates)
- ▶ protocol of choice for many apps
- ▶ hot-plug and hot-swap
- ▶ other protocols (40Gb Ethernet) also possible

Backplane image from: PICMG® MicroTCA.4
Enhancements for Rear I/O and Timing R1.0

Backplane connections

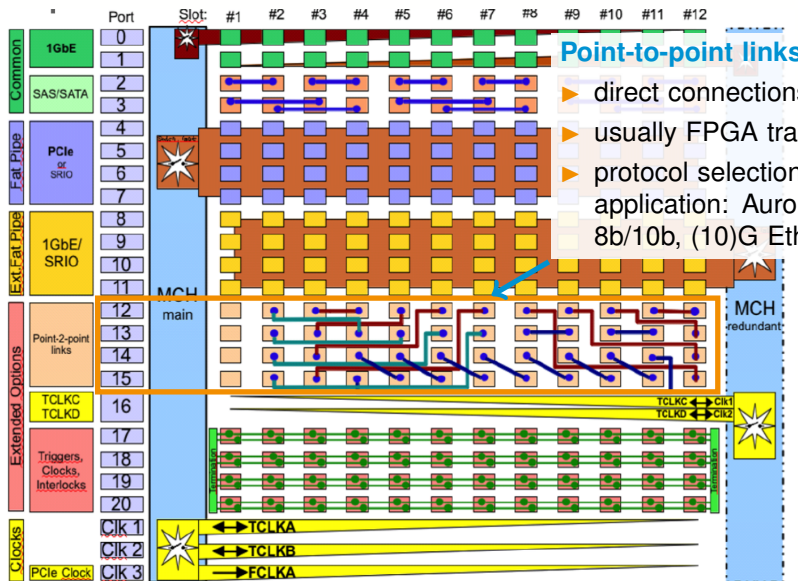


Redundant PCle

- ▶ connected to the 2nd MCH (opt.)
- ▶ standard is flexible, can be used for other purposes
- ▶ at EuXFEL used as additional p2p links

Backplane image from: PICMG® MicroTCA.4
Enhancements for Rear I/O and Timing R1.0

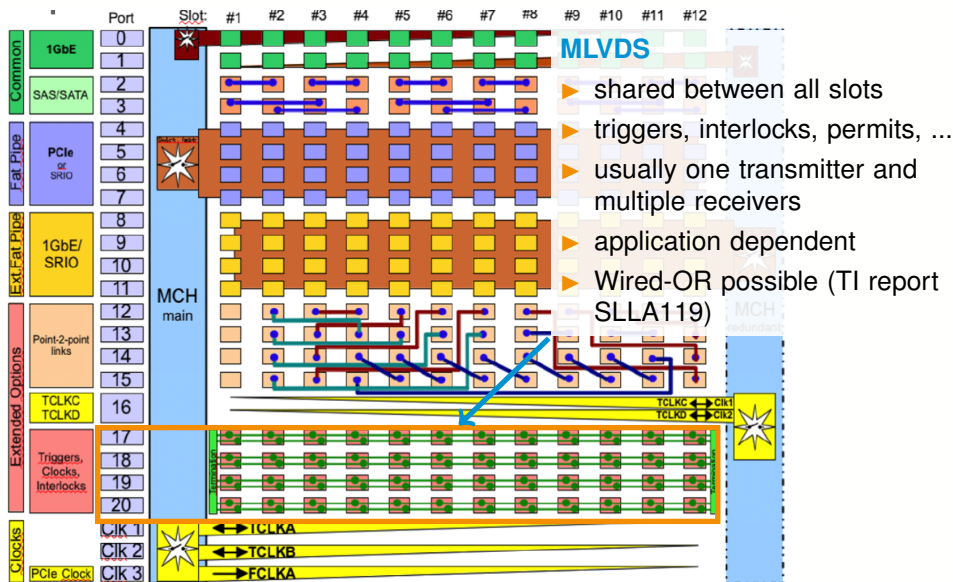
Backplane connections



Point-to-point links

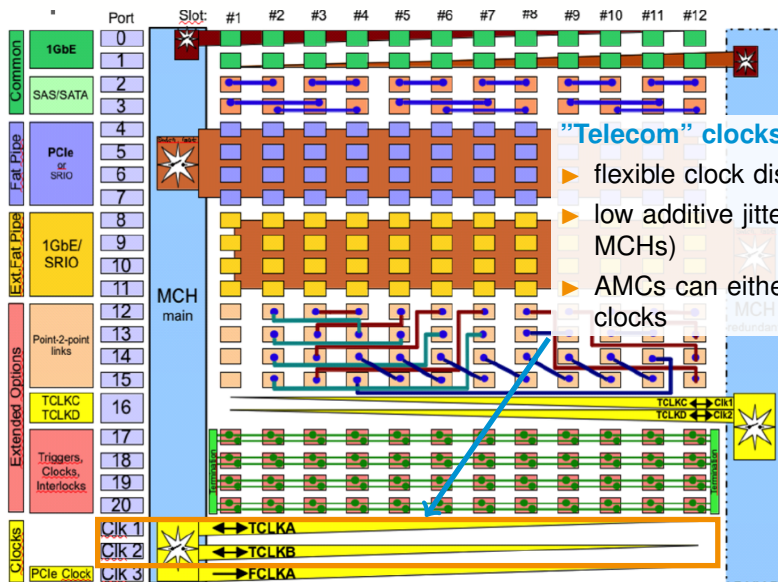
- ▶ direct connections between boards
- ▶ usually FPGA transceivers
- ▶ protocol selection up to the application: Aurora, custom 8b/10b, (10)G Ethernet

Backplane connections



Backplane image from: PICMG® MicroTCA.4
Enhancements for Rear I/O and Timing R1.0

Backplane connections

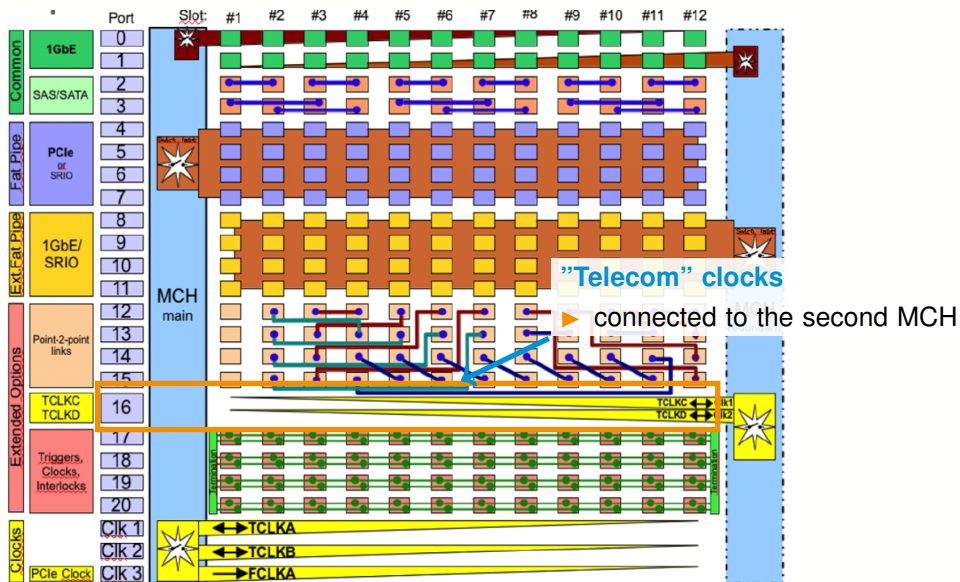


"Telecom" clocks

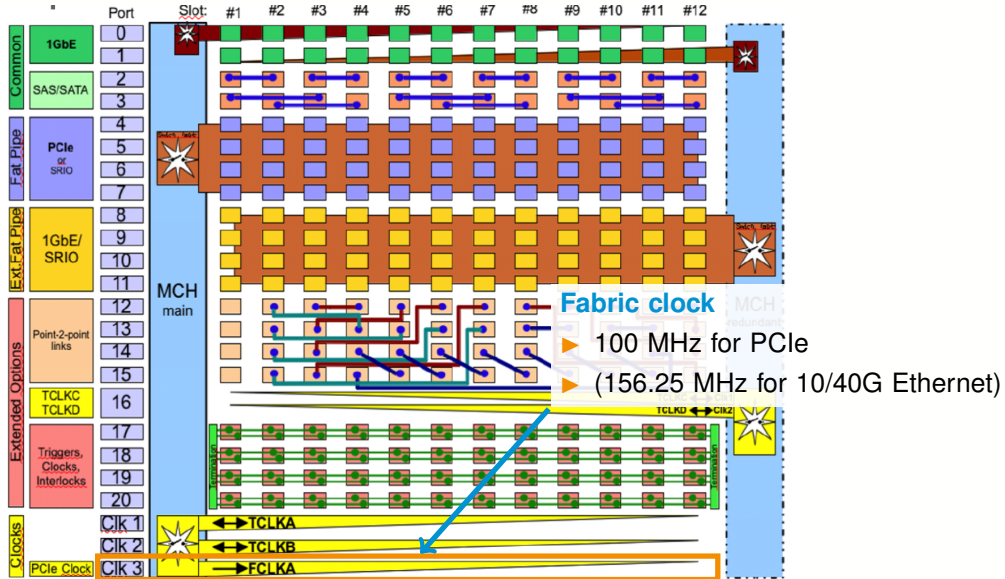
- ▶ flexible clock distribution scheme
- ▶ low additive jitter mux (some MCHs)
- ▶ AMCs can either drive or receive clocks

Backplane image from: PICMG® MicroTCA.4
Enhancements for Rear I/O and Timing R1.0

Backplane connections



Backplane image from: PICMG® MicroTCA.4
Enhancements for Rear I/O and Timing R1.0



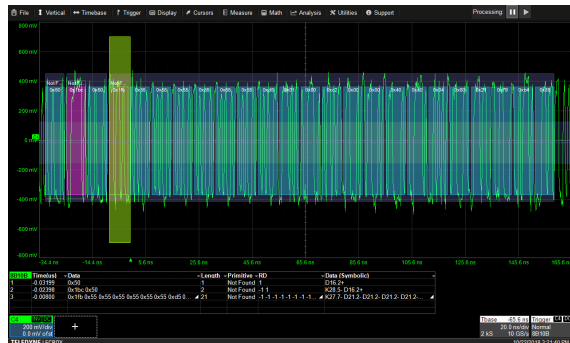
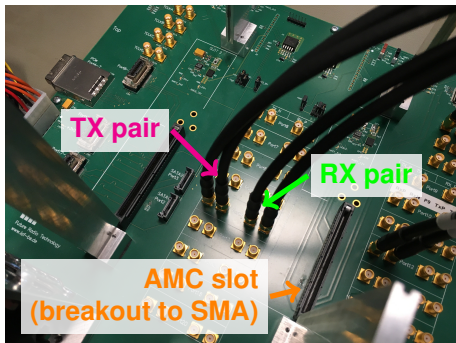
Backplane connections in FPGA

- ▶ Ethernet is well-known protocol, most people familiar with -T (twisted pair) physical medium.
- ▶ In MicroTCA¹ -**KX** "variant" is used on port 0: 1.25 Gbaud, NRZ, 8b/10b encoding, single TX and RX diff pair



By Raysonho @ Open Grid Scheduler / Grid Engine - Own work, CC0,

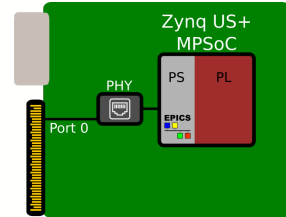
<https://commons.wikimedia.org/w/index.php?curid=39134324>



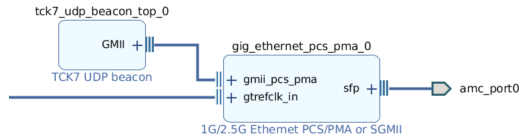
¹as specified in PICMG AMC.2 standard

On our Zynq-based boards Gigabit Ethernet on port 0 is connected to Processing System (ARM)

- ▶ experience of a computer;
developers can SSH into the board
- ▶ control system servers (EPICS/DOOCS/TANGO/...) can be deployed to the board
- ▶ Web interfaces can be provided



Ethernet connection can also be implemented with an FPGA transceiver; see our example on DAMC-TCK7 (<https://github.com/MicroTCA-Tech-Lab/damc-tck7-fpga-bsp>)



```
➔ ~ sudo tcpdump -n udp dst port 12345 -v -X
tcpdump: listening on eno1, link-type EN10MB (Ethernet), capture size 262144
11:28:40.724347 IP (tos 0x0, ttl 64, id 49655, offset 0, flags [DF], proto U
192.168.1.234.32929 > 255.255.255.255.12345: UDP, length 139
0x0000:  4500 00a7 c1f7 4000 4011 b5bc c0a8 01ea  E....@.....
0x0010:  ffff ffff 80a1 3039 0093 4015 4d6f 696e  ....09...Moin
0x0020:  2120 4865 6c6c 6f20 6672 6f6d 2044 414d  !.Hello.from.DAM
0x0030:  432d 5443 4b37 2c20 7468 6973 2069 7320  C-TCK7,.this.is.
0x0040:  5544 5020 6272 6f61 6463 6173 7420 6265  UDP.broadcast.be
0x0050:  6163 6f6e 2072 756e 6e69 6e67 2069 6e20  acon.running.in.
0x0060:  4650 4741 2061 6e64 2074 7261 6e73 6d69  FPGA.and.transmi
0x0070:  7474 696e 6720 5544 5020 7061 636b 6167  tting.UDP.packag
0x0080:  6573 206f 7665 7220 4769 6761 6269 7420  es.over.Gigabit.
0x0090:  4574 6865 7265 6e65 7420 6f66 2041 4d43  Ethernet.of.AMC
0x00a0:  2070 6f72 7420 30
^C
1 packet captured
1 packet received by filter
0 packets dropped by kernel
➔ ~
```

PCI Express is high-speed protocol for PC extension cards.
Different form-factors are also available → e.g. AMC

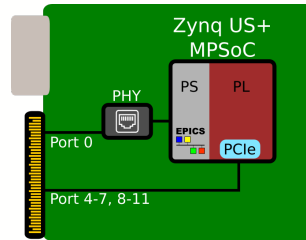
MicroTCA backplane connections as specified by **MicroTCA.4** standard:

REQ 6-7 Port 4 to 7 **should** be used for PCIe.

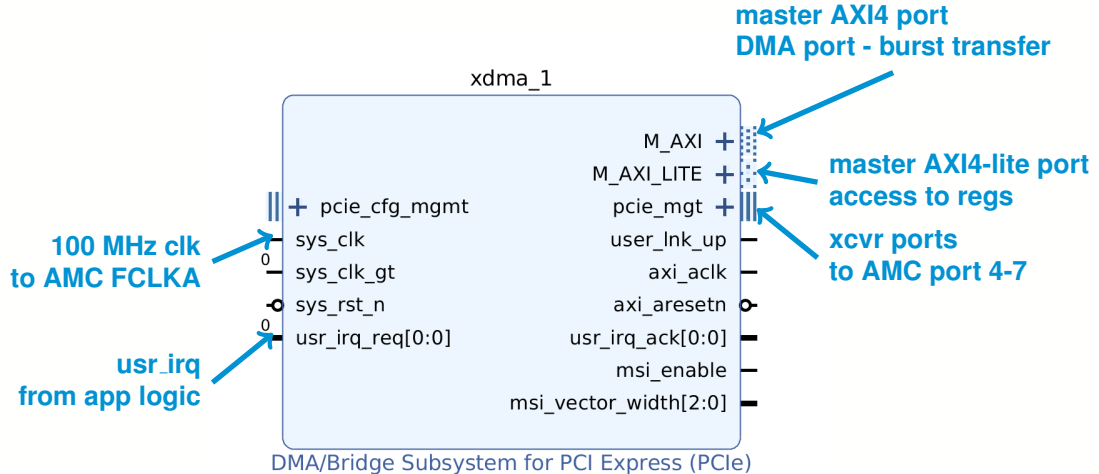
from PICMG® Specification MTCA.4 Revision 1.0: MicroTCA Enhancements for Rear I/O and Precision Timing

- ▶ serial protocol (differential pairs), point-to-point
- ▶ packet-based protocol
- ▶ tree structure, switches, addressing
- ▶ discovery (enumeration) mechanism
- ▶ gen 3 (8 GT/s),
x4 or x8 (special backplane)
- ▶ Hot Plug and Hot Swap
(speeds up the development!)

	AMC3	
	4..11	
	x8	
	8 GT/s	



One way to implement PCIe endpoint (or root complex) is to use Xilinx xdma (Xilinx DMA Subsystem for PCI Express):



Driver for `xdma` available on: https://github.com/Xilinx/dma_ip_drivers/tree/master/XDMA/

Xilinx DMA driver provides several char devices:

```
$ ll /dev | grep xdma
drwxr-xr-x  3 root root          60 Jun 20 17:19 xdma
crw-rw-rw-  1 root root    238,  36 Jun 20 17:19 xdma0_c2h_0
crw-rw-rw-  1 root root    238,  1 Jun 20 17:19 xdma0_control
crw-rw-rw-  1 root root    238, 10 Jun 20 17:19 xdma0_events_0
crw-rw-rw-  1 root root    238, 11 Jun 20 17:19 xdma0_events_1
[...]
crw-rw-rw-  1 root root    238, 24 Jun 20 17:19 xdma0_events_14
crw-rw-rw-  1 root root    238, 25 Jun 20 17:19 xdma0_events_15
crw-rw-rw-  1 root root    238, 32 Jun 20 17:19 xdma0_h2c_0
crw-rw-rw-  1 root root    238,  0 Jun 20 17:19 xdma0_user
crw-rw-rw-  1 root root    238,  2 Jun 20 17:19 xdma0_xvc
```

c2h

AXI4 port (DMA from device)

AXI4 port (DMA to device)

h2c

user

AXI4-Lite port

**events_N
interrupts**

MTCAWS 2019 - longer presentation about PCIe:

<https://github.com/MicroTCA-Tech-Lab/damc-tck7-fpga-bsp/tree/demo-mtcaws2019/docs/demo>

- ▶ Direct connections between (adjacent) slots
- ▶ Protocol selection application-specific:
 - ▶ Aurora 8b/10b or Aurora 64b/66b
 - ▶ custom protocol (common clock or clock drift compensation)
 - ▶ Ethernet or 10 Gigabit Ethernet
 - ▶ other
- ▶ Data aggregation (FOFB, MPS, LLRF, ...); central slots on some backplanes (e.g. Schroff)

Aurora 64b/66b at 10 Gbps - 250 ns (clock comp visible)



Latency test setup



Custom 64b/66b at 10 Gbps - 68 ns



- ▶ Shared between slots, term. on backplane
- ▶ Implemented with an MLVDS transceiver
- ▶ Interface to FPGA: (TX, RX, TXEN) * 8, "normal" LVCMOS
- ▶ Our boards have MLVDS **Type-2** receivers
- ▶ Wired-OR: TX to '1', drive TXEN²
- ▶ Ideally: make the lane selection SW-configurable in firmware

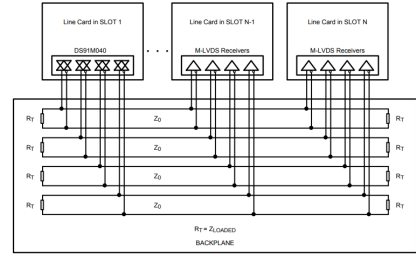


figure from: DS91M040 Datasheet

Use cases:

- ▶ Interlocks, permits
- ▶ Triggers, synchronization
- ▶ Data broadcast → consider source-synchronous data transfer

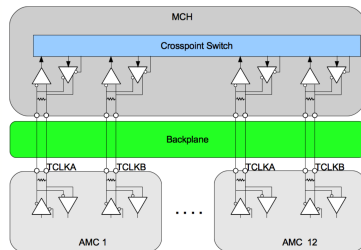
An example from EuXFEL - x2timer distributes **data** and **data-clock** on port 17 TX and port 17 RX respectively

Backplane Clocks & Triggers					enable Port:
BACK.TRG1	D-Clock 108MHz	☒	17 R		
BACK.TRG2	Data 108MHz	☒	17 T		
BACK.TRG3	Trigger 59	☒	17.13ms	18 R	
			LLRF Trig		

²no driver should actively drive '0'

MicroTCA (and also FMC carriers) provide several clocks

- ▶ on-board oscillators
- ▶ Fabric clock (FCLKA)
- ▶ TCLKA, TCLKB, TCLKC, TCLKD
- ▶ FMC clocks (M2C, C2M)
- ▶ front-panel input
- ▶ RTM clocks



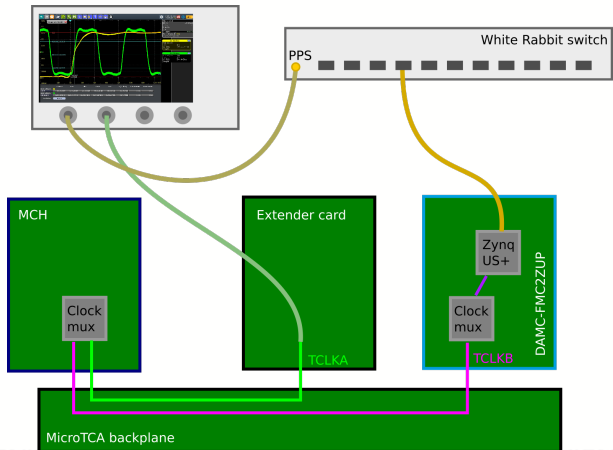
from: MicroTCA.4 Enhancements for Rear I/O and Timing R1.0

Solution (on DAMC-FMC2ZUP):
16-port, low-jitter cross-point switch

```
@enum.unique
class ZupPortName(enum.IntEnum):
    FMC1_CLK3_BIDIR = 0
    FMC1_CLK2_BIDIR = 1
    CPS_GC2 = 2
    CPS2MPLL = 3
    CPS_GC1 = 4
    Z3_AMC_TCLK = 5
    Z3_AMC_CLK1 = 6
    Z3_RTM_CLK1 = 7
    TCLKA = 8
    TCLKB = 9
    <...>
```

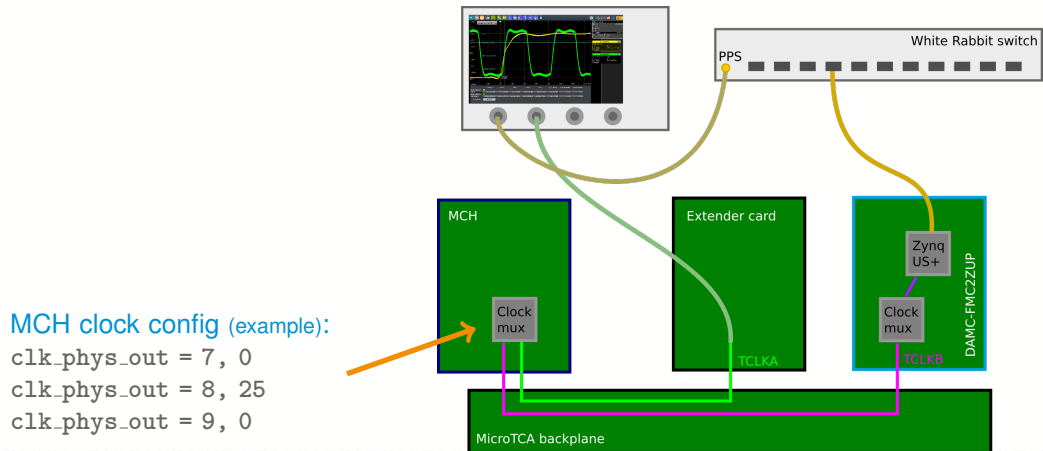
Clocking - example

Example: distributing the clock from DAMC-FMC2ZUP to other boards in the crate

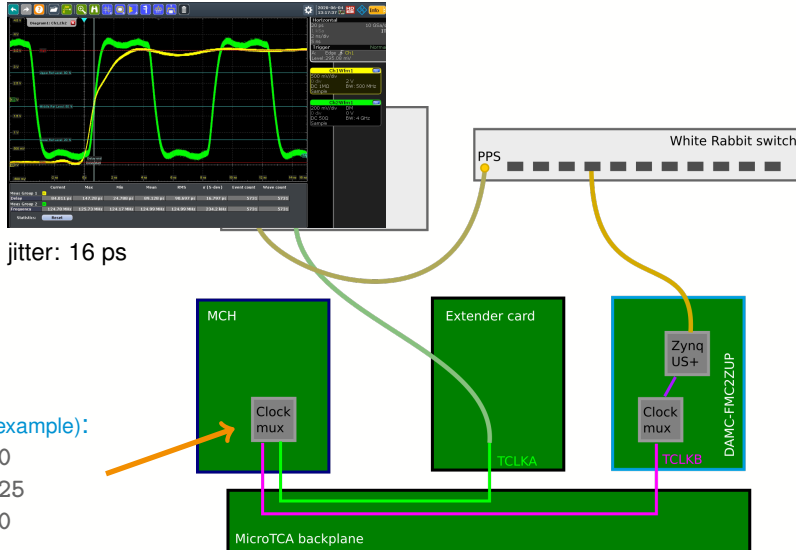


Clocking - example

Example: distributing the clock from DAMC-FMC2ZUP to other boards in the crate



Example: distributing the clock from DAMC-FMC2ZUP to other boards in the crate



MCH clock config (example):

```
clk_phys_out = 7, 0  
clk_phys_out = 8, 25  
clk_phys_out = 9, 0
```

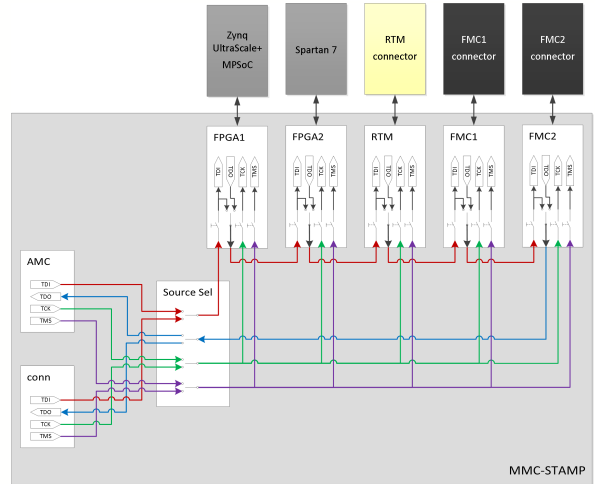
DAMC-FMC2ZUP and DAMC-FMC1Z7IO have a flexible **JTAG architecture**.

JTAG "clients":

- ▶ FPGA1: Zynq US+ (FPGA and ARM)
- ▶ FPGA2: Spartan 7
- ▶ RTM
- ▶ FMC1 and FMC2

JTAG "sources":

- ▶ on-board connector (Xilinx 14 pin)
- ▶ AMC connector (backplane)



More info:

https://techlab.desy.de/products/module_management_controller/mmc_stamp/

JTAG Switching Module - JSM



```
DAMC-FMC2ZUP@0x82 MMC>
DAMC-FMC2ZUP@0x82 MMC>sj bp fpga12
EEPROM value = 0x23
source: bp, dest: fpga12
DAMC-FMC2ZUP@0x82 MMC>v
Firmware version : V0.07-1-4a3b8841
Build date       : 2020-11-26T10:24:59Z
Build host       : ac84b46258fc
Compiler version : 9.3.1 20200408 (release
IPMI version     : 1.5
Vendor ID:       : 0x053F
Product ID:      : 0x200B
Board:           : DAMC-FMC2ZUP
Debug Level:     : 3
```

NAT-MCH by N.A.T.

JTAG Switch Module Configuration

Setup

Base Configuration

Switch: BASC 104 v

Age Time

Port 0x0ff

Port VLAN

802.1Q VLAN

802.1X

802.1P

Port Mirroring

Junco Frame

Link Aggregation

RSTP

Serial SGMII

Link Status

1GBE counters

Switch PCE 180

PCE Virtual

Bethlens

Error Counters

Link Status

Maintenance

Board Management

Board Information

System Information

Release NAT-MCH

Update BCH

Change Password

N.A.T. Webpage

Home

Active

JTAG Device Settings is not available, because Xilinx Virtual Cable operation is running.

Xilinx Virtual Cable

Xilinx Virtual Cable Server

enabled

Base TCP Port

2542

Maximal User Defined JTAG Frequency

2.0000

JTAG Device	TCP Port	JTAG Device	TCP Port
AMC1	2542	AMC7	2548
AMC2	2543	AMC8	2549
AMC3	2544	AMC9	2550(connected)
AMC4	2545	AMC10	2551
AMC5	2546	AMC11	2552
AMC6	2547	AMC12	2553

Apply

Discard

Reset Configuration

[illegible]


```
DAMC-FMC2ZUP@0x82 MMC>
DAMC-FMC2ZUP@0x82 MMC>sj bp fpga12
EEPROM value = 0x23
source: bp, dest: fpga12
DAMC-FMC2ZUP@0x82 MMC>v
Firmware version : V0.07-1-4a3b8841
Build date       : 2020-11-26T10:24:59Z
Build host       : ac84b46258fc
Compiler version : 9.3.1 20200408 (release
IPMI version     : 1.5
Vendor ID:       : 0x053F
Product ID:      : 0x200B
Board:           : DAMC-FMC2ZUP
Debug Level:     : 3
```

NAT-MCH by N.A.T.

Setup

Base Configuration

Switch: BASIC10GE

Age Time

Port on/off

Port VLAN

802.1Q VLAN

802.1X

802.3p

Port Mirroring

Jumbo Frame

Link Aggregation

RSTP

Serial/Gigabit

Link Status

10GE counters

Switch Ports 480

PoE Virtual

Switches

Error Counters

Link Status

Maintenance

Single Management

Board Information

System Information

Recover NAT-MCH

Update MCH

Change Password

N.A.T. Webpage

Home

JTAG Switch Module Configuration

Active JTAG Device Settings is not available, because Xilinx Virtual Cable operating is running.

Xilinx Virtual Cable

Xilinx Virtual Cable Server

enabled

Base TCP Port

2542

Maximum User Defined JTAG Frequency

2.00MHz

JTAG Device	TCP Port	JTAG Device	TCP Port
AMC1	2542	AMC7	2548
AMC2	2543	AMC8	2549
AMC3	2544	AMC9	2550 (occupied)
AMC4	2545	AMC10	2551
AMC5	2546	AMC11	2552
AMC6	2547	AMC12	2553

Apply

Discard

Reset Configuration

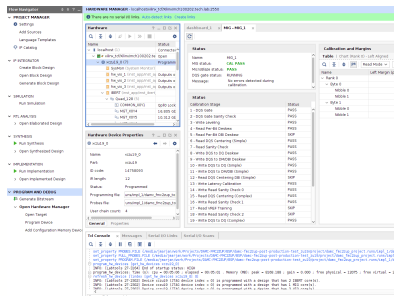
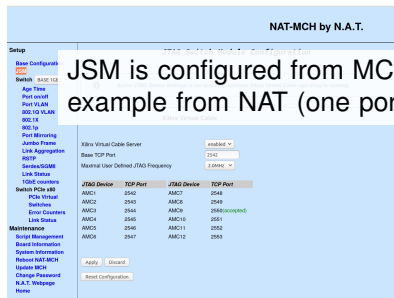
The screenshot displays the Xilinx IDE interface with three main windows open:

- Project Manager:** Shows the project hierarchy for 'myproj'. The 'Sources' tab is active, listing files like 'myproj.srcs/sources_1/bd/bd_1.ooc' and 'myproj.srcs/sources_1/bd/bd_1.ooc'. The 'Properties' tab is also visible, showing details for the 'myproj.srcs/sources_1/bd/bd_1.ooc' file, including its location and size.
- Properties:** Displays the properties of the selected file, including its location and size.
- Messages:** Shows the compilation messages for the project. It includes a warning about the 'myproj.srcs/sources_1/bd/bd_1.ooc' file and a message about the 'myproj.srcs/sources_1/bd/bd_1.ooc' file.

JTAG Switching Module - JSM



```
DAMC-FMC2ZUP@0x82 MMC>
DAMC-FMC2ZUP@0x82 MMC>sj bp fpga12
EEPROM value = 0x23
source: bp, dest: fpga12
DAMC-FMC2ZUP@0x82 MMC>v
Firmware version : V0.07-1-4a3b8841
Build date       : 2020-11-26T10:24:59Z
Build host       : ac84b46258fc
Compiler version : 9.3.1 20200408 (release
IPMI version     : 1.5
Vendor ID:       : 0x053F
Product ID:      : 0x200B
Board:           : DAMC-FMC2ZUP
Debug Level:     : 3
```



JTAG Switching Module - JSM

Tutorial 4: Using FPGA boards in MTCA
J. Marjanovic, 2020-11-02, Page 21/25



```
DAMC-FMC2ZUP@0x82 MMC>
DAMC-FMC2ZUP@0x82 MMC>sj bp fpga12
EEPROM value = 0x23
source: bp, dest: fpga12
DAMC-FMC2ZUP@0x82 MMC>v
Firmware version : V0.07-1-4a3b8841
Build date       : 2020-11-26T10:24:59Z
Build host       : ac84b46258fc
```

MMC is configured (either over 200408 (release
console or over IPMI)

```
Product ID: : 0x200B
Board: : DAMC-FMC2ZUP
Debug Level: : 3
```

NAT-MCH by N.A.T.

JTAG Switch Module Configuration

Active JTAG Device Settings is not available, because Xilinx Virtual Cable operating is running.

Xilinx Virtual Cable

Xilinx Virtual Cable Server:

Basic TCP Port:

Maximal User Defined JTAG Frequency:

JTAG Device	TCP Port	JTAG Device	TCP Port
AMC1	2540	AMC7	2548
AMC2	2543	AMC8	2549
AMC3	2544	AMC9	2550 (occupied)
AMC4	2545	AMC10	2551
AMC5	2546	AMC11	2552
AMC6	2547	AMC12	2553

Buttons: Apply, Discard, Reset Configuration

Hardware Manager

Hardware: Architecture:

Hardware Status Properties:

Name	Value	Status
0 - JTAG Core	OK	OK
1 - JTAG Core	OK	OK
2 - JTAG Core	OK	OK
3 - JTAG Core	OK	OK
4 - JTAG Core	OK	OK
5 - JTAG Core	OK	OK
6 - JTAG Core	OK	OK
7 - JTAG Core	OK	OK
8 - JTAG Core	OK	OK
9 - JTAG Core	OK	OK
10 - JTAG Core	OK	OK
11 - JTAG Core	OK	OK
12 - JTAG Core	OK	OK
13 - JTAG Core	OK	OK
14 - JTAG Core	OK	OK
15 - JTAG Core	OK	OK
16 - JTAG Core	OK	OK
17 - JTAG Core	OK	OK
18 - JTAG Core	OK	OK
19 - JTAG Core	OK	OK
20 - JTAG Core	OK	OK
21 - JTAG Core	OK	OK
22 - JTAG Core	OK	OK
23 - JTAG Core	OK	OK
24 - JTAG Core	OK	OK
25 - JTAG Core	OK	OK
26 - JTAG Core	OK	OK
27 - JTAG Core	OK	OK
28 - JTAG Core	OK	OK
29 - JTAG Core	OK	OK
30 - JTAG Core	OK	OK
31 - JTAG Core	OK	OK

Calibration and Charges

Table	Start	End	Left	Right
Table 1	0x00000000	0x00000000	0x00000000	0x00000000
Table 2	0x00000000	0x00000000	0x00000000	0x00000000
Table 3	0x00000000	0x00000000	0x00000000	0x00000000
Table 4	0x00000000	0x00000000	0x00000000	0x00000000
Table 5	0x00000000	0x00000000	0x00000000	0x00000000
Table 6	0x00000000	0x00000000	0x00000000	0x00000000
Table 7	0x00000000	0x00000000	0x00000000	0x00000000
Table 8	0x00000000	0x00000000	0x00000000	0x00000000
Table 9	0x00000000	0x00000000	0x00000000	0x00000000
Table 10	0x00000000	0x00000000	0x00000000	0x00000000
Table 11	0x00000000	0x00000000	0x00000000	0x00000000
Table 12	0x00000000	0x00000000	0x00000000	0x00000000
Table 13	0x00000000	0x00000000	0x00000000	0x00000000
Table 14	0x00000000	0x00000000	0x00000000	0x00000000
Table 15	0x00000000	0x00000000	0x00000000	0x00000000
Table 16	0x00000000	0x00000000	0x00000000	0x00000000
Table 17	0x00000000	0x00000000	0x00000000	0x00000000
Table 18	0x00000000	0x00000000	0x00000000	0x00000000
Table 19	0x00000000	0x00000000	0x00000000	0x00000000
Table 20	0x00000000	0x00000000	0x00000000	0x00000000
Table 21	0x00000000	0x00000000	0x00000000	0x00000000
Table 22	0x00000000	0x00000000	0x00000000	0x00000000
Table 23	0x00000000	0x00000000	0x00000000	0x00000000
Table 24	0x00000000	0x00000000	0x00000000	0x00000000
Table 25	0x00000000	0x00000000	0x00000000	0x00000000
Table 26	0x00000000	0x00000000	0x00000000	0x00000000
Table 27	0x00000000	0x00000000	0x00000000	0x00000000
Table 28	0x00000000	0x00000000	0x00000000	0x00000000
Table 29	0x00000000	0x00000000	0x00000000	0x00000000
Table 30	0x00000000	0x00000000	0x00000000	0x00000000
Table 31	0x00000000	0x00000000	0x00000000	0x00000000
Table 32	0x00000000	0x00000000	0x00000000	0x00000000
Table 33	0x00000000	0x00000000	0x00000000	0x00000000
Table 34	0x00000000	0x00000000	0x00000000	0x00000000
Table 35	0x00000000	0x00000000	0x00000000	0x00000000
Table 36	0x00000000	0x00000000	0x00000000	0x00000000
Table 37	0x00000000	0x00000000	0x00000000	0x00000000
Table 38	0x00000000	0x00000000	0x00000000	0x00000000
Table 39	0x00000000	0x00000000	0x00000000	0x00000000
Table 40	0x00000000	0x00000000	0x00000000	0x00000000
Table 41	0x00000000	0x00000000	0x00000000	0x00000000
Table 42	0x00000000	0x00000000	0x00000000	0x00000000
Table 43	0x00000000	0x00000000	0x00000000	0x00000000
Table 44	0x00000000	0x00000000	0x00000000	0x00000000
Table 45	0x00000000	0x00000000	0x00000000	0x00000000
Table 46	0x00000000	0x00000000	0x00000000	0x00000000
Table 47	0x00000000	0x00000000	0x00000000	0x00000000
Table 48	0x00000000	0x00000000	0x00000000	0x00000000
Table 49	0x00000000	0x00000000	0x00000000	0x00000000
Table 50	0x00000000	0x00000000	0x00000000	0x00000000
Table 51	0x00000000	0x00000000	0x00000000	0x00000000
Table 52	0x00000000	0x00000000	0x00000000	0x00000000
Table 53	0x00000000	0x00000000	0x00000000	0x00000000
Table 54	0x00000000	0x00000000	0x00000000	0x00000000
Table 55	0x00000000	0x00000000	0x00000000	0x00000000
Table 56	0x00000000	0x00000000	0x00000000	0x00000000
Table 57	0x00000000	0x00000000	0x00000000	0x00000000
Table 58	0x00000000	0x00000000	0x00000000	0x00000000
Table 59	0x00000000	0x00000000	0x00000000	0x00000000
Table 60	0x00000000	0x00000000	0x00000000	0x00000000
Table 61	0x00000000	0x00000000	0x00000000	0x00000000
Table 62	0x00000000	0x00000000	0x00000000	0x00000000
Table 63	0x00000000	0x00000000	0x00000000	0x00000000
Table 64	0x00000000	0x00000000	0x00000000	0x00000000
Table 65	0x00000000	0x00000000	0x00000000	0x00000000
Table 66	0x00000000	0x00000000	0x00000000	0x00000000
Table 67	0x00000000	0x00000000	0x00000000	0x00000000
Table 68	0x00000000	0x00000000	0x00000000	0x00000000
Table 69	0x00000000	0x00000000	0x00000000	0x00000000
Table 70	0x00000000	0x00000000	0x00000000	0x00000000
Table 71	0x00000000	0x00000000	0x00000000	0x00000000
Table 72	0x00000000	0x00000000	0x00000000	0x00000000
Table 73	0x00000000	0x00000000	0x00000000	0x00000000
Table 74	0x00000000	0x00000000	0x00000000	0x00000000
Table 75	0x00000000	0x00000000	0x00000000	0x00000000
Table 76	0x00000000	0x00000000	0x00000000	0x00000000
Table 77	0x00000000	0x00000000	0x00000000	0x00000000
Table 78	0x00000000	0x00000000	0x00000000	0x00000000
Table 79	0x00000000	0x00000000	0x00000000	0x00000000
Table 80	0x00000000	0x00000000	0x00000000	0x00000000
Table 81	0x00000000	0x00000000	0x00000000	0x00000000
Table 82	0x00000000	0x00000000	0x00000000	0x00000000
Table 83	0x00000000	0x00000000	0x00000000	0x00000000
Table 84	0x00000000	0x00000000	0x00000000	0x00000000
Table 85	0x00000000	0x00000000	0x00000000	0x00000000
Table 86	0x00000000	0x00000000	0x00000000	0x00000000
Table 87	0x00000000	0x00000000	0x00000000	0x00000000
Table 88	0x00000000	0x00000000	0x00000000	0x00000000
Table 89	0x00000000	0x00000000	0x00000000	0x00000000
Table 90	0x00000000	0x00000000	0x00000000	0x00000000
Table 91	0x00000000	0x00000000	0x00000000	0x00000000
Table 92	0x00000000	0x00000000	0x00000000	0x00000000
Table 93	0x00000000	0x00000000	0x00000000	0x00000000
Table 94	0x00000000	0x00000000	0x00000000	0x00000000
Table 95	0x00000000	0x00000000	0x00000000	0x00000000
Table 96	0x00000000	0x00000000	0x00000000	0x00000000
Table 97	0x00000000	0x00000000	0x00000000	0x00000000
Table 98	0x00000000	0x00000000	0x00000000	0x00000000
Table 99	0x00000000	0x00000000	0x00000000	0x00000000
Table 100	0x00000000	0x00000000	0x00000000	0x00000000

JTAG Switching Module - JSM

Tutorial 4: Using FPGA boards in MTCA
J. Marjanovic, 2020-11-02, Page 21/25



NAT-MCH by N.A.T.

JTAG Switch Module Configuration

Active JTAG Device Settings is not available, because Xilinx Virtual Cable operating is running.

Xilinx Virtual Cable

Xilinx Virtual Cable Server: **enabled**

Base TCP Port: **2542**

Maximal User Defined JTAG Frequency: **2.0MHz**

JTAG Device	TOP-Port	JTAG Device	TOP-Port
AMC1	2542	AMC7	2548
AMC2	2543	AMC8	2549
AMC3	2544	AMC9	2546 (occupied)
AMC4	2545	AMC10	2551
AMC5	2546	AMC11	2552
AMC6	2547	AMC12	2553

Buttons: Apply, Discard, Reset Configuration

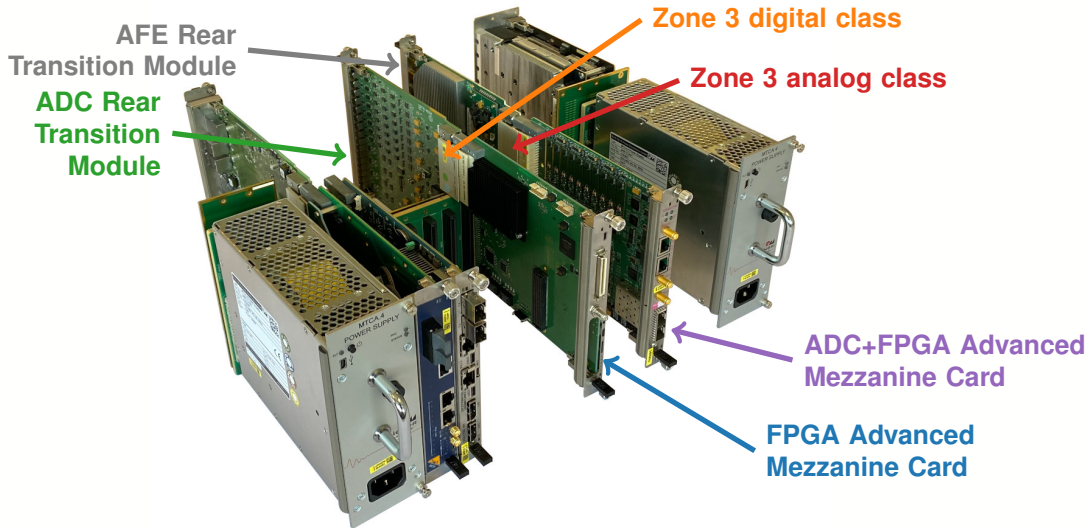
```
DAMC-FMC2ZUP@0x82 MMC>
DAMC-FMC2ZUP@0x82 MMC>s j bp fpga12
EEPROM value = 0x23
source: bp, dest: fpga12
DAMC-FMC2ZUP@0x82 MMC>v
Firmware version : V0.07-1-4a3b8841
Build date       : 2020-11-26T10:24:59Z
Build host      : ac84b46258fc
Compiler version : 9.3.1.20200408 (release
IPMI version    : 1.5
Vendor ID       : 0x053F
Product ID      : 0x200B
Board           : DAMC-FMC2ZUP
Debug Level     : 3
```

Vivado connects to XVC in crate;
everything is as with a JTAG cable ³

³XVC over MCH is slower than SmartLynq cable

Rear Transition Module

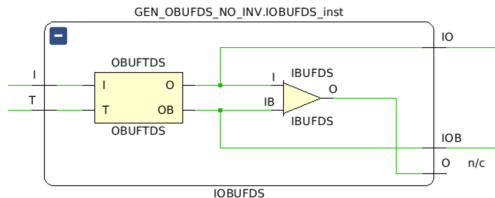
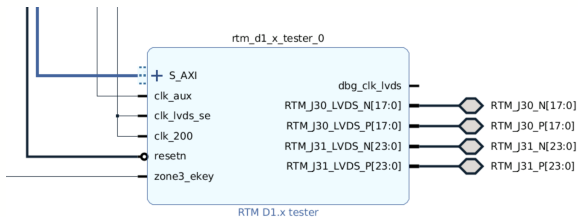
Front view



Zone 3 - e-keying

- ▶ MGTs are AC-coupled
→ no action necessary from the FPGA logic
- ▶ LVDS and single-ended signals need to be disabled in logic
→ input from the MMC (`RTM_EKEY`)

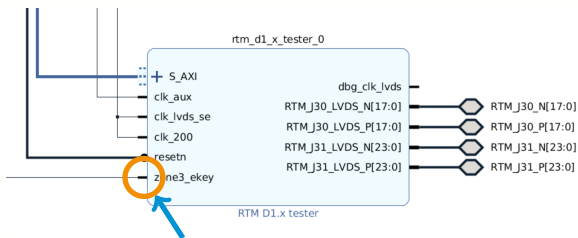
	LVDS I/O	MGT
Class D1.0	48	
Class D1.1	42	2
Class D1.2	38	4
Class D1.3	28	8
Class D1.4	8	16



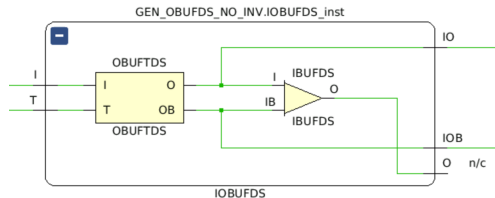
Zone 3 - e-keying

- ▶ MGTs are AC-coupled
→ no action necessary from the FPGA logic
- ▶ LVDS and single-ended signals need to be disabled in logic
→ input from the MMC (RTM_EKEY)

	LVDS I/O	MGT
Class D1.0	48	
Class D1.1	42	2
Class D1.2	38	4
Class D1.3	28	8
Class D1.4	8	16

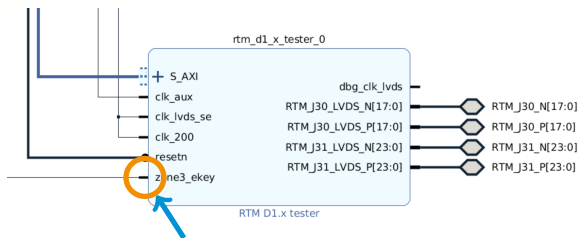


output from the MMC should be connected to RTM interface IP

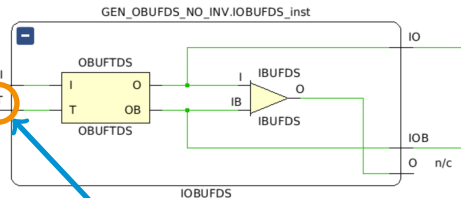


- ▶ MGTs are AC-coupled
→ no action necessary from the FPGA logic
- ▶ LVDS and single-ended signals need to be disabled in logic
→ input from the MMC (RTM_EKEY)

	LVDS I/O	MGT
Class D1.0	48	
Class D1.1	42	2
Class D1.2	38	4
Class D1.3	28	8
Class D1.4	8	16



output from the MMC should be connected to RTM interface IP



e.g. LVDS interface is disabled by asserting T input on IOBUFDS

Thank you

<https://techlab.desy.de>
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Deutsches Elektronen-Synchrotron DESY
A Research Centre of the Helmholtz Association
Notkestr. 85, 22607 Hamburg, Germany

MicroTCA Training courses:

- ▶ Basic Training:
3 - 4 February 2021, VIRTUAL
- ▶ Advanced Training:
24 - 25 February 2021, VIRTUAL

<https://techlab.desy.de/services/training/>

Zone 3 - performance

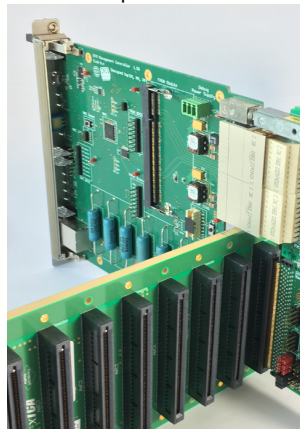
RTM loopback test on FMC2ZUP (over S7), at 800 Mbps⁴:

```
lane, valid win, first e, second e, init, status, nr ok
-----
0 < skipped >
1 < skipped >
2 < skipped >
3 9 8 17 1 DONE 255
4 10 7 17 0 DONE 255
5 10 7 17 0 DONE 255
6 9 8 17 1 DONE 255
7 9 8 17 0 DONE 255
8 10 7 17 0 DONE 255
9 9 8 17 0 DONE 255
10 10 7 17 0 DONE 255
11 11 6 17 0 DONE 255
12 8 9 17 0 DONE 255
13 10 7 17 0 DONE 255
14 11 6 17 1 DONE 255
15 9 8 17 0 DONE 255
16 10 7 17 1 DONE 255
17 11 6 17 1 DONE 255
18 9 8 17 1 DONE 255
19 10 7 17 1 DONE 255
20 10 7 17 1 DONE 255
```

from Spartan 7 data sheet:

LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

RTM loopback/load card



https://techlab.desy.de/products/module_management_controller/legacy_mmc_kit/index_eng.html

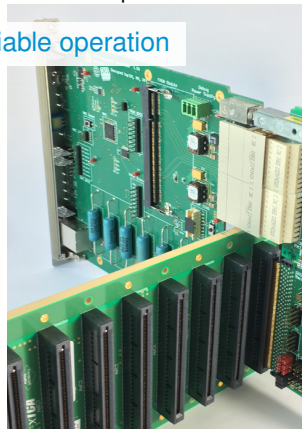
Zone 3 - performance

RTM loopback test on FMC2ZUP (over S7), at 800 Mbps⁴:

data valid window wide enough for reliable operation

```
lane, valid win, first, second e, init, status, nr ok
-----
0 < skipped >
1 < skipped >
2 < skipped >
3 9 8 17 1 DONE 255
4 10 7 17 0 DONE 255
5 10 7 17 0 DONE 255
6 9 8 17 1 DONE 255
7 9 8 17 0 DONE 255
8 10 7 17 0 DONE 255
9 9 8 17 0 DONE 255
10 10 7 17 0 DONE 255
11 11 6 17 0 DONE 255
12 8 9 17 0 DONE 255
13 10 7 17 0 DONE 255
14 11 6 17 1 DONE 255
15 9 8 17 0 DONE 255
16 10 7 17 1 DONE 255
17 11 6 17 1 DONE 255
18 9 8 17 1 DONE 255
19 10 7 17 1 DONE 255
20 10 7 17 1 DONE 255
```

RTM loopback/load card



https://techlab.desy.de/products/module_management_controller/legacy_mmc_kit/index_eng.html

from Spartan 7 data sheet:

LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

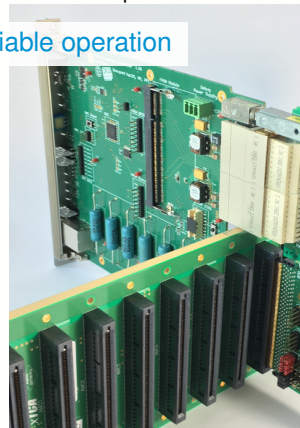
RTM loopback test on FMC2ZUP (over S7), at 800 Mbps⁴:

data valid window wide enough for reliable operation

data successfully transferred

lane	valid	win	first	second	e	init	status	nr	ok
0	<	skipped	>						
1	<	skipped	>						
2	<	skipped	>						
3	9	8	17	1	DONE		255		
4	10	7	17	0	DONE		255		
5	10	7	17	0	DONE		255		
6	9	8	17	1	DONE		255		
7	9	8	17	0	DONE		255		
8	10	7	17	0	DONE		255		
9	9	8	17	0	DONE		255		
10	10	7	17	0	DONE		255		
11	11	6	17	0	DONE		255		
12	8	9	17	0	DONE		255		
13	10	7	17	0	DONE		255		
14	11	6	17	1	DONE		255		
15	9	8	17	0	DONE		255		
16	10	7	17	1	DONE		255		
17	11	6	17	1	DONE		255		
18	9	8	17	1	DONE		255		
19	10	7	17	1	DONE		255		
20	10	7	17	1	DONE		255		

RTM loopback/load card



https://techlab.desy.de/products/module_management_controller/legacy_mmc_kit/index_eng.html

from Spartan 7 data sheet:

LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

⁴1250 Mbps is possible with a faster speed grade FPGA (Spartan 7)