

Enabling low-power MAPS-based space trackers: a sparsified readout based on smart clock gating for the High Energy Particle Detector-02

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The adoption of pixel sensors for space-based tracking detectors requires low power consumption and enhanced heat dissipation to cope with the satellite power and cooling constraints. The High Energy Particle Detector (HEPD) tracker onboard the CSES-02 will be the first application of monolithic active pixel sensors (MAPS) to a satellite-based experiment. This result is achieved with a parallel sparsified readout architecture implemented on a single low-power FPGA chip, which manages the 150 ALPIDE chips of the three-plane tracker. The power consumption is reduced by reading out the ALPIDE chips via the control line instead of the high speed data link, and by distributing the clock only to the portions of the detector crossed by a particle. The readout concept presented in this contribution allows to deal with both the required performance and the power constraints, and is scalable to larger and more complex detectors.

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