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On behalf of the CMS Tracker group

Transverse momentum discriminating silicon modules for the Phase-II Upgrade of the CMS Outer Tracker

MATTER AND TECHNOLOGIES MEETING
02.02.2021

HELMHOLTZ RESEARCH FOR GRAND CHALLENGES

CMS Compact Muon Solenoid

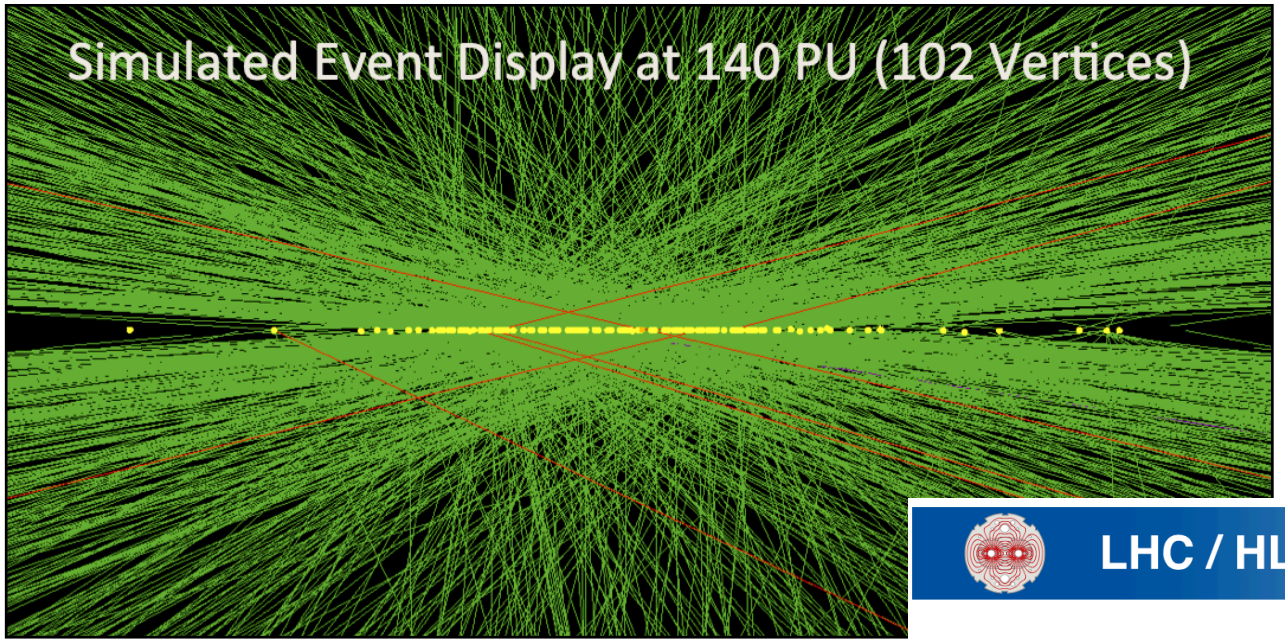
DESY.

Overview

- **CMS Outer Tracker Upgrade**
  - High Luminosity LHC
  - CMS experiment upgrade
  - CMS Outer Tracker upgrade
- **Momentum discriminating silicon module**
  - Pixel-Strip silicon module concept
  - Pixel-Strip silicon module design
  - Pixel-Strip ASIC architecture
- **DAQ Test Systems**
  - Data acquisition test system
  - Micro Data-Trigger-Control firmware
  - MUX crate based test system
- **Summary & Outlook**

CMS Outer Tracker Upgrade

High Luminosity LHC



- Unprecedented radiation levels up to $1.1 \times 10^{15}\ n_{eq} \times cm^{-2}$
- 10 times higher pile-up
- Higher data rates and trigger latency

- Major LHC accelerator upgrade
- Peak instantaneous luminosity

$$5 - 7.5 \times 10^{34} cm^{-2} s^{-1}$$

- $300\ fb^{-1}$ per year and up to $3000\ fb^{-1}$ over ~10 years

Phase II Experiments Upgrade

https://hilumilhc.web.cern.ch/content/hl-lhc-project

CMS experiment Phase II Upgrade

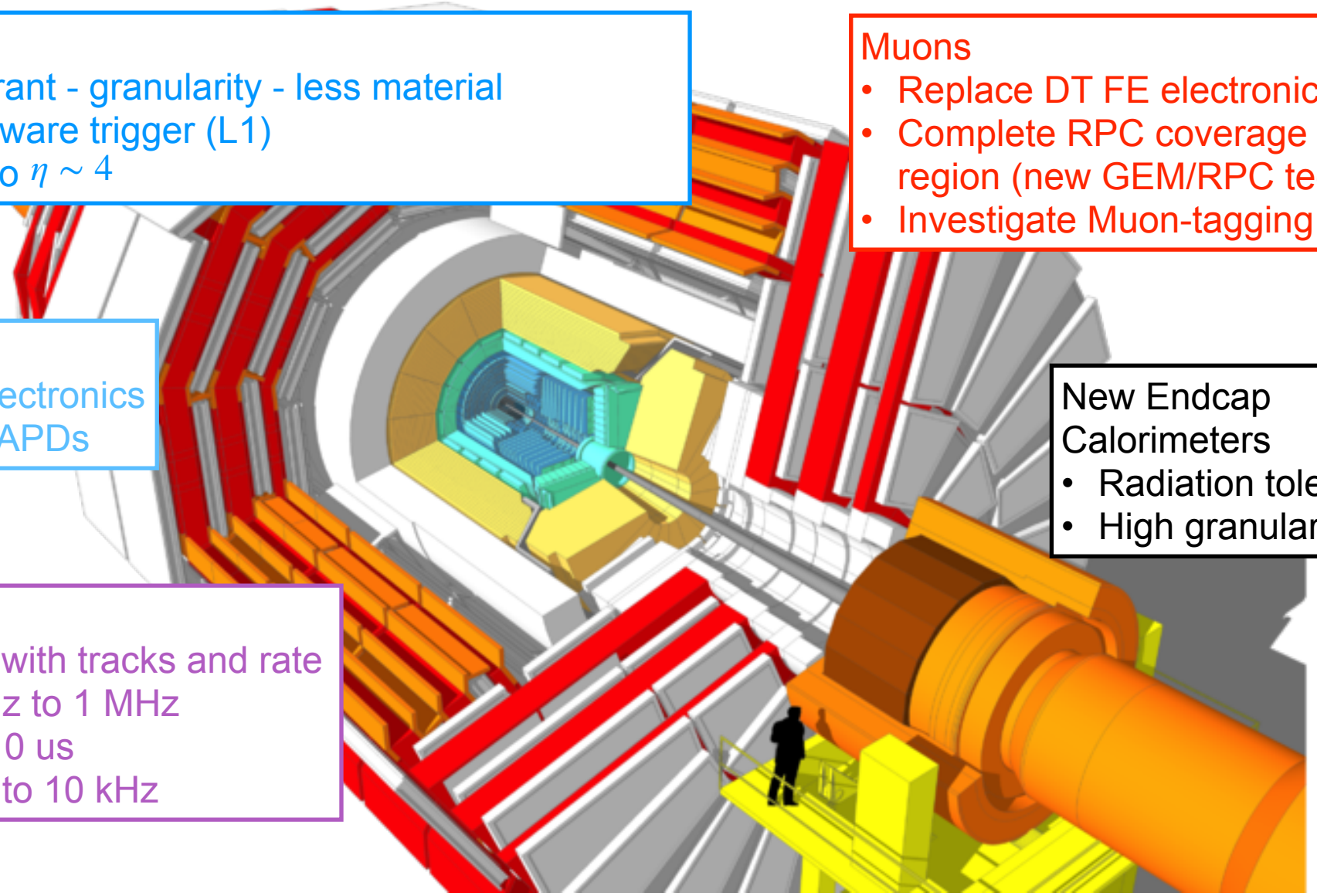
New Tracker
- Radiation tolerant - granularity - less material
- Tracks in hardware trigger (L1)
- Coverage up to $\eta \sim 4$

Muons
- Replace DT FE electronics
- Complete RPC coverage in forward region (new GEM/RPC technology)
- Investigate Muon-tagging up to $\eta \sim 4$

Barrel ECAL
- Replace FE electronics
- Cool detector/APDs

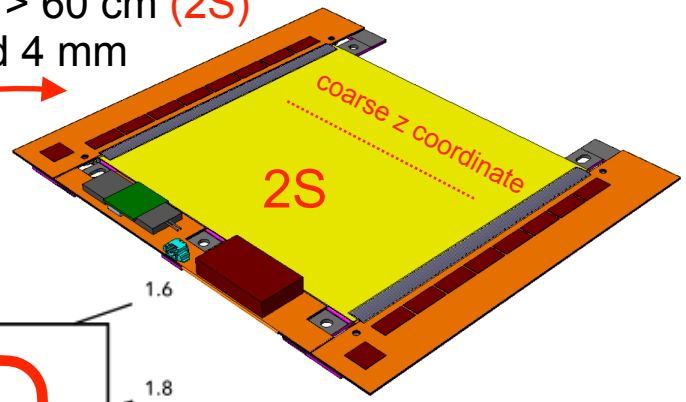
New Endcap Calorimeters
- Radiation tolerant
- High granularity

Trigger/DAQ
- L1 (hardware) with tracks and rate up to ~ 500 kHz to 1 MHz
- L1 Latency > 10 us
- HLT output up to 10 kHz



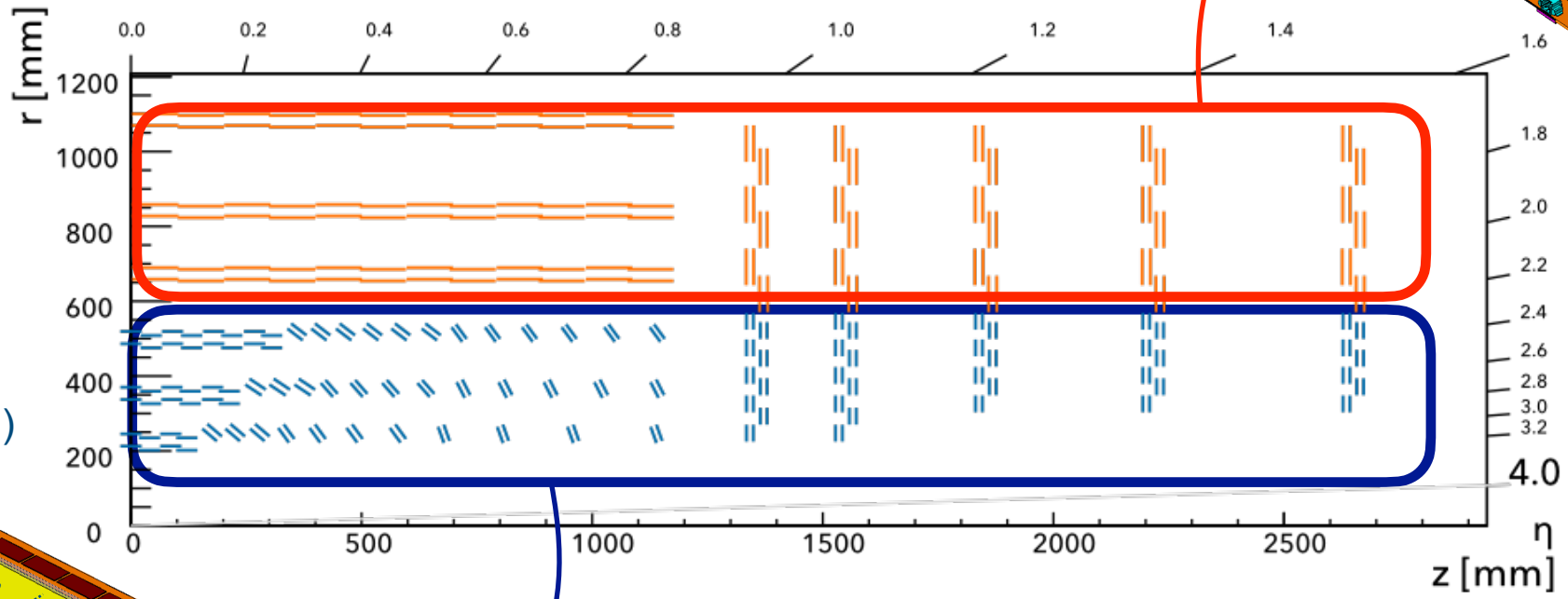
CMS Outer Tracker Phase II Upgrade

- Stack of two strip sensors at r > 60 cm (2S)
- Sensor spacings : 1.8 mm and 4 mm

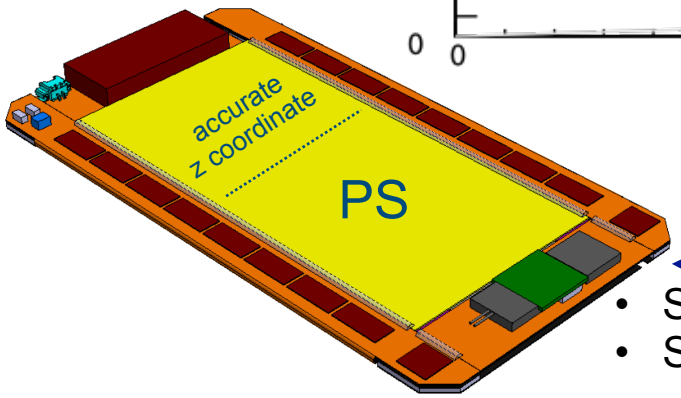


Strip-Strip (2S) Modules

Layout with 6 barrel layers and 5 end cap double disks



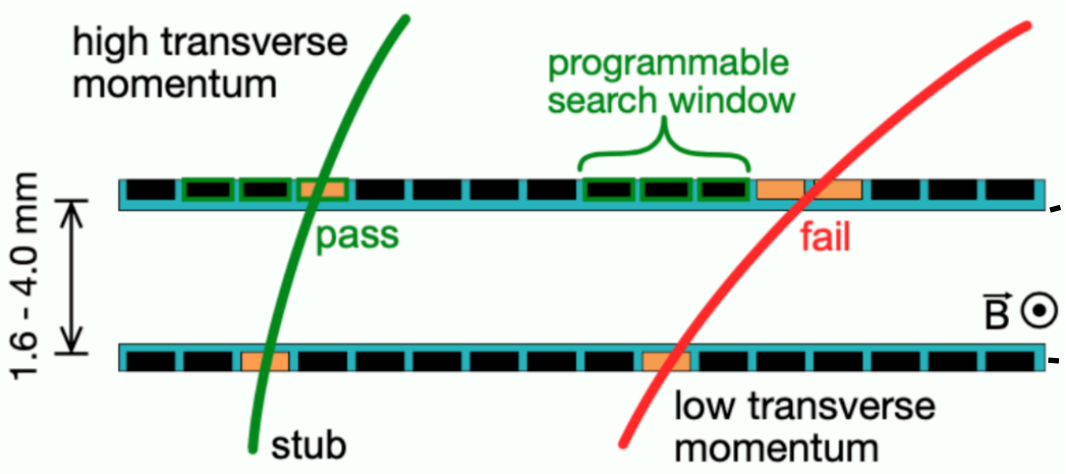
Pixel-Strip (PS) Modules

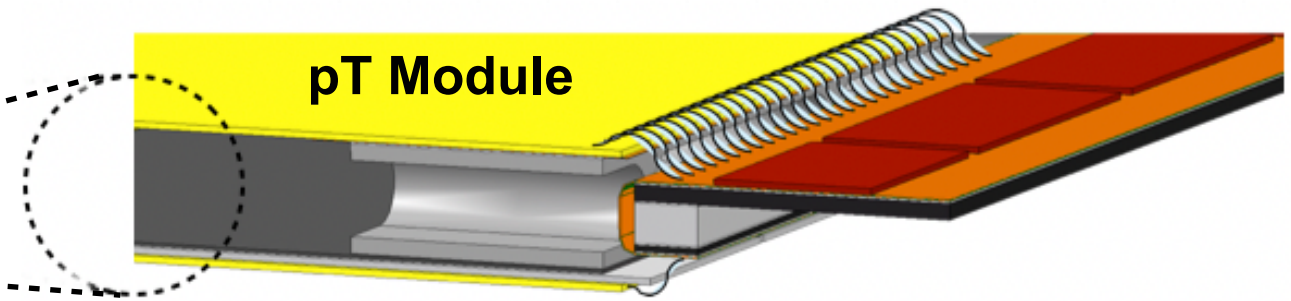


- Stack of pixel and strip sensor at r < 60 cm (PS)
- Sensor spacings : 1.6 mm, 2.6 mm and 4 mm

pT Discriminating Si Modules

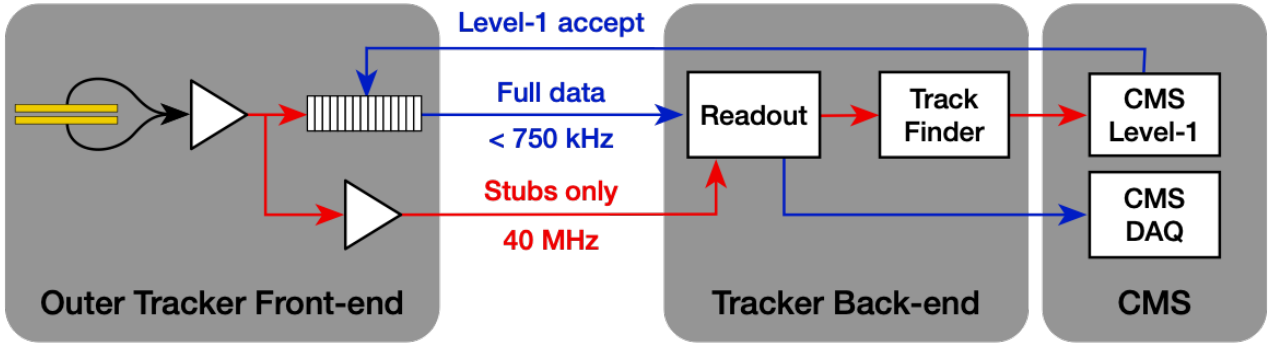
Pixel-Strip (PS) Silicon Module Concept



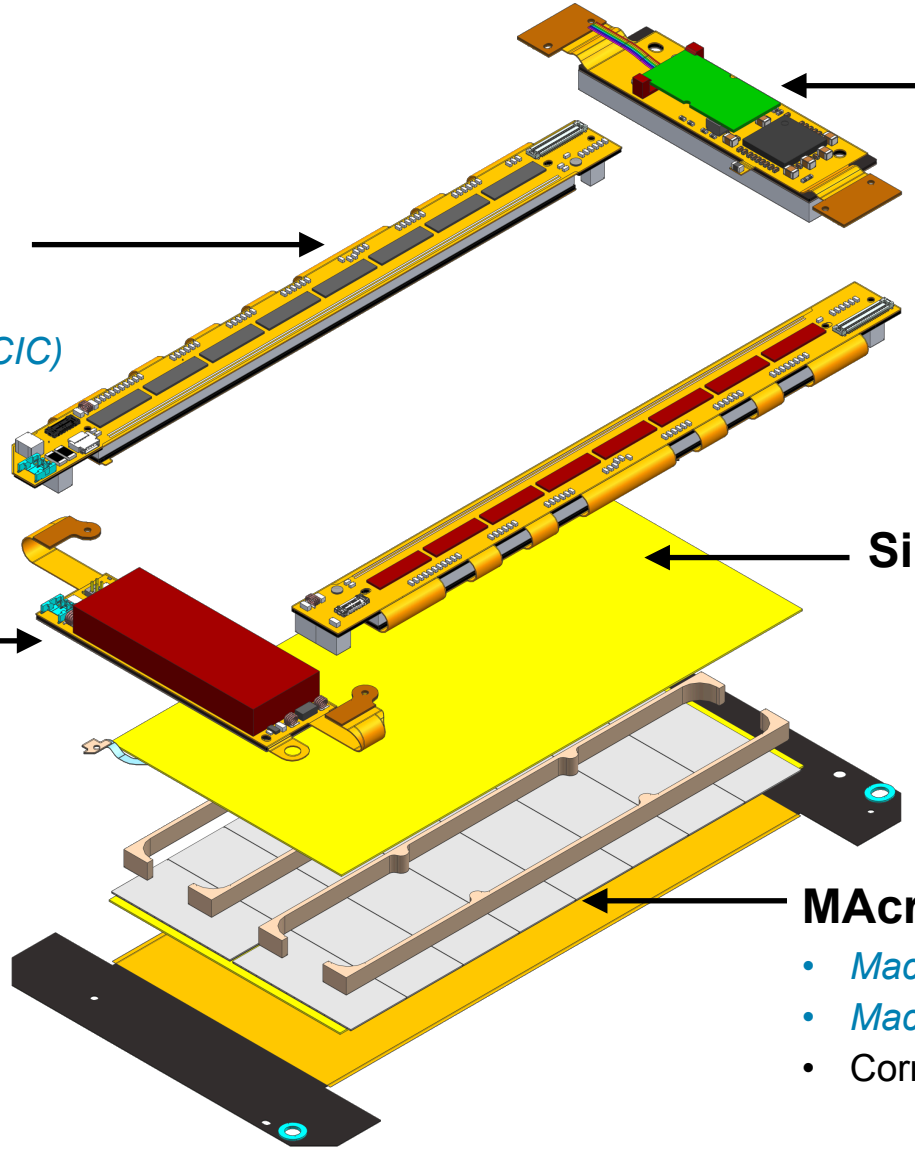


- Modules with on-board pT discrimination
  - Correlation of signals from two closely spaced sensors
  - Strong magnetic field exploited for local pT measurement
  - Local rejection of low-pT tracks to reduce data volume

- Modules provide both Level-1 and readout data
  - Trigger data (“stubs”) sent every bunch crossing (40MHz)
  - Readout data up to 750KHz
  - “stubs” are used to form Level-1 tracks



Pixel-Strip (PS) Silicon Module Design



SSA Front-End Hybrid

- *Single-Strip ASIC (SSA)*
- *Concentrator Integrated Circuit (CIC)*
- Handles signal from strip sensor
- Transfers data to pixel chip

Power Hybrid

- DC-DC converter
- Used for module power

Read-Out Hybrid

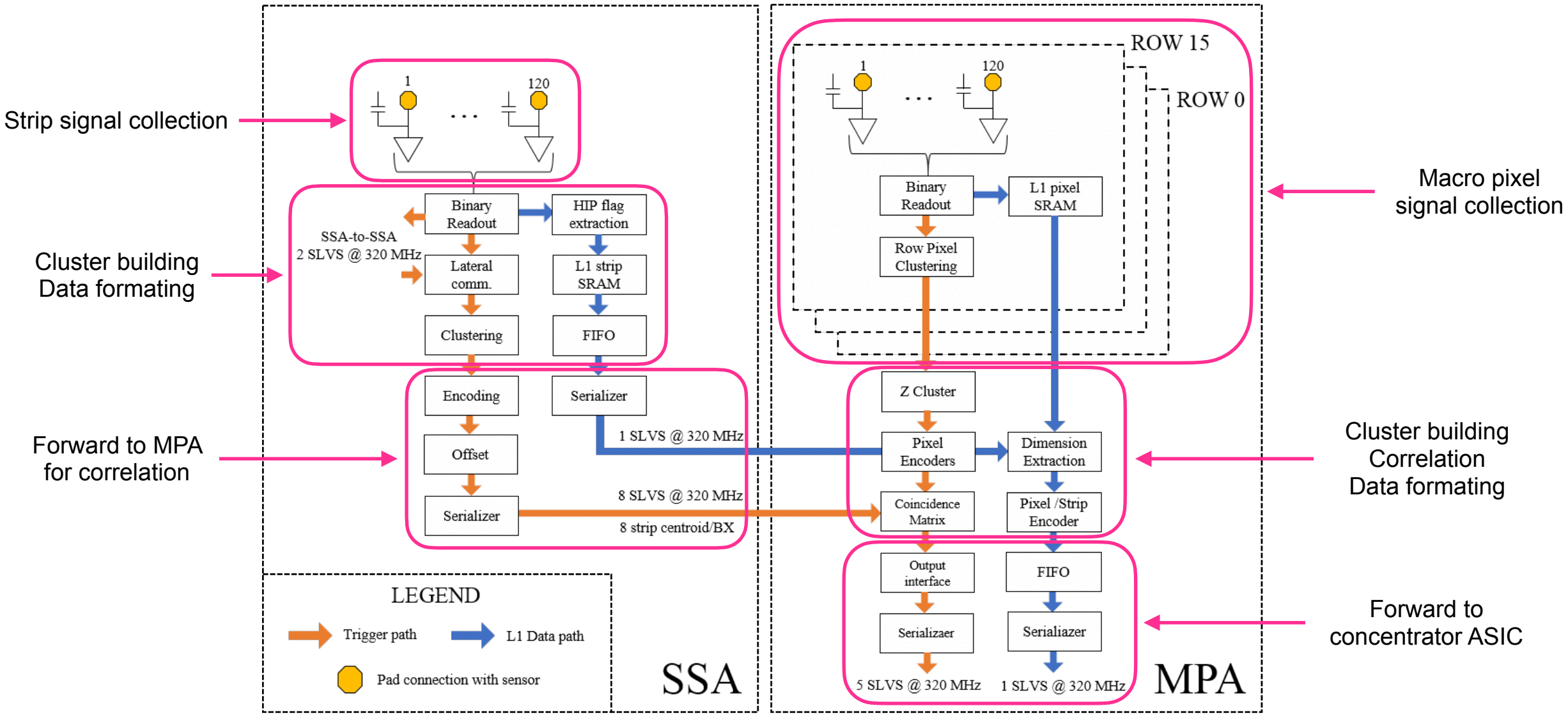
- *Low-power Gigabit Transceiver (LpGBT)*
- *VTRx+* optical module
- Transmits data over optical fibre

Silicon Strip Sensor

MAcro Pixel Sub Assembly (MAPSA)

- *Macro Pixel ASIC*
- *Macro Pixel Silicon sensor 1400 x 100 um*
- Correlates signal from both sensors

Pixel-Strip (PS) ASIC Architecture

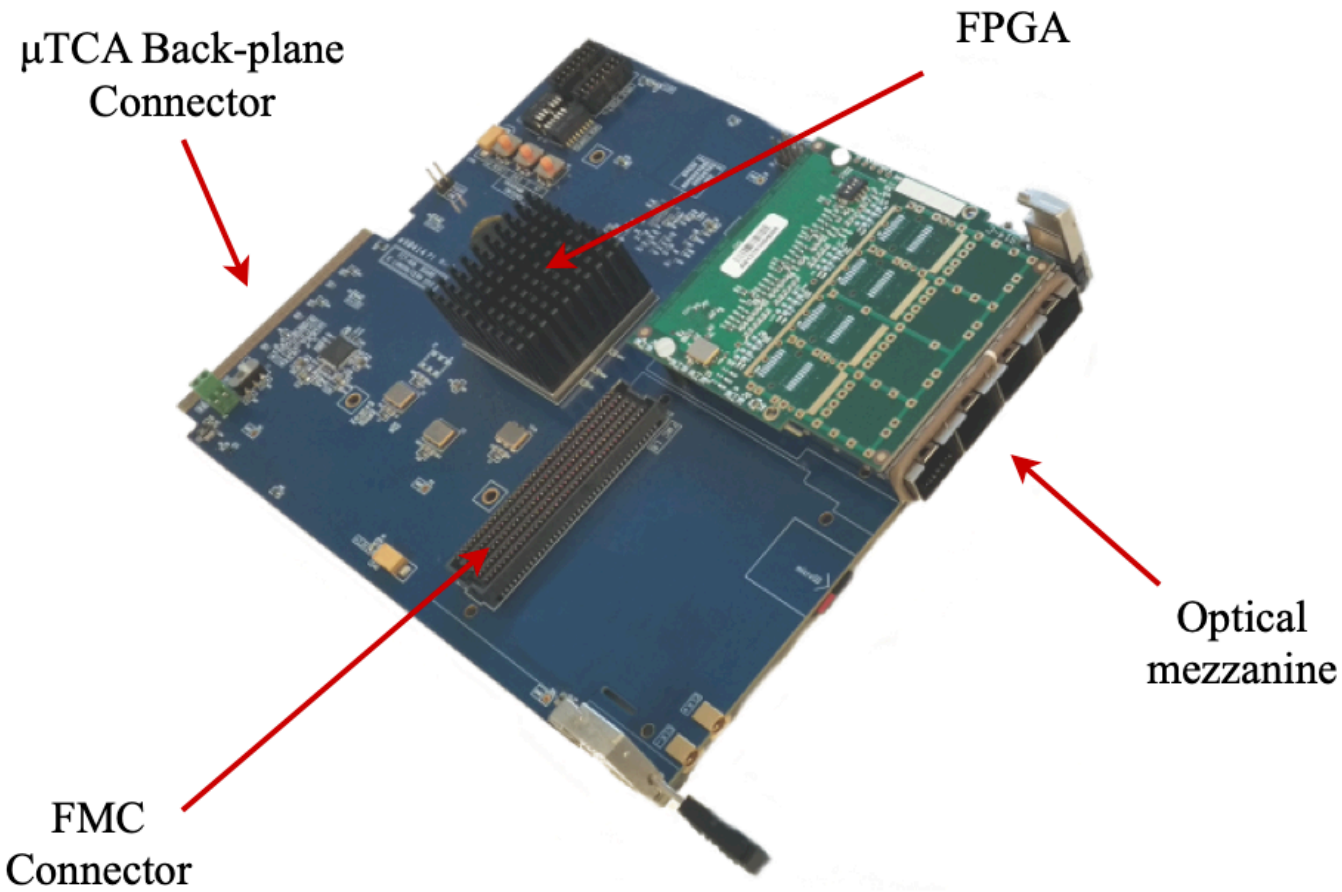


DAQ Test System

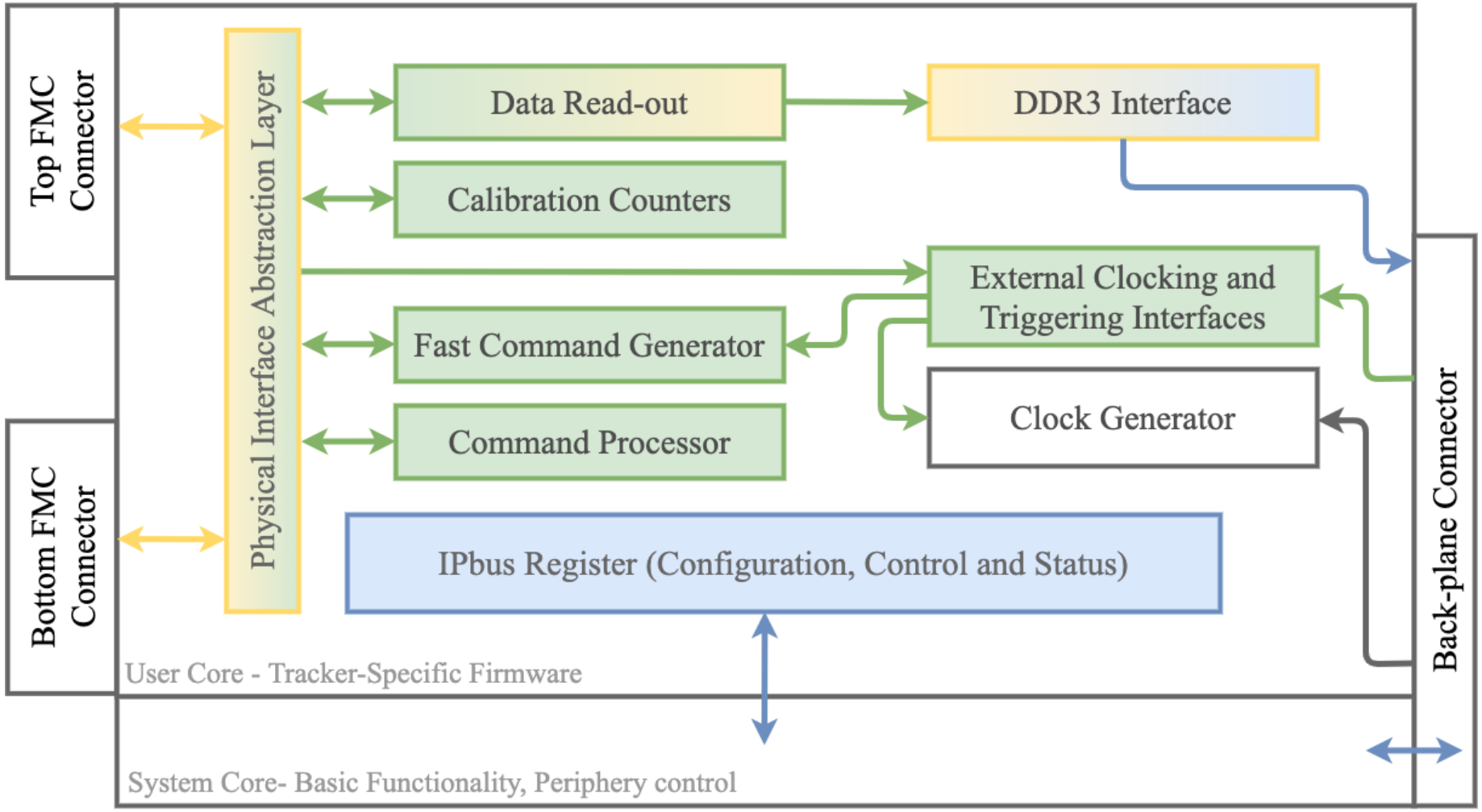
Data Acquisition Test System

- Exploits ***FC7*** uTCA-compatible board for generic data acquisition and control applications
  - Kintex-7 FPGA
  - 2 FMC Connectors
  - Advanced clock distribution system
  - External DDR3 memory
  - uTCA integration

- Several custom interface are supported by the system in case of needed synchronous operation
  - Trigger Logic Unit (TLU)
  - DIO5 (5 LEMO I/O)
  - AMC13 (interface to the TCDS)
  - …



Micro Data-Trigger-Control Firmware (uDTC)



Clock Domains :

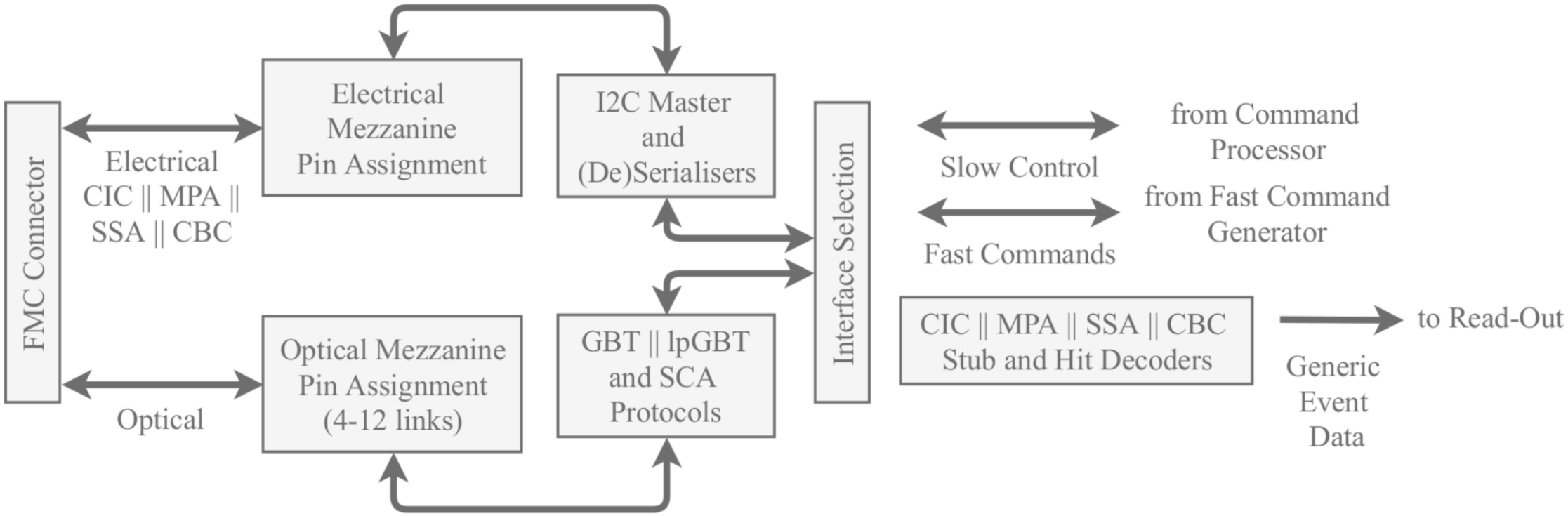
40 MHz | 31.25 MHz | 120 - 320 MHz

Physical Interface Abstraction Layer

Abstraction layer introduced for a more efficient implementation,

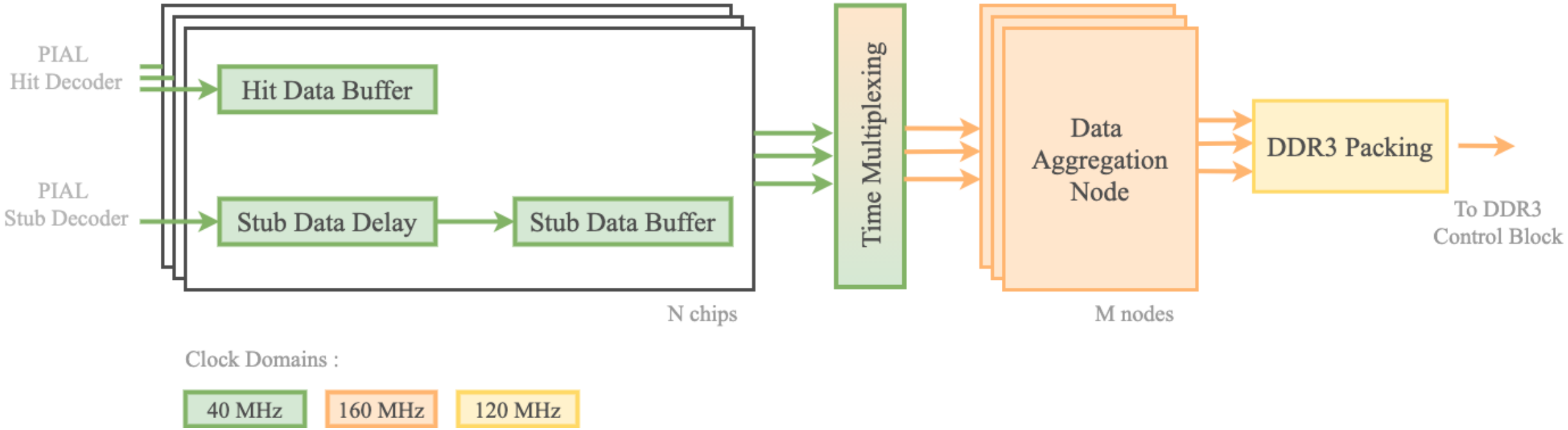
providing needed support for all different front-end flavours (CIC, SSA, MPA, CBC)

including control of various interface boards



Data Read-out Block

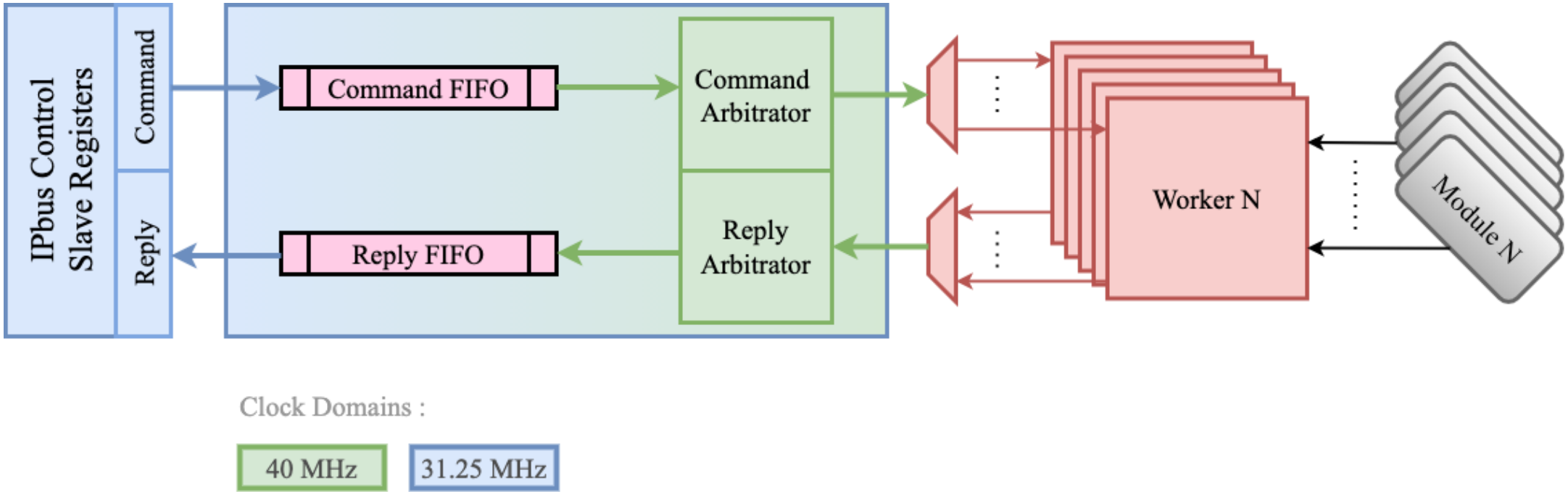
- Aggregation of data from the Physical Interface Abstraction layer
  - Data from all front-end chips/modules
- Event formatting and loading to the DDR3 memory, further read via IPbus
- Time multiplexing method for job distribution to the data aggregation nodes



Command Processor Block

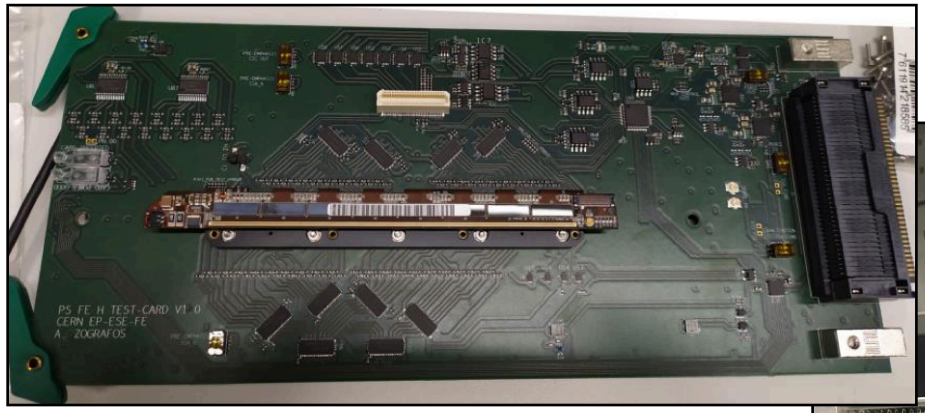
- Command Processor Core
  - Unpacking/Packing command and replies from/to IPbus
  - Command and Reply FIFOs for Clock Domain Crossing

- Command Processor Worker
  - Implements module slow control functions and routines



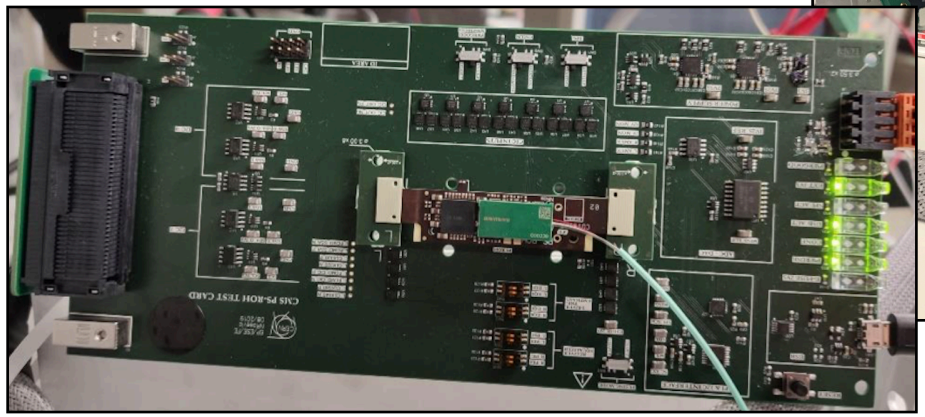
MUX Crate-based Test System

SSA Front-End Hybrid Test Card



Multiplexing Crate

Read-Out Hybrid Test Card



Dedicated firmware block developed for MUX Crate control and electrical tests of single components

Conclusion

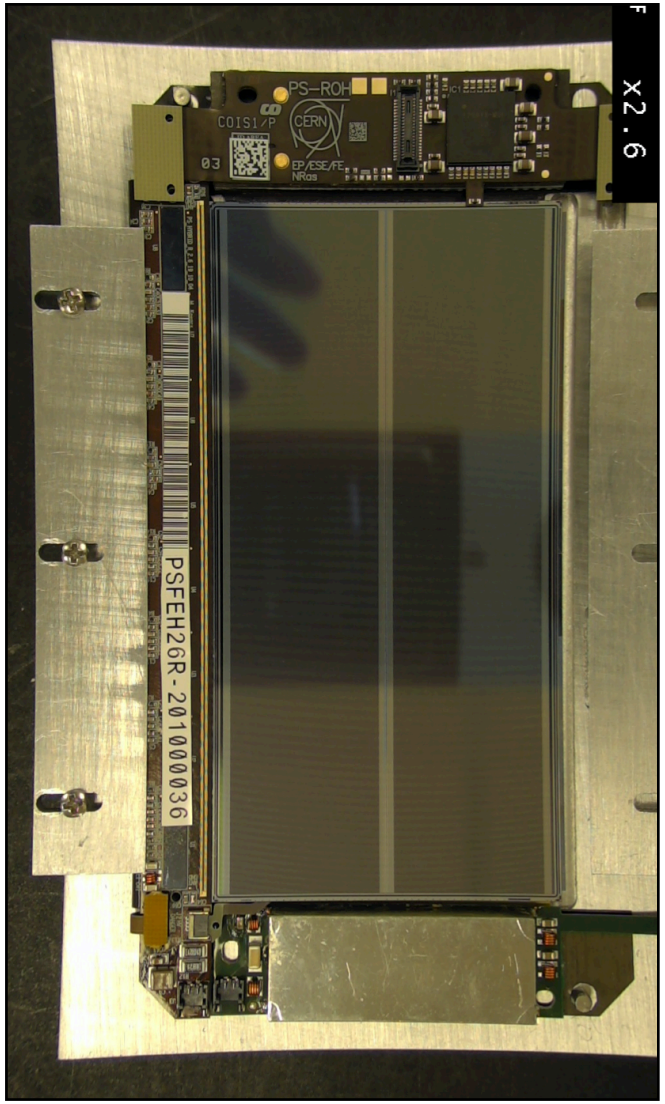
Summary & Outlook

Summary

- Introduction of new Tracker module design for the needs of High Luminosity LHC upgrade
- Momentum discriminating design based on cluster correlation between two closely stacked Si sensor
- Data acquisition firmware developed for the needs of prototype testing and module production
- MUX crate based test system with custom test cards for single component testing of large production batches

Outlook

- DAQ Firmware and test systems development still ongoing
- First 1/2 PS Module soon to go for beam test



First 1/2 Pixel-Strip Module

THANK YOU.

Contact

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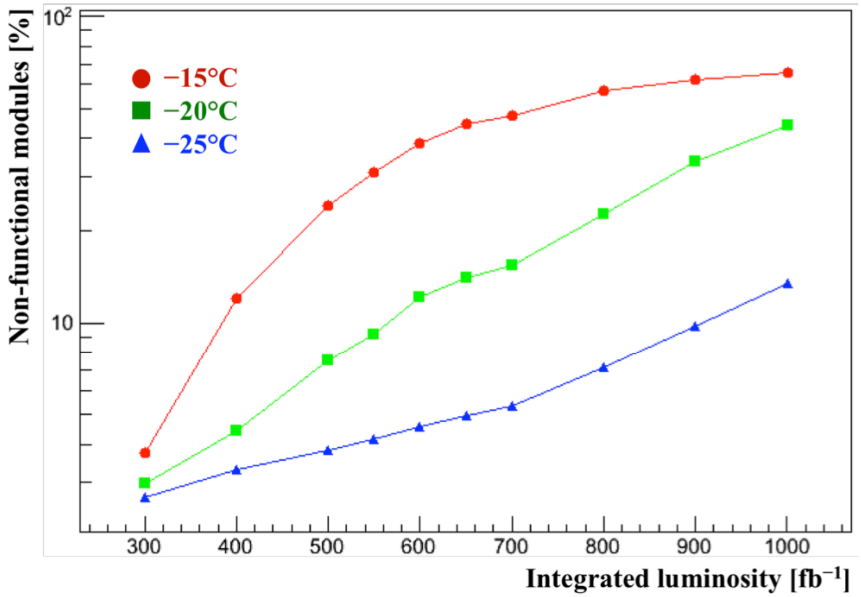
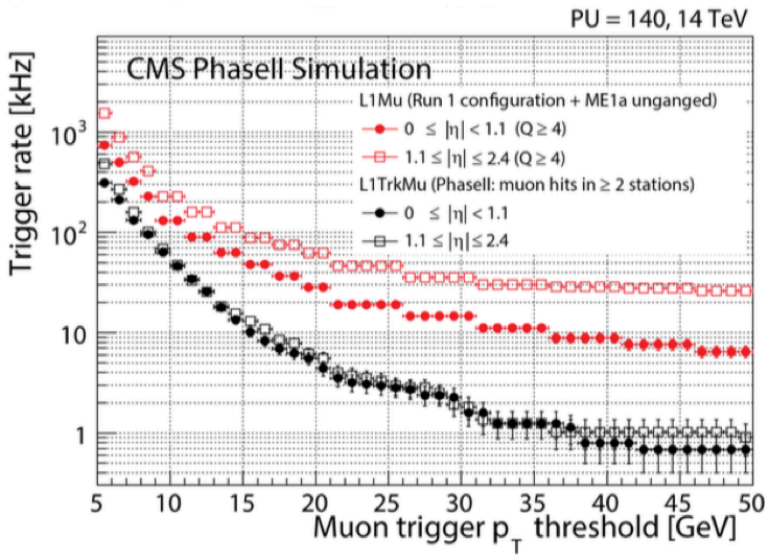
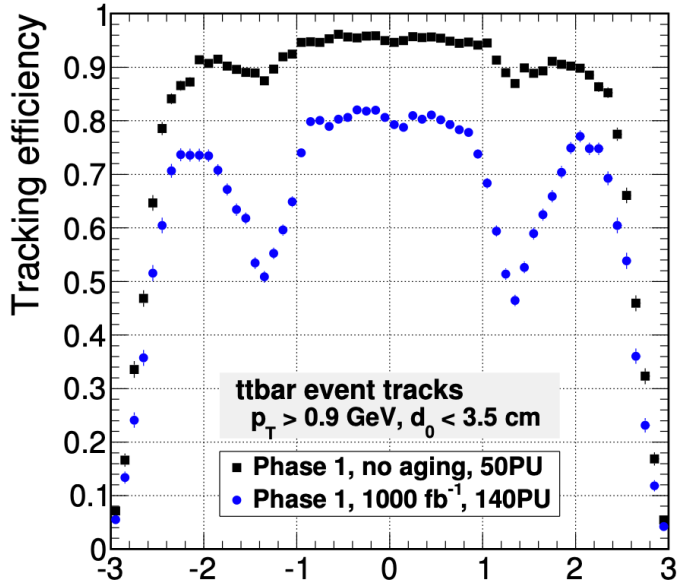
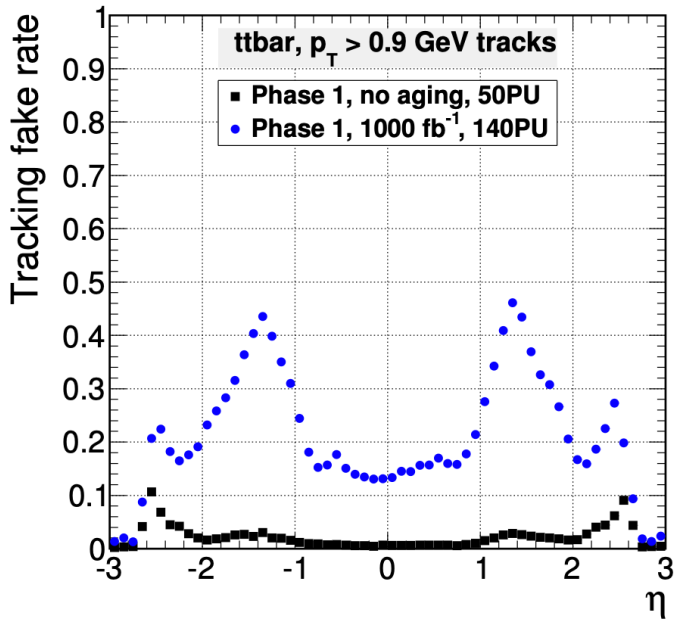
Back-Up

Limitations of the current tracker









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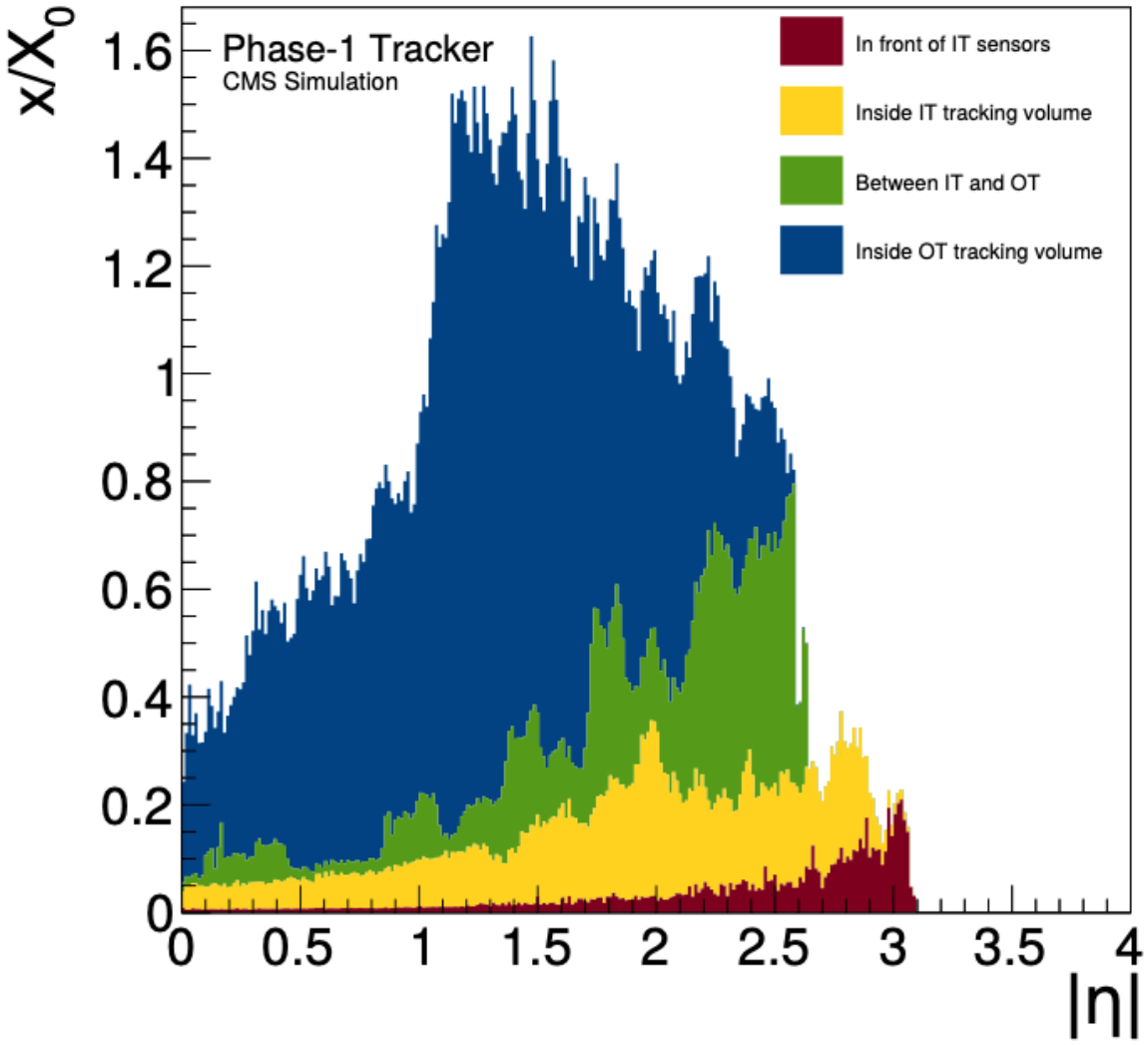
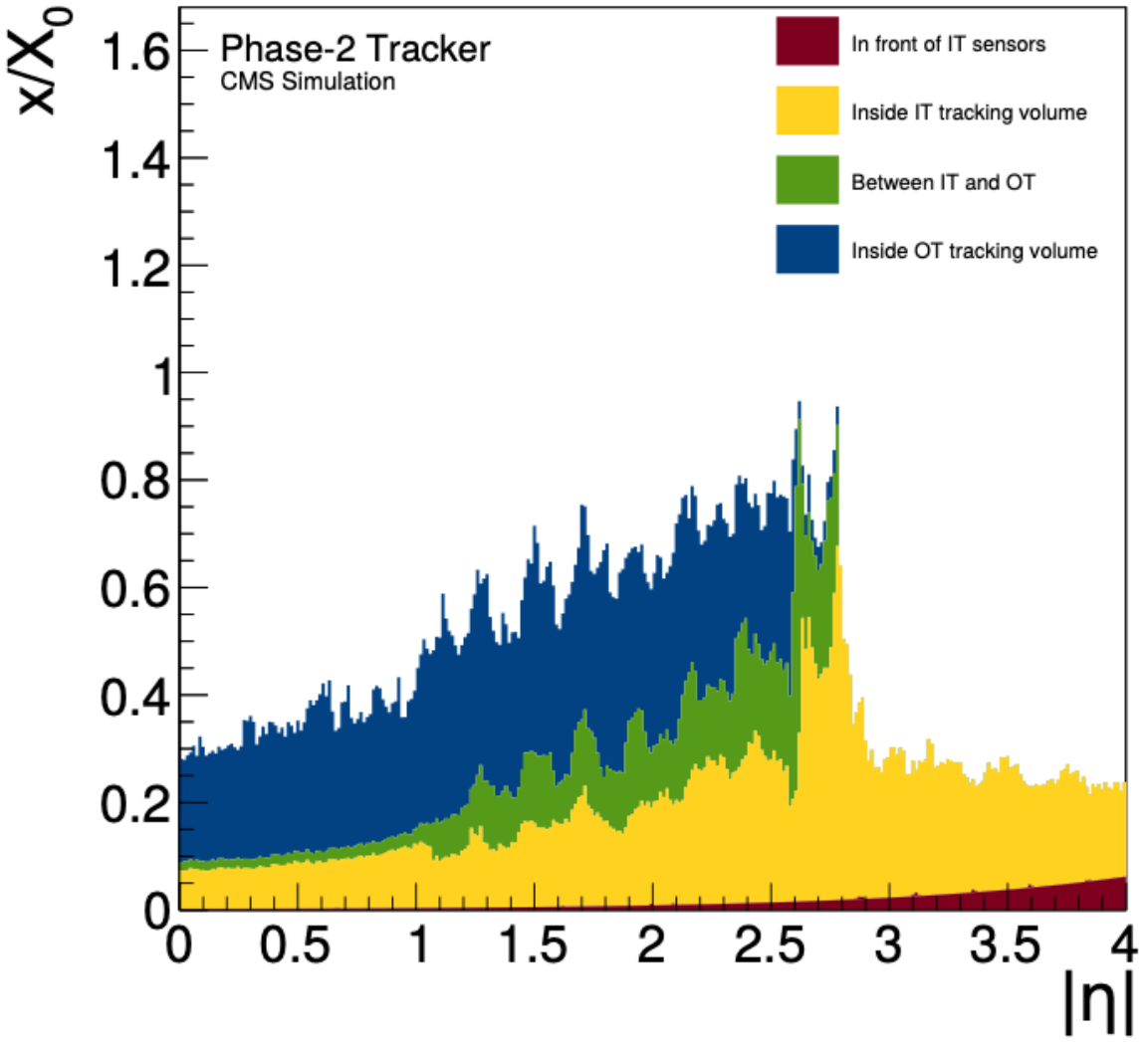
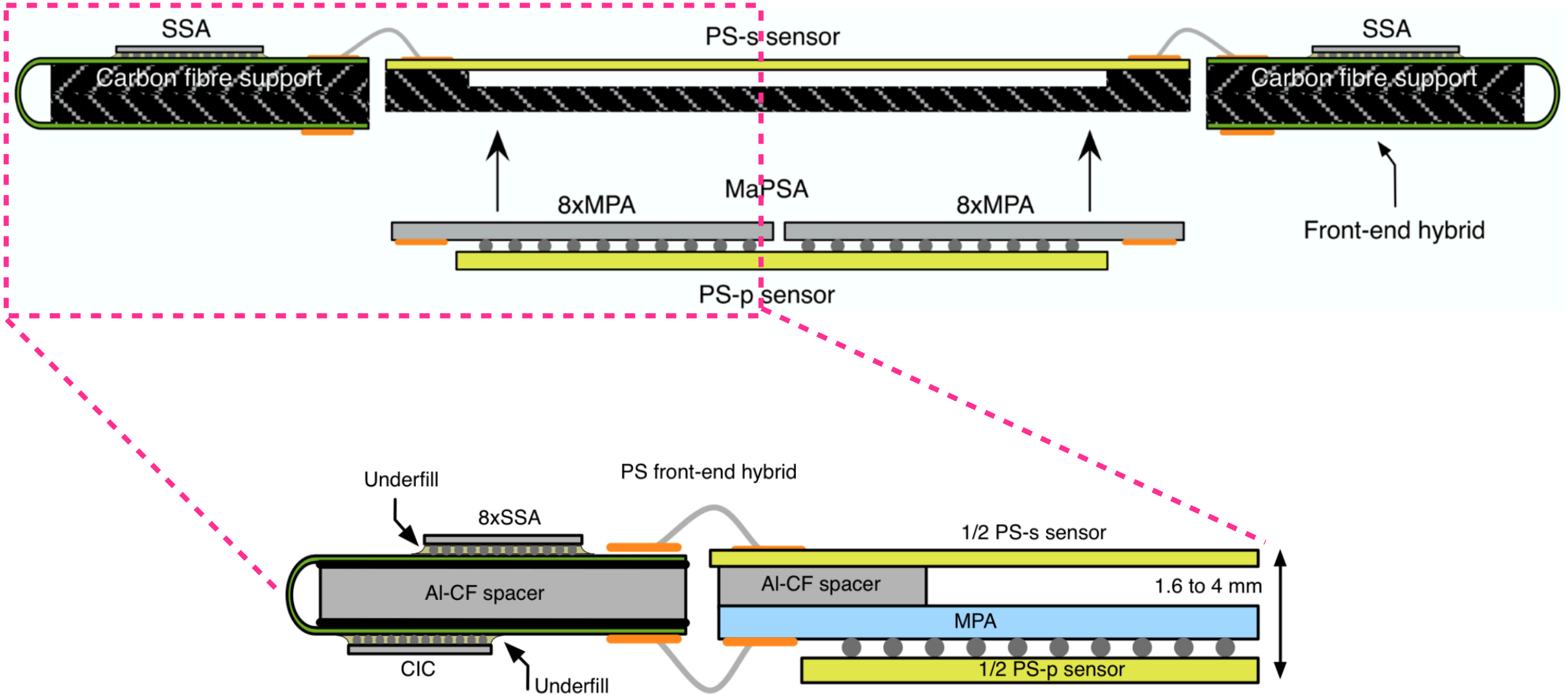
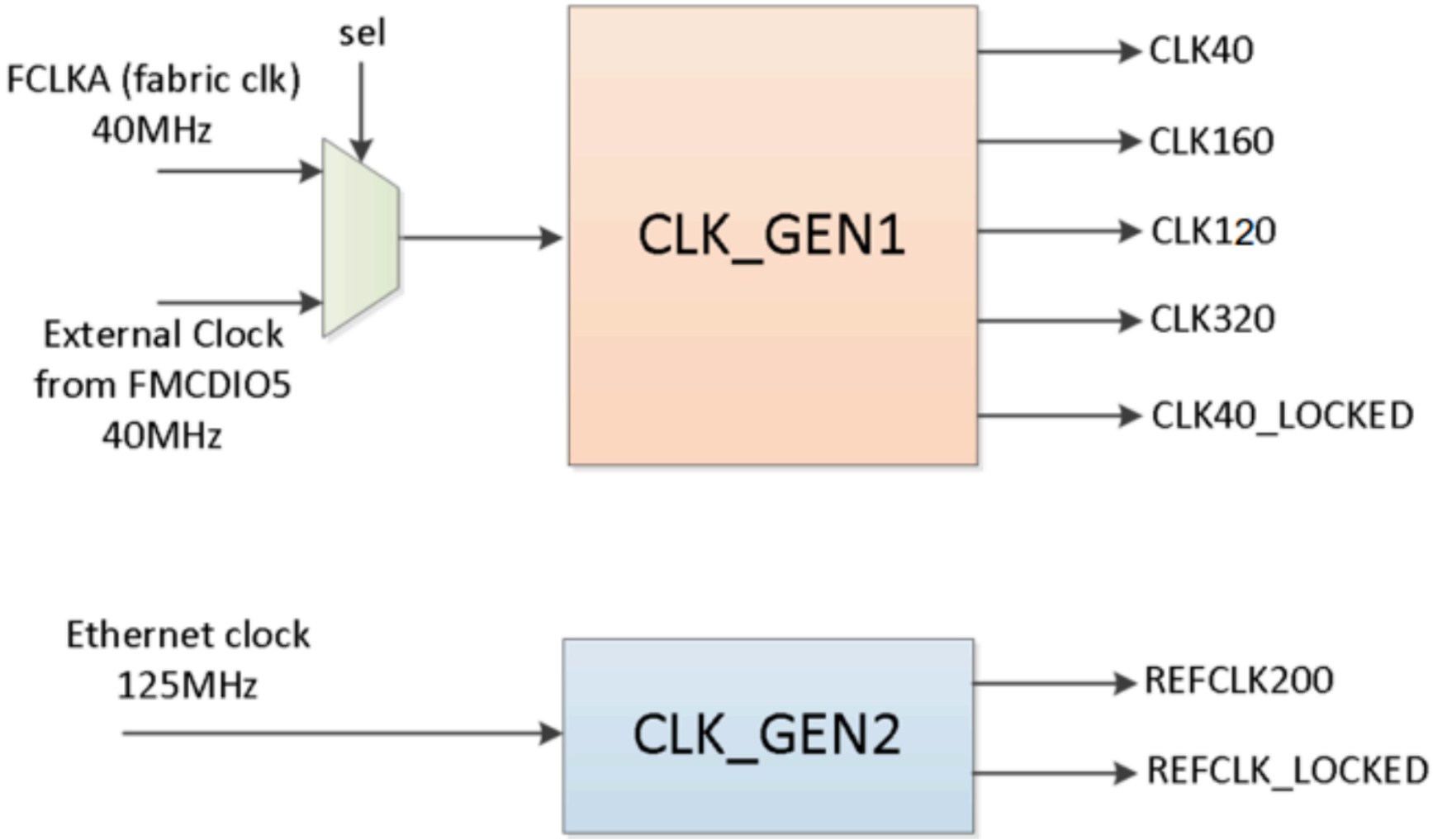




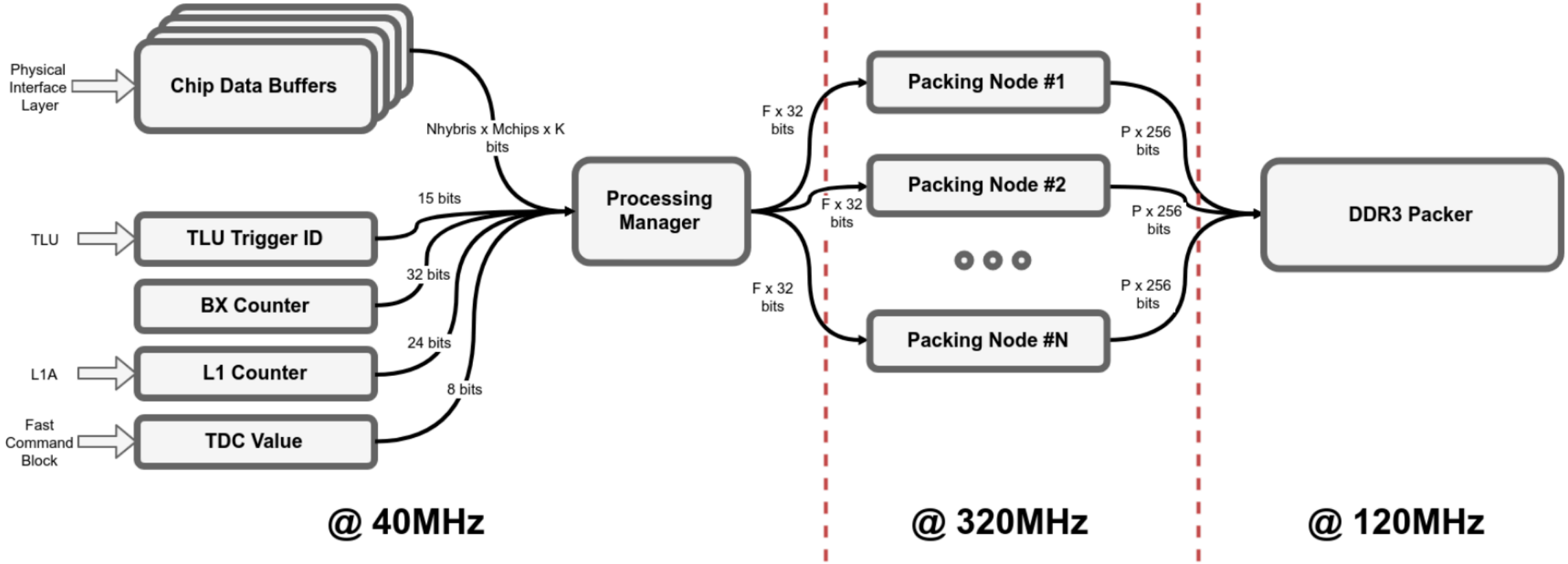
Cut through the Pixel-Strip Module



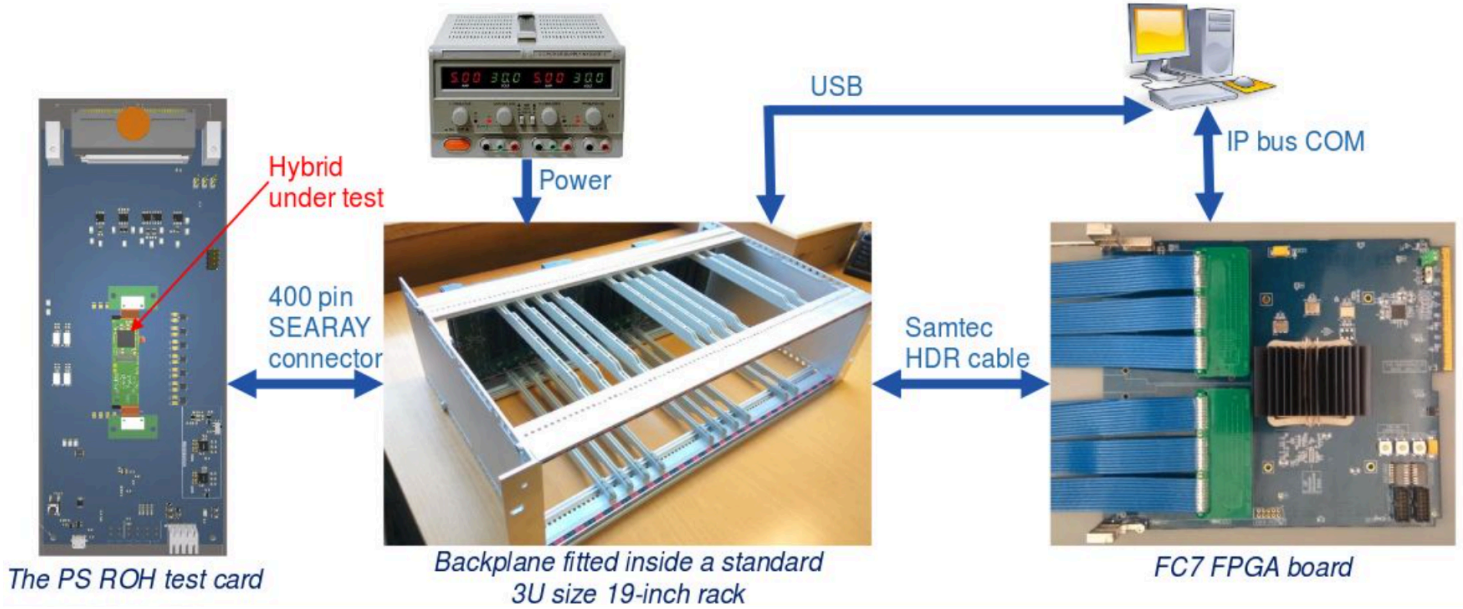
Clock Generator block

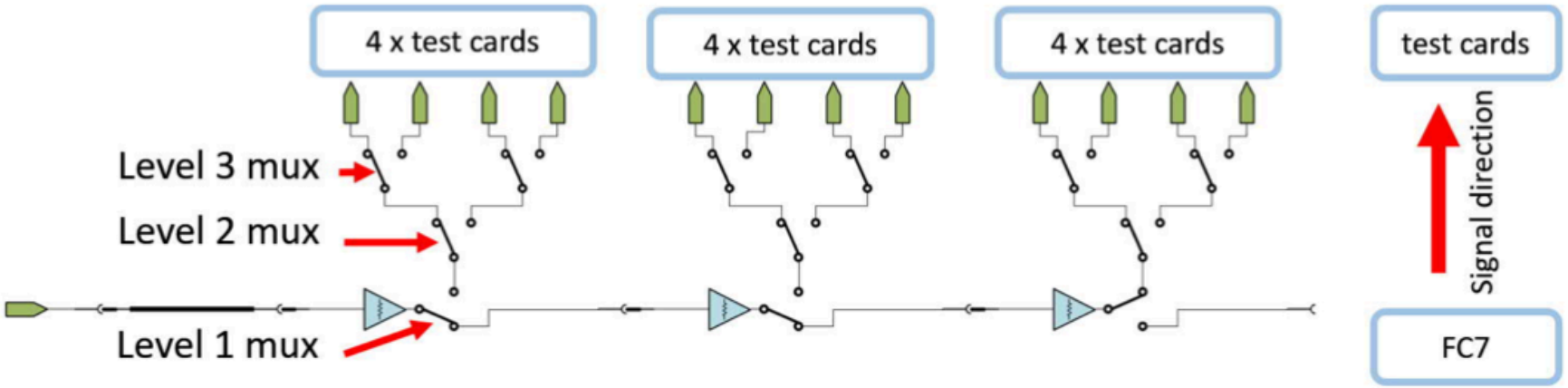


Readout block data flow diagram



MUX Crate System

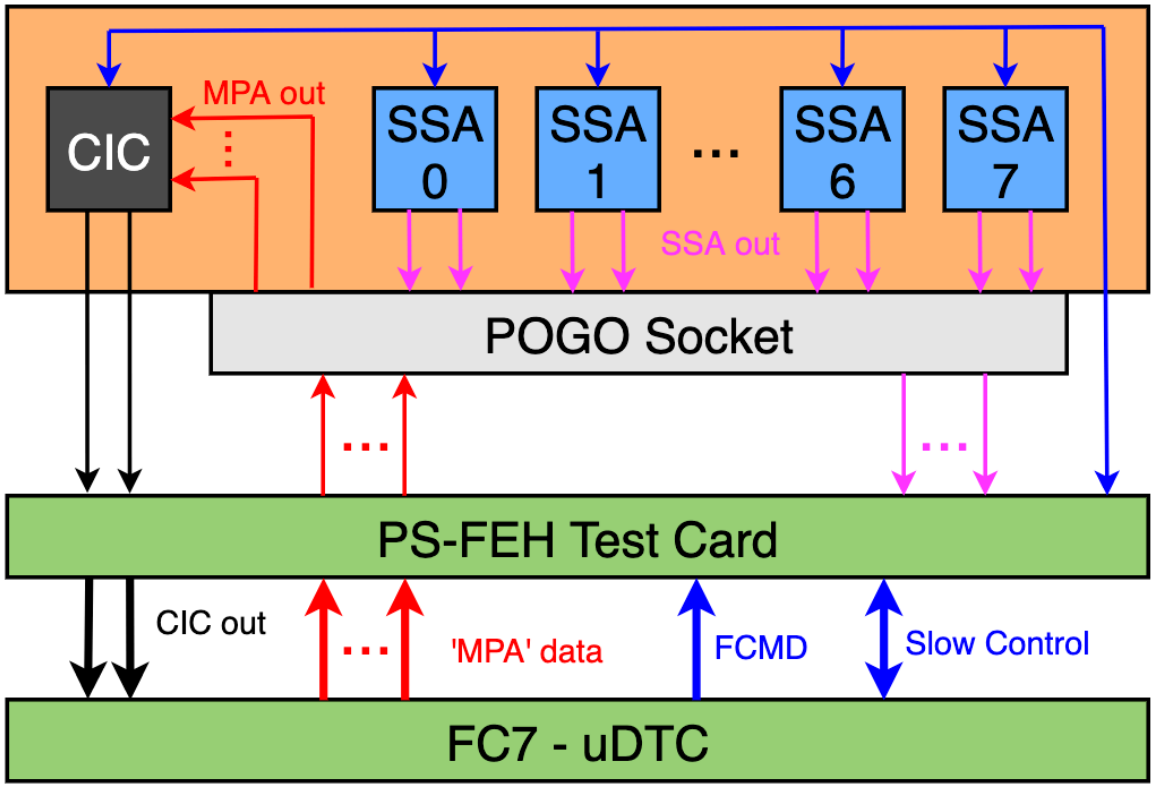




PS-FEH Firmware

FC7 (electrical readout)

- **SC/FCMD/Data CIC* blocks**
  - I2C, FCMD, Data decoder, Stub data
- **Crate multiplexing block**
  - Selection of hybrid to be powered
- **Single SSA readout**
- **SSA output clock testing**
  - Binary counters for signal rising edges
- **SSA output fast command testing**
  - FCMD pattern/payload check
- **MPA test vectors (CIC inputs)**
  - Configurable data player @320MHz / 640MHz



PS-ROH Firmware

Control FC7

- **Crate multiplexing block**
  - Selection of hybrid to be powered
- **Clock testing**
  - Binary counters for signal rising edges
- **Fast command testing :**
  - BRAM based test block
- **I2C Slave Interface (SC) :**
  - 18 slaves (9 per hybrid)
- **CIC test vectors**
  - Configurable data player @320MHz / 640MHz

BackEnd FC7

- lpGBT-FPGA implementation for single/multi-link
- GBT-SC (v2.0) for use of lpGBT Serial Interface
- VIO debug core