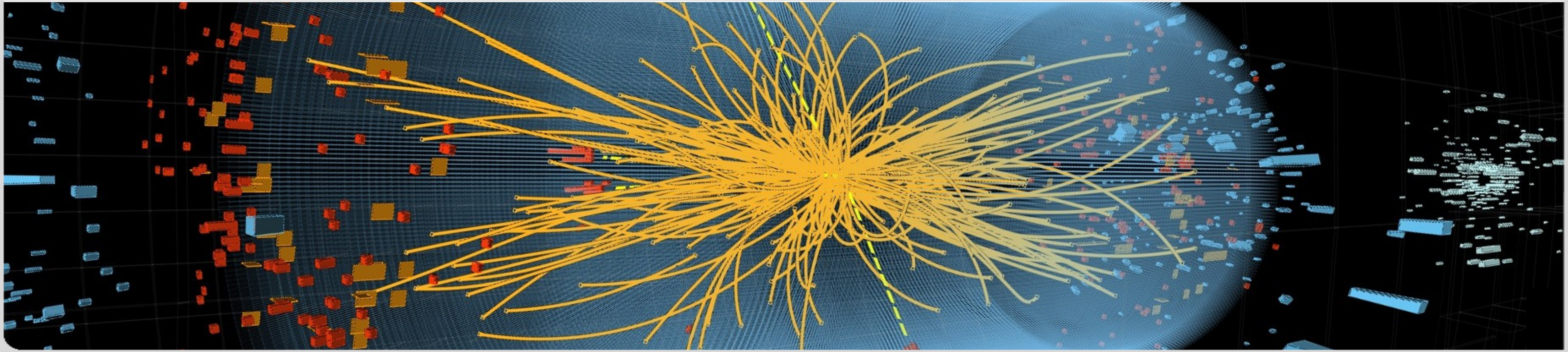
Karlsruher Institut für Technologie

HELMHOLTZ
RESEARCH FOR GRAND CHALLENGES

The CMS Tracker Back-End Electronics System for the HL-LHC

Luis Ardila, Matthias Balzer, Oliver Sander, Michael Schleicher, Denis Tcherniakhovski

INSTITUTE FOR DATA PROCESSING AND ELECTRONICS (IPE)



Agenda

Introduction: High Luminosity Large Hadron Collider (HL-LHC)

- CMS Tracker Upgrade
- Track Finder Architecture

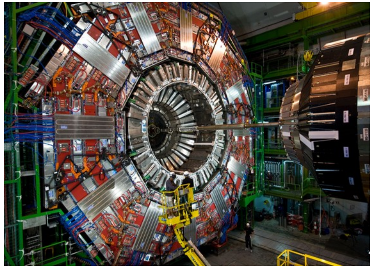
Track Finding Algorithms

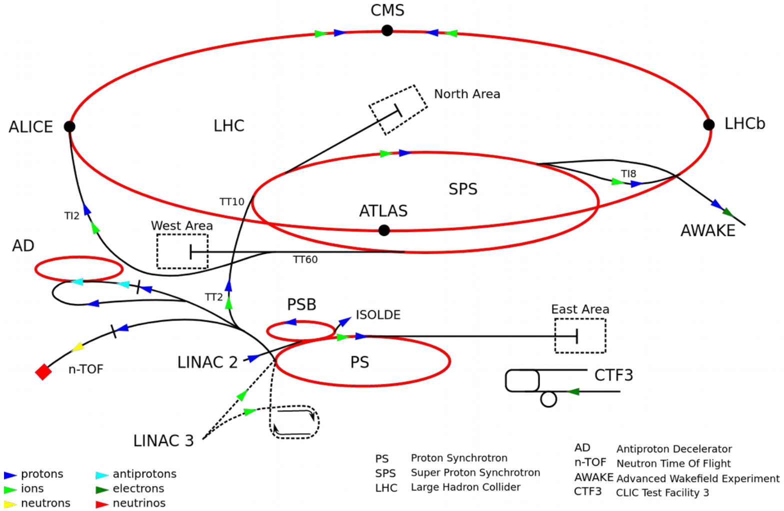
- Tracklet
- Time-Multiplexed Track Trigger (TMTT)
- Hybrid

Hardware R&D

- Hardware Prototyping Platforms
- Integrated Board Management Module

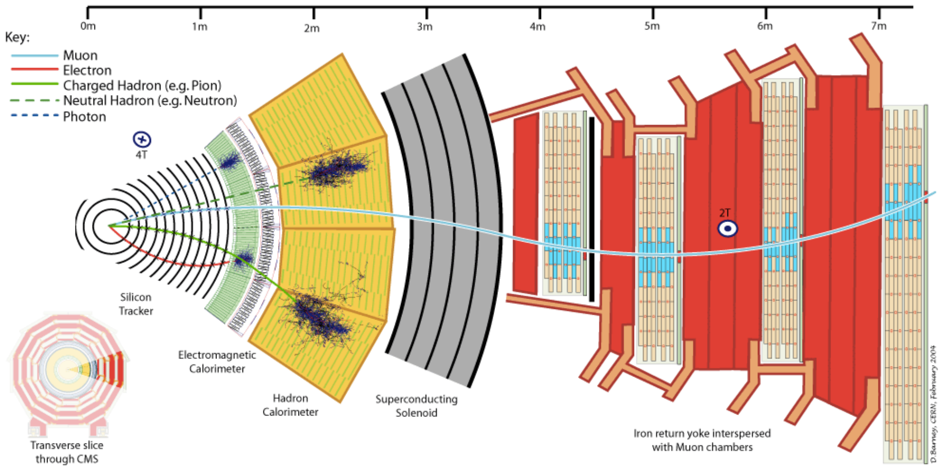
Summary

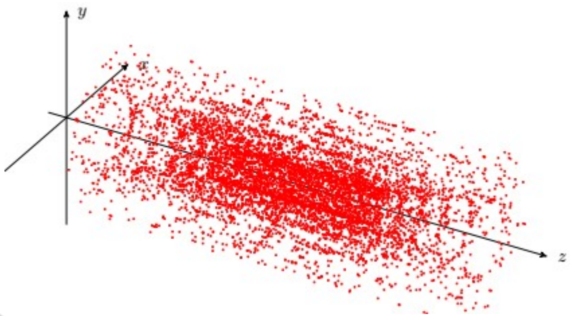


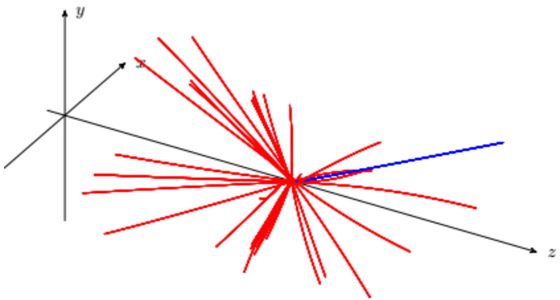


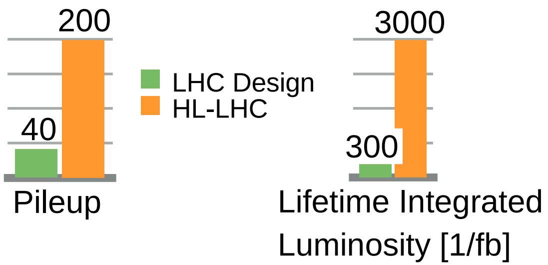
High Luminosity LHC – CMS

- By 2026 the LHC will be upgraded in luminosity   5-7 x 1034 / cm2 / s
- Silicon strip tracker will be replaced
- Challenging high occupancy conditions. ~10,000 charged particles per bunch crossing
- Necessary to include tracking information at first level of triggering









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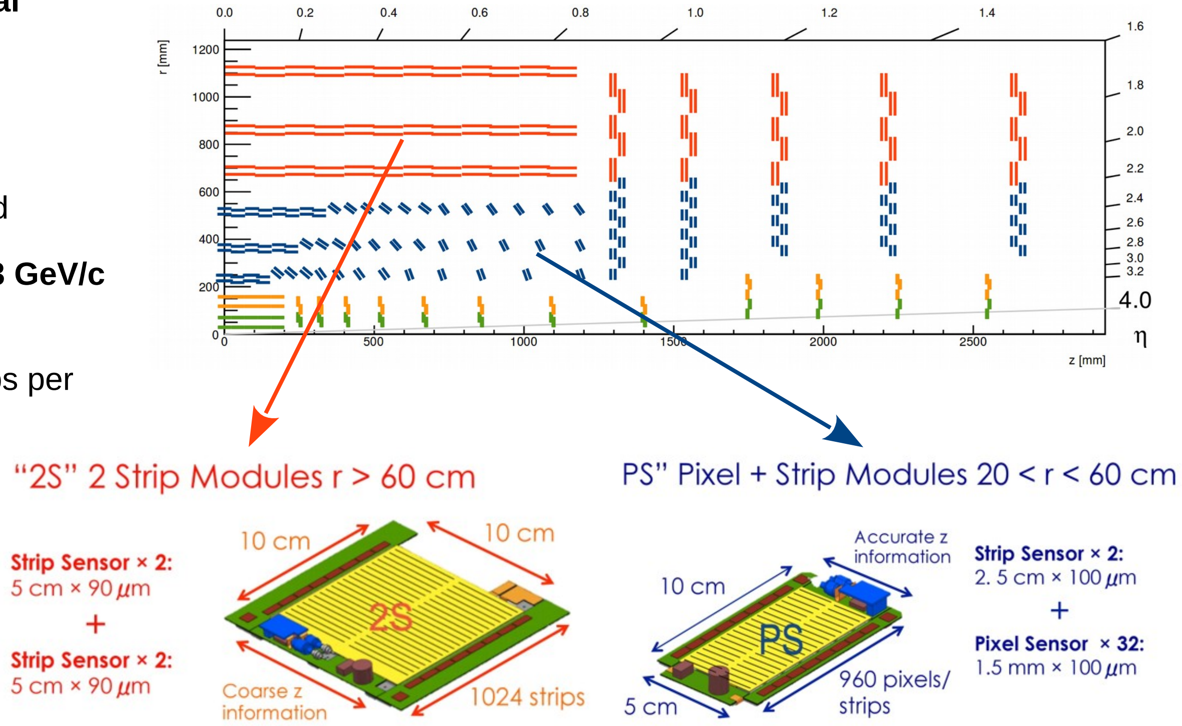
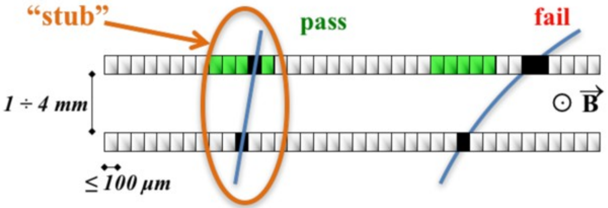
CMS Tracker Upgrade

p_T discrimination provided by use of special modules

- Pairs of closely spaced silicon sensors, separated 1.6 - 4 mm
- Signals from each sensor are correlated
- Only hit pairs compatible with **p_T > 2 – 3 GeV/c (“Stubs”) are forwarded off-detector**
- Factor ~10 data reduction ~15,000 stubs per bunch crossing





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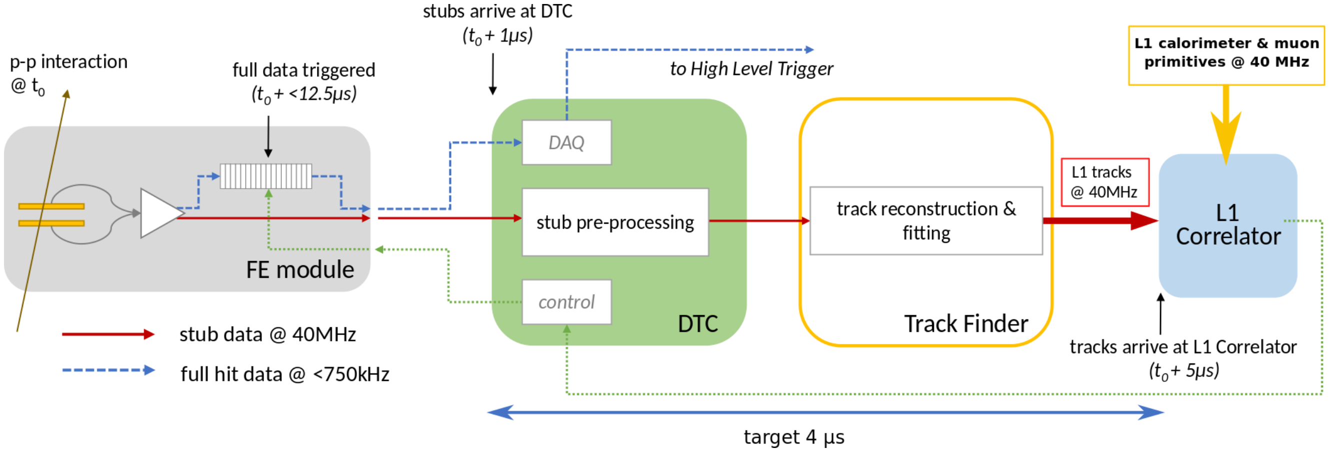
Tracker → Trigger Data Flow



Average 15,000 stubs every 25ns (200PU) → **Stub bandwidth O(20) Tb/s**

L1 hardware trigger reduces event rate from **40 MHz to < 750 kHz** using calorimeter, muon and tracker primitives

- **Tracker primitives are all tracks (pT > 2-3 GeV/c) from Outer Tracker**
- L1-Accept triggers all front-end buffers to read out to DAQ → HLT farm

FE L1 latency buffers limited to 12.5 μs

Transmission of stubs to back-end electronics	1 μs
Correlation of trigger primitives (inc. tracks)	3.5 μs
Broadcast of L1-Accept to front-end buffers	1 μs
Safety Margin	3 μs

- Track finding from stubs must be performed in 4 μs

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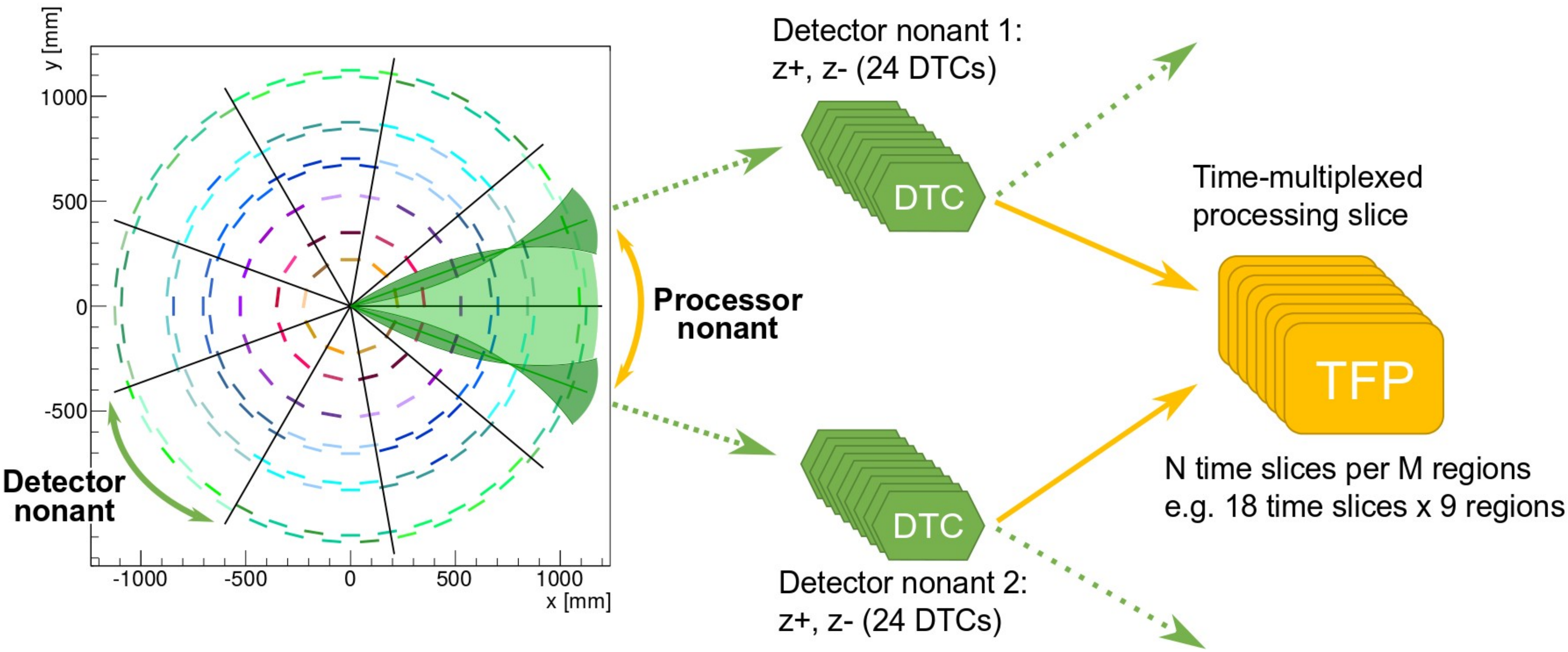
Track Finder Architecture



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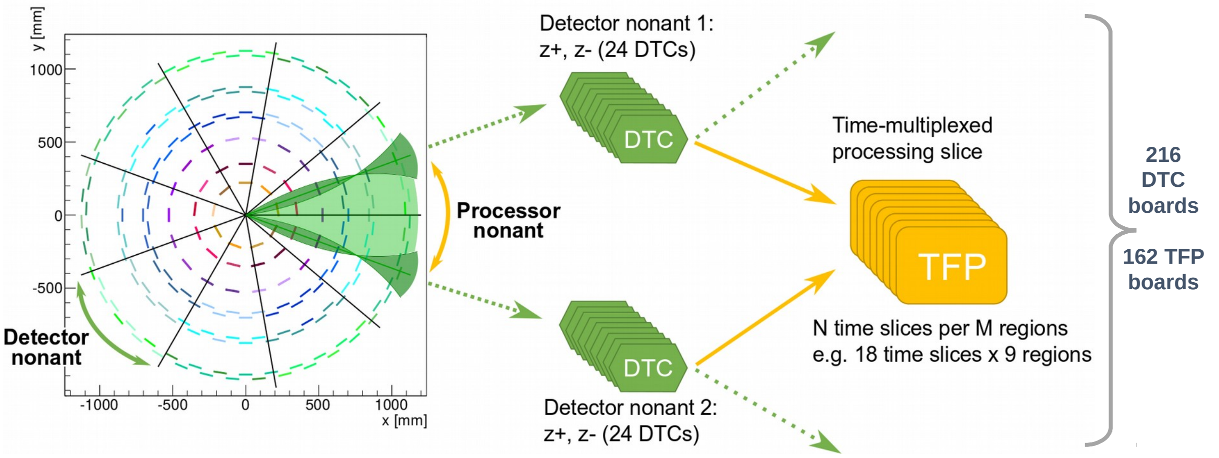


Outer Tracker cabled into **nonants**

Use of time-multiplexing to increase parallelization

- Time-multiplexing directs data from multiple sources to a single processing node
- **1 bunch crossing per processing node**

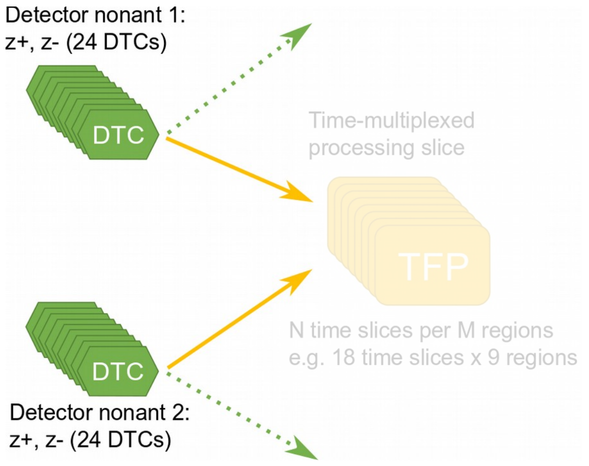
Processors are independent entities → simplifies commissioning and operation

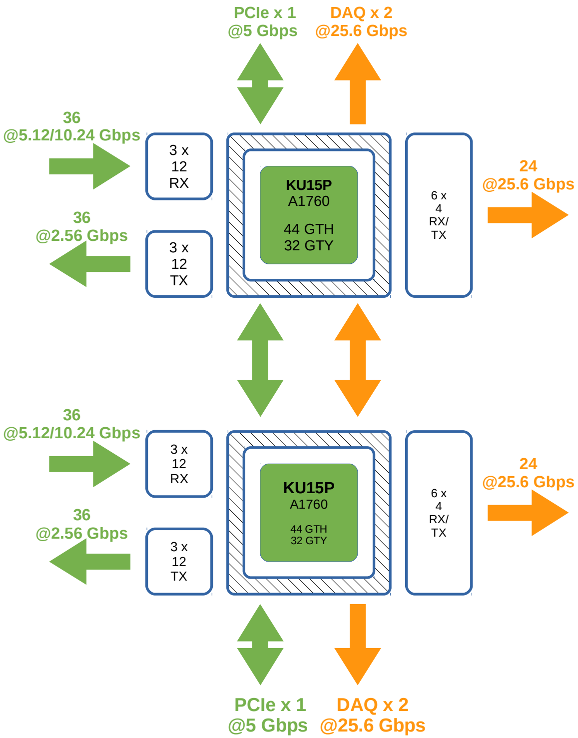
Spare nodes available for redundancy

Two stages of data processing

- **Data, Trigger and Control (DTC) layer**
- **Track Finding Processor (TFP) layer**
- **All-FPGA** processing system
- **ATCA** form factor; CMS standard dual-star backplane

Track Finder Architecture – DTC





DTC card must handle

- **<=72 modules (5G/10G lpGBT opto-links)**
- Control/Readout for each module
- Direct L1 stream to central DAQ (16G/25G)
- Direct stub stream to TFPs (25G)

Stub pre-processing includes:

- **Local** → **Global** look up, position calibration
- Sort and pre-duplication
- Time-multiplexing

→ **216 DTC boards, 18 crates, 1 rack/nonant**

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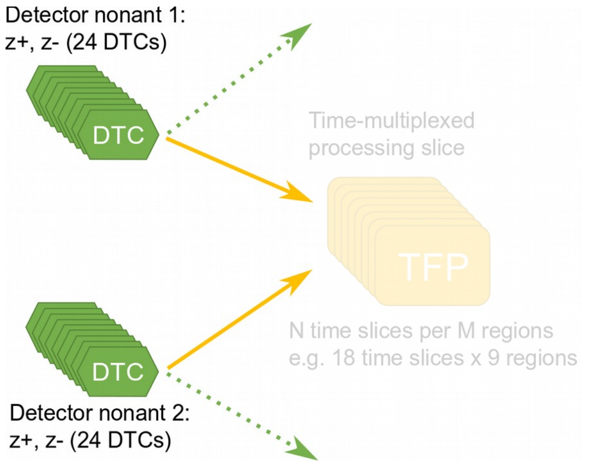
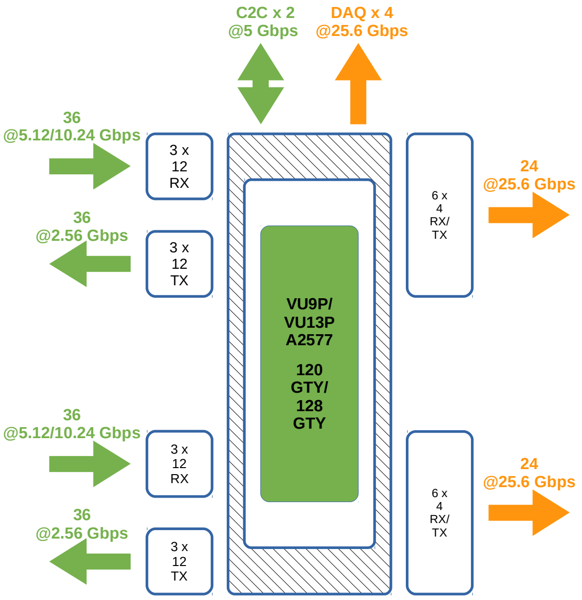
Track Finder Architecture – DTC





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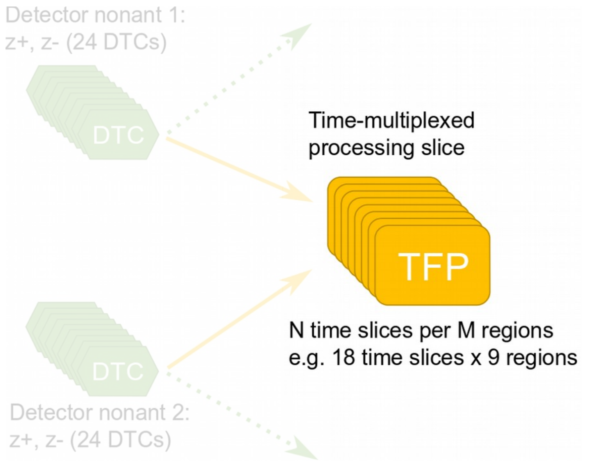
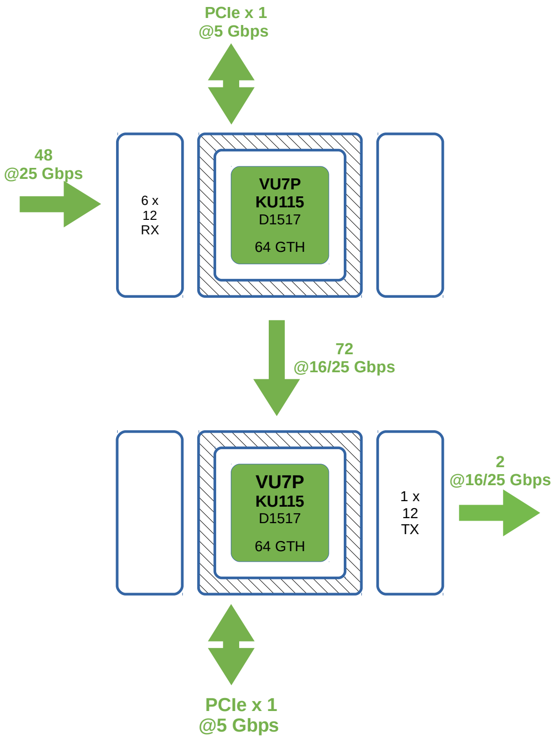
Track Finder Architecture – TFP





TFP card must handle

- **Up to 48 DTCs (25G optical links)**
- Track Finding from stubs
- Track Fitting
- Transmission to L1 Correlator Trigger

High bandwidth processing card

- **~1 Tb/s** processing bandwidth
- Rate to L1 Correlator much lower < 30 Gb/s

→ **162 TF boards, 18 crates (one per time-node)**

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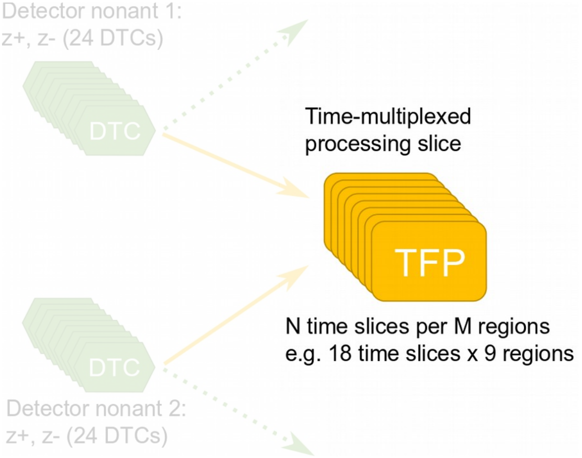
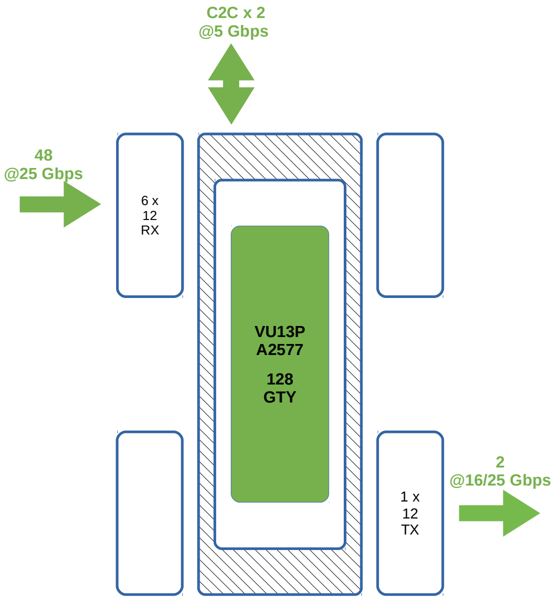
Track Finder Architecture – TFP





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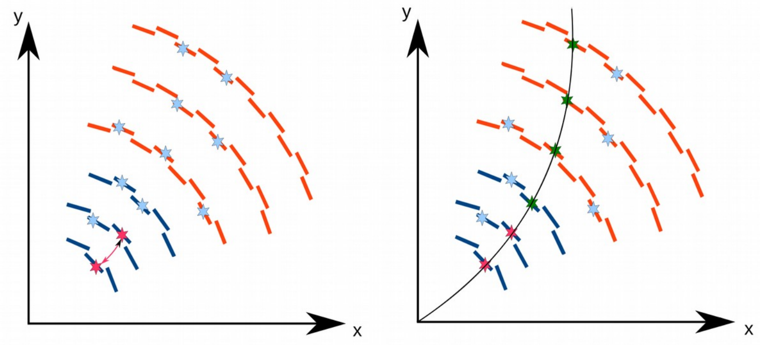
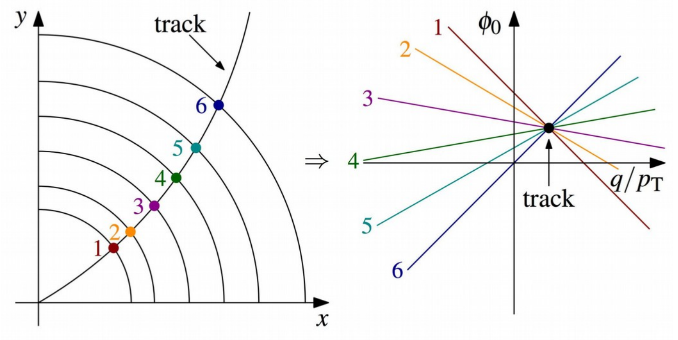
Track Finding Algorithms

Two main algorithms for reconstructing tracks, plus a number of hybrids, variation and options





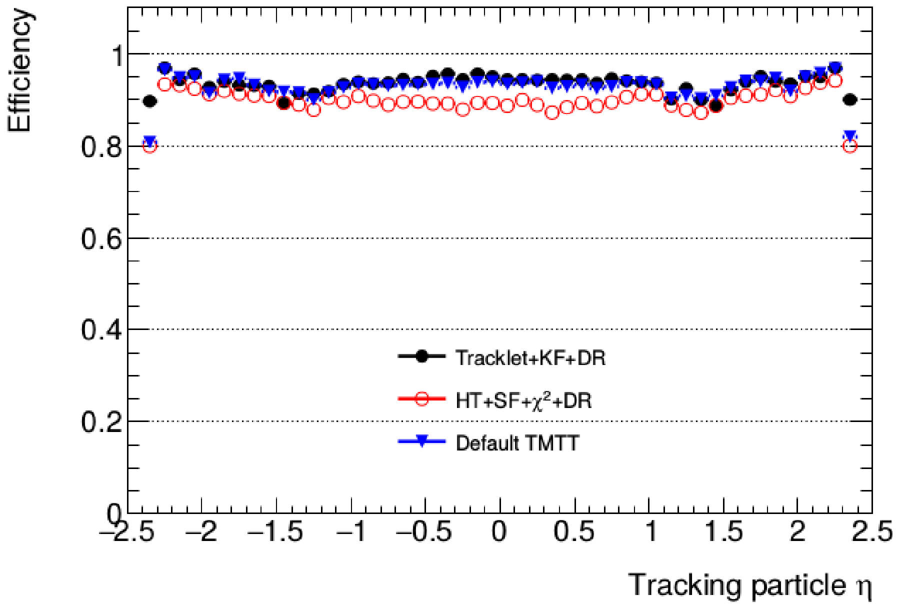
TRACKLET + CHI2 FIT APPROACH

- Combinatorial approach using **pairs of stubs as seeds**
- **Extrapolation** to other layers → hit matching
- **Linearized χ2** fit on candidates
- Uses **full resolution stubs** at earliest stage of processing
- N time-slices x M regions → 6 x 24, 9 x 18

HOUGH TRANSFORM + KALMAN FILTER APPROACH

- Uses a **Hough Transform** to detect coarse candidates
- Candidates are filtered and fitted in a single subsequent step using a **Kalman Filter**
- Combinatorial problem pushed to latter stages of processing
- N time-slices x M regions → 18 x 9

Hybrid Comparison



Efforts towards **merging** the two approaches, working on defining a **reference algorithm** with the best from both.

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Hybrid Performance

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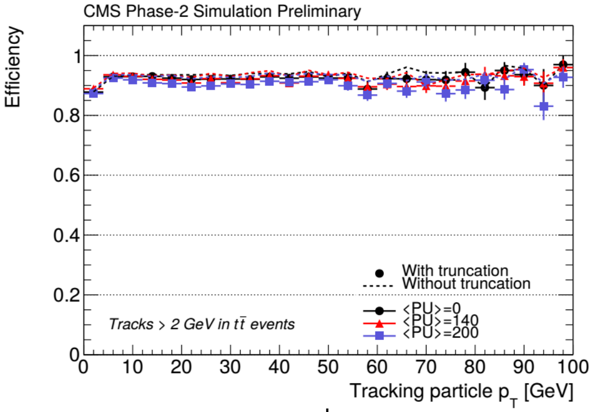
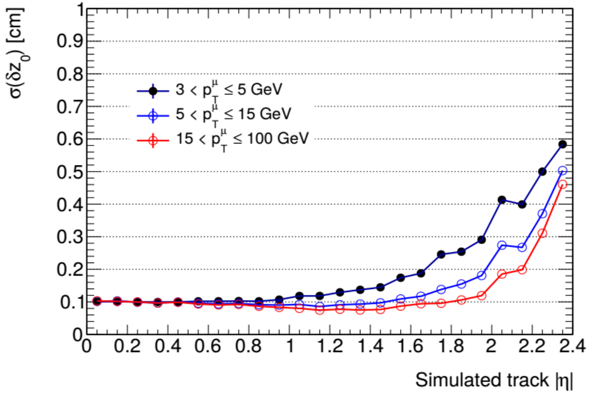
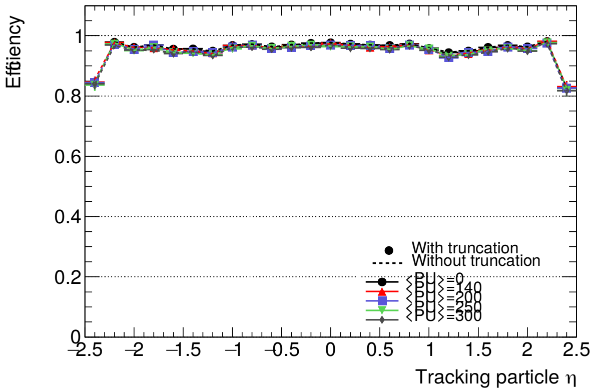
- Average track finding **efficiency** for $t\bar{t}$ tracks **> 95% (> 3 GeV)**
- **z_0 resolution ~1 mm** (barrel)
- **p_T resolution ~1%** (barrel)
- Per event average **~60 tracks (3 GeV) ~200 (2GeV)** ($t\bar{t}$ at 200 PU)

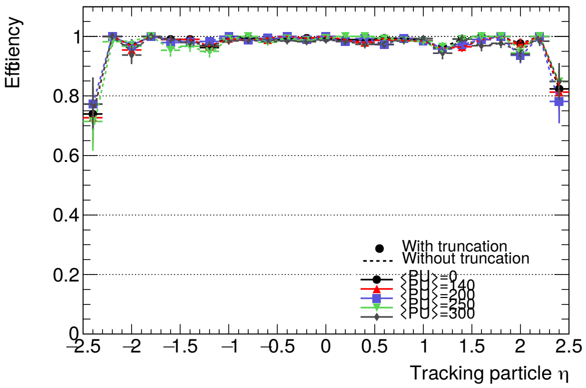




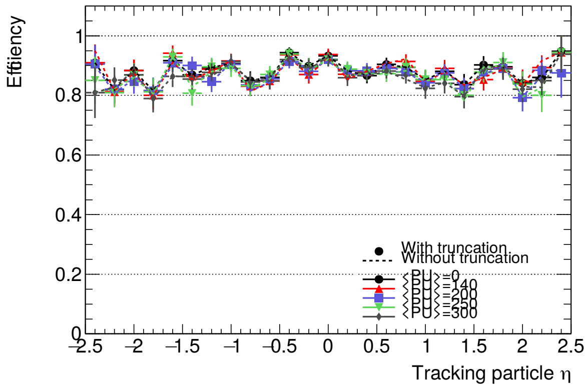
tt



$\mu^+\mu^-$

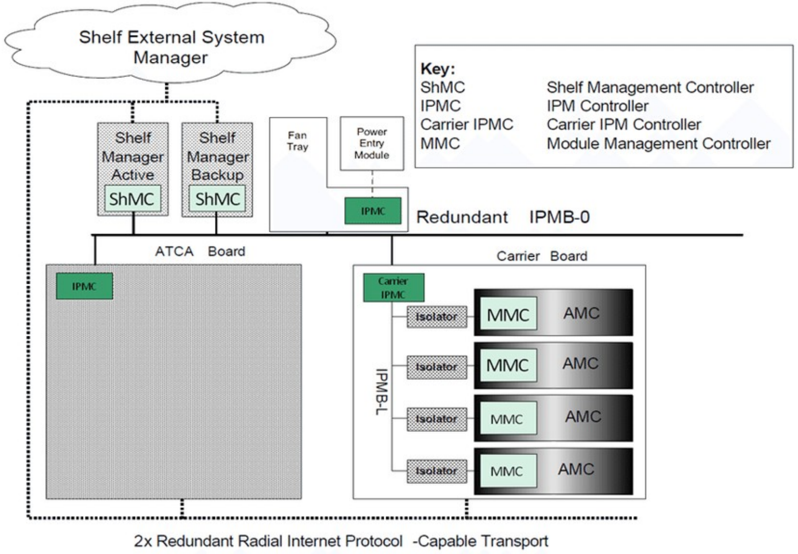


e^+e^-



Hardware R&D: ATCA

Advanced Telecommunications Computing Architecture (ATCA)



280 x 322 mm
board size

All CMS Phase-2 back-end electronics will be ATCA-based

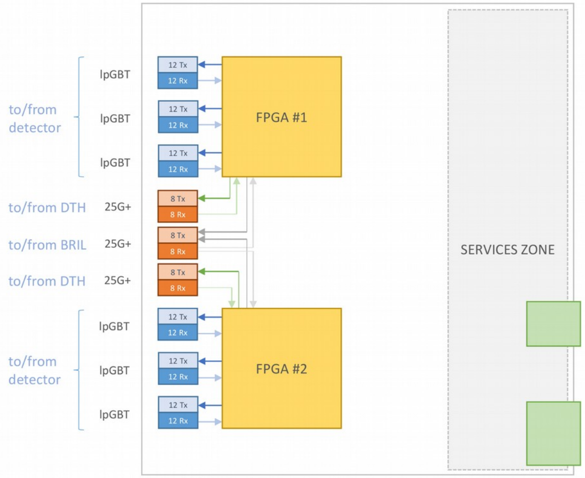
- Dual-star backplane

Standardized the use of the backplane for Ethernet, clocks, and timing & throttling signals

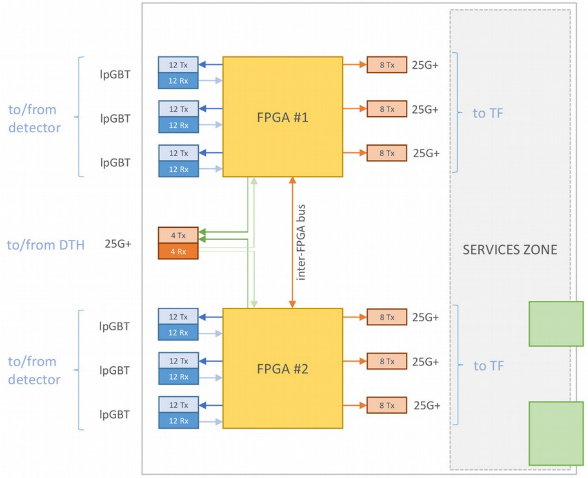
- LHC bunch-crossing clock (**40.08MHz**)
- Precision crossing clock (**320.64MHz**)
- TTC2 trigger and fast-control stream (from DTH to back-ends)
- TTS2 throttling stream (from back-ends to DTH)

The three Back-End Boards

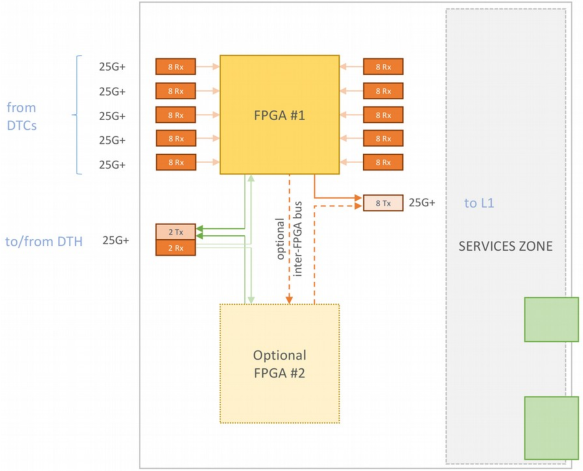
IT-DTC



OT-DTC



TF



Tracker_EOWorkshop_270618

HW – R&D: Apollo V1

Apollo uses coplanar PCBs with Back-Plane Connectors in between

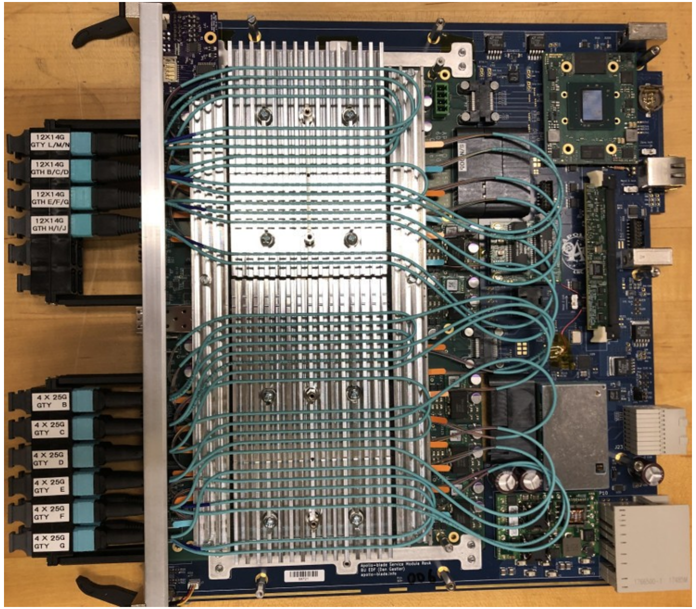
- Flexibility (e.g. FPGA+Optics)
- Modularity; separate complex and simpler part of the board design

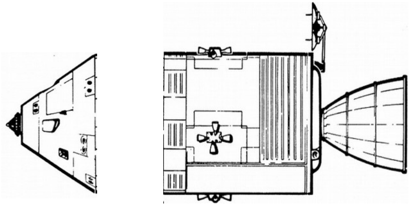
On-board computing and control variety

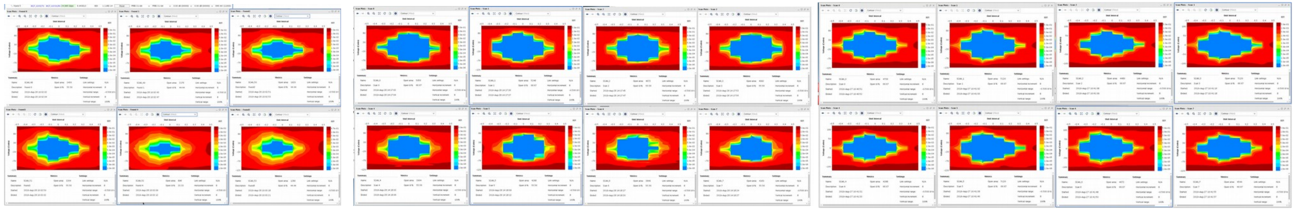
- Zynq SoC
- CERN-IPMC or UW-IPMC or OpenIPMC

PCB Characteristics:

- 16 layers / Megtron-6 / 1.8 mm
- 12 layers / FR4 / 2 mm
- Apollo analogy: Split into “Command” and “Service” modules







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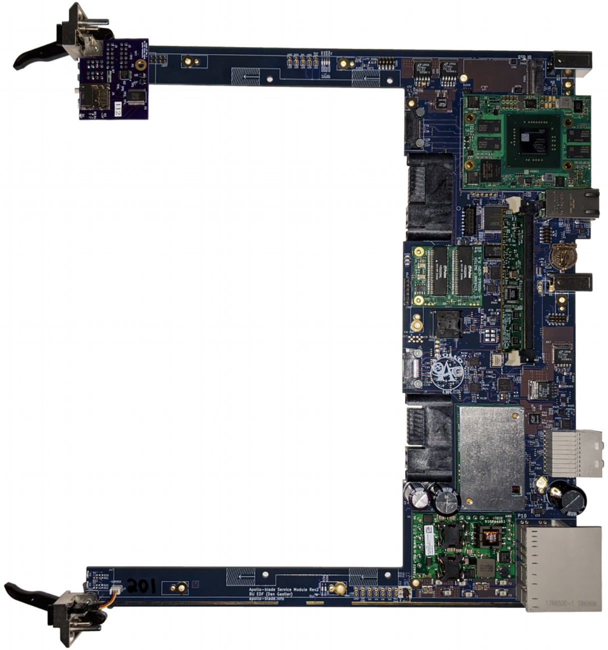

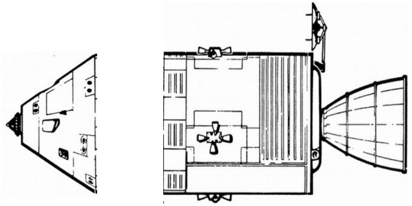

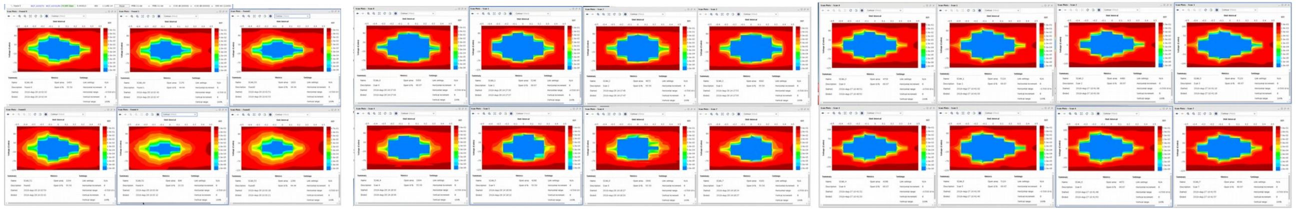

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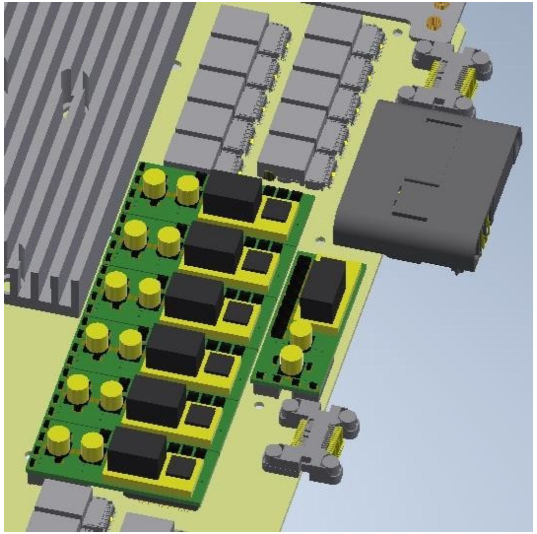
HW – R&D: Apollo V2

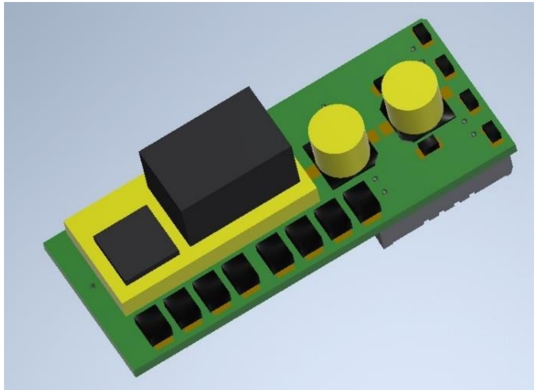
Power Supplies

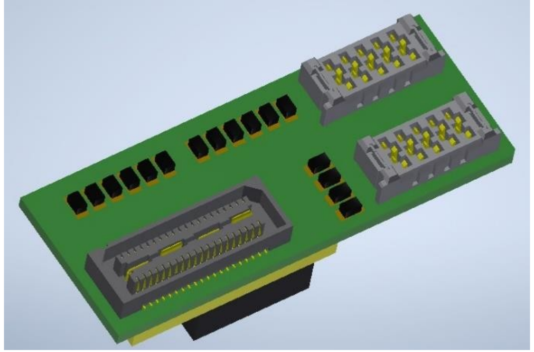
- First revision had a problematic power supply (IND072) converter-on-module
- Use same supplies as core power (LGA80D)
- Make pluggable power modules (improve repairability, greatly decrease main board parts count)

Clock Distribution

- Provide two GTY “REFCLKs” to every GTY quad (one from oscillator, other from SM) to operate DAQ even when LHC clock is ramping up
- All external clocking/timing signals from SM







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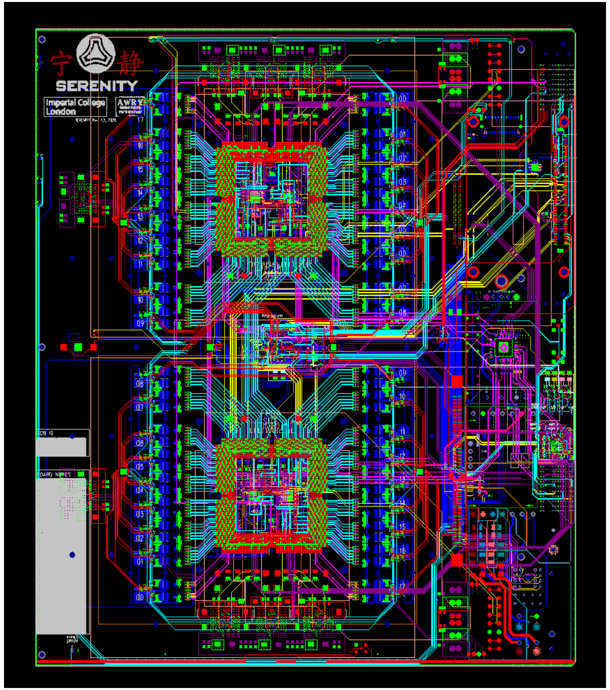
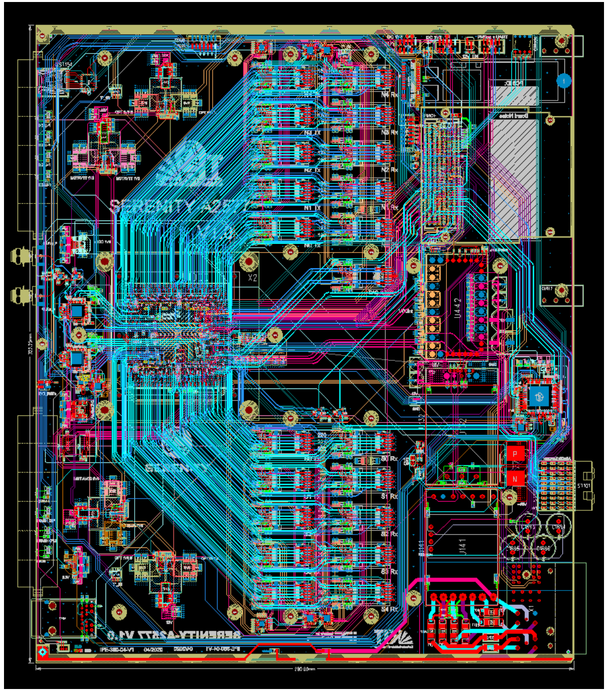
HW – R&D: Serenity

Serenity-Z-V1.2



Serenity-A-V1.0



HW – R&D: Serenity-Z

Bristol University, Imperial College, Ioannina, INFN, KIT, RAL, SACLAY, TIFR

ATCA infrastructure

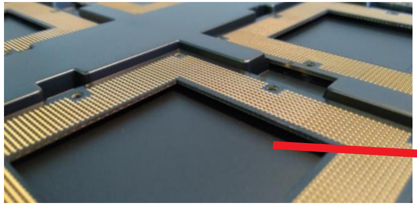
- Systematic **thermal studies** about air cross-section and impact on opto-lifetime
- Backplane signal integrity → important for DAQ/timing

Use of **interposer technology**

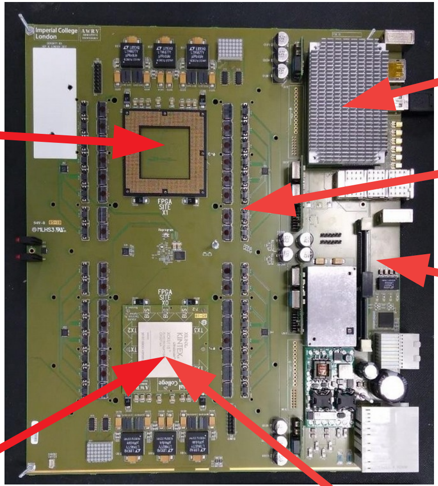
- Flexibility (e.g. FPGA)
- Mitigate losses/costs due to yield issues
- **Modularity**; separate complex and simpler part of the board design

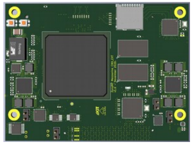
On-board computing and control variety

- Standard on-board PC (COM Express mini)
- ZynqUS+ SoC
- Intelligent Platform Management Controller (IPMC)



Samtec Z-RAY interposer





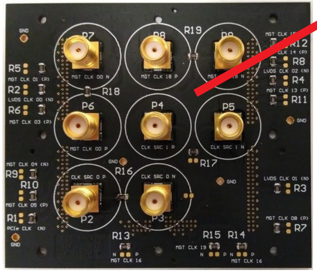
COM Express or ZynqMP

Samtec Firefly x12 RX/TX pairs

133 x 30 mm

CERN-IPMC Or OpenIPMC

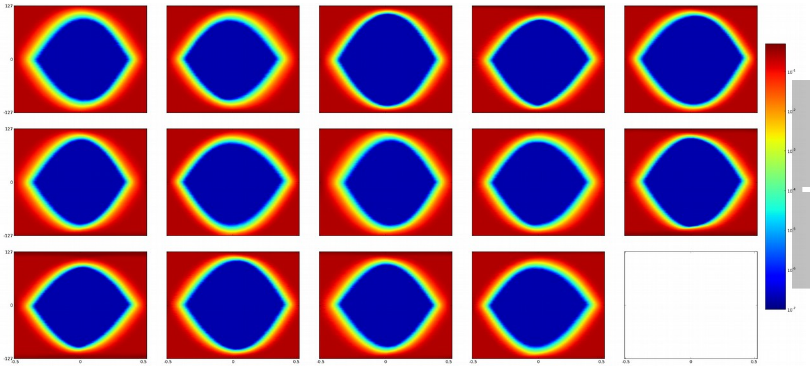
Clock test daughtercard



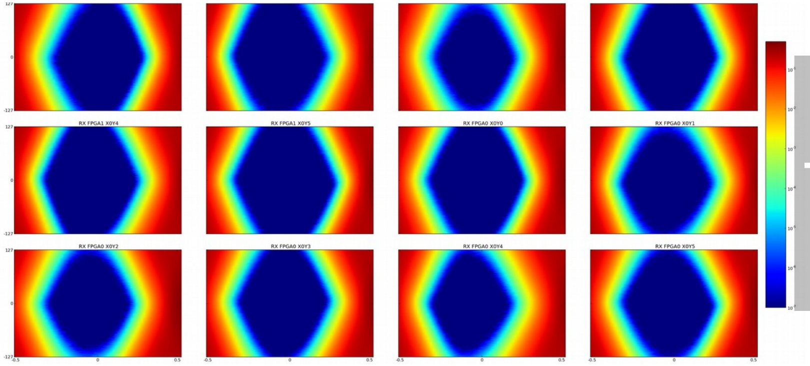
FPGAs
KU115
KU15P
VU9P
daughtercards

HW – R&D: Serenity-Z

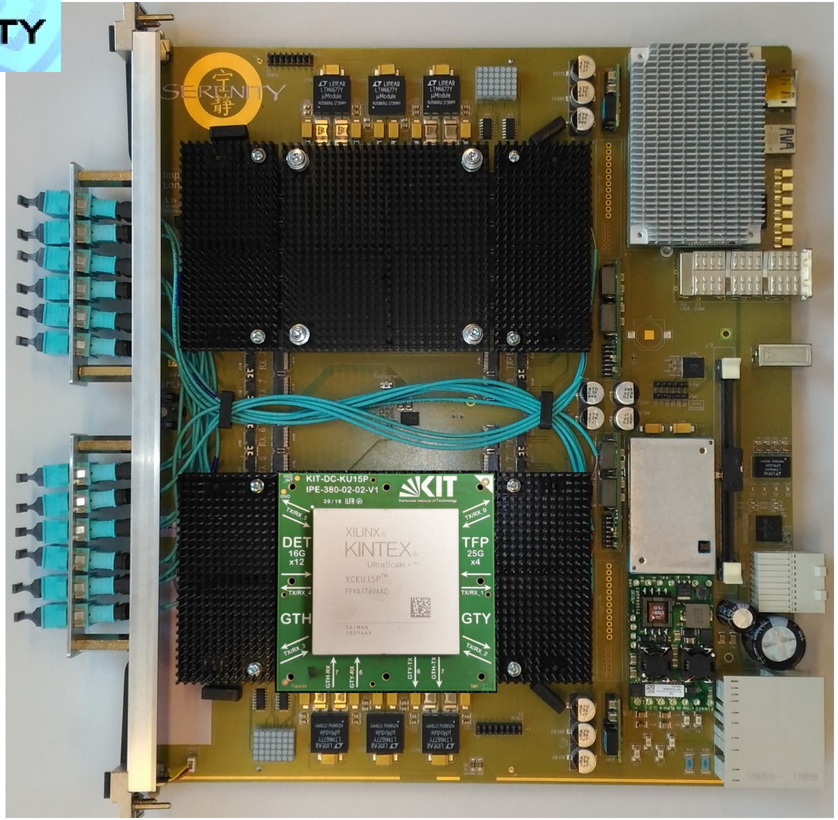
DUAL KU15P



16 Gbps



25.6 Gbps



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HW – R&D: Serenity-Z

SERENITY

2x DUAL KU15P

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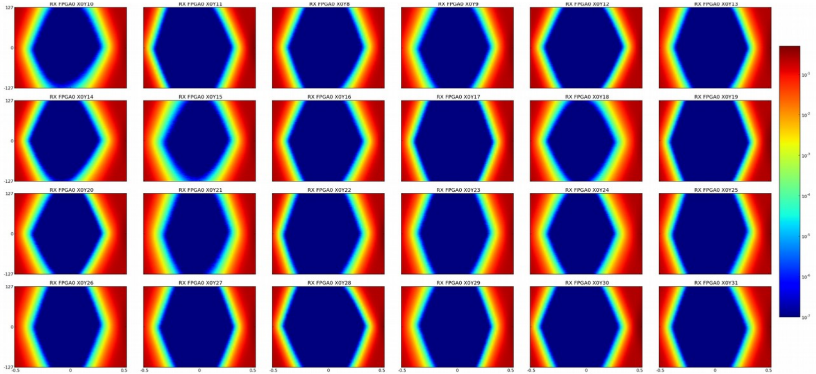
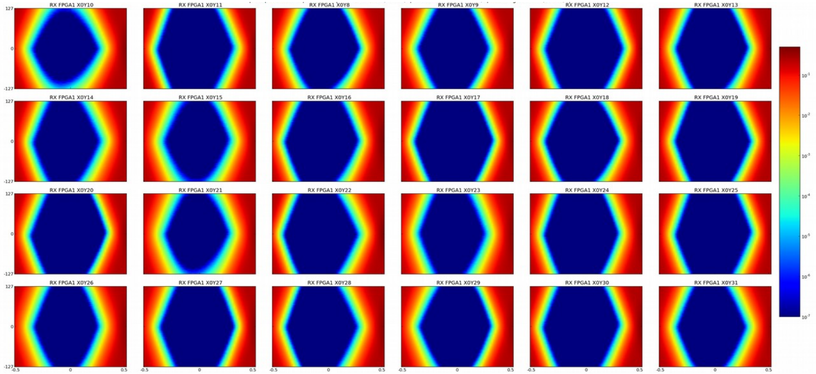
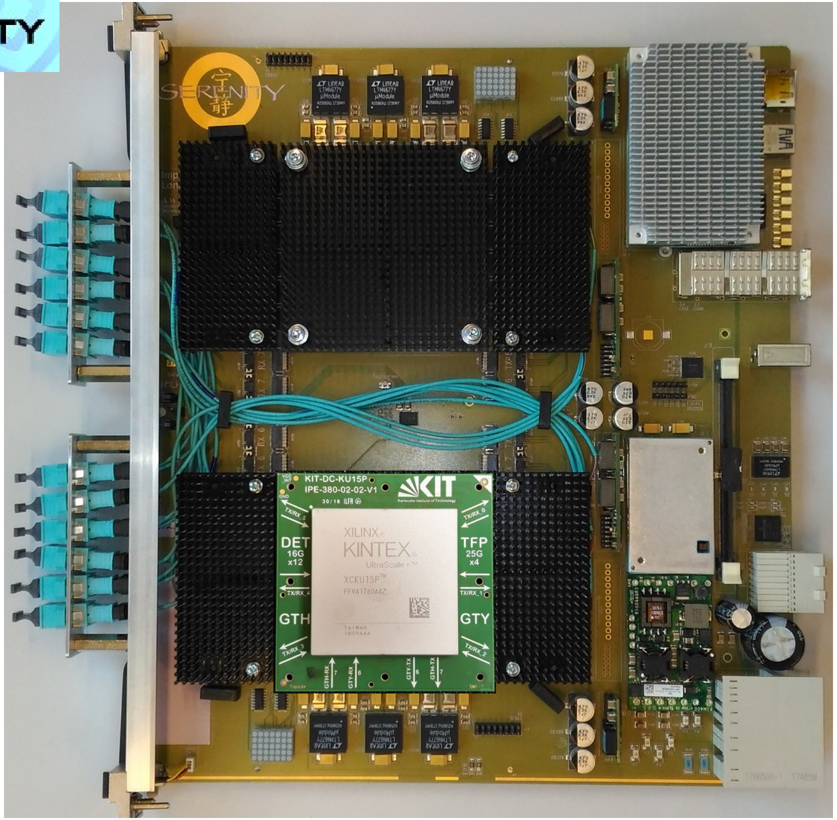


25.6 Gbps



25.6 Gbps



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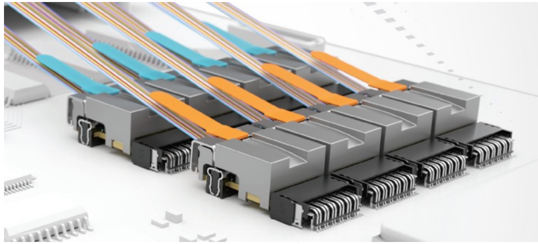
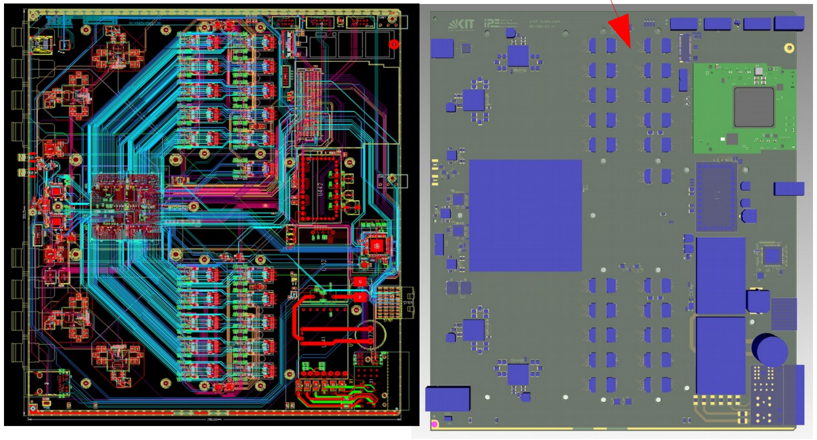
HW – R&D: Serenity-A2577



- **One FPGA** design using VU9P / VU13P with up to 120/128 GTY links
- TCDS2 backplane signals **directly routed** to main FPGA
- 10 Firefly sites with 12x TX or RX and one 4x-Bidir, all 25 Gbps capable
- FMC+ management module



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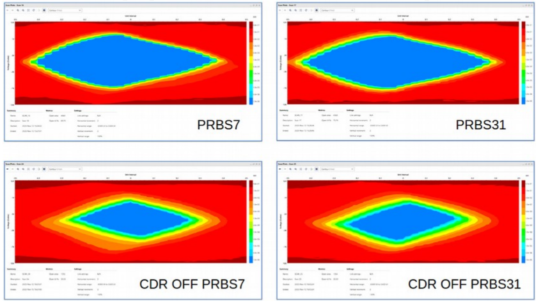
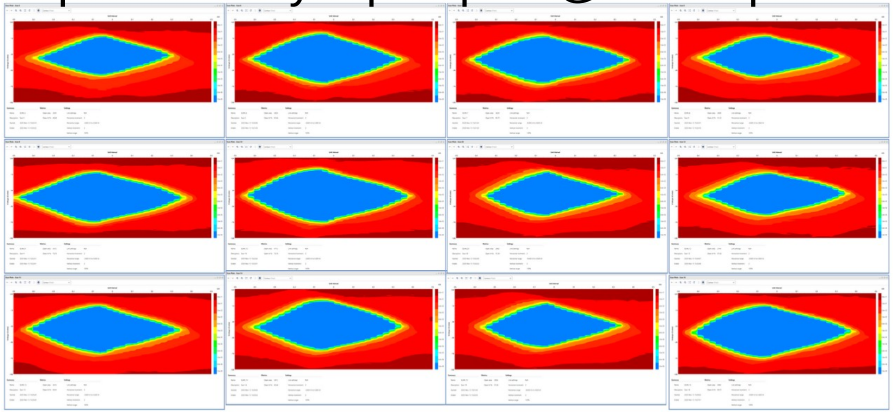
HW – R&D: Serenity-A2577

Copper @ 25 Gbps



Optical Firefly Alpha part @ 25 Gbps



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HW R&D: ZynqMP management modules

Karlsruher Institut für Technologie

CMX-EXT module

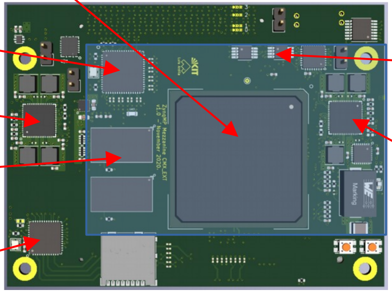
ZU4EG-B900

Si5395

IRPS5401 PMIC

2G DDR4

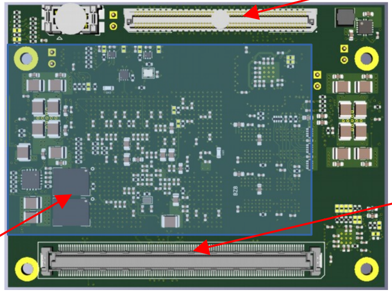
KSZ9031 ETH PHY



I2C IPMC I/O

IRPS5401 PMIC

QSPI FLASH



12 PL MGTs

4 PL MGTs
4 PS MGTs

FMC+ module

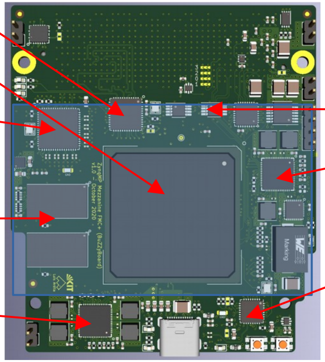
KSZ9031 ETH PHY

ZU4EG-B900

Si5395

2G DDR4

IRPS5401 PMIC

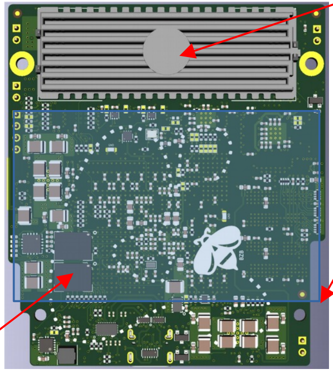


I2C IPMC I/O

IRPS5401 PMIC

USB PHY

QSPI FLASH



16 PL MGTs
4 PS MGTs

Highlighted area is common between them

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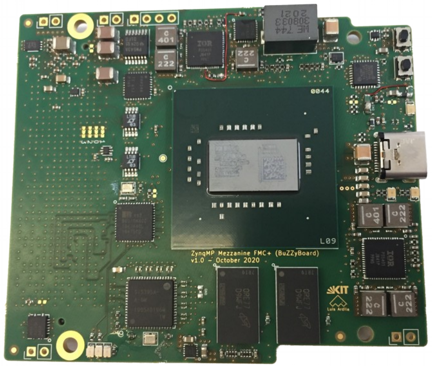
HW R&D: ZynqMP management modules

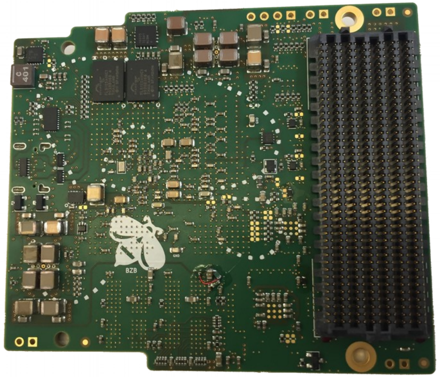


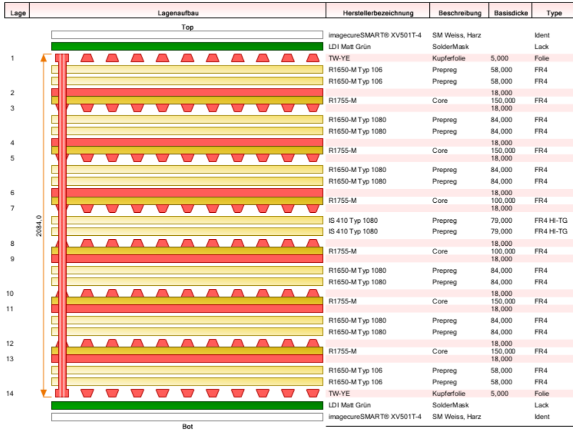
Features

- 2mm thickness, 14 layer, impedance controlled traces
- 4 routing layers enclosed by solid GND planes
- 2 power planes
- Fabricated in FR4 with 22.5 degree rotation

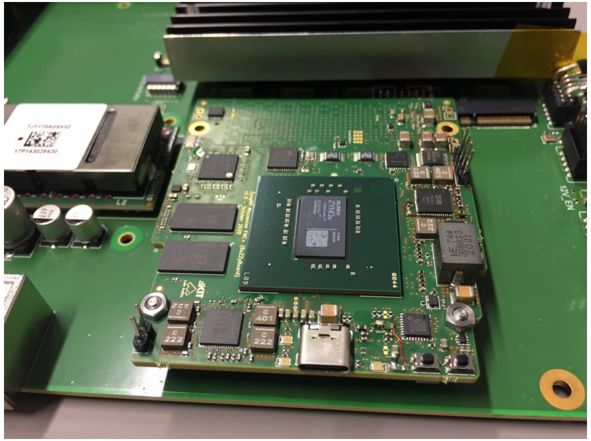
Status

- One board was assembled without ZynqMP to test power regulator configurations
- Second board fully assembled yesterday, power rails tested and





Lage	Lagenaufbau	Herstellerbezeichnung	Beschreibung	Basisdicke	Type
	Top				
		imagecureSMART® XV501T-4	SM Weiss, Harz		Ident
		LDI Matt Grün	SolderMask		Lack
1		TW-YE	Kupferfolie	5,000	Folie
		R1650-M Typ 106	Prepreg	58,000	FR4
		R1650-M Typ 106	Prepreg	58,000	FR4
2				18,000	
		R1755-M	Core	150,000	FR4
3				18,000	
		R1650-M Typ 1080	Prepreg	84,000	FR4
		R1650-M Typ 1080	Prepreg	84,000	FR4
4				18,000	
		R1755-M	Core	150,000	FR4
5				18,000	
		R1650-M Typ 1080	Prepreg	84,000	FR4
		R1650-M Typ 1080	Prepreg	84,000	FR4
6				18,000	
		R1755-M	Core	100,000	FR4
7				18,000	
	2084,0	IS 410 Typ 1080	Prepreg	79,000	FR4 HI-TG
		IS 410 Typ 1080	Prepreg	79,000	FR4 HI-TG
8				18,000	
		R1755-M	Core	100,000	FR4
9				18,000	
		R1650-M Typ 1080	Prepreg	84,000	FR4
		R1650-M Typ 1080	Prepreg	84,000	FR4
10				18,000	
		R1755-M	Core	150,000	FR4
11				18,000	
		R1650-M Typ 1080	Prepreg	84,000	FR4
		R1650-M Typ 1080	Prepreg	84,000	FR4
12				18,000	
		R1755-M	Core	150,000	FR4
13				18,000	
		R1650-M Typ 106	Prepreg	58,000	FR4
		R1650-M Typ 106	Prepreg	58,000	FR4
14		TW-YE	Kupferfolie	5,000	Folie
		LDI Matt Grün	SolderMask		Lack
		imagecureSMART® XV501T-4	SM Weiss, Harz		Ident
	Bot				



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Karlsruher Institut für Technologie

Summary

- CMS **needs** tracks at L1 trigger to cope with HL-LHC pileup conditions
- p_T modules provide **first layer** of efficient **data reduction**
- **Highly flexible** track-finder/pattern recognition algorithms were demonstrated in hardware
- **Highly scalable**, time/physical segmentation could be as large/small as required based on data rates
- **Proven** with **currently available hardware**, that a level-1 track-trigger based on **FPGAs** is **feasible**
- Lots of **flexibility** with an **all-FPGA solution**

Common infrastructure Hardware R&D

- Current prototypes showed very good **optical performance**, even at 25 Gbps
- Evaluation of other optical drivers is planned in the future
- New **interposer technology** has proven to be **reliable** regarding **signal integrity**, brings simplification and flexibility to the motherboard
- **Soldering reliability** of power-on-modules is a concern, its high mass makes them incompatible with standard processes. PSU with connector could alleviate yield concerns
- **Integrated** IPMC functionality on a single SoC mezzanine is an attractive possibility, a **self-designed** SoC module is an insurance for its future **availability**

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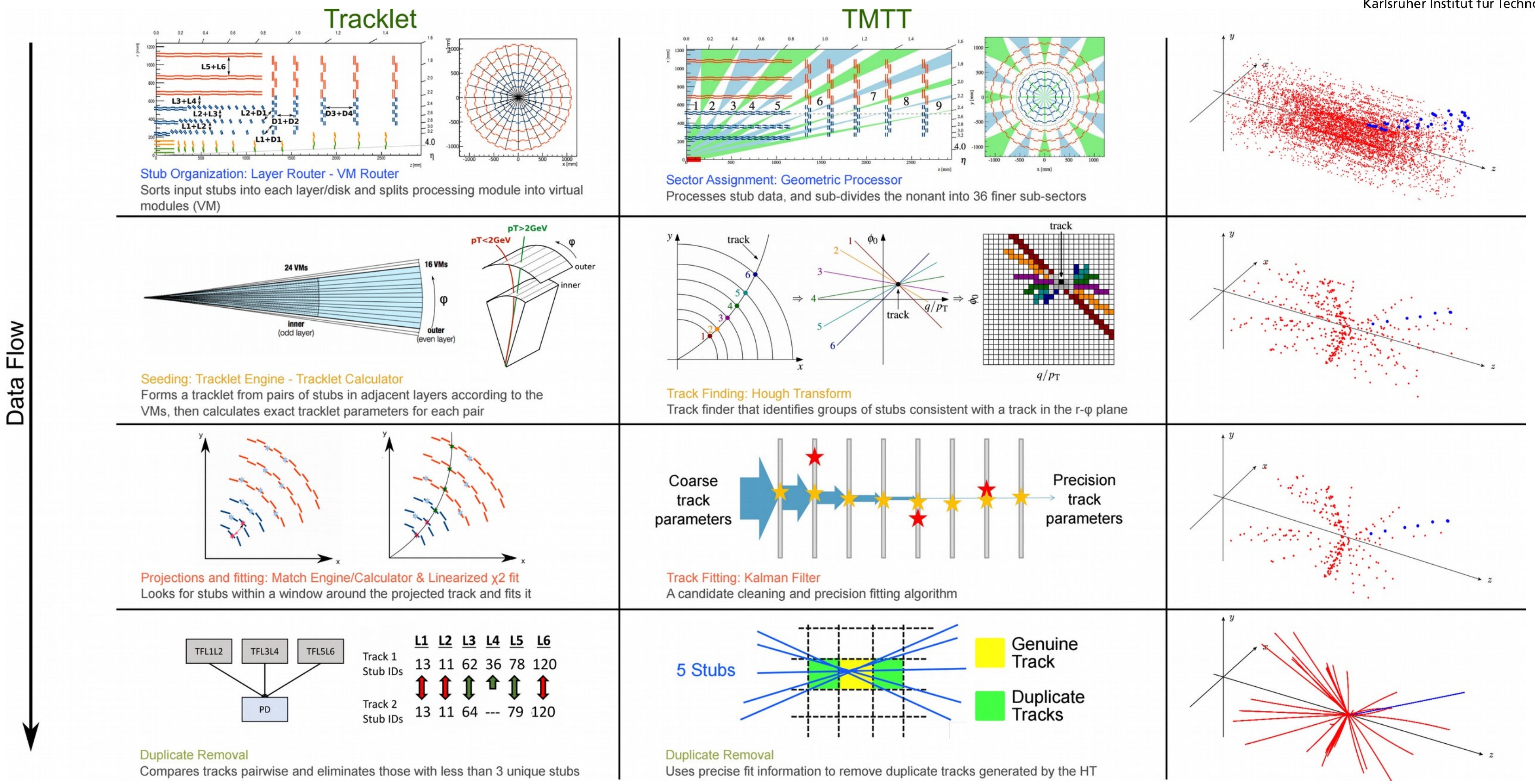
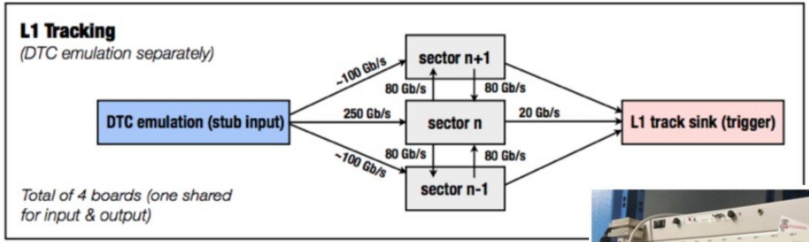
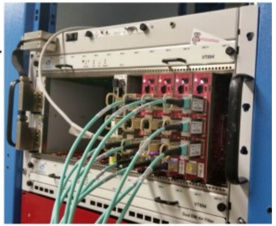
Track Finding Algorithms



Hardware Demonstrators - 2016

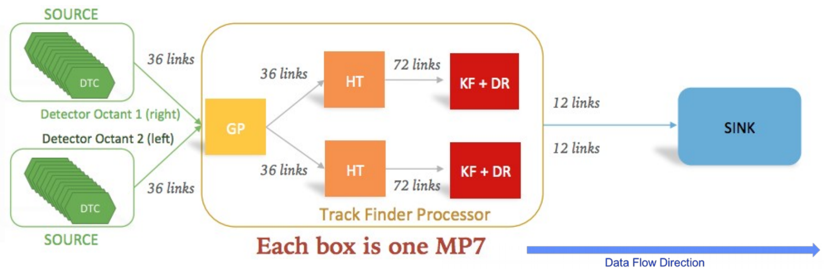


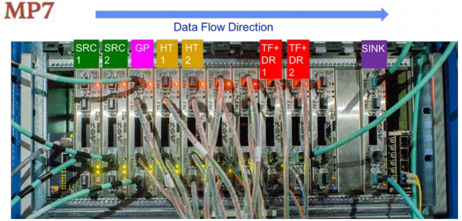


Half a barrel demonstrator in hardware, verified using emulation software

Hardware demonstrator has been built to validate the algorithm and measure latency

- 4 CTP7 boards with Virtex-7 FPGA – 3 CTP7 cover 3 Φ sectors – 1 CTP7 emulate DTC
- 1 AMC13 card for clock and synchronization
- 240 MHz internal fabric speed
- Measured latency of **3.33 µs** in agreement with latency model – without duplicate removal step





Both Demonstrators were tested with samples from PU 0 → 200

Demonstrator in hardware and emulation

- One per time multiplexing and detector nonant
- Each box is one MP7 board with Virtex-7 FPGA
- Can compare hardware output directly with software
- 240 MHz internal fabric speed
- Latency verified to be **3.5 µs**

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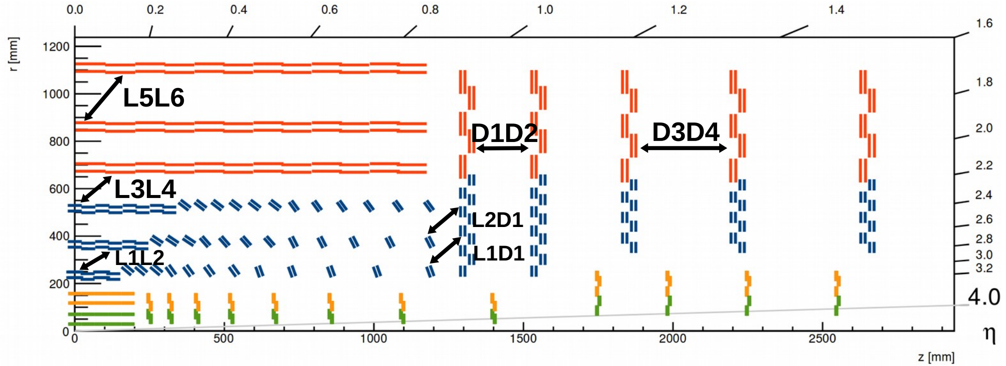
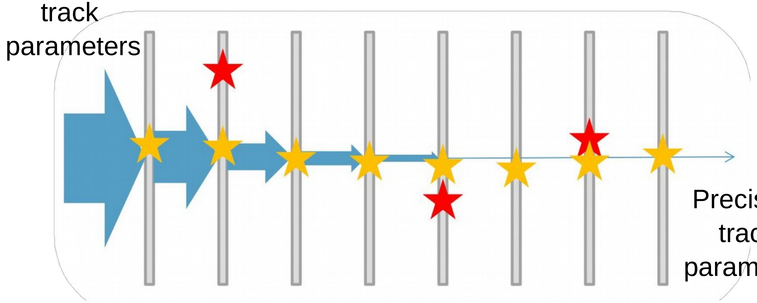
Hybrid Algorithm

Tracklet Seeding + Kalman Filter





1. Tracklet Seeds formed in multiple layer combinations

2. Projection and match in other layers

3. Candidates sharing stubs are merged

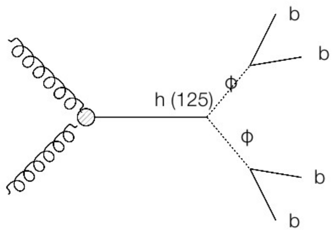
4. Kalman Filter fits track and selects best stubs candidates

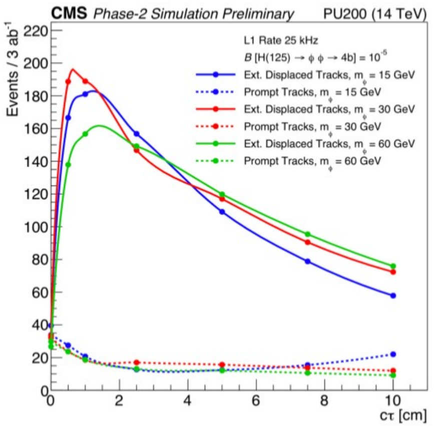
- 9 Φ sectors
- No η division
- Time-Multiplex Period of 18

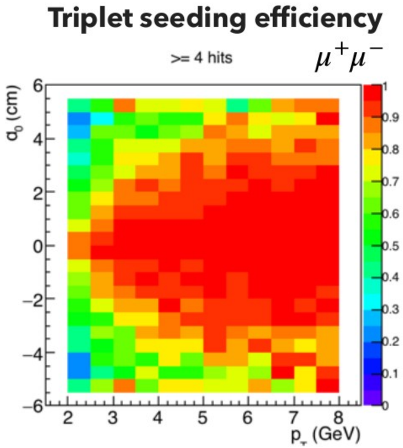
Displaced Track Finding

http://cds.cern.ch/record/2647987

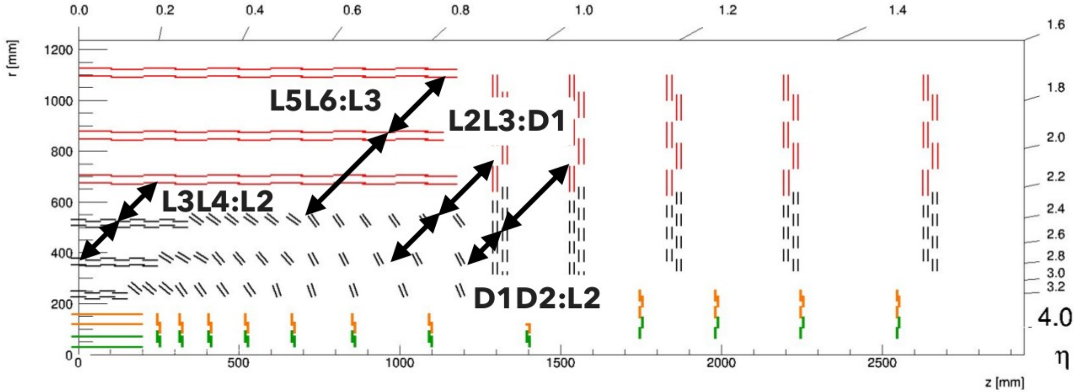
- **Motivation**
  - Lots of **interesting physics** with displaced tracks e.g rare Higgs decay to a long lived (dark matter) ϕ (~no background)
  - Alternative to **expensive dedicated experiments**







- **Challenges**
  - No beam point constraint -> higher (but manageable) fake rates
  - **Increased processing requirements** - truncation vs FPGA resources
- **Adaptations**
  - Seed with stub triplets
  - Fit with 5 param fit (d_0)



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Slow Control at Tracker R&D Boards

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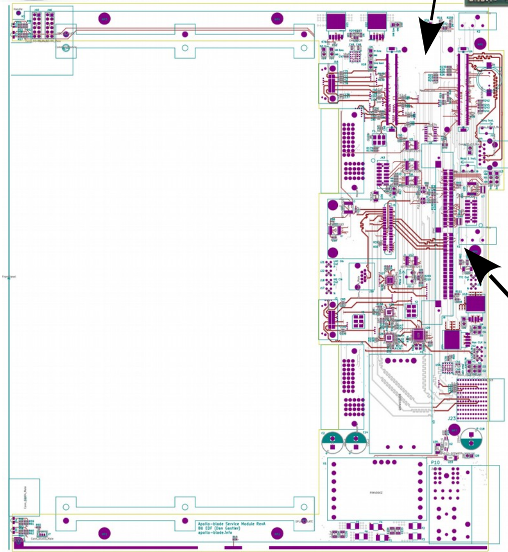
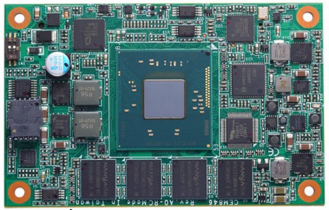
Enclustra ZX1
- AXI-C2C
- TCDS
- Eth

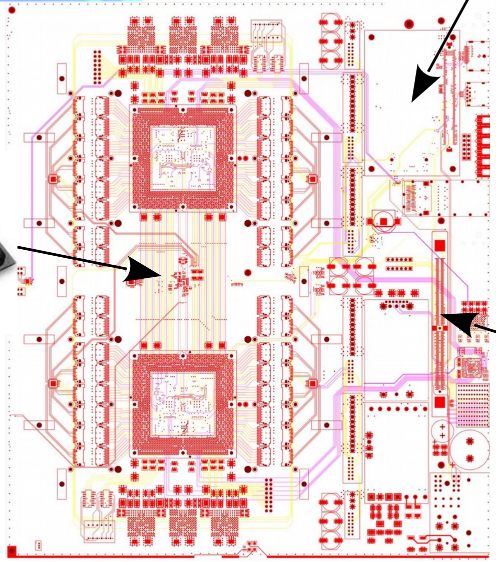


CERN-IPMC
- IPMI
- Eth
- PMBus

Com-Express
- PCIe
- Eth



Artix 7
- TCDS
- Eth
- I2C
- PMBus



CERN-IPMC
- IPMI
- Eth
- PMBus

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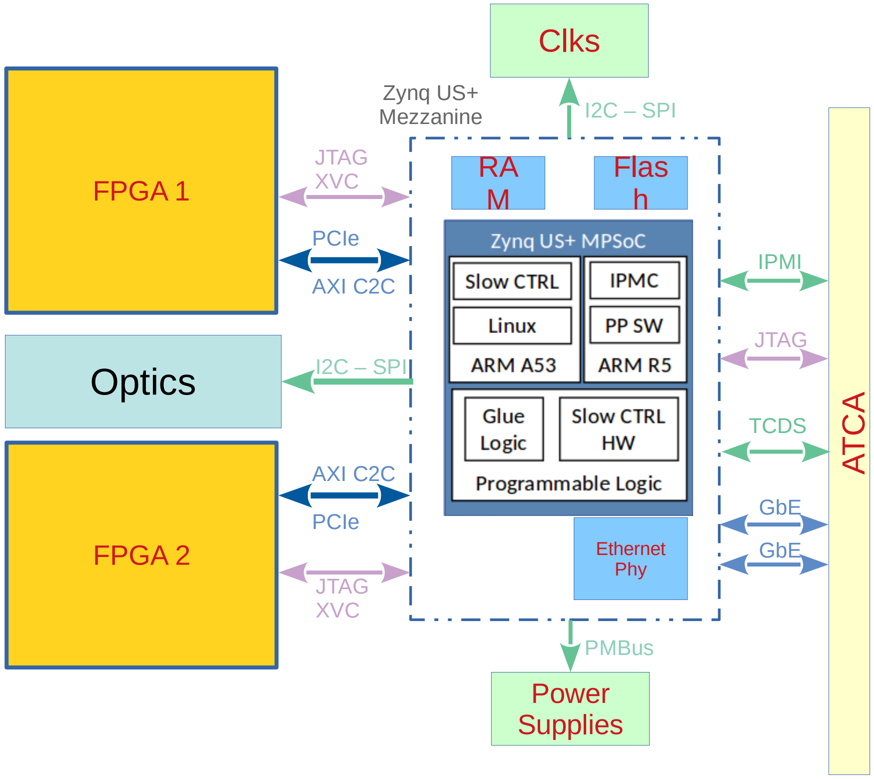
Integrated Board Management

Integrate IPMC, GPP based slow control functionality and FPGA in a **single heterogeneous MPSoC** (Zynq Ultrascale+)

- **Intelligent Platform Management Interface (IPMI)** in ARM-R5 processor running freeRTOS
- **Timing and Control Distribution System (TCDS)** in PL-FPGA
- Xilinx Virtual Cable (**XVC**) JTAG
- **AXI Chip2Chip** slow control capable



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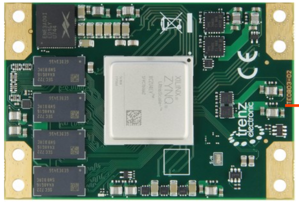
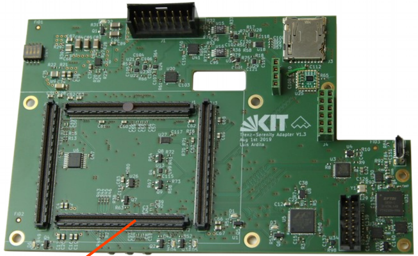
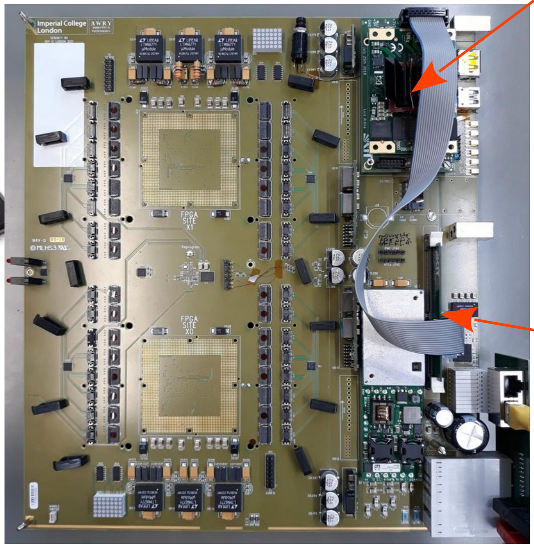
Proof Of Concept: Adapter On Serenity

Trenz
ZynqUS+
4EG





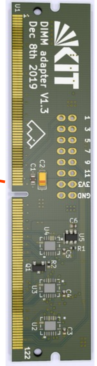
Adapter v1.3

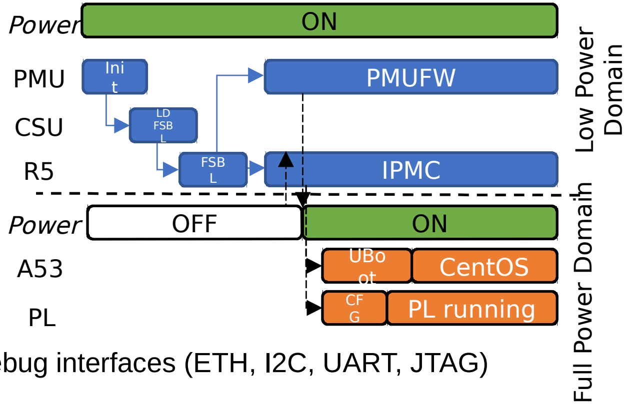


Serenity v1.0 by Imperial College

Artix 7
- TCDS
- Eth
- I2C
- PMBus

IPMC signals





☑ Test and debug interfaces (ETH, I2C, UART, JTAG)

☑ **Pigeon Point IPMC** standalone software compiled for the ARM-R5 processors

- ☑ IPMC boot, ☑ Com with Shelf Manager, ☑ Board activation/deactivation, ☑ Power-up/power-down sequence, ☑ Read of IPMC sensors, ☑ Cold reset, ☑ Initiating boot of Linux, ☑ Coexistence of Linux & IPMC, ☐ JTAG on Linux (XVC, not integrated)

☑ **Petalinux & CentOS** running on the ARM-A53 Processors

- ☑ SSH to Linux on ZynqUS+

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Integrated Board Management

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Low Power Domain – always active:

- **Intelligent Platform Management Interface (IPMI)** application running in one of the R5 cores.
- It uses the On-chip-Memory and the I2C peripherals
- IPMC memory region protected through system configuration
- SPI and PMBus

High Power Domain – active upon request of full power from the crate:

- Runs Yocto/CentOS based Linux
- FPGA configuration and monitoring
- Slow-control to FPGAs
- Test patterns to firmware

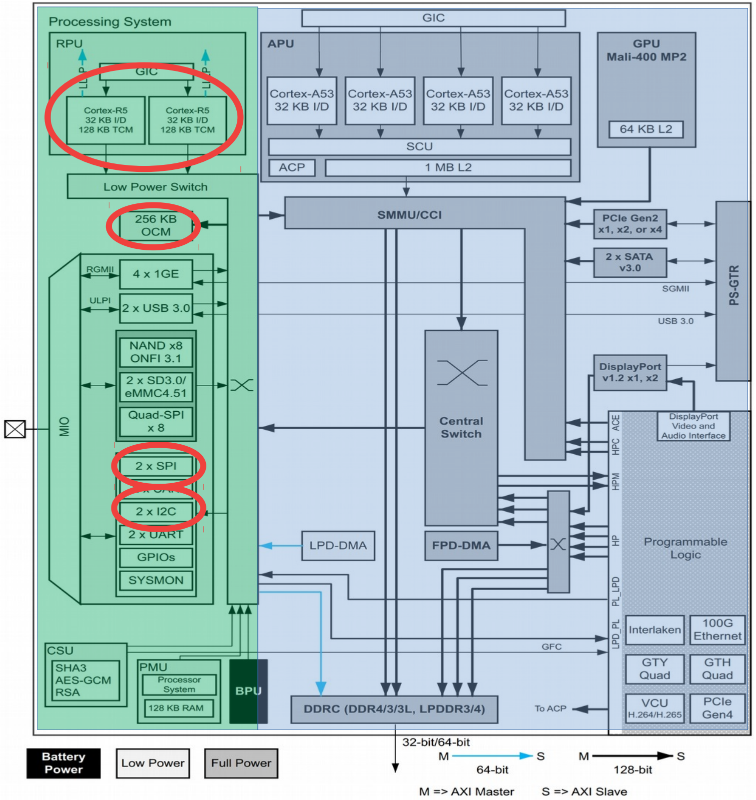


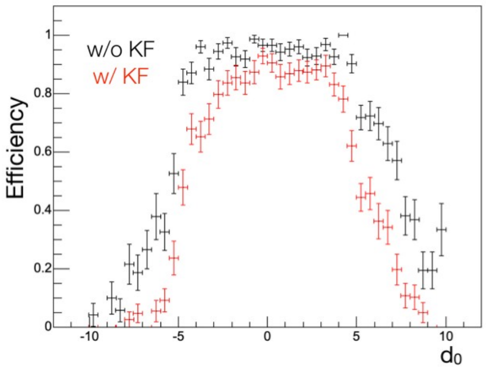
Figure 2-1: **Zynq UltraScale+ MPSoC Device Hardware Architecture**

Displaced Track Finding

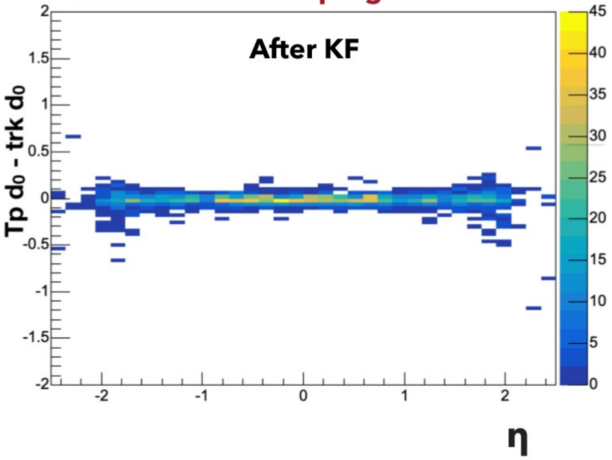
- **Efficiency**
  - Up to 5 - 10 cm
  - Limitation is bend cut on FE in inner layers
- **Rate**
  - 1.2 x increase in rate w.r.t 5 param prompt
  - 1.4 x increase w.r.t 4 param prompt

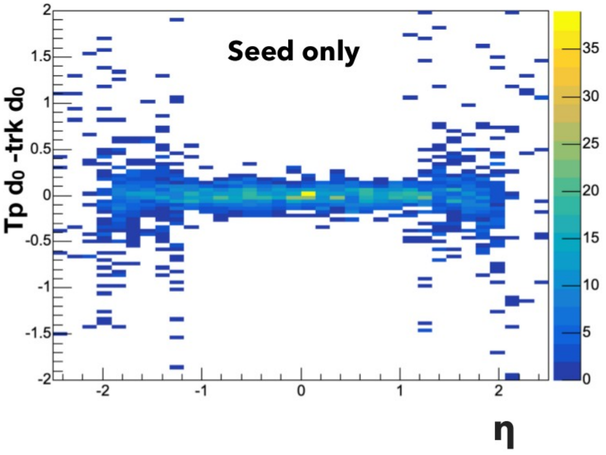
CMS R&D work in progress

$\eta < |1.8|$, $p_T > 3$ GeV



CMS R&D work in progress





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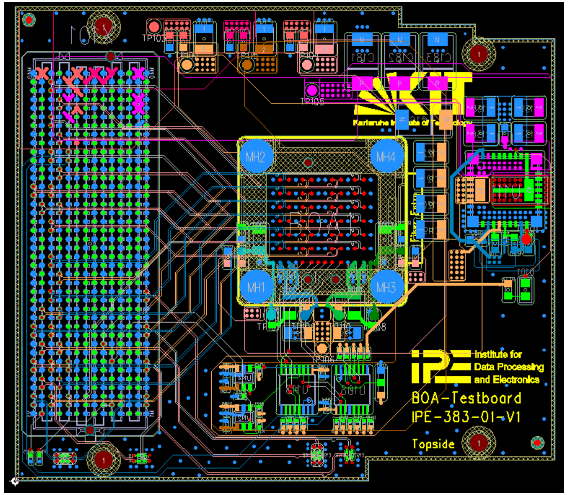
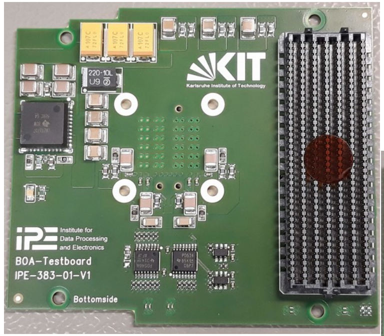
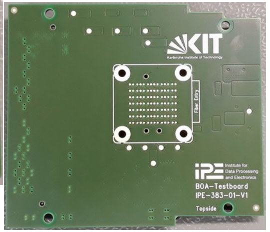
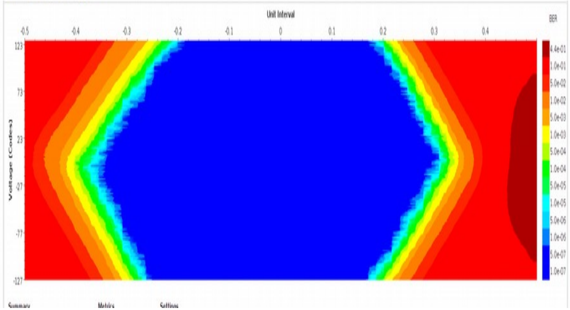
High-Speed Optical Evaluation

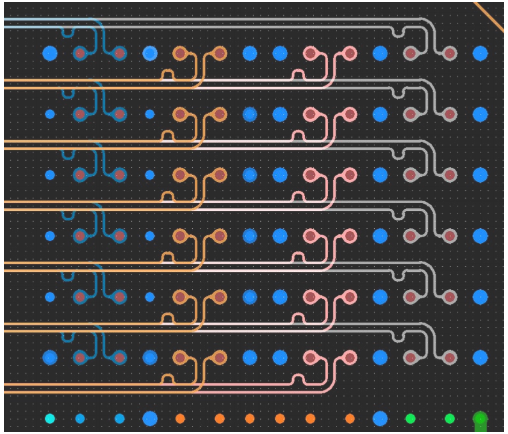
- FMC+ sized board for evaluation of the Finisar BOA 25 Gb/s transceiver
- 12 TX and 12 RX integrated in the same package
- 4 Electrical loop-back channels capacitively coupled with different features
- Skew < 20 µm
- MT ferrule optical interface
- Performance of capacitively coupled lanes looks good











Thermal Simulation And Tests

Simulation setup

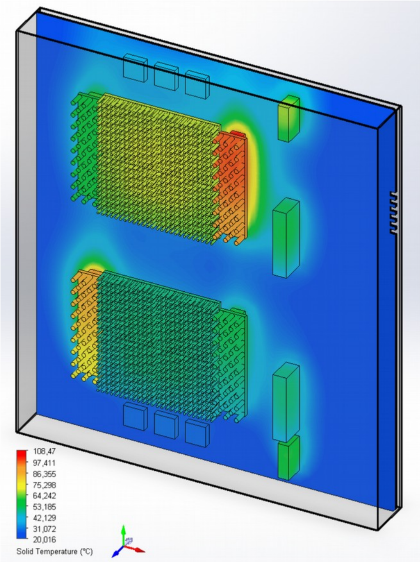
- PCB imported from PADS
- Placed in a 33 mm deep tunnel
- 4 m/s airflow from bottom (20 °C) to top

Placed components

- KU15P (50 W) doubled θ_{JB} to take interposer into account
- Firefly banks 25 G (30W) and 16 G (12 W)
- **Total power 205.4 W**

Test setup

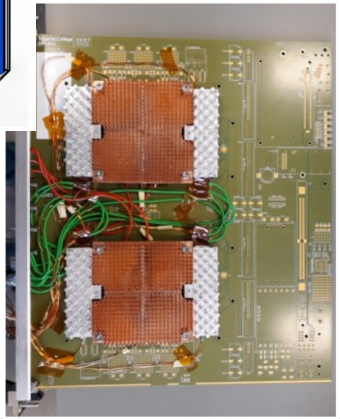
- Two heat-pads **45 mm x 45 mm** and **12 mm x 70 mm**
- Just one mockup board is present, it will be put in between two additional soon
- **~11 W for 6x block** of 16 Gbps optics
- **~10 W for 6x block** of 25 Gbps optics

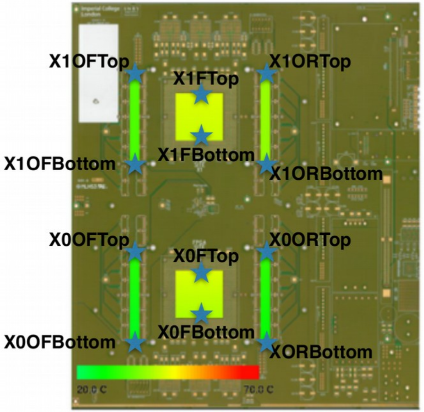


Test1 (°C)
4xFan-block speed=50%
Exhaust temp ~17°C (~amb)
Power on FPGA heaters = 86 W
Power on Optics heaters = 41 W

X1FTop = 60.7
X1FBottom = 59.1
X1ORTop = **50.8**
X1ORBottom = **49.7**
X1OFTop = 43.1
X1OFBottom = 41.7

X0FTop = 53.7
X0FBottom = 50.1
X0OFTop = 35.8
X0OFBottom = 28.2
X0ORTop = 37.2
X0ORBottom = 31.1





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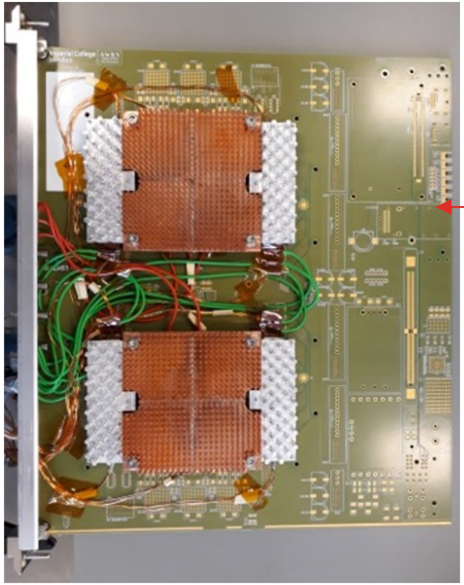
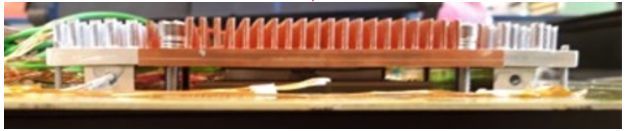
THERMAL & MECHANICAL TESTS

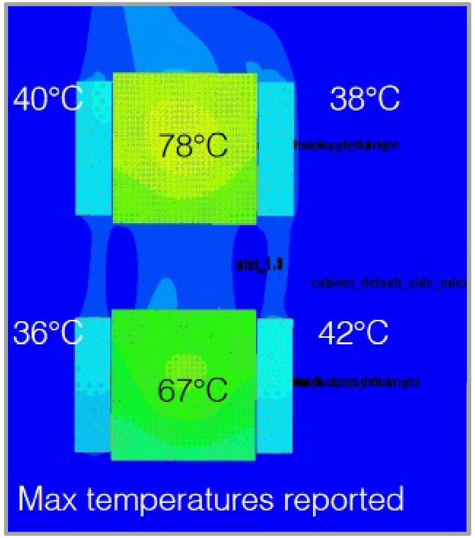


Thermal simulations

Physical thermal studies at CERN

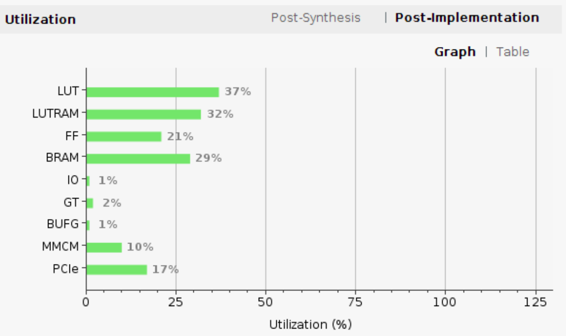
Mechanical component design studies into stress on FPGA solder balls and stress on PCBs at IC



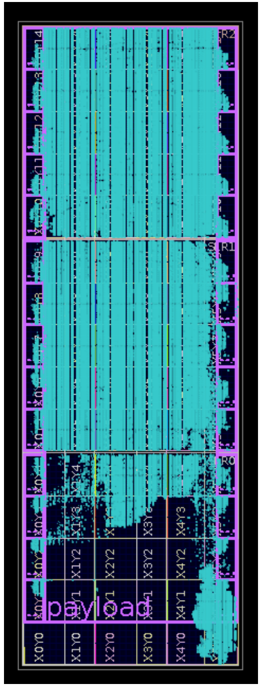


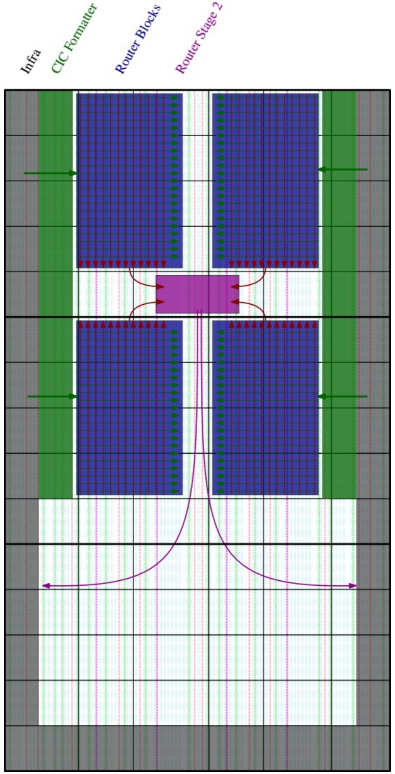
DTC Firmware in VU9P

- Target single FPGA (VU9P) to avoid side wise communication
- Use of EMP framework with 64 bit frames at 320 MHz
- Input packet structure of 58 data frames + 6 frames gap
- 5 gbps modules send up to 16 stubs per CIC in 8 BX packets
- 10 gbps modules send up to 35 stubs per CIC in 8 BX packets
- One 64 bit word contains a Stub from CIC0 and a Stub from CIC1



Taken from Thomas Schuh





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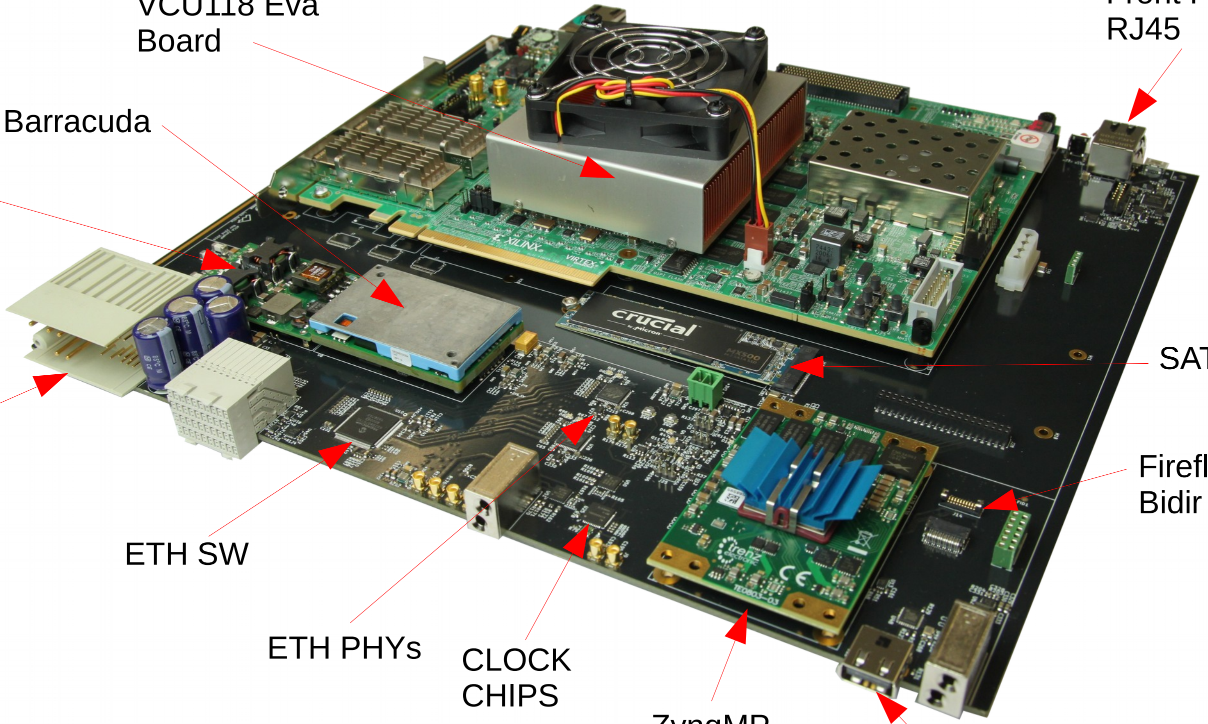
ZynqMP-IPMC ATCA Test Board



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Integrated Management Module Architecture

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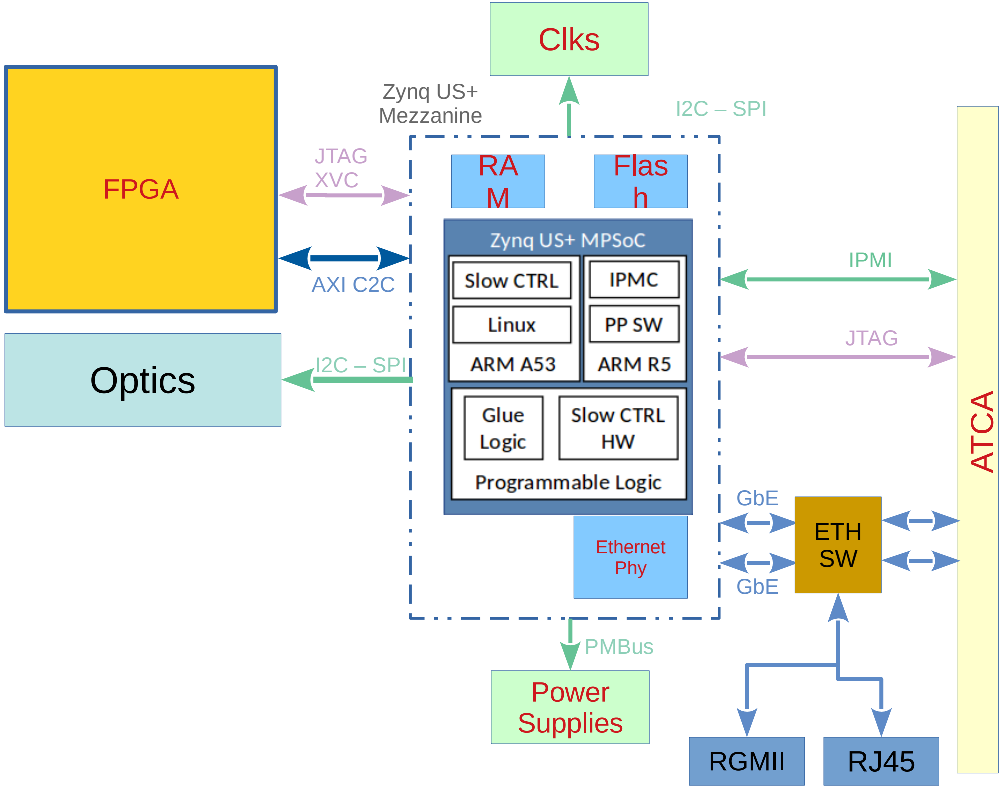

- **IPMI** (standalone/RTOS) on ARM-R5 processor
- **Slow Control** (Linux) on ARM-A53 Cores
- Xilinx Virtual Cable (**XVC**) JTAG
- **2 Links to main FPGAvia PL-MGTs** (AXI C2C)
- **I2C-SPI** to configure Optics/Clocks
- **PMBus** to configure Power Supplies
- **Eth** and **I2C** backplane connection

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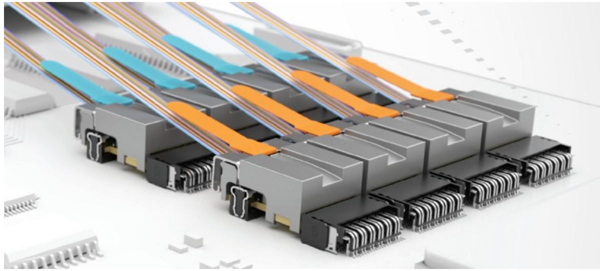
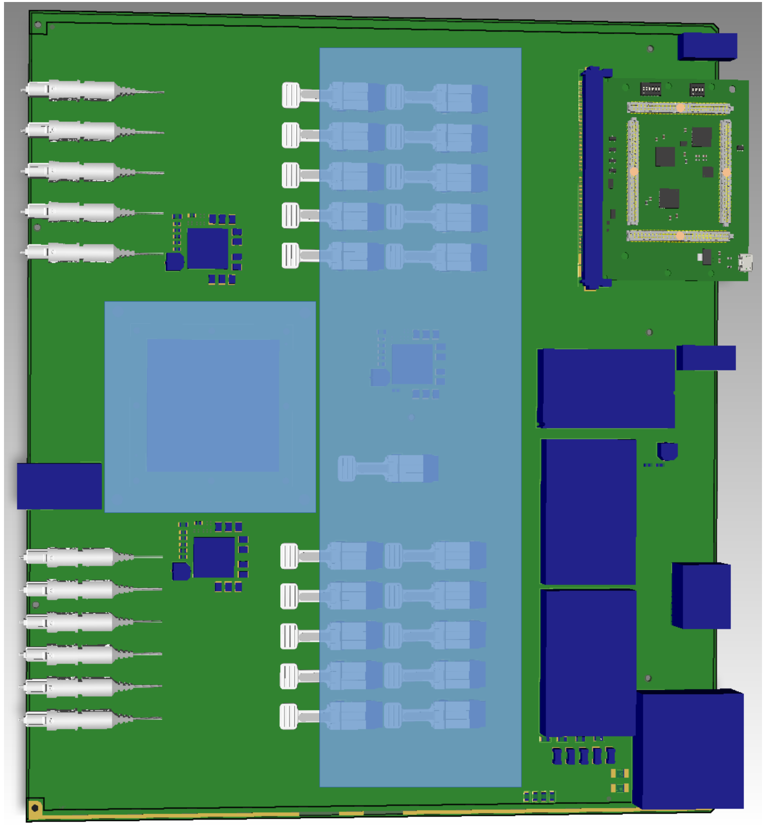
ATCA Layout

- One FPGA design **VU9P / VU13P**
  - **No inter-FPGA** communication
- **TCDS** backplane signals directly routed to main FPGA
- Integrated **IPMC** slow control solution
- **Monolithic** heat sink for all optics
- Clean Optical Cable management
- **Only one type of Firefly cable x10**





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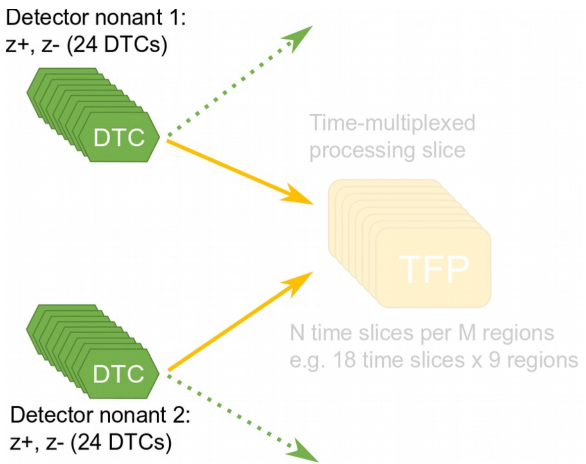
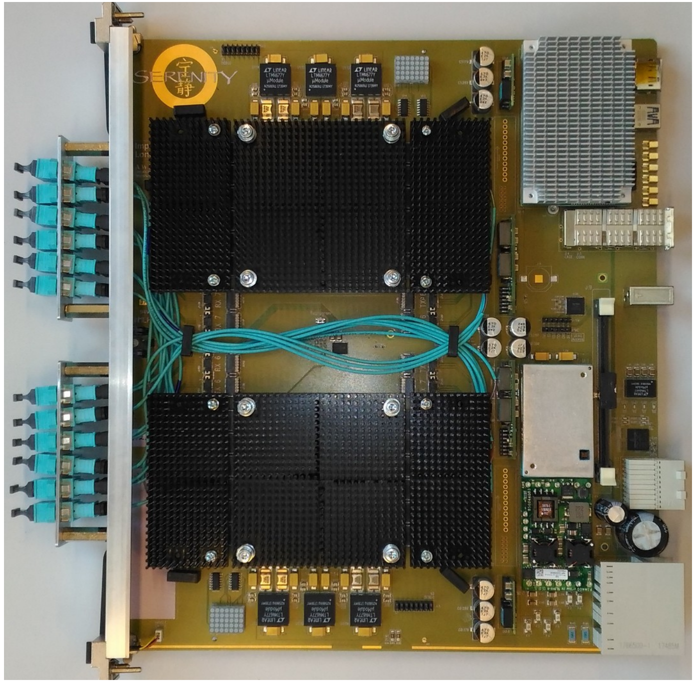
Track Finder Architecture – DTC



Two stages of data processing

- **DAQ, Trigger and Control (DTC) layer**
- **Track Finding Processor (TFP) layer**
- **All-FPGA** processing system
- **ATCA** form factor; CMS standard dual-star backplane



DTC card must handle

- **<=72 modules (5G/10G lpGBT opto-links)**
- Control/Readout for each module
- Direct L1 stream to central DAQ (16G/25G)
- Direct stub stream to TFPs (25G)

Stub pre-processing includes:

- **Local** → **Global** look up, position calibration
- Sort and pre-duplication
- Time-multiplexing

→ **216 DTC boards, 18 crates, 1 rack/nonant**

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