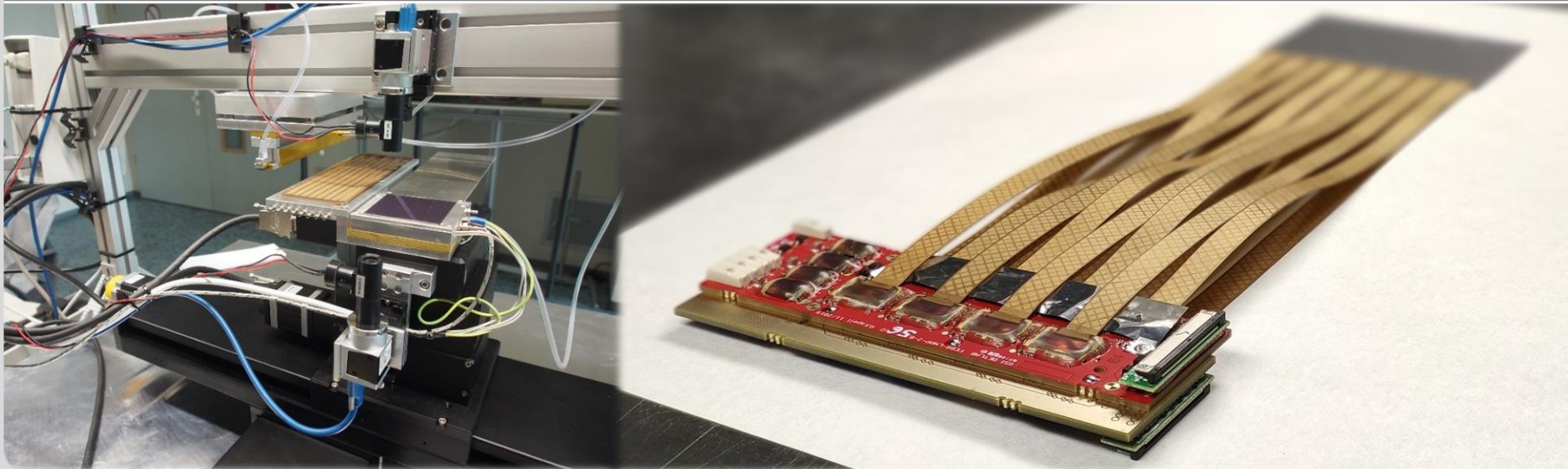


Development and characterization of a novel high-density interconnection technology for the CBM Silicon Tracking System at FAIR

Patrick Pfistner, Thomas Blank, Michele Caselle,
for the CBM collaboration

Institute for Data Processing and Electronics

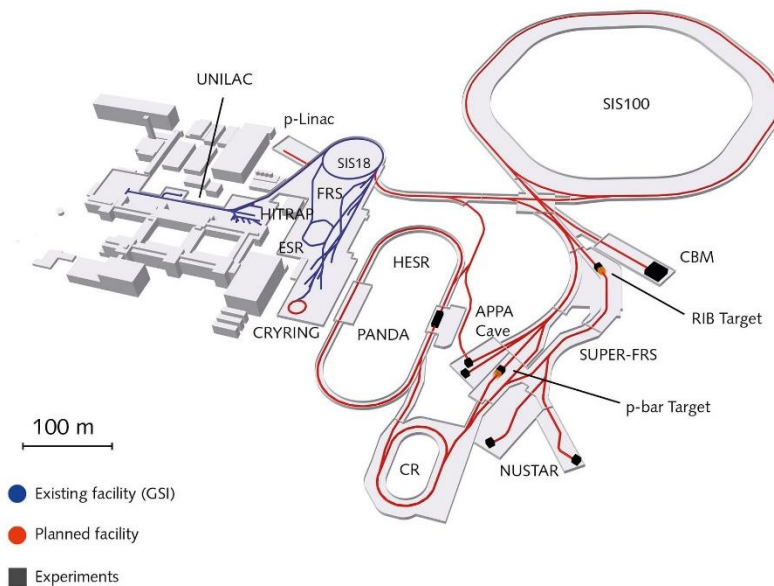


Outline

- Compressed Baryonic Matter (CBM) experiment @ FAIR
- Silicon Tracking System (STS)
- STS detector module
- High-density interconnection based on aluminum microcables and TAB
- Novel high-density interconnection technology based on Gold stud – solder bump bonding
- Characterization of prototype modules in copper technology

CBM @ FAIR

- CBM is one of the major scientific programs at FAIR
- Investigation of QCD phase diagram at high net-baryon densities and moderate temperatures



https://www.gsi.de/fileadmin/_processed_/8/9/csm_FAIR-beschriftet_MS_V_DE_Feb18_4408267c7b.gif

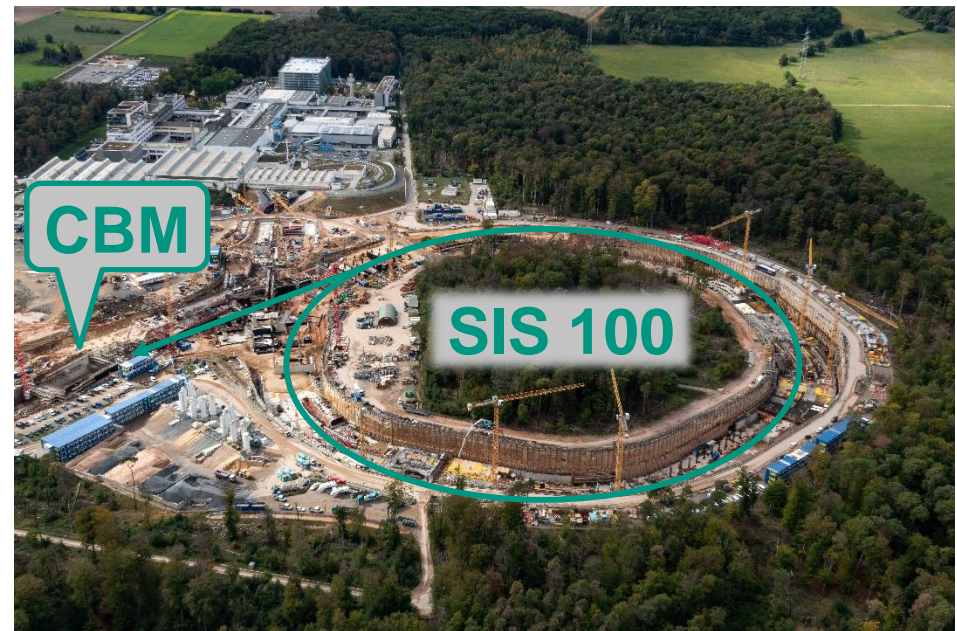
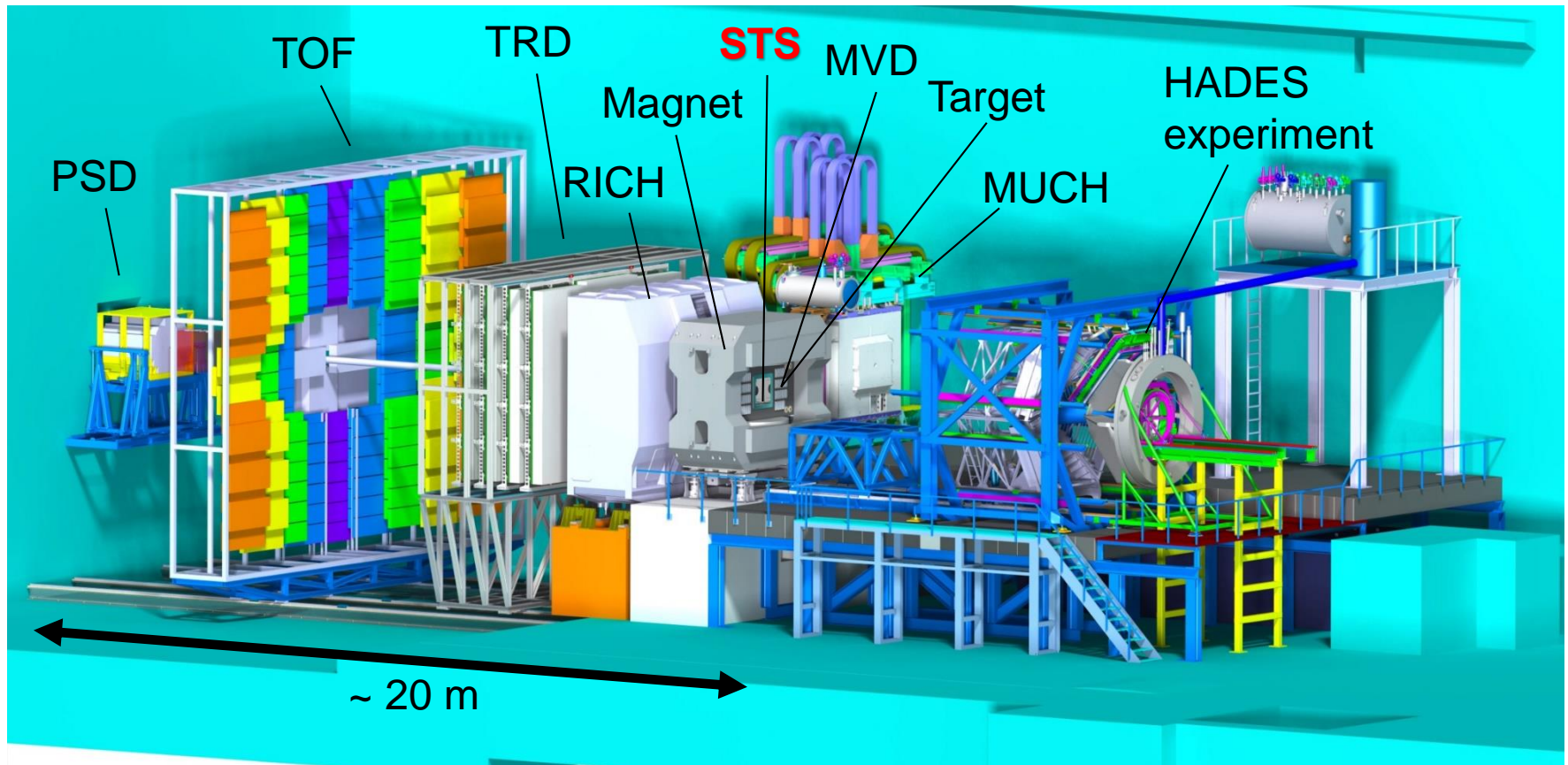


Image: D. Fehrenz/GSI/FAIR

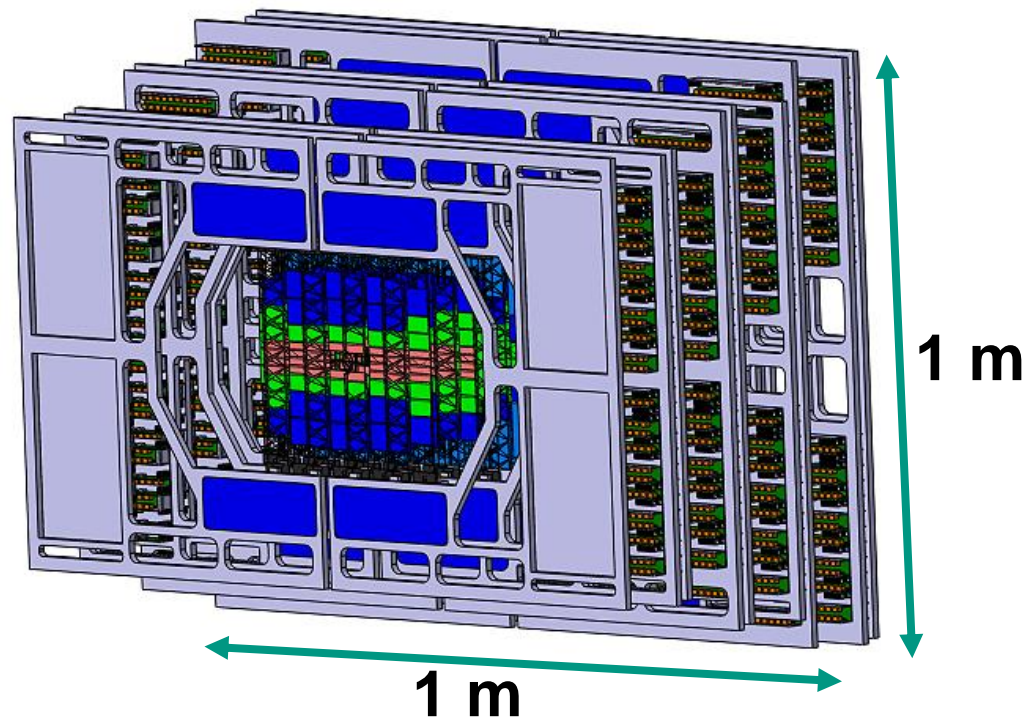
Drone video of FAIR construction site:
<https://www.youtube.com/watch?v=8cSLI557CQk>

CBM experimental setup

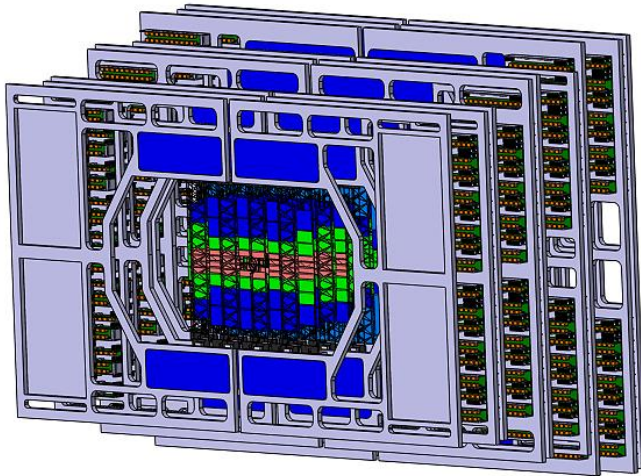


Silicon Tracking System (STS)

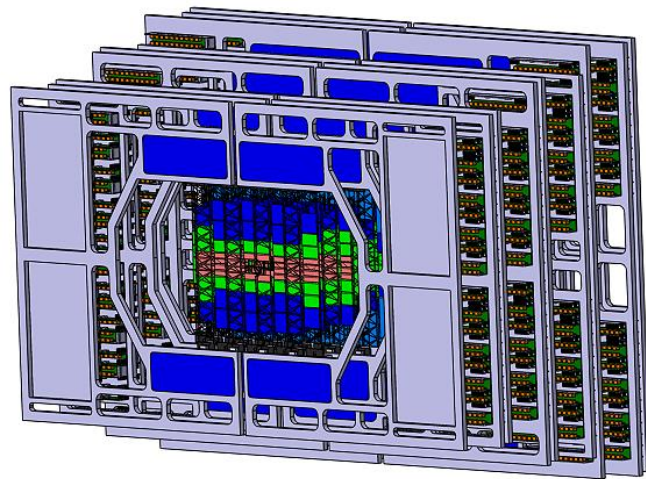
- Track identification and momentum determination of charged particles
- Track mult. ≤ 700 per central Au+Au collision in aperture $2.5^\circ < \theta < 25^\circ$
- Lifetime fluence up to $1 \times 10^{14} \text{ n}_{\text{eq}} \text{ cm}^{-2}$
- Momentum resolution $\Delta p/p < 2\%$



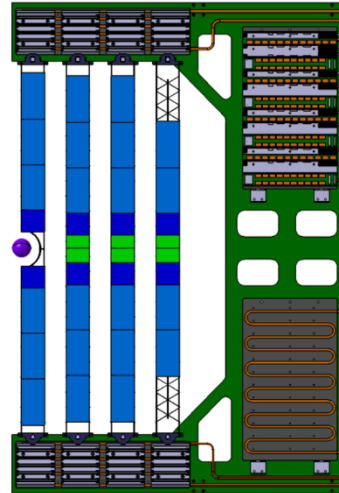
STS conception



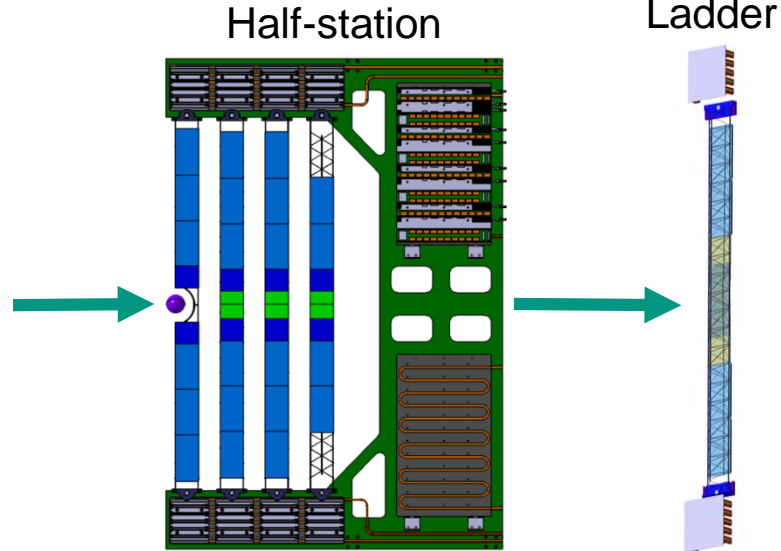
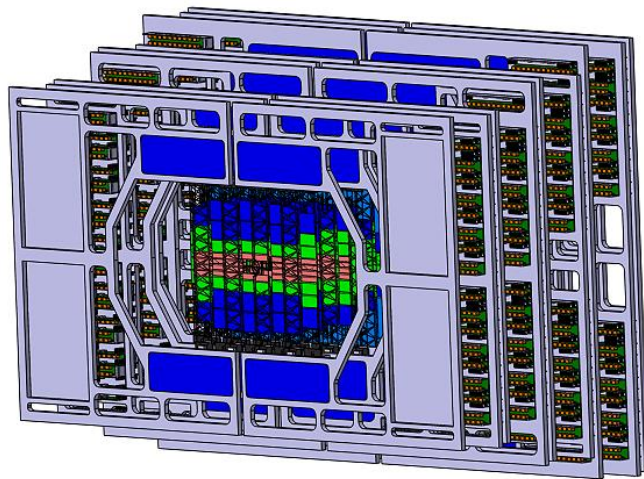
STS conception



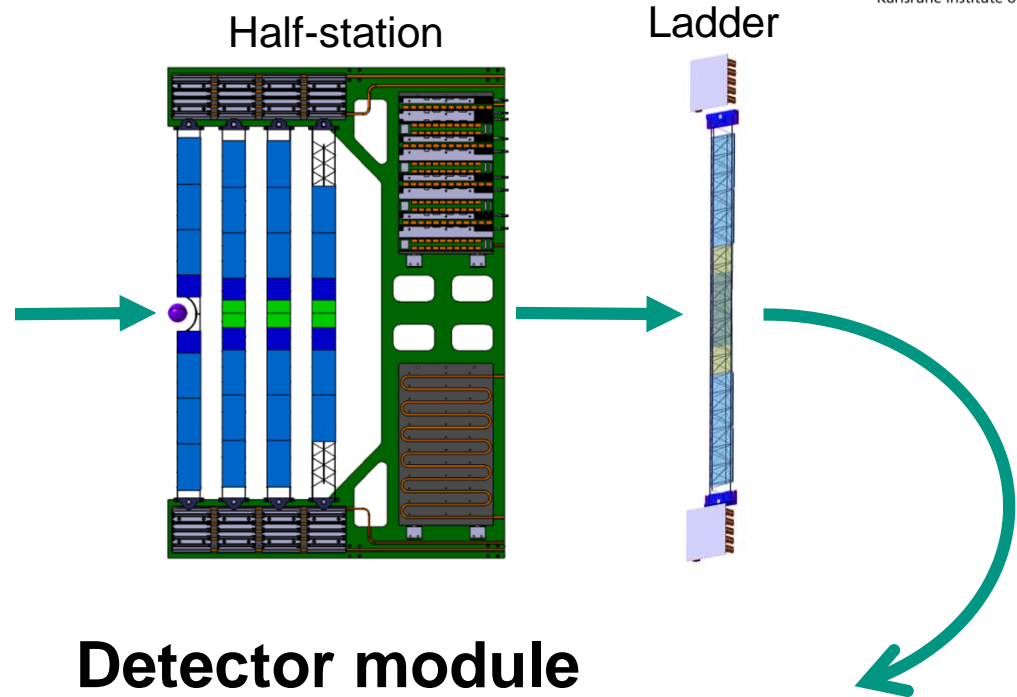
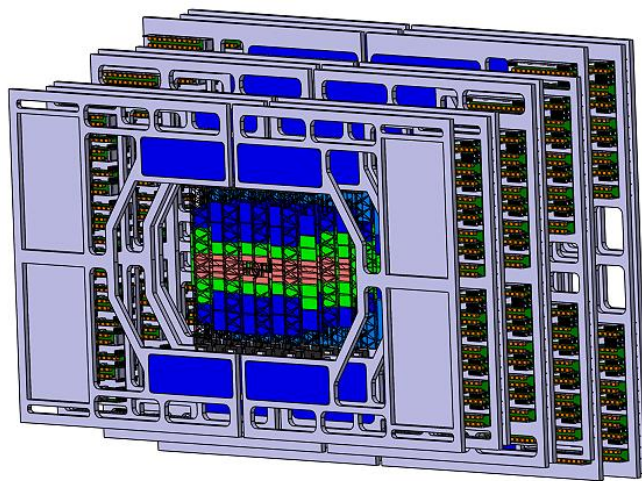
Half-station



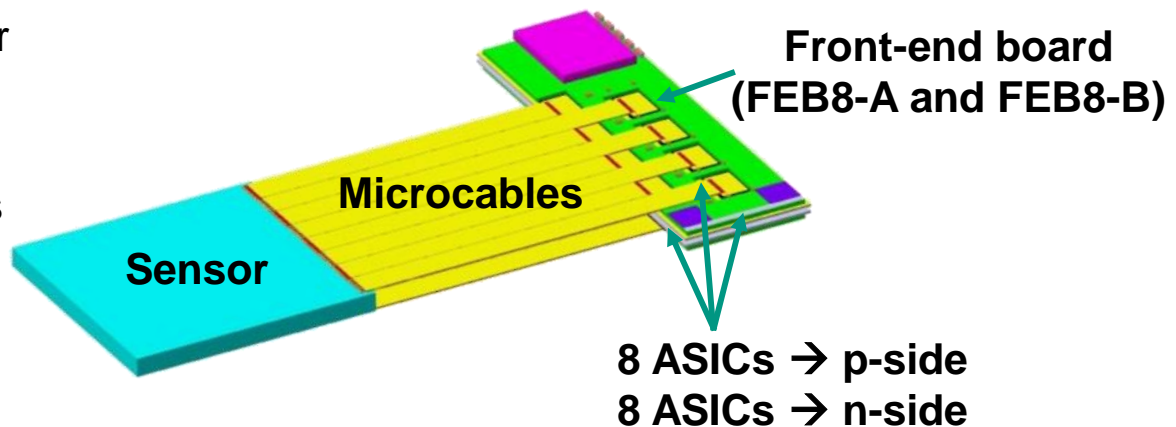
STS conception



STS conception



- Double-sided microstrip sensor
 - Pitch: 58 μm
 - 2 x 1024 channels
- 2 x 8/16 low mass microcables
- 2 x FEB-8
- 2 x 8 STS-XYTER ASICs



TAB interconnection

ALUMINUM TECHNOLOGY

Aluminum microcables

Aluminum microcable

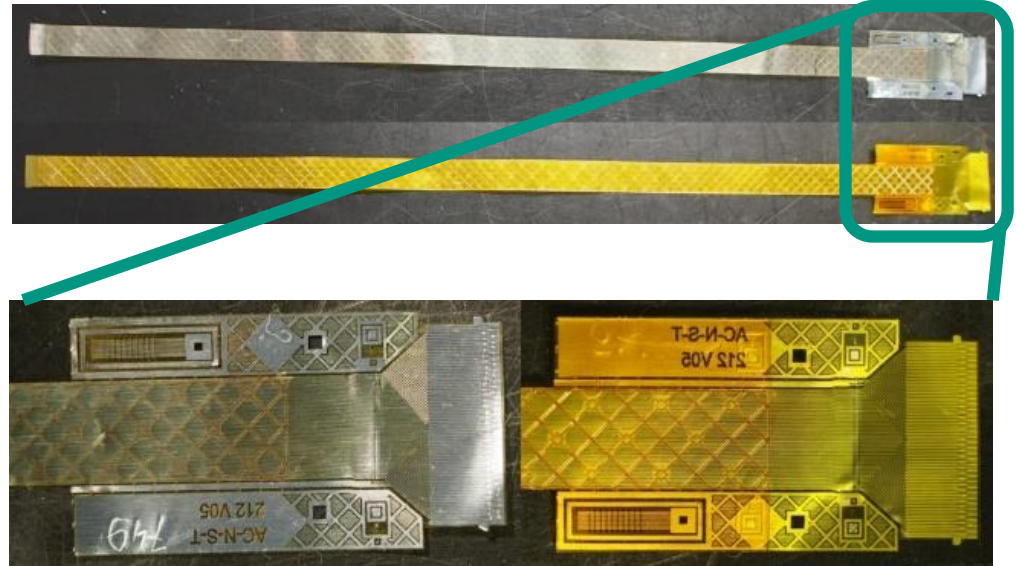
- 15 μm Al on 10 μm Polyimide
- Meshed PI spacer
- 64 signal lines
- Pitch: 116 μm
- Capacitance ~ 0.35 pF/cm
- $X/X_0 \sim 0.03$ %
- 32 microcables per sensor



Aluminum microcables

Aluminum microcable

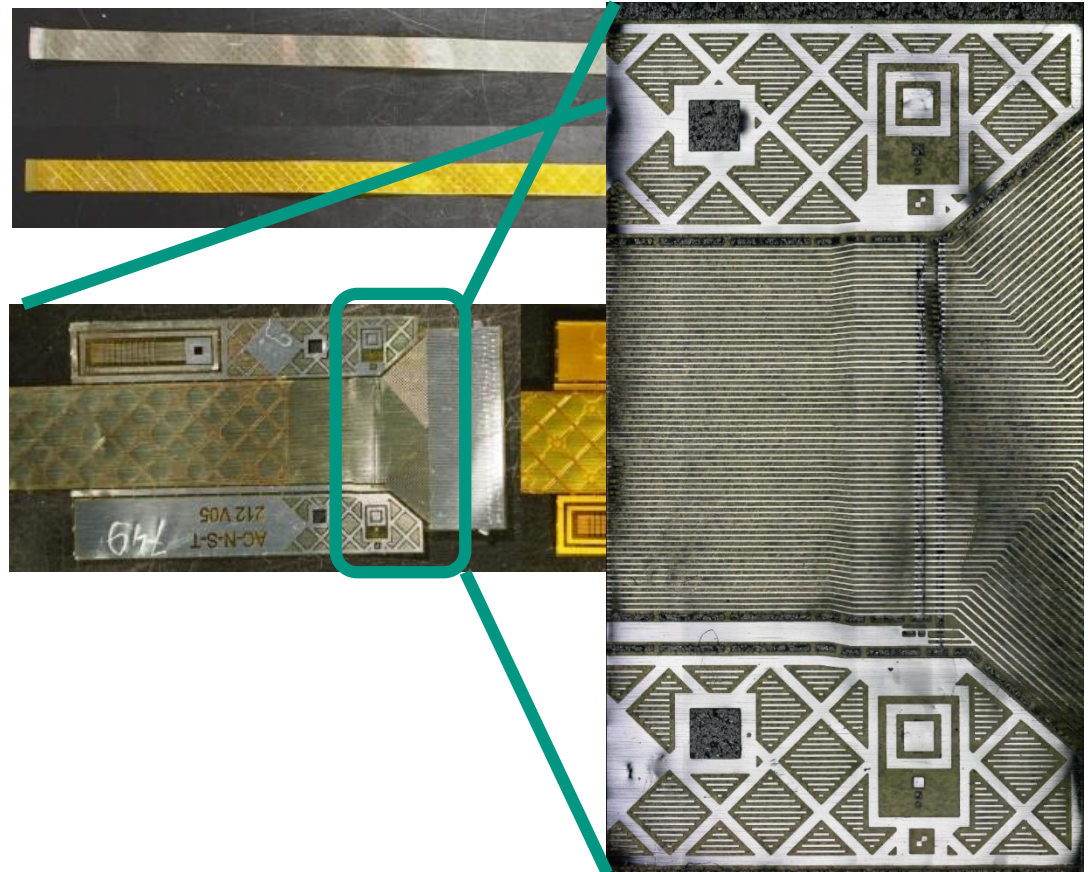
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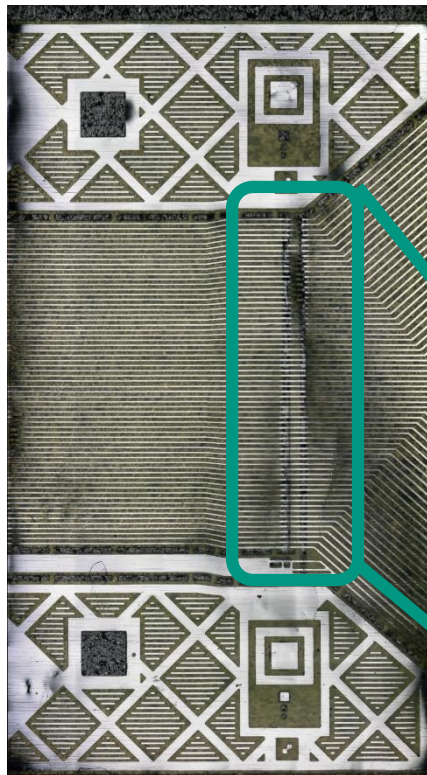
Aluminum microcables

Aluminum microcable

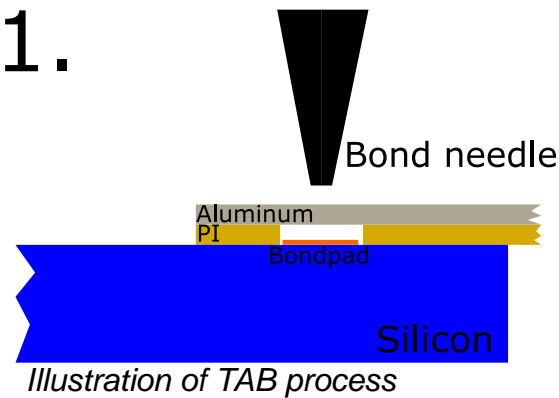
- 15 μm Al on 10 μm Polyimide
- Meshed PI spacer
- 64 signal lines
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- Capacitance ~ 0.35 pF/cm
- $X/X_0 \sim 0.03$ %
- 32 microcables per sensor



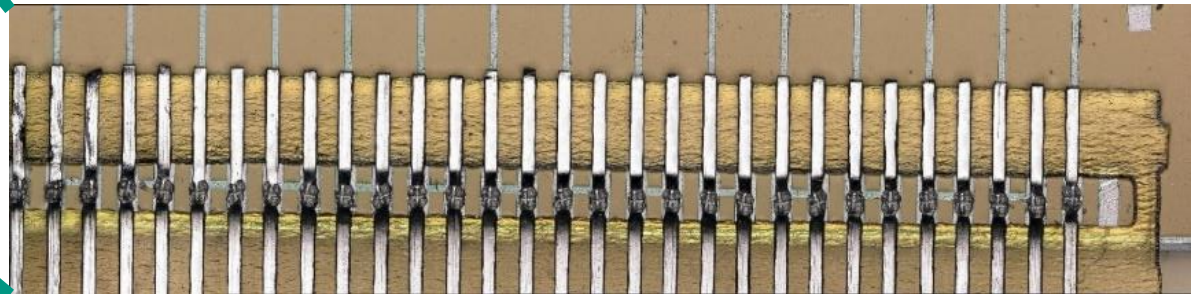
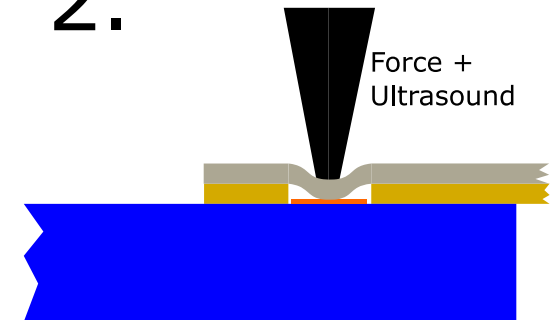
Interconnection by TAB process



1.



2.



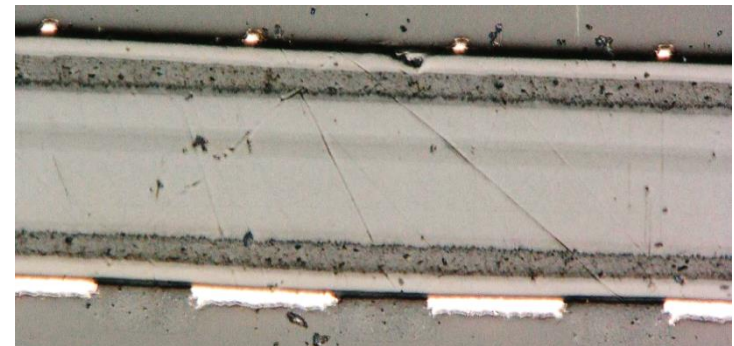
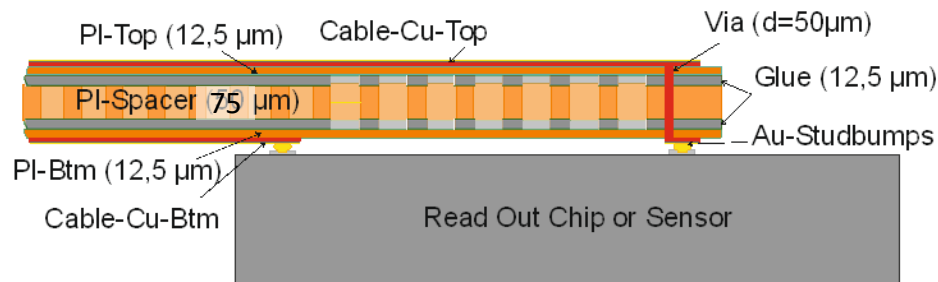
- Room temperature process
- Well-established, proven to work
- Manual and time-consuming
- Single supplier of aluminum microcables (LTU Ltd, Kharkov, Ukraine)

Gold stud – solder bump bonding

COPPER TECHNOLOGY

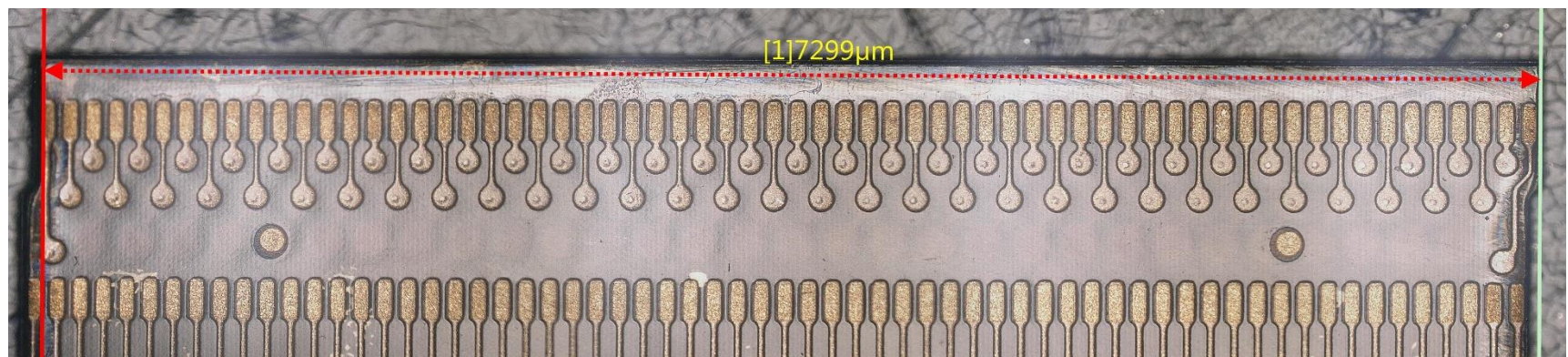
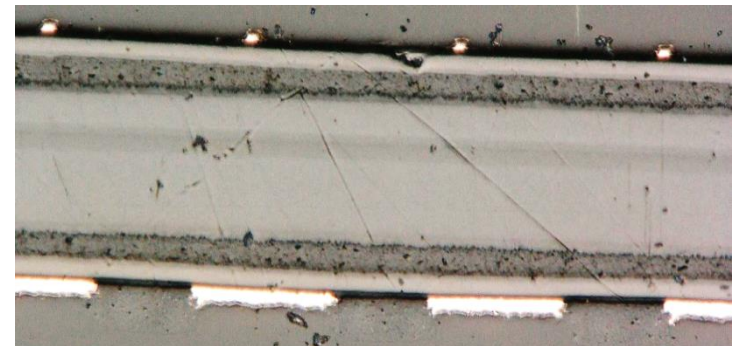
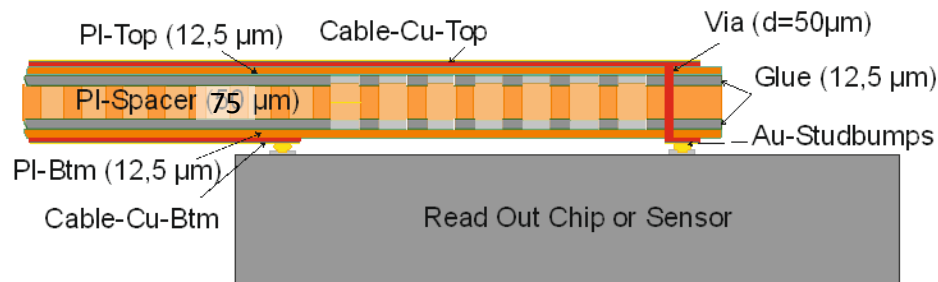
Copper microcables for Au-solder process

- Two signal layers: 2 x 64 channels
- Bond pitch 116 μm
- Thickness 140 μm
- Capacitance $\sim 0.38 \text{ pF/cm}$
- $X/X_0 \sim 0.05 \%$



Copper microcables for Au-solder process

- Two signal layers: 2 x 64 channels
- Bond pitch 116 μm
- Thickness 140 μm
- Capacitance $\sim 0.38 \text{ pF/cm}$
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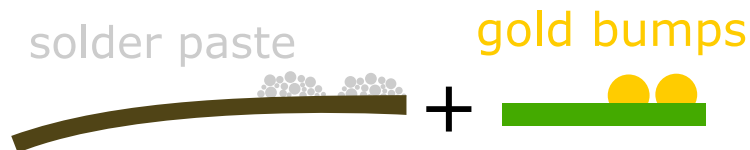


Novel approach: Gold stud – solder process

1. cable and chip



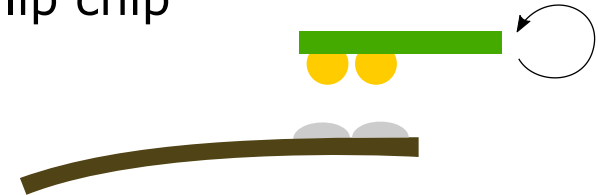
2. place bumps on chip and solder paste on cable



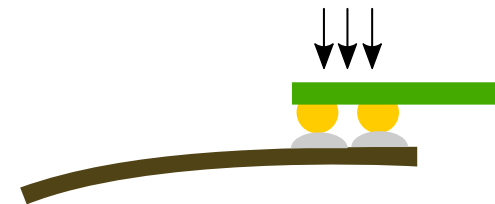
3. reflow



4. flip chip



5. thermocompression bonding



6. underfill

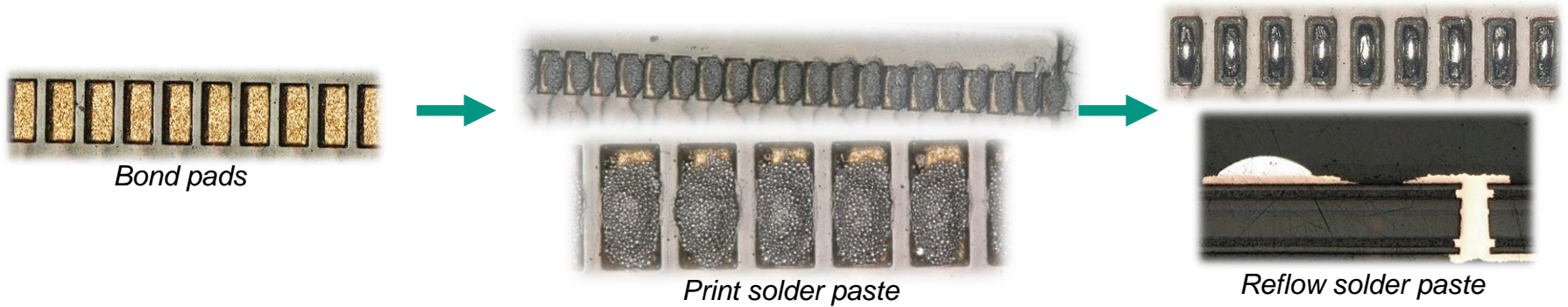


A schematic diagram of the sensor assembly. It consists of three main layers: a top green layer labeled "Sensor or ASIC", a middle thin white layer with a thickness indicated as $\sim 25\mu\text{m}$, and a bottom brown layer labeled "Cable". Yellow circles representing solder bumps are shown at the interface between the green layer and the white layer.

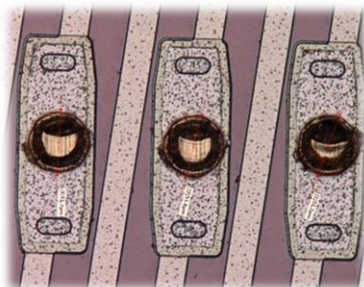
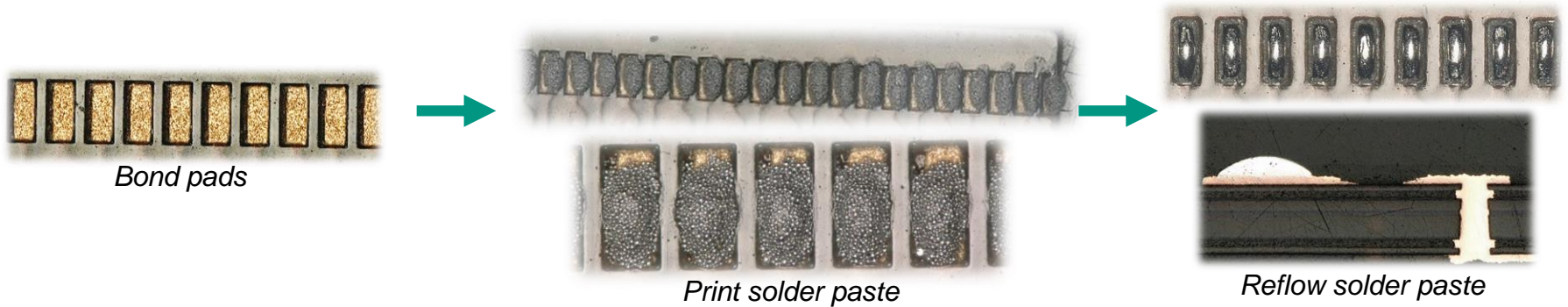
Sensor

The diagram illustrates the layout of a sensor array. It features two main sections, Cable 1 and Cable 2, which are part of a larger array of 8 such units. Cable 1 has a width of 116 μm and a height of 140 μm . It contains two rows of components, each with 64 elements. The top row has three white rectangular components, and the bottom row has two white rectangular components. Cable 2 has a width of 20 μm and a height of 60 μm . It contains two rows of components, each with 64 elements. The top row has three white rectangular components, and the bottom row has two white rectangular components. The bottom row of Cable 2 is labeled "Bond pads". The entire array is composed of 8 such units, as indicated by the "x 8" label.

Realization of Au stud – solder process

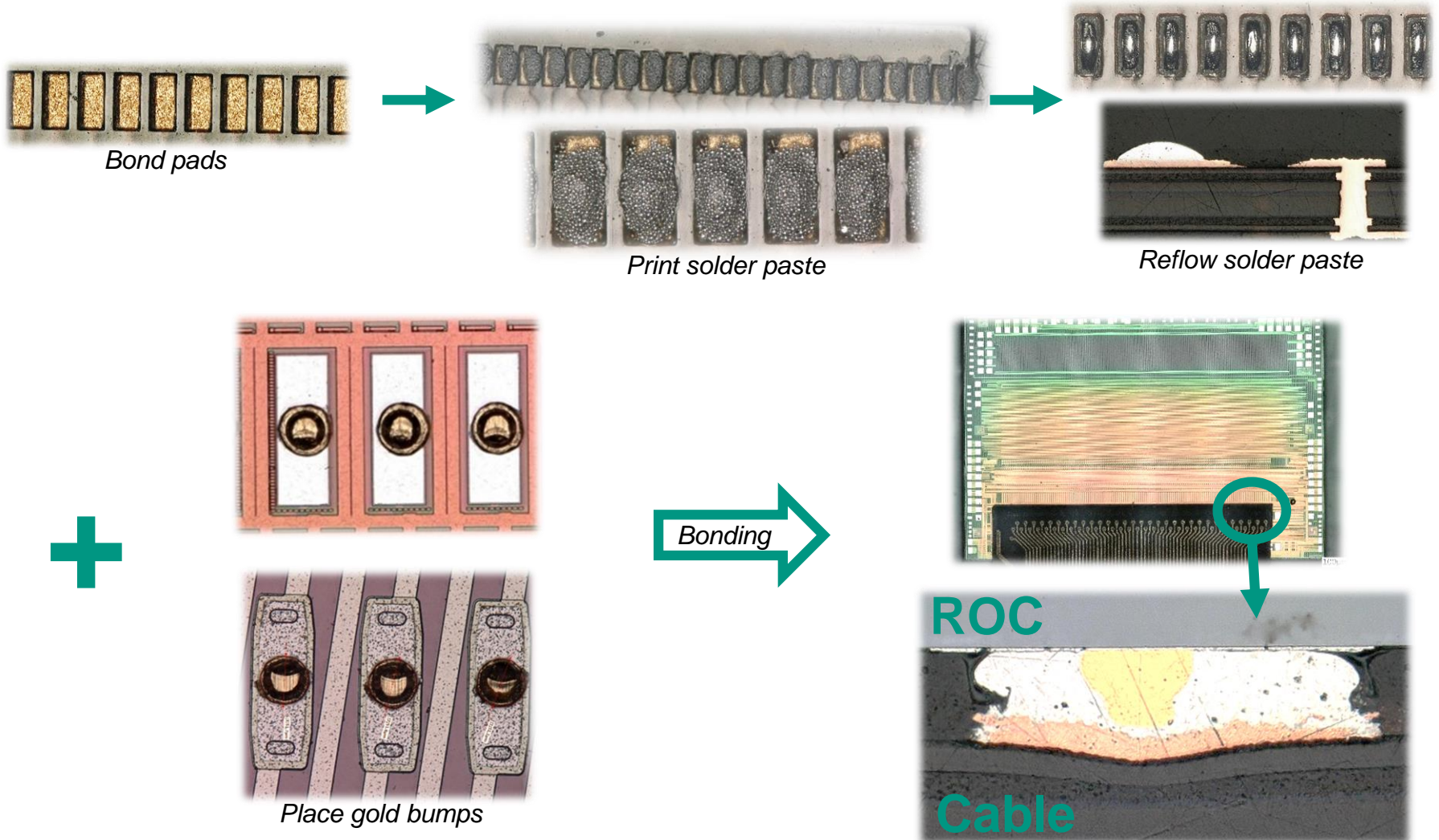


Realization of Au stud – solder process



Place gold bumps

Realization of Au stud – solder process

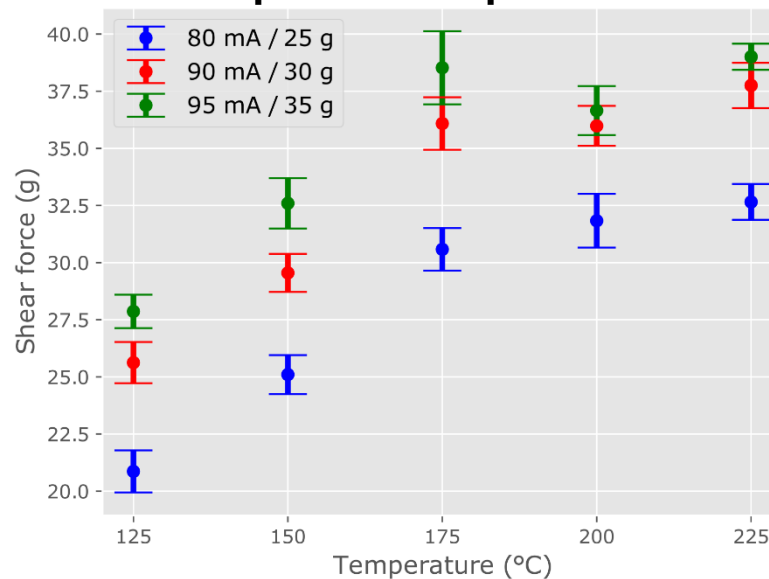


Gold stud bumping process optimization

■ Gold bumping parameter scan

- Temperature
- Bond force
- Ultrasonic current (USG)

Temperature dependence

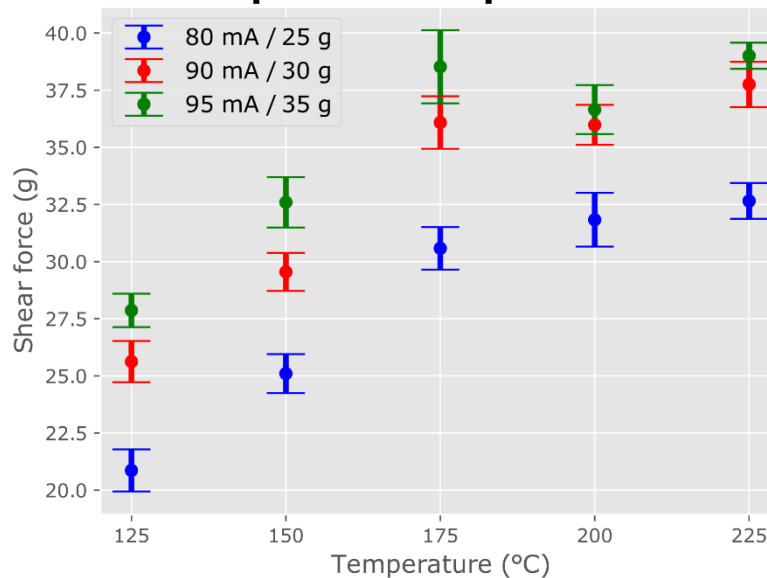


Gold stud bumping process optimization

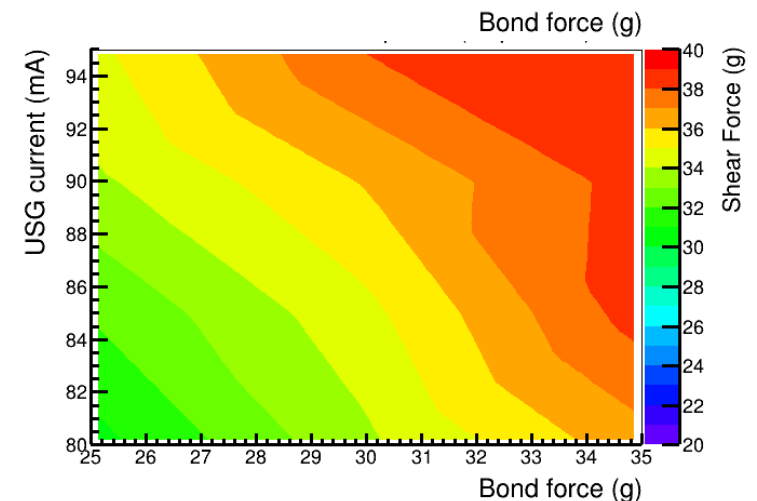
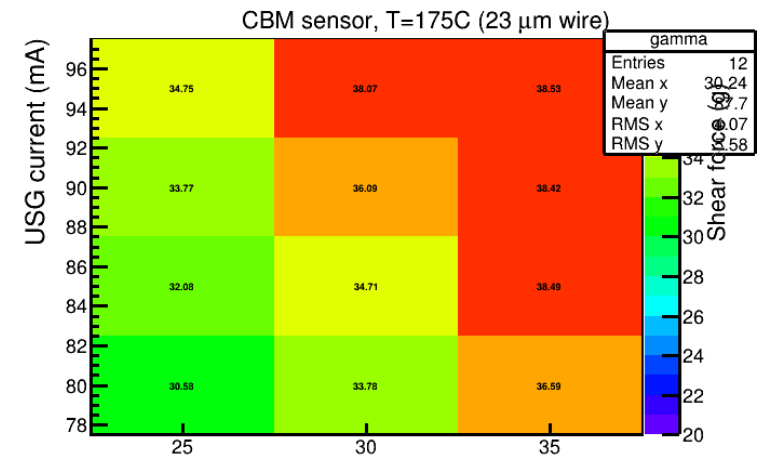
Gold bumping parameter scan

- Temperature
- Bond force
- Ultrasonic current (USG)

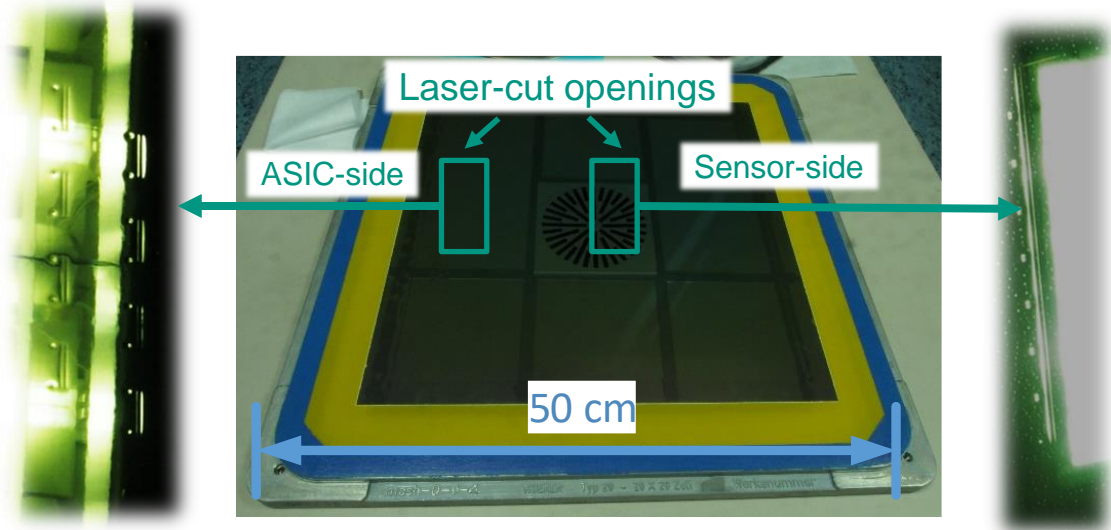
Temperature dependence



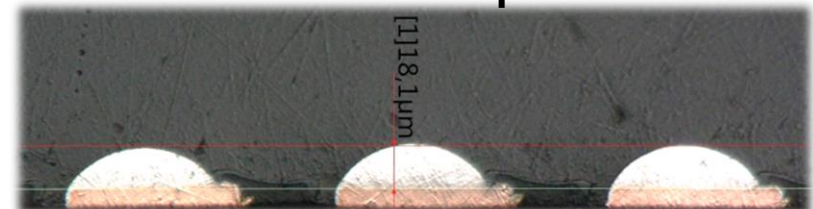
Bond force – USG scan



Solder paste type 7/8 printing and reflow



Uniform solder deposition



Tackling the thermal mismatch

- Process temperature reduction
- Downscaling of microcable pitch

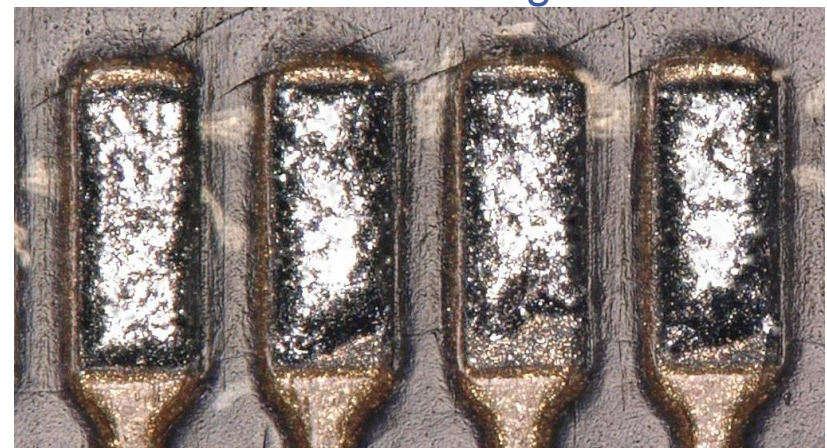
Solder paste type 7/8

Alloy	T_{melt} (°C)
Sn96.5Ag3.0Cu0.5 (SAC305)	217
Sn63Pb37	183
Sn42Bi58	138
Sn42Bi57.6Ag0.4	131

SAC305

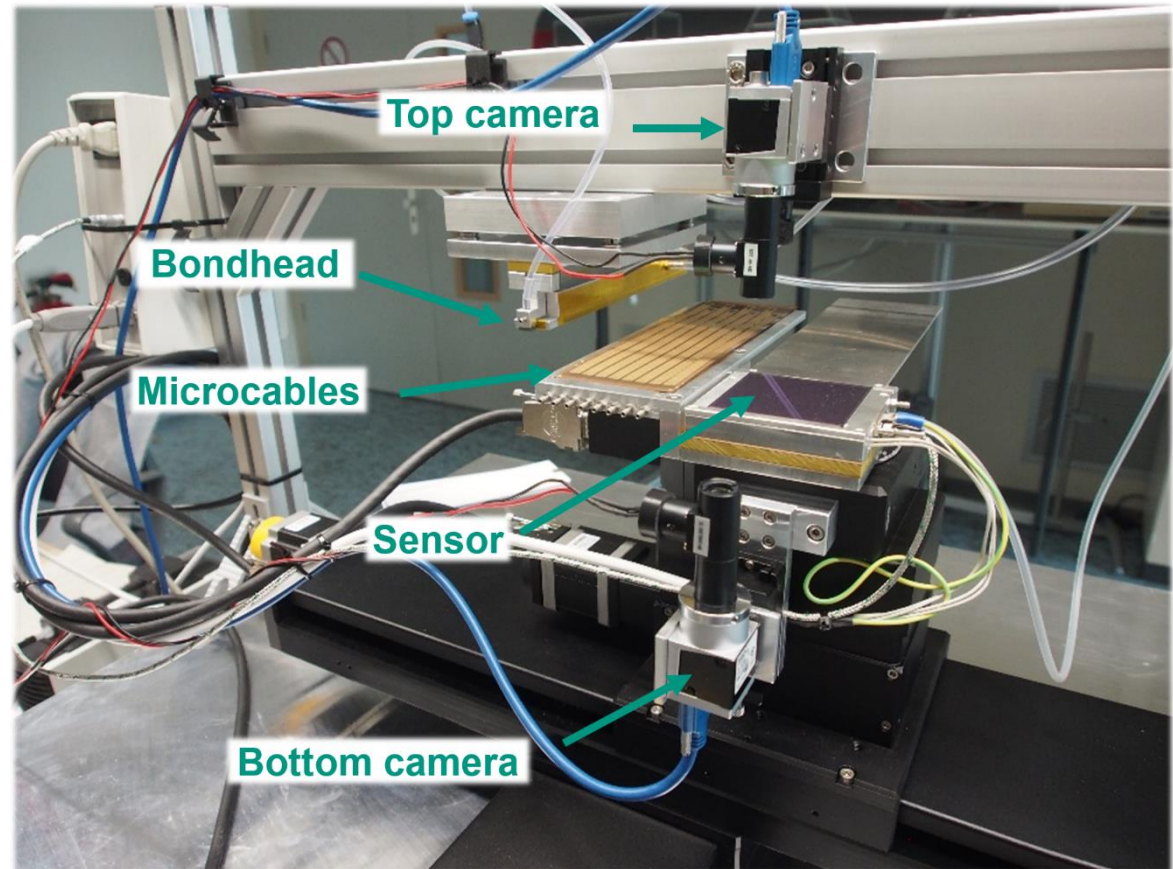


Sn42Bi57.6Ag0.4



In-house bonding machine for sensor-side interconnection

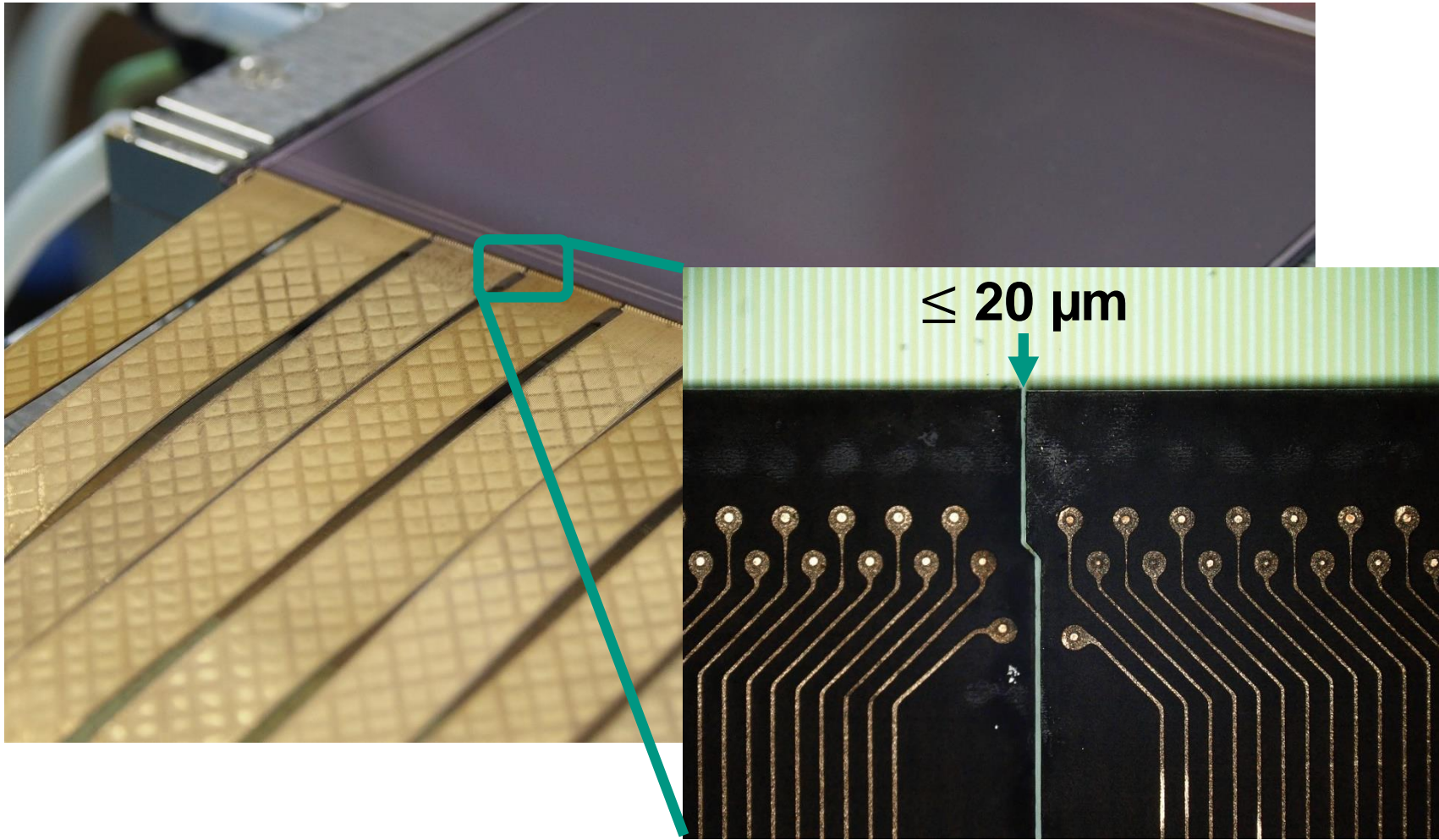
- Four stepper motors (x,y,z, φ) with sub-micron resolution
- Temperature regulated heatable bond head and sensor plate
- Dual-camera optical system
- Automated vacuum control



Complete single-sided assembly

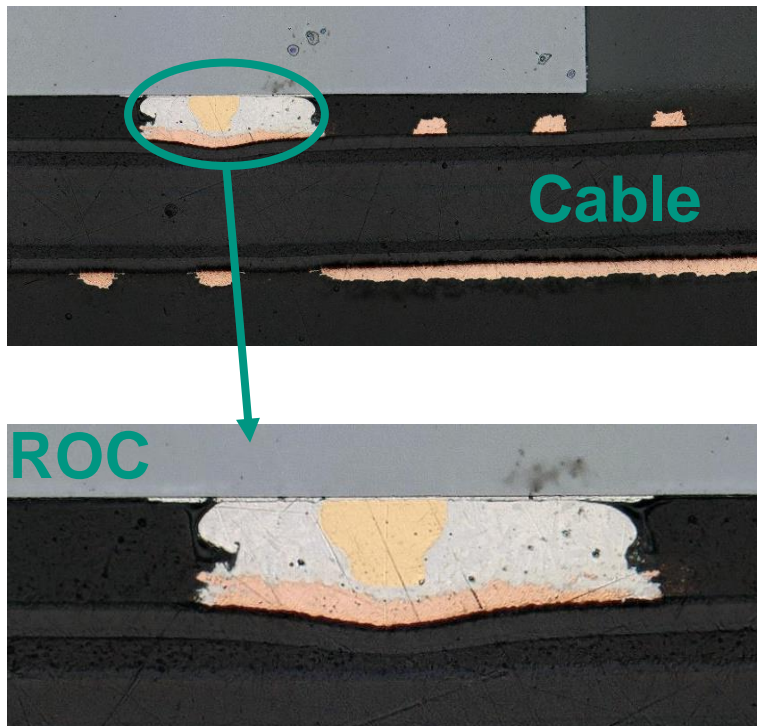


Complete single-sided assembly

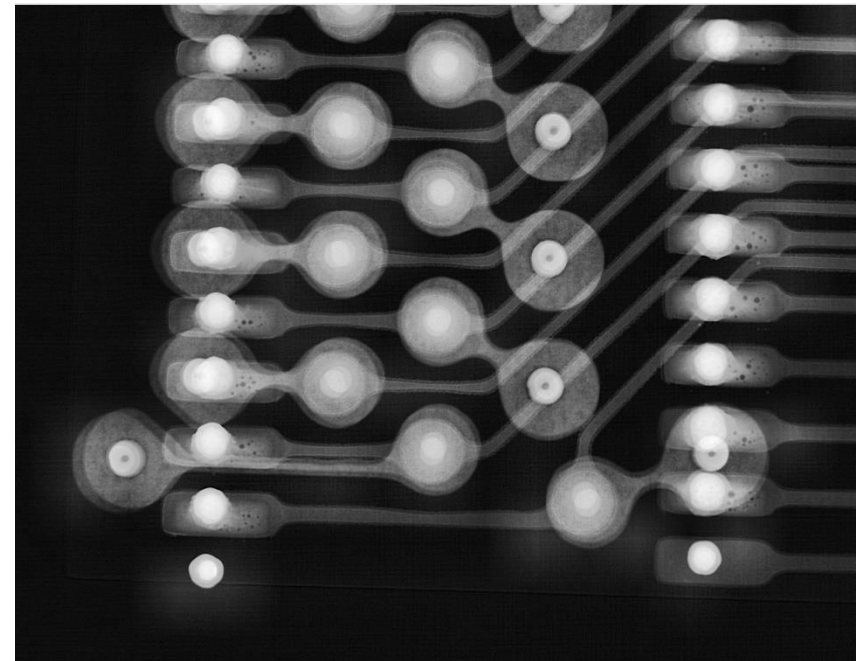


Quality assurance

Cross-sections

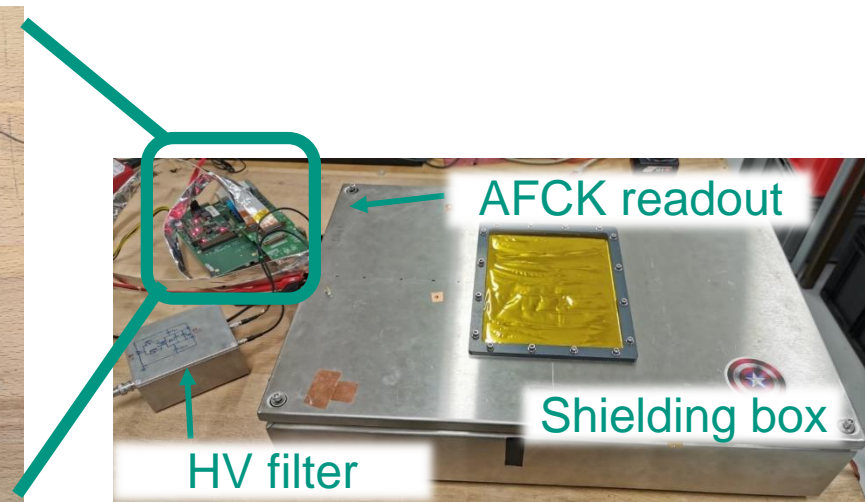
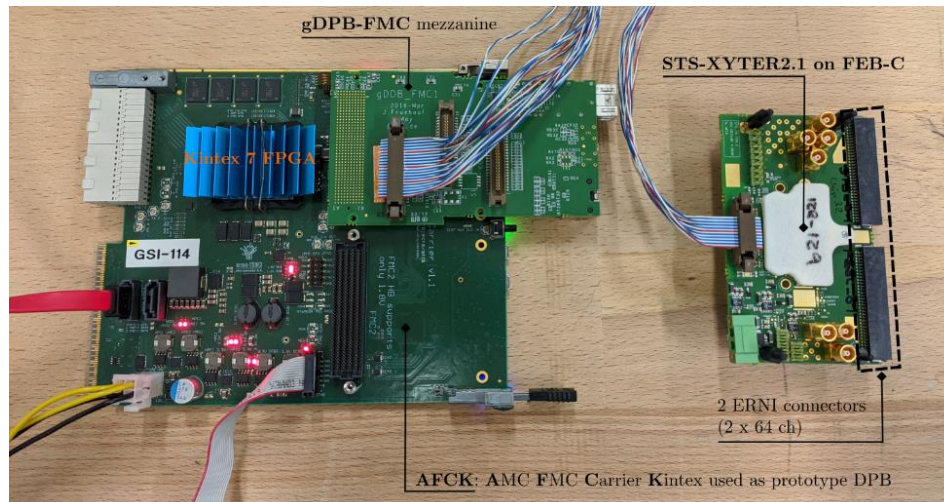
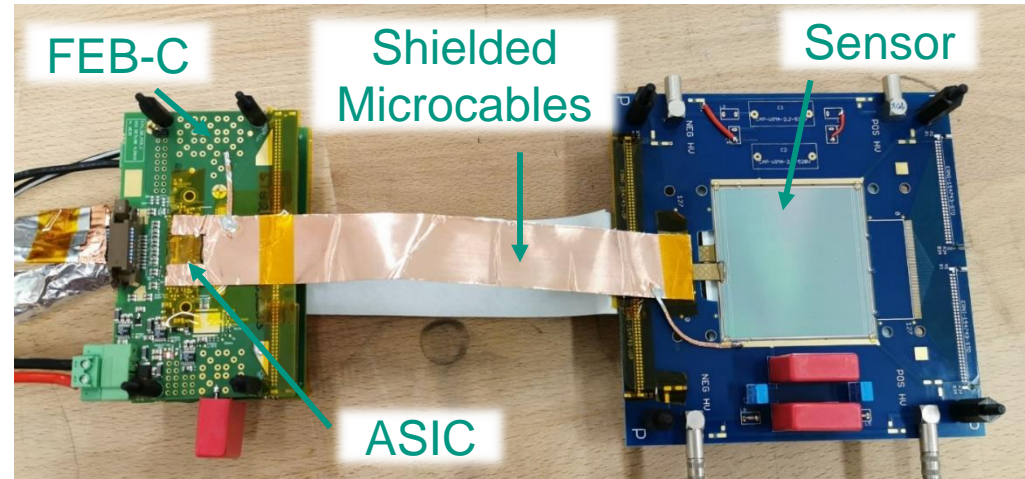


X-ray inspection



Test setup small-scale prototypes

- Asymmetric bias at 150 V
- One microcable each on n- and p-side
- 2 x FEB-C each hosting one readout ASIC
- Readout via AFCK hosting Kintex7 FPGA controlled by IPbus protocol



ENC evaluation on prototype modules

- Simple ENC parametrization based on capacitive load seen by CSA

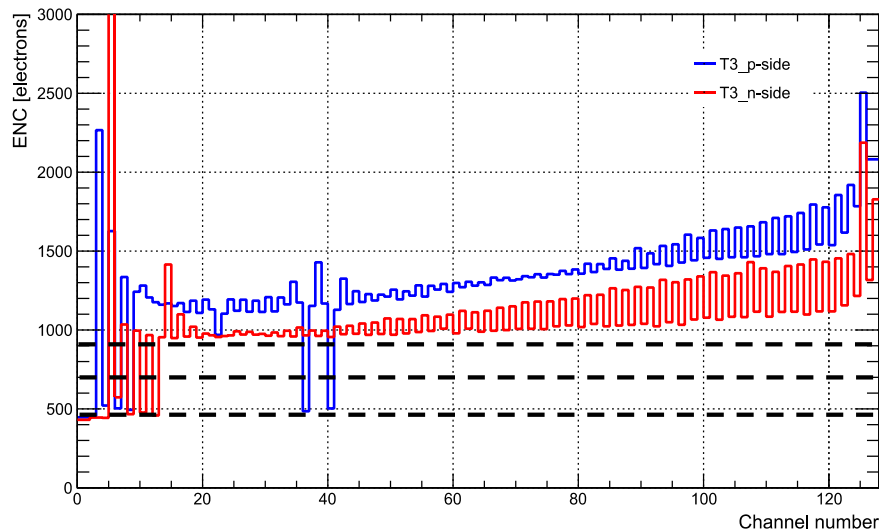
ASIC	Cable	Sensor	
Alu: 460 e ⁻	+ (0.35 $\frac{\text{pF}}{\text{cm}}$ * 25 cm	+ 1.52/1.74 $\frac{\text{pF}}{\text{cm}}$ * 4.2 cm)	* 27.4 $\frac{\text{e}^-}{\text{pF}}$ = 875/900 e⁻
Cu: 460 e ⁻	+ (0.38 $\frac{\text{pF}}{\text{cm}}$ * 20 cm	+ 1.52/1.74 $\frac{\text{pF}}{\text{cm}}$ * 6.2 cm)	* 27.4 $\frac{\text{e}^-}{\text{pF}}$ = 926/964 e⁻

ENC evaluation on prototype modules

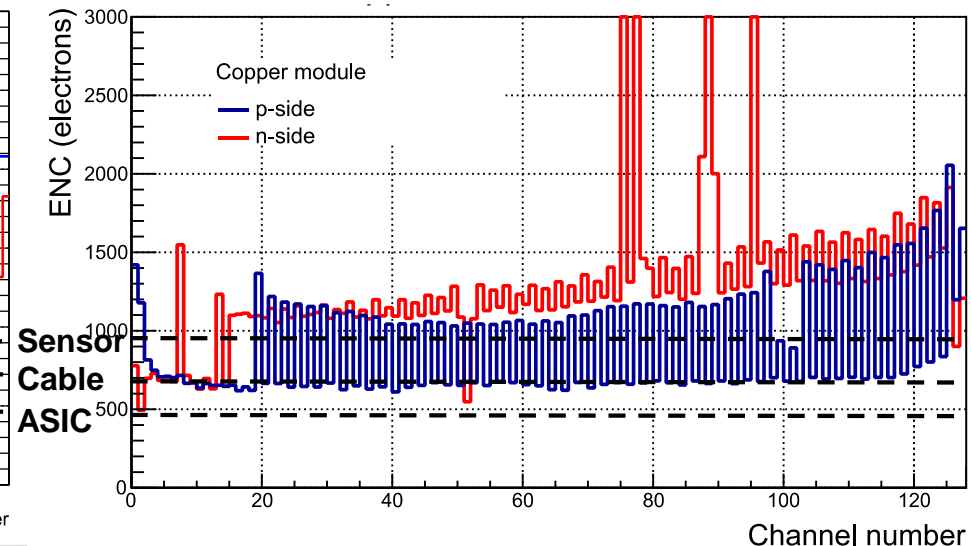
- Simple ENC parametrization based on capacitive load seen by CSA

$$\begin{array}{c}
 \text{ASIC} \qquad \qquad \text{Cable} \qquad \qquad \text{Sensor} \\
 \text{Alu: } 460 \text{ e}^- + \left(0.35 \frac{\text{pF}}{\text{cm}} * 25 \text{ cm} + 1.52/1.74 \frac{\text{pF}}{\text{cm}} * 4.2 \text{ cm} \right) * 27.4 \frac{\text{e}^-}{\text{pF}} = \mathbf{875/900 \text{ e}^-} \\
 \text{Cu: } 460 \text{ e}^- + \left(0.38 \frac{\text{pF}}{\text{cm}} * 20 \text{ cm} + 1.52/1.74 \frac{\text{pF}}{\text{cm}} * 6.2 \text{ cm} \right) * 27.4 \frac{\text{e}^-}{\text{pF}} = \mathbf{926/964 \text{ e}^-}
 \end{array}$$

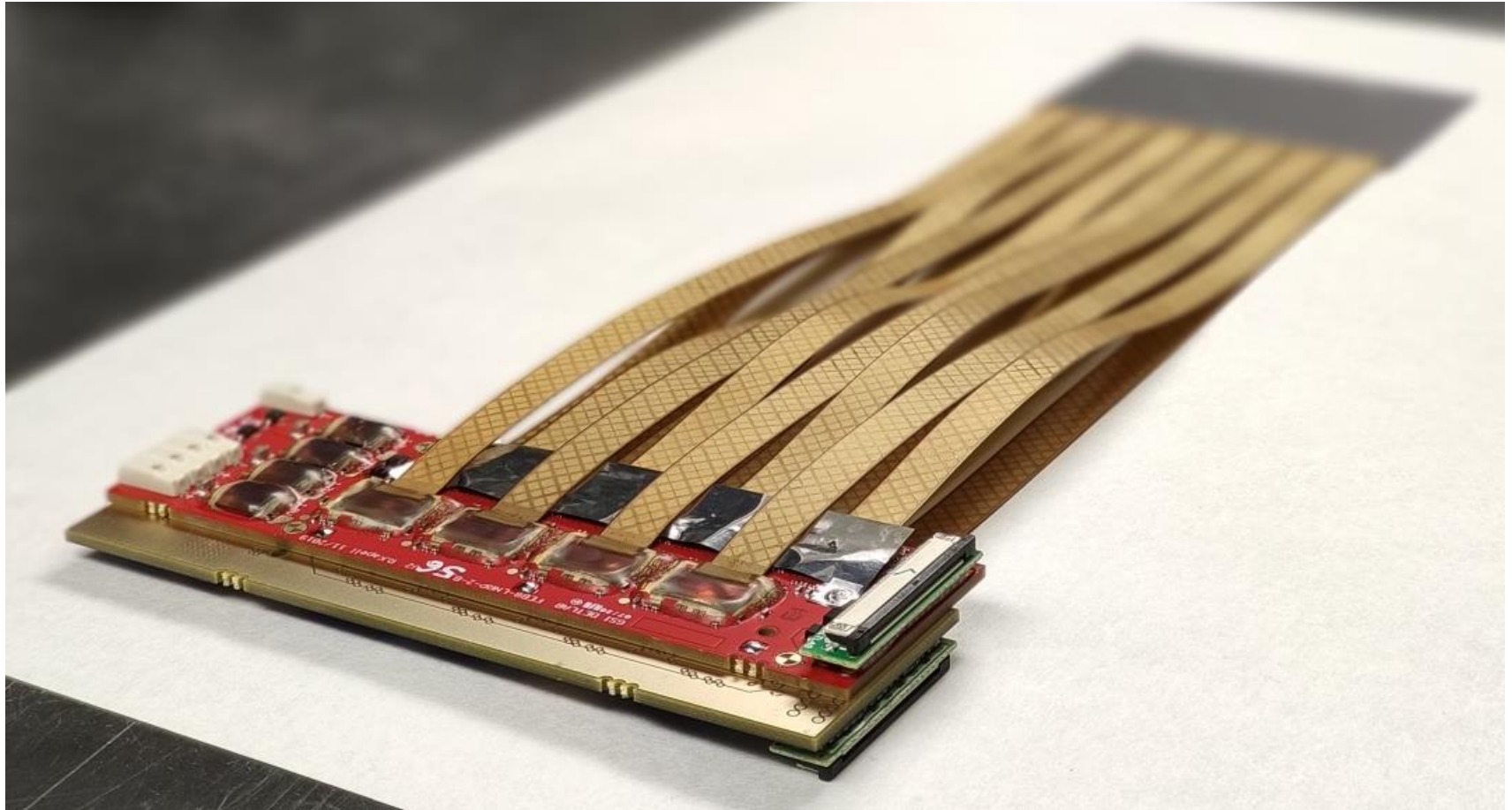
Alu



Cu

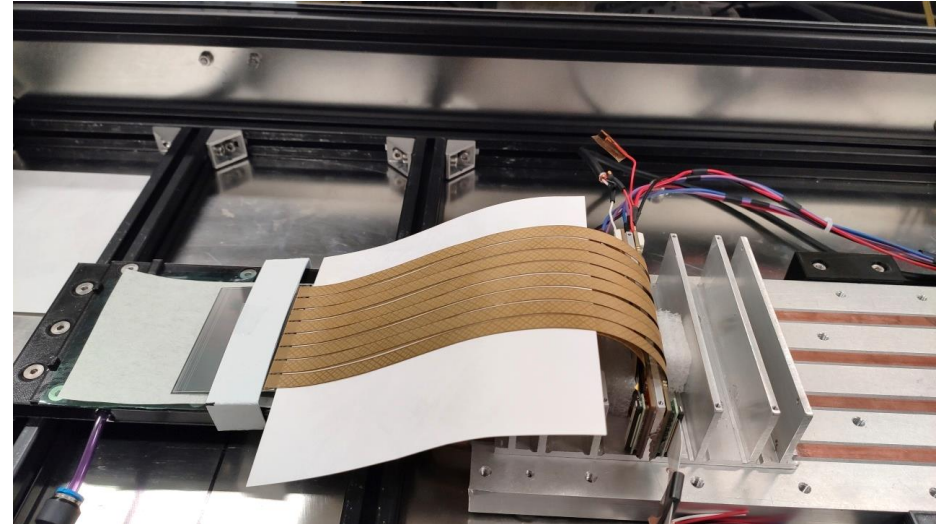


Full-scale prototype

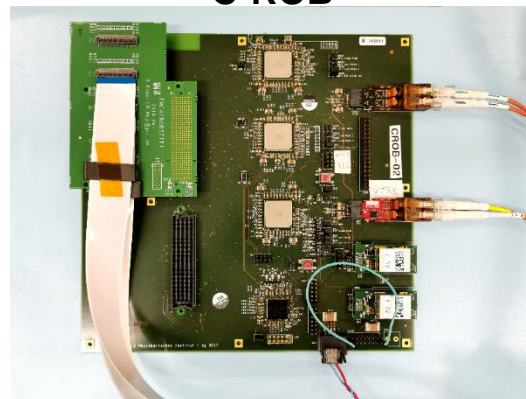


Full-scale prototype testing

- Light-tight shielding box
- Symmetric bias ± 75 V
- Water cooling system
- Readout chain
 - 1. FEB-8
 - 2. C-ROB: data aggregation, electrical to optical interface
 - 3. Data Processing Board (DPB) based on AFCK



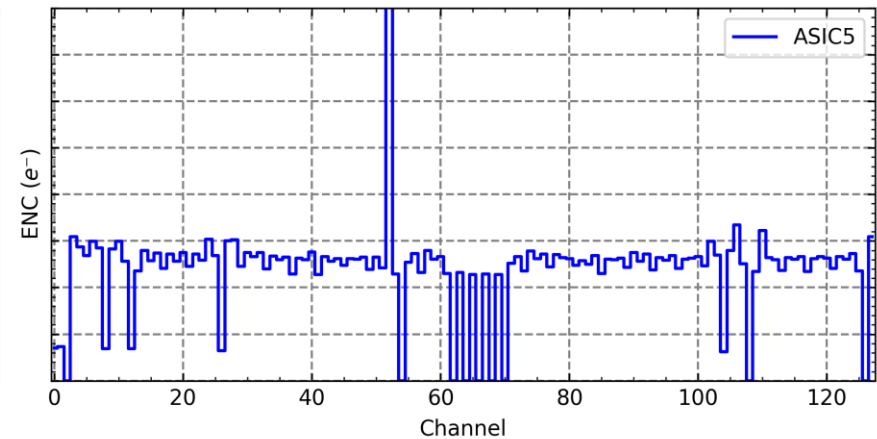
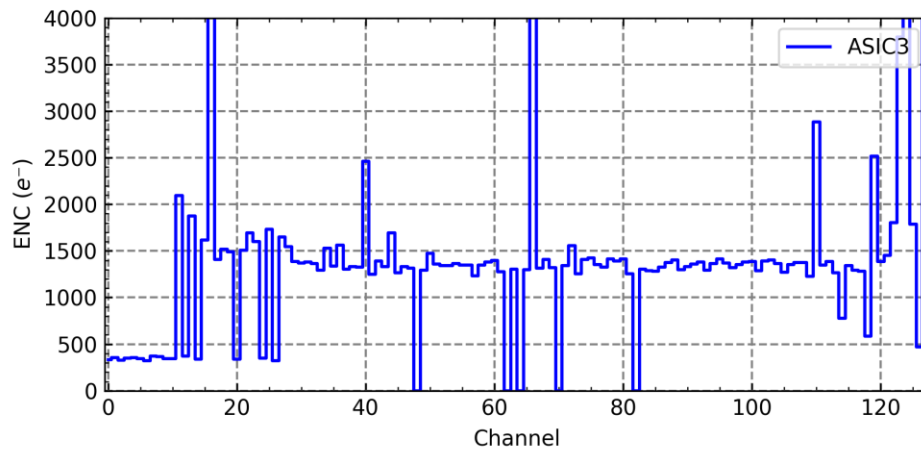
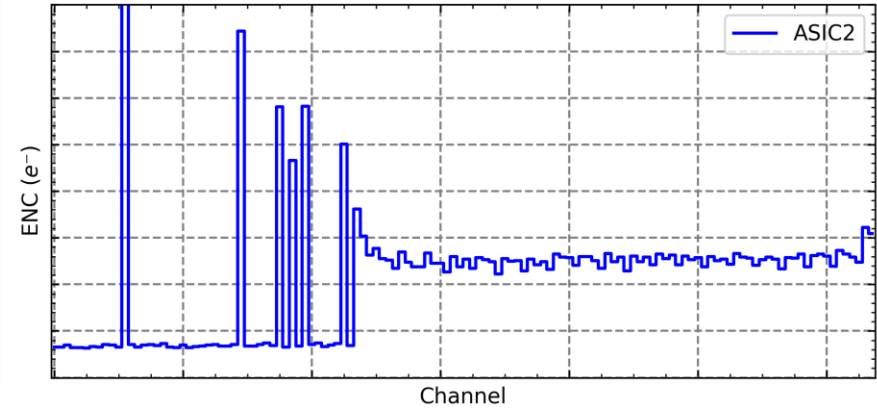
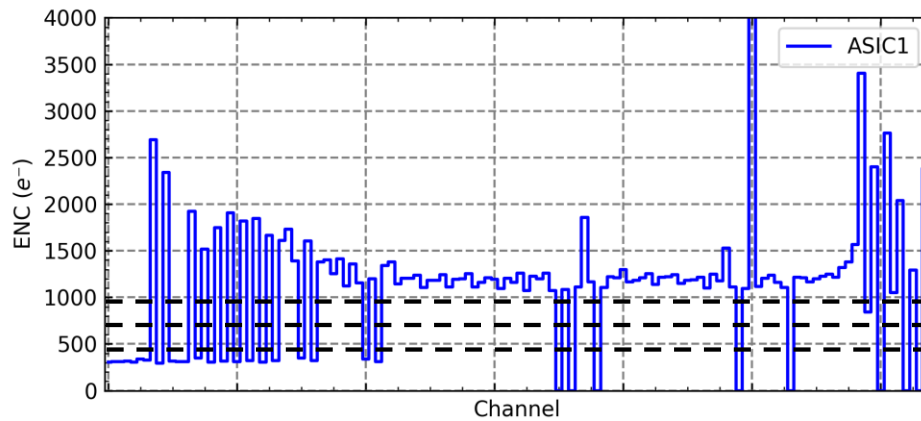
C-ROB



DPB in μ TCA



ENC full-scale prototype: ASICs 1,2,3,5 n-side



Challenges

- Double-layered fine-pitch flex technology on the edge of manufacturing capabilities (yield, cost)
- High demands on precision solder printing
- High demands on planarity between die and cable
- Copper microcable stiffness complicates assembly
- Thermal mismatch due to need for elevated process temperature
- Slightly higher capacitance and material budget compared to aluminum cables

Summary

- A double-layered (2x64 channels) fine-pitch copper cable was developed and characterized
 - Capacitance: 0.38 pF/cm (Alu: 0.35 pF/cm)
 - Material budget: $X/X_0 = 0.05\%$ (Alu: 0.03%)

- A novel high-density interconnection technology has been established
 - Gold stud bumping on the die combined with precision solder printing on the cable assembled in a flip-chip process
 - High degree of automization achievable

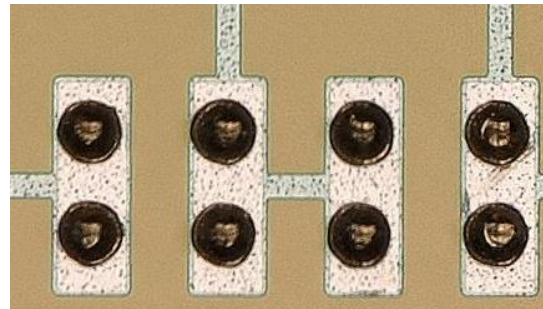
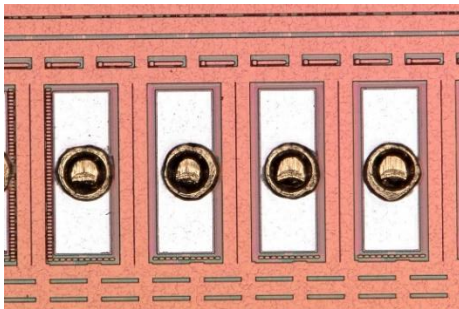
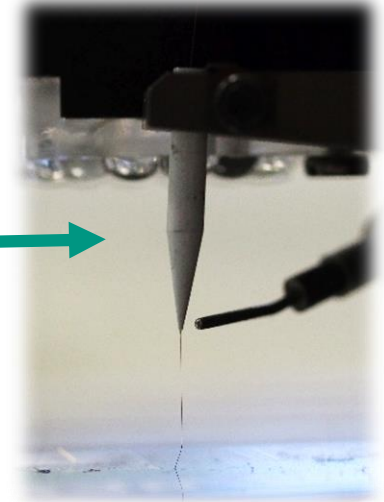
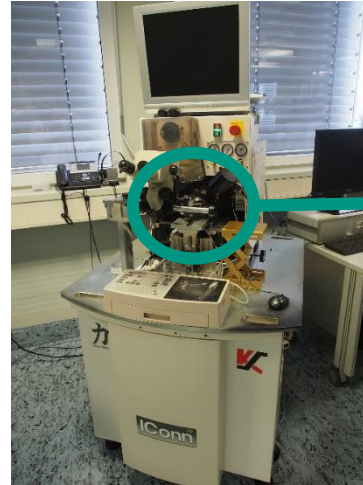
- Prototype modules show electronic performance comparable to established aluminum TAB modules

Thank you for your attention!

BACKUP

ASIC and sensor: Gold stud bumping

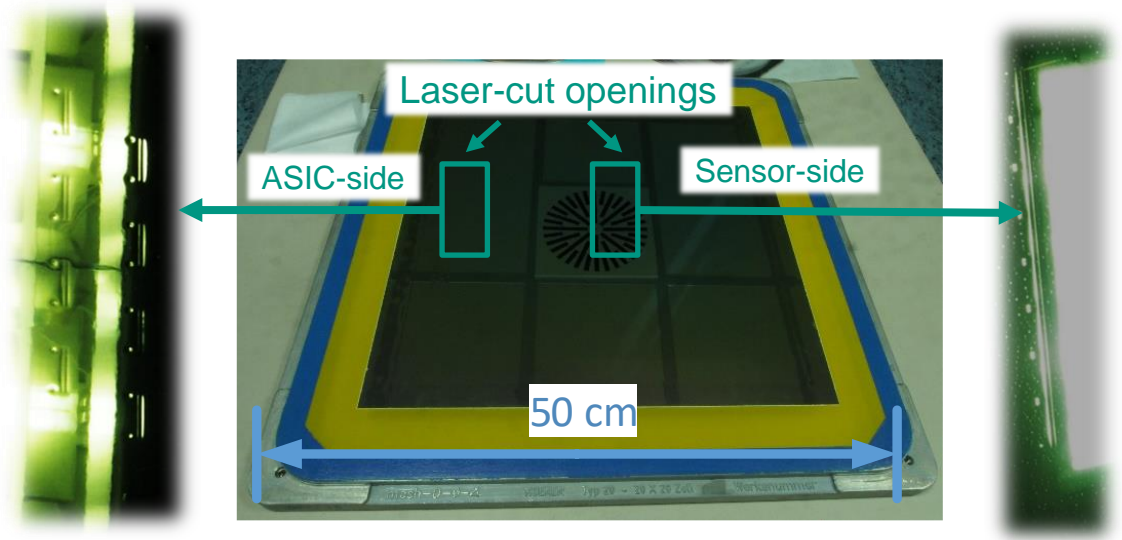
- Iconn ball wire bonder
 - 20 bumps/s
- STS parameters
 - 23 μm Au wire
 - Bump diameter 55 μm
 - Bump height: 30 μm



Fast, flexible, reliable

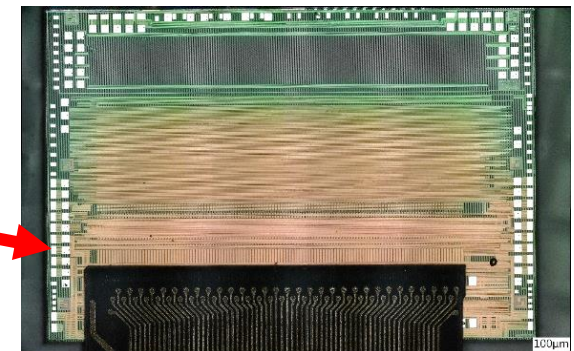
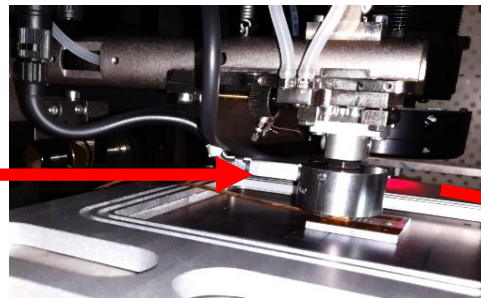
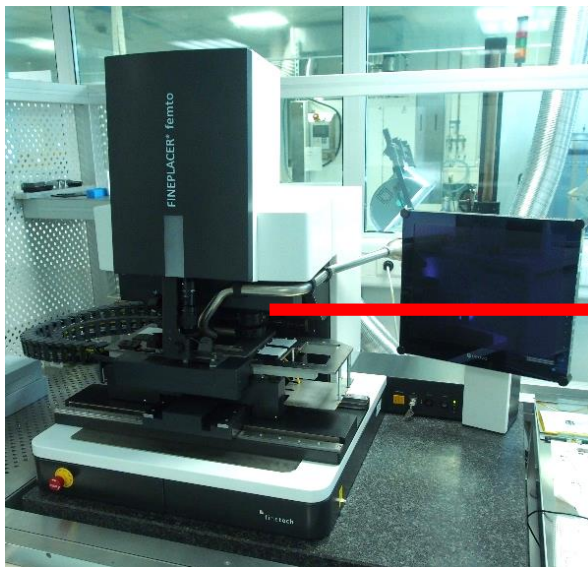
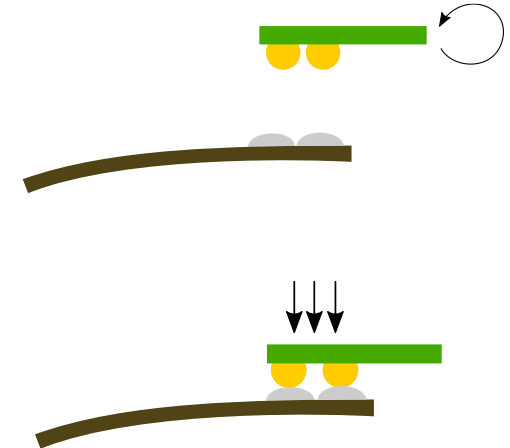
Solder paste type 7/8 printing and reflow

solder paste



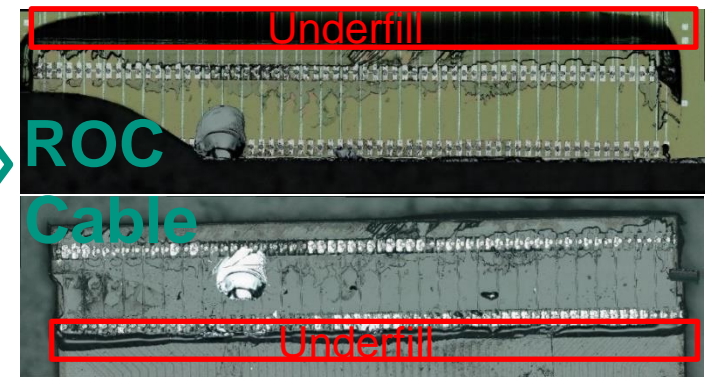
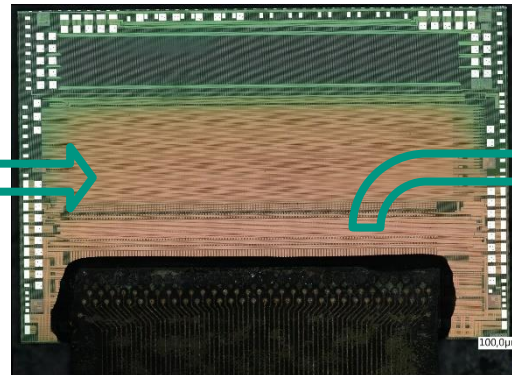
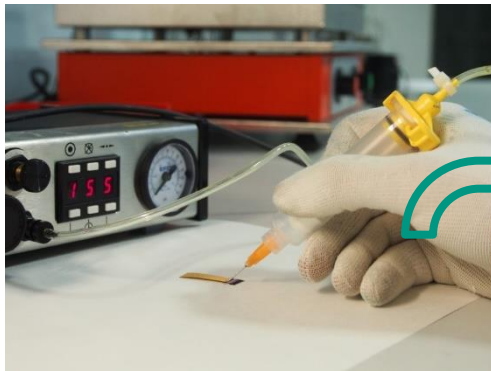
ASIC – microcable interconnection

- Fineplacer femto flip chip machine with 0.5 μm alignment accuracy
- Thermocompression bonding process
 - $F = 40\text{ N}$
 - $T = 230\text{ }^{\circ}\text{C}$



Underfill application

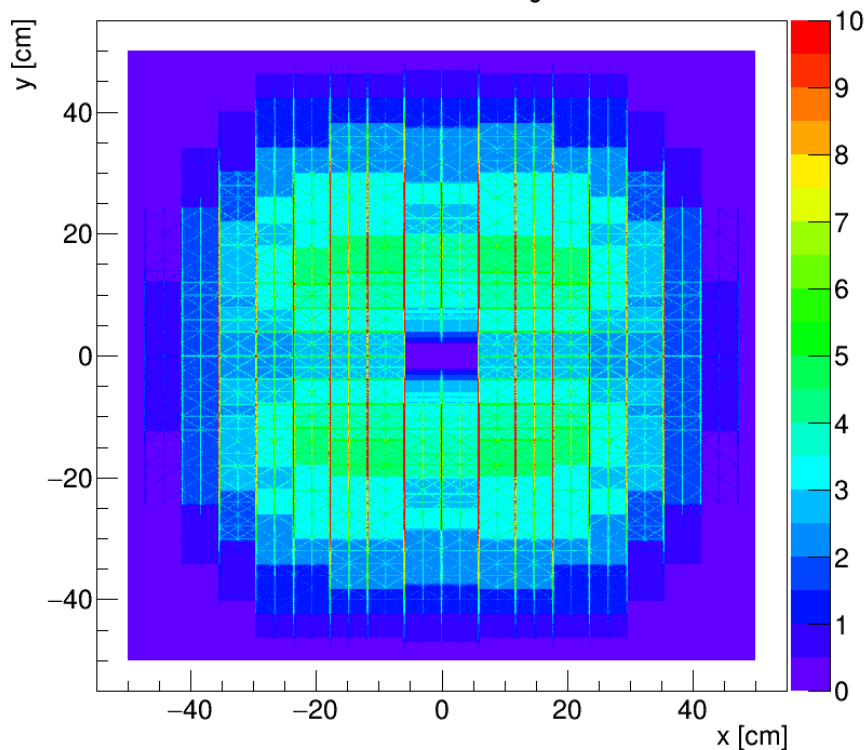
- Improves mechanical strength to survive CBM lifetime of 10 years
- Spark protection between LV microcable and HV sensor edge
- Gap height $\sim 25 \mu\text{m}$, obstructions by gold bumps
- Polytec EP601-LV ()



STS material budget simulations

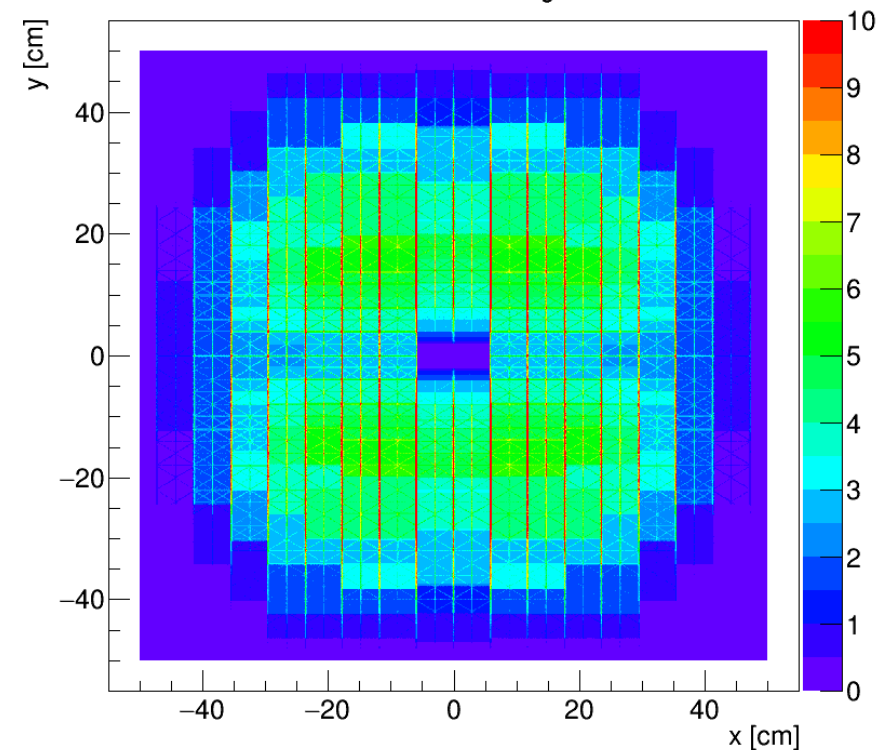
Aluminum microcables

Material Budget x/X_0 [%], STS

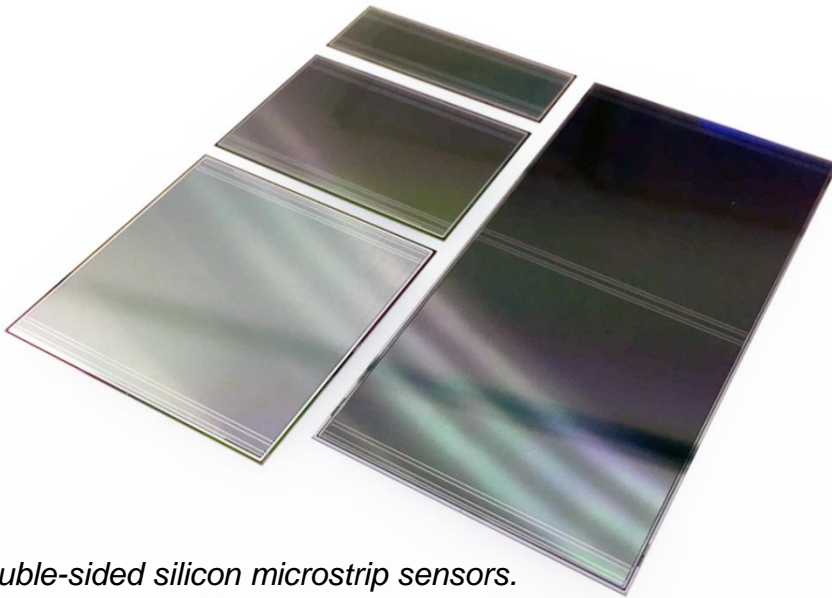


Copper microcables

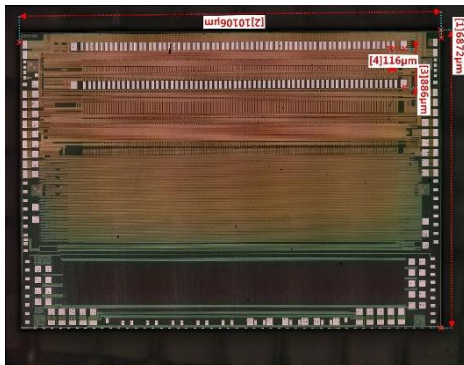
Material Budget x/X_0 [%], STS



Module components



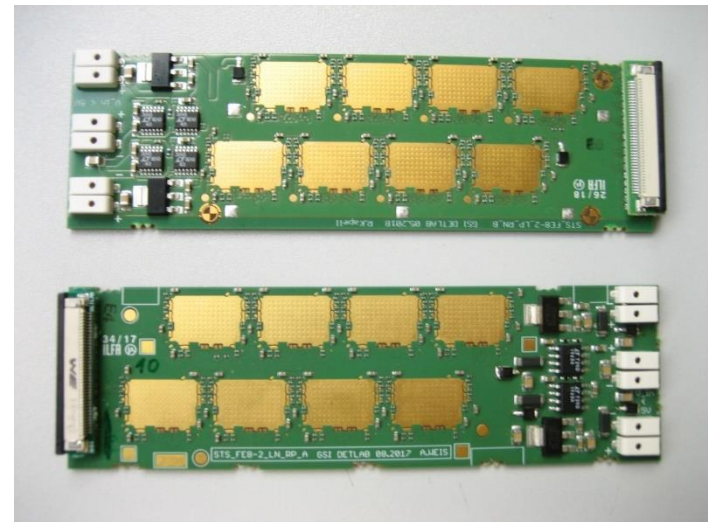
*Double-sided silicon microstrip sensors.
Thickness: 300 μm . Sizes: 62 mm x 22, 42, 62,
124 mm*



STS-XYTER



Low mass microcables with varying length. Top: single cable. Bottom: sheet of 8 cables.



FEB-8 for p- and n-side

Silicon microstrip sensors

- $285/320 \pm 15 \mu\text{m}$ thick
- n-type silicon
- double-sided segmentation
- 1024 strips of $58 \mu\text{m}$ pitch
- strip length 2/4/6/12 cm
- angle front/back: $7.5/0^\circ$
- n-side strip insulation: modulated p-spray
- read-out from top edge
- double-metal routing on p-side
- rad. tol. up to $10^{14} \text{ n}_{\text{eq}}/\text{cm}^2$
- rad tol. w.r.t. TID?

