# Tracking charged particles with 10 ps timing precision: 3D-trench silicon pixels

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For the



## The Geometric approach and MEMS technology



## The Geometric approach and sensor speed: CCT



Comparing timing performance of different 3D geometries

Charge Collection Time distributions for different 3D geometries (total drift times of charge carriers) CCT distributions is strictly related to the corresponding ToA distributions and time resolution  $\sigma_t$  (according to the specific F/E stage) Small CCT gives also better radiation resistance





### **Intrinsic resolution of a 3D-trench sensor** Separation of the electronics contribution and first estimate of the

"intrinsic" resolution of the sensor  $\boldsymbol{\sigma}_{ej} = \sigma_n \left[ \frac{dV}{dt} \right]_{Thr}^{-1} \approx t_r \left( \frac{S}{N} \right)^{-1}$ sd] [9 وا [bs] 24 β onic jitter ntrinsic time resolution 22 20 20 18 18 16 14 14 12 12 -120 -100 -80 -60 -140 -120 -100 -80 -60 -40 -20 -20 V<sub>bias</sub> [V] -140 -40 V<sub>biac</sub> [V] Jitter (electronics only, estimate [1]) Intrinsic (sensor only, estimate [1])

π <sup>+</sup> beam	+
	1
MCP-PMT 1 MCP-PMT 2	
3D sensor	
	A.

 $\sigma_t$  is obtainable as the quadrature sum of the two contributions.  $\sigma_t$  is dominated by the contribution of the front-end electronics This estimate is pessimistic especially for the intrinsic resolution as includes inextricable systematic effects

(correlations, extrinsic noise)

For further details:

[1] L. Anderlini et al., Intrinsic time resolution of 3D-trench silicon pixels for charged particle detection. *Journal of Instrumentation, 15, P09029,* 2020.

[2] D. Brundu et al., Accurate modelling of 3D-trench silicon sensor with enhanced timing performance and comparison with test beam measurements. arXiv:2106.08191v1 [physics.ins-det], in press on JINST (2021).

Simulation [2]			Measurement [2]	
$V_{\text{bias}}[V]$	$\sigma_{intrinsic}[ps]$	$\sigma_{t}[ps]$	$V_{bias}[V]$	$\sigma_{t}[ps]$
-50	9.6 ± 0.1	18.9 ± 0.2	-50	20.7 ± 0.3
-100	8.0 ± 0.1	16.7 ± 0.2	-110	19.8 ± 0.2
-150	7.0 ± 0.1	16.3 ± 0.2	-140	19.0 ± 0.2

Impinging particles:  $\pi^+$  @ 270 MeV/c



## Speed and uniformity: 3D-trench vs 3D-hexagonal **BEWARE the tails !!!**







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# Timespot1 ASIC 28-nm CMOS

Presently under test

INFN Cagliari, Milano, Torino (Bergamo: LVDS drivers)

Analog row (16x2 AFE)

Digital row: 16x2 TDC + Controls, Conf. registers, I<sup>2</sup>C I/F)

#### Analog (service) column:

- 1 BandGap
- 5 DAC sigma-delta (producing analog levels used by pixels)
- Programmable bias cell (for power consumption)
- bias replicas with source followers.

LVDS driver



## **Timespot1: Analog Front End and TDC**



#### Inverter core amplifier with double Krummenacher FB





#### High resolution – "low" consumption TDC based on DCO and a Vernier architecture

To maximize sustainable rate, **1 TDC** per pixel channel has been integrated

Maximum input signal TDC rate = 3 MHz 24 bits output word (ToA + ToT) serial @160 MHz

Power depends on input rate ≈ 20 µW (stby) – 175 μW (3 MHz)



The TDC gives the phase of the signal wrt the master 40MHz clock The TDC and the counter use the same DCO-generated Clk (~1 GHz)



50x31.5 µm<sup>2</sup>

# **Timespot1 ASIC operation**

**Still very preliminary results**, to be taken as an indication of correct circuit operation. Circuit performance still to be analyzed and understood in detail



Channel #

960 992 1024

TA with ToT corr. [ps]

Istituto Nazionale di Fisica Nucleare

200

150

50

50

45

64

96 128 160

0 32

192 224 256 288 320 352 384

448 480 512 544 576

608

416

σ<sub>τοA</sub> [ps]

V [mV]

INFN



# **Conclusions and perspectives**



- 3D-trench silicon sensors reach intrinsic time resolutions of  $\leq$  10 ps
- They keep to the minimum the impact of slower spots which can cause tails in the ToA distributions
- This is not the case for different, though fast, 3D geometries
- The bottleneck in time resolution is by far due to the electronic stage
- Discrete-component Si-Ge front-ends can reach  $\sigma_{ej} \leq 15 \text{ ps}$  with MIPs (TimeSPOT result)
- In CMOS technology limitations are even higher, especially in large matrix readout (power constraints, uniformity among channels)
- The CMOS 28nm Timespot1 ASIC shows that ≤30 ps on the full chain can be obtained at a reasonably low power consumption. Is this sufficient? How to exploit the higher sensor potential in time resolution?
- The really great challenges on pixel with timing for the inner trackers of the future are
  - 1) integrated electronics,
  - 2) integrated electronics,
  - 3) integrated electronics ...
- More studies and R&D are imperative in this respect.

# Thank you all