Latest developments and characterisation results of the MALTA sensors in TowerJazz 180nm for the High Luminosity LHC

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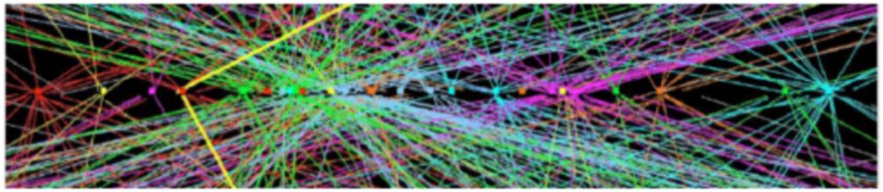
Requirements for future experiments at HL-LHC and beyond

- HL-LHC will deliver 3000 fb^{-1} after Phase II
- Luminosities from 7.5 to $30 \times 10^{34}\ cm^{-2}s^{-1}$
- And from 200 up to 1000 interactions per bunch crossing
- These upgrades present many challenges for electronics and radiation hardness

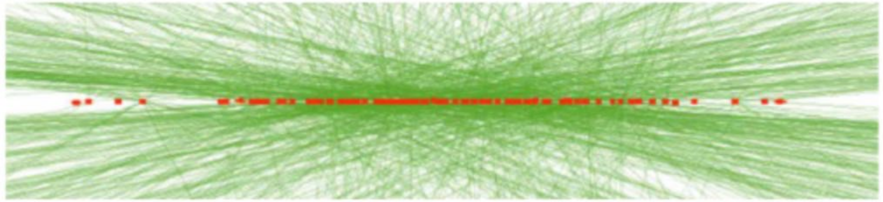
- We need high granularity and time resolution to contribute to the physics searches.
- Aim for small pitch ~30 μm^2 and sub-nanosecond time resolution

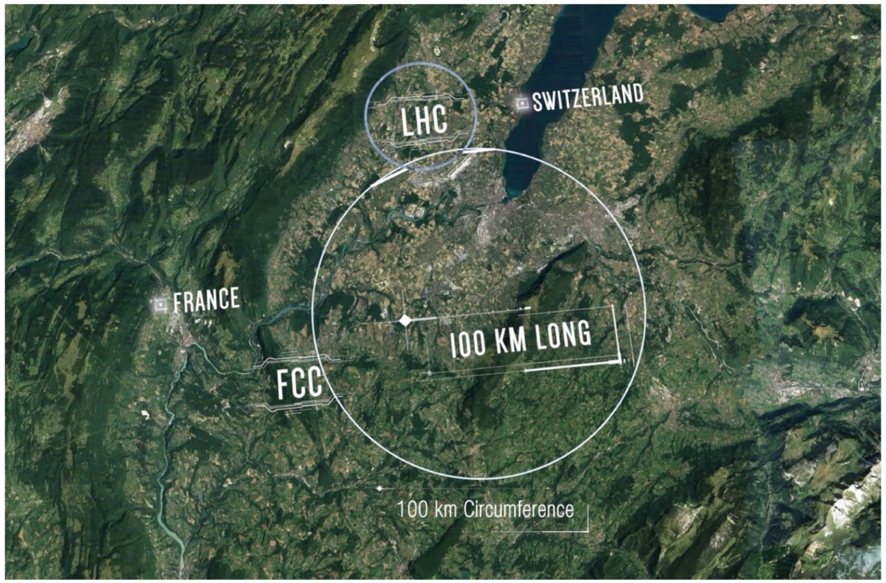
- **Monolithic pixel detectors could address these challenges for the HL-LHC and beyond**

Current LHC: ~25 vertices



High-Luminosity LHC: ~200 vertices

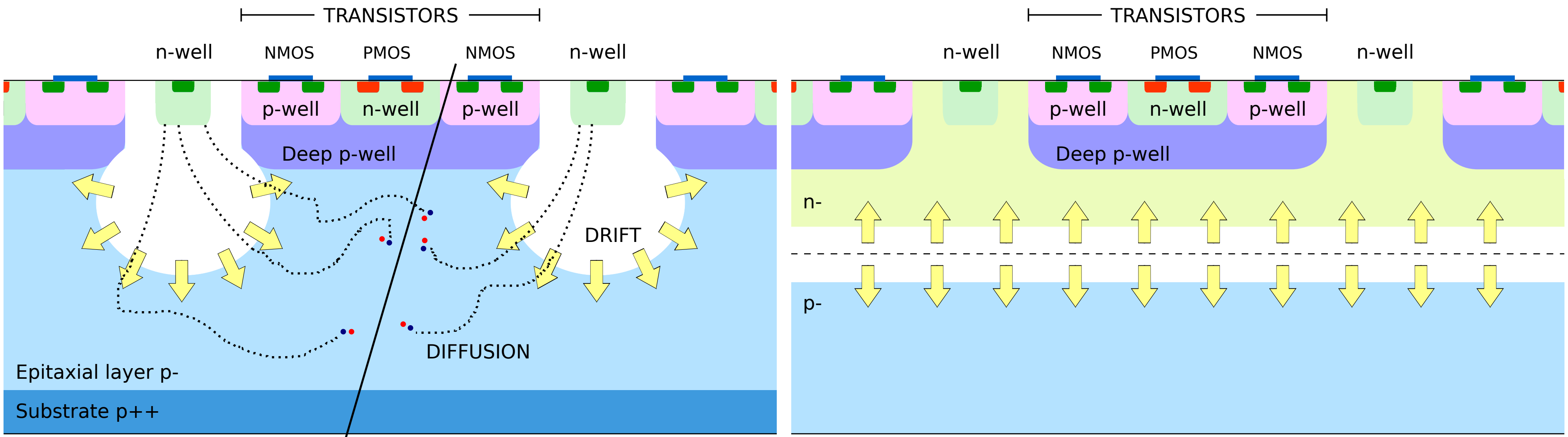




TowerJazz 180 nm CMOS technology

- Commercial TJ 180nm CMOS imaging process with quadruple well with high resistivity (>1 kOhm·cm) epi-layers
- Small collection electrode (3 μm^2)
- Small input capacitance (< 5 fF)
- Small depletion depth (~20 μm) with high signal to noise ratio
- Modified process to ensure full lateral depletion
- Successfully implemented for the ALICE ITS & MALTA development

https://doi.org/10.1016/j.nima.2017.07.046

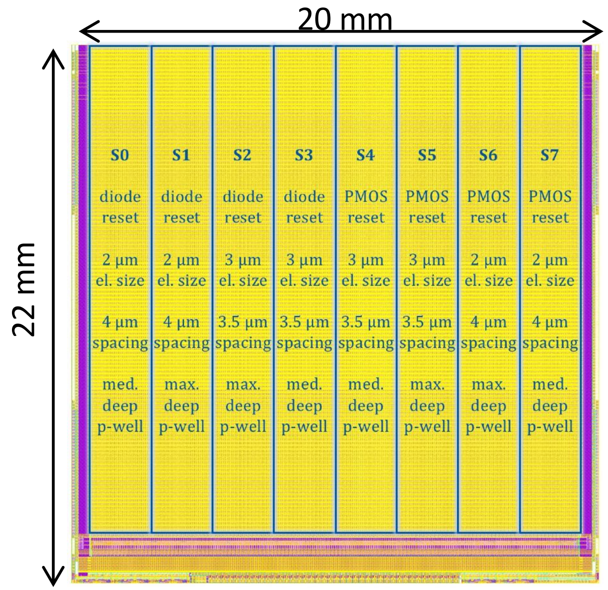


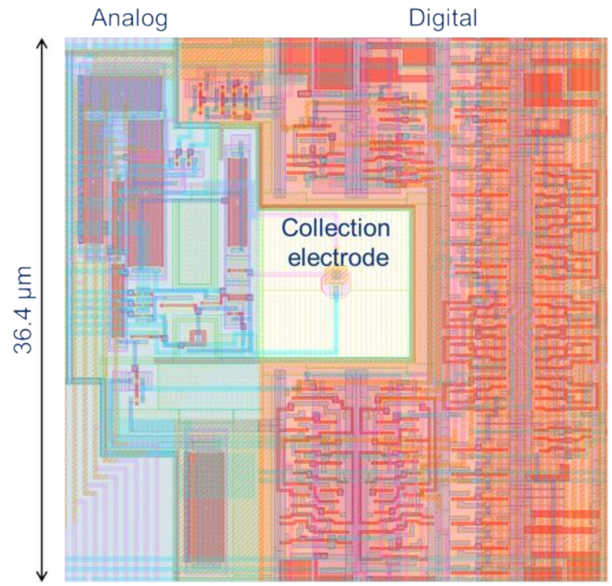
Standard Process

Modified Process

The MALTA Chip

A new R&D development for radiation hard large area monolithic pixel chip.



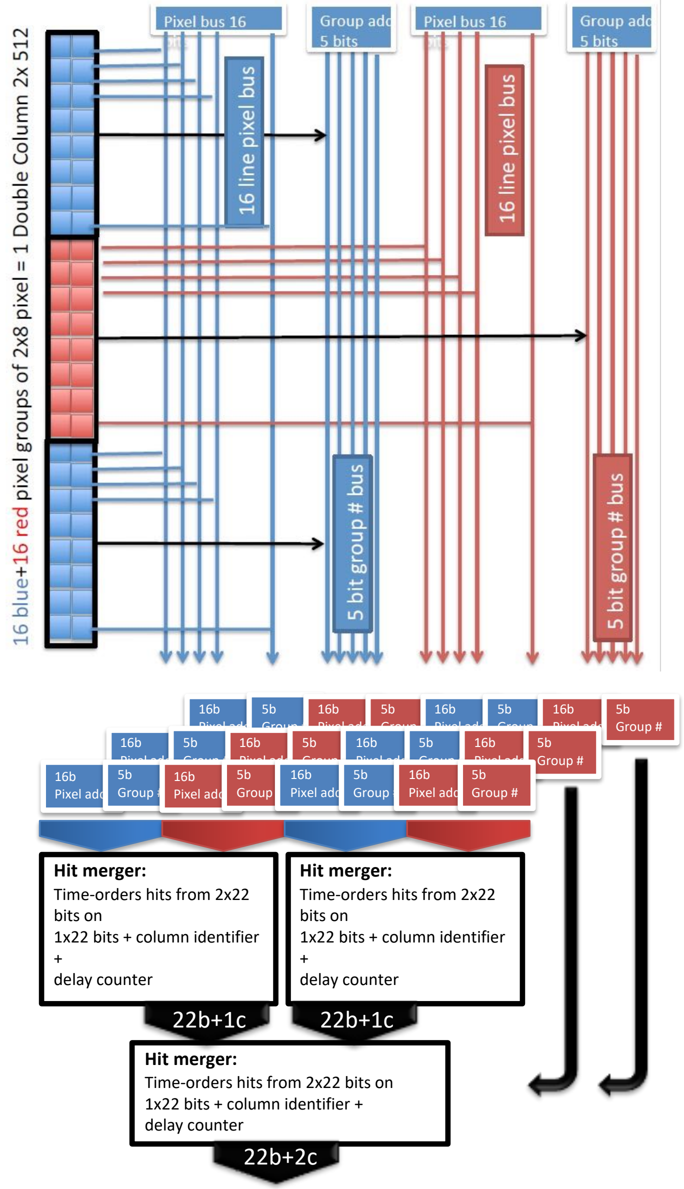


- 22 x 20 mm^2 full size demonstrator
- 512 x 512 pixels
- 8 sectors with different pixel flavors
- Fully clock-less matrix architecture
- Charge information from time-walk
- 10 mW/cm^2 digital power

- Pixel size 36.4 x 36.4 μm^2
- 2-3 μm collection electrode
  - small input capacitance
- 3.4 - 4 μm spacing to electronics
  - low cross talk
- 1 μW/pixel analog power
  - 70 mW/cm^2 analog power

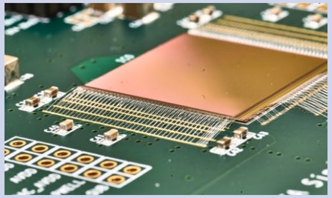
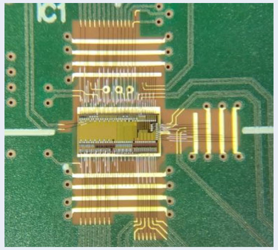
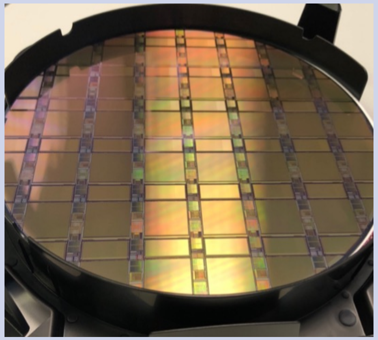
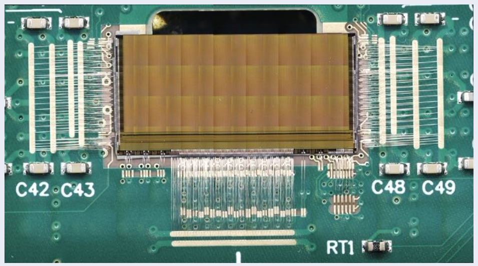
MALTA read-out architecture

- Novel asynchronous readout architecture for high hit rate capability with 40 bit parallel data bus for data streaming
  - Groups of 2x8 pixels with pattern assignment to reduce data size from clusters
  - Front-end discriminator output is processed by a double-column digital logic
  - Pulse width adjustable between 0.5 ns and 2 ns
  - Data transmitted asynchronously over high-speed bus to end of column
- At the periphery, arbitration and merging resolves timing conflicts of simultaneous signals
  - Timing information stored in dedicated bits
  - Output signals transmitted by 5 Gbps LVDS driver



2018 JINST 13 C01023

MALTA R&D Stages

Design	Date	Sensor modifications	Summary
MALTA1 & MALTA1 MLVL 	Jan 2018 Jun 2018	• Continuous n-layer • MLVLC	• Large demonstrator • Asynchronous readout • SlowControl issues
Mini-MALTA & Mini-MALTA ATTRACT 	Jan 2019 Jun 2020	• Cascoded FE • Process modification	• Small demonstrator $1.7x0.5cm^2$ • Serial output • Full efficiency after $1E15\ n_{eq}/cm^2$
MALTA C & MALTA Cz 	Aug 2019	3 types of process modifications	• Large demonstrator $2x2cm^2$ • Slow control improvements • Enlarged cluster size and improved time resolution
MALTA2 	Oct 2020	• Mini-MALTA FE • 3 types of process modifications • Different doping levels	• Smaller matrix $2x1cm^2$ • New SlowControl • Baseline for CERN EP R&D WP 1.2

MALTA1 Performance - Cluster size & Efficiency results

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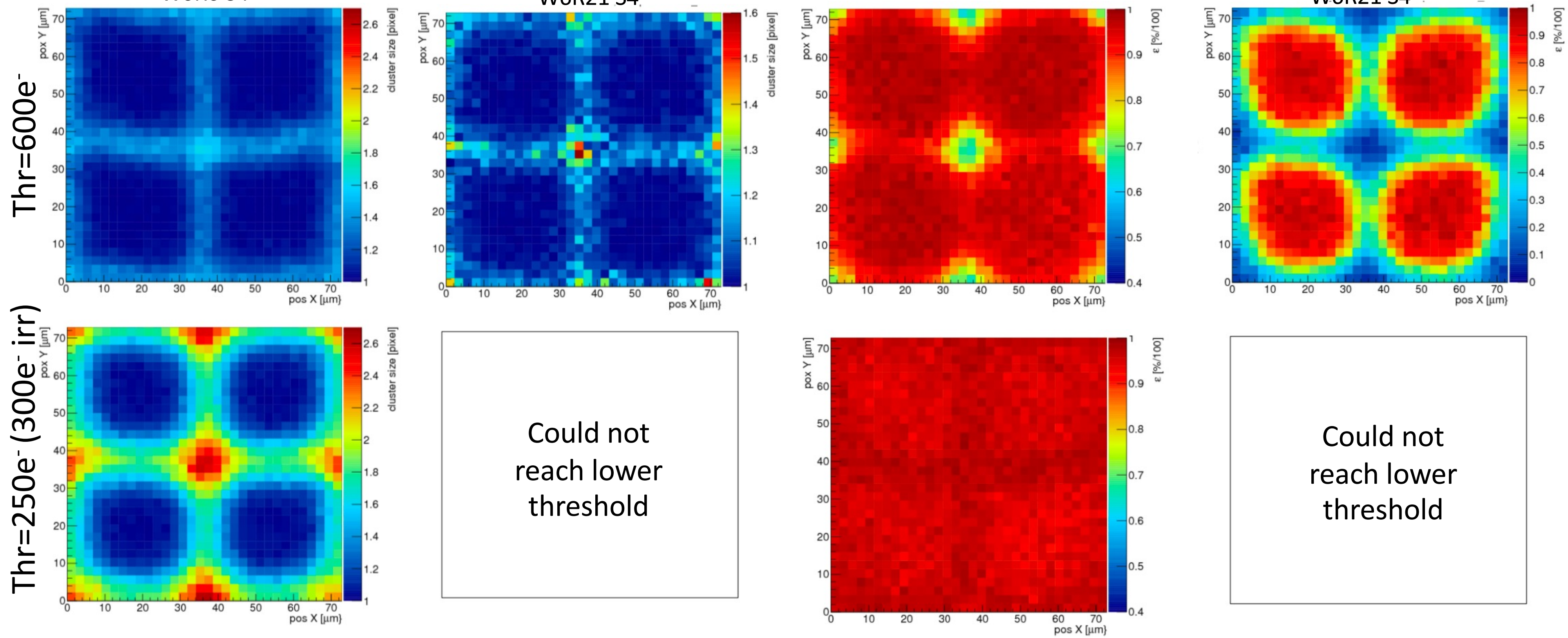
Cluster Size

Efficiency

Unirradiated W6R6 S4 | $5E14\ n_{eq}/cm^2$ W6R21 S4 | Unirradiated W6R6 S4 | $5E14\ n_{eq}/cm^2$ W6R21 S4

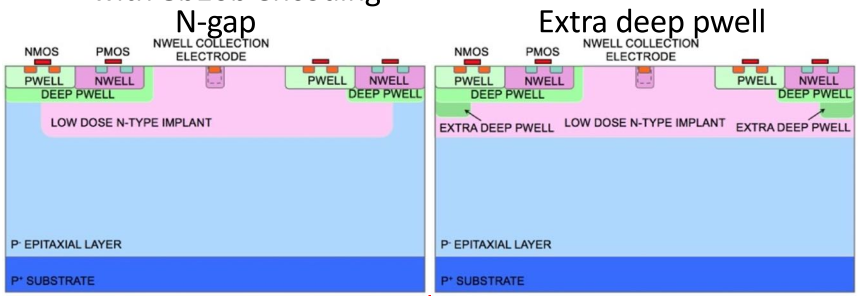


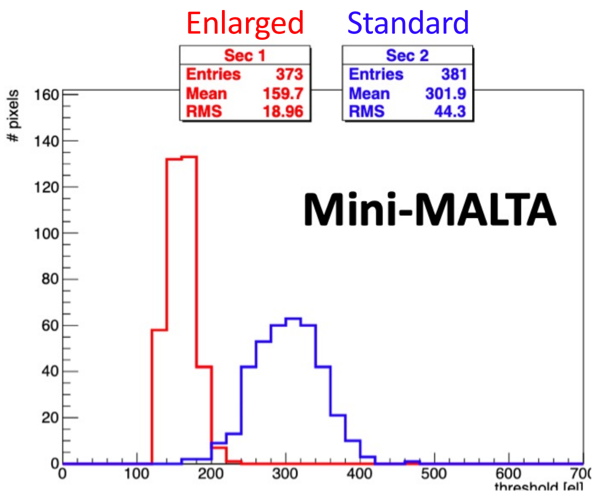
- Efficiency losses observed in pixel corners, which are further lowered after irradiation.
- Measurement at low threshold could not be achieved for irradiated samples. Addressed in next R&D iterations.

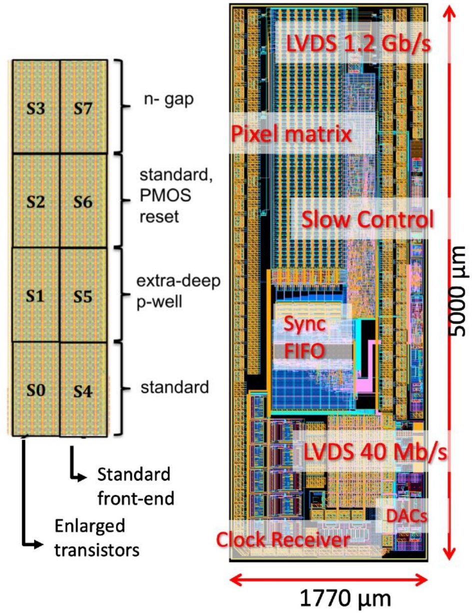
The Mini-MALTA chips

Aim to improve MALTA efficiency loss after irradiation

- Matrix 64x16 pixel with 36.4µm pitch
- 8 sectors with different analogue front-end design
- Single serial data stream: 40Mbps or 1.2 Gbps with 8b10b encoding





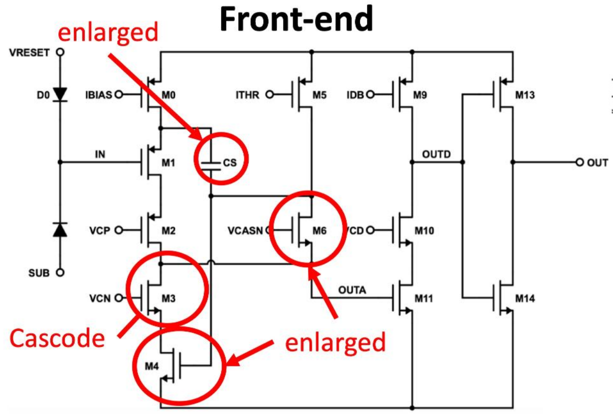


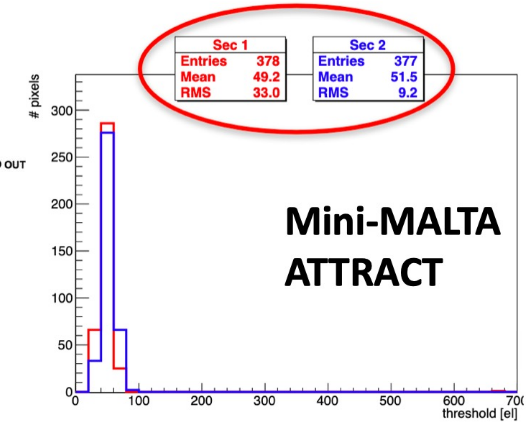
- **Improved SlowControl implementation**
- **Implemented gap in n-layer and extra deep p-well process modifications**
- **Periphery data synchronization using a custom RAM memory**
- **Larger capacitors to reduce noise**

Further design iteration:
The Mini-MALTA ATTRACT

- All sectors have cascode front-end (M3) and enlarged transistors

- **Mini-MALTA design lead to reduced noise**
- **Mini-MALTA ATTRACT allowed even lower threshold**





Mini-MALTA Performance - Efficiency

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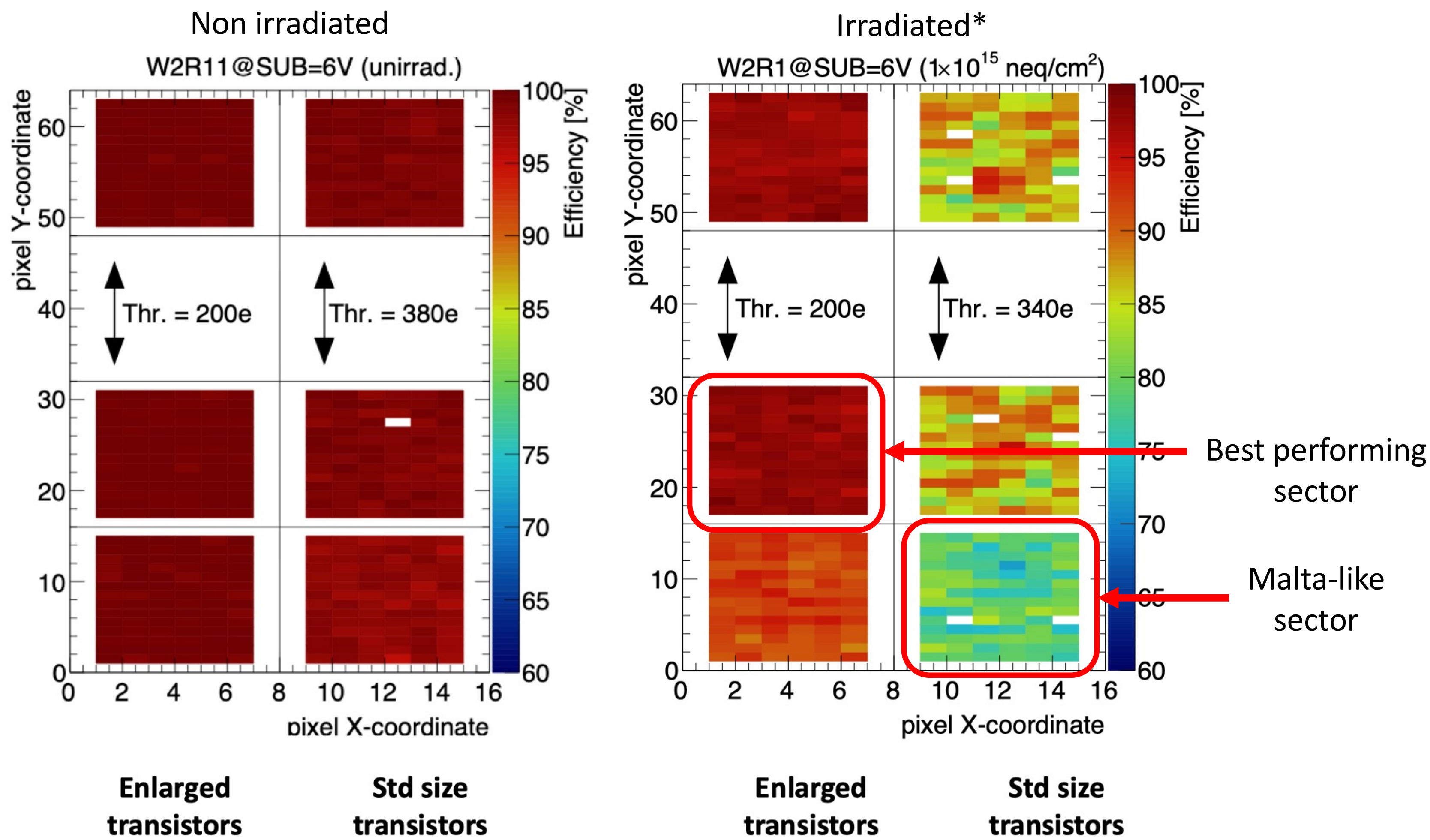
- Full efficiency after irradiation at $200e^-$ threshold at 6V bias on sectors with enlarged transistors.
- Due to improved charge collection in the pixel corners with respect to previous design (MALTA1).
- Also observed with focused x-ray beam at Diamond Light Source, NIM A 956 (2020) 163381
- Higher efficiency for enlarged transistors, being above 97%.
- *Irradiated to 1E15 n_{eq}/cm^2 , and measured with 2 GeV electron beam at ELSA, with 6V bias voltage.



Mini-MALTA ATTRACT Performance - Threshold

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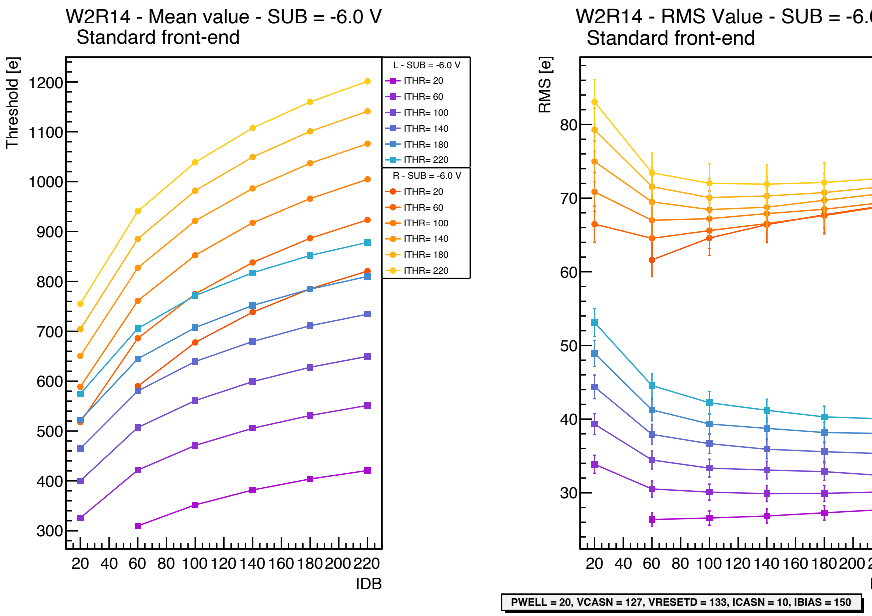
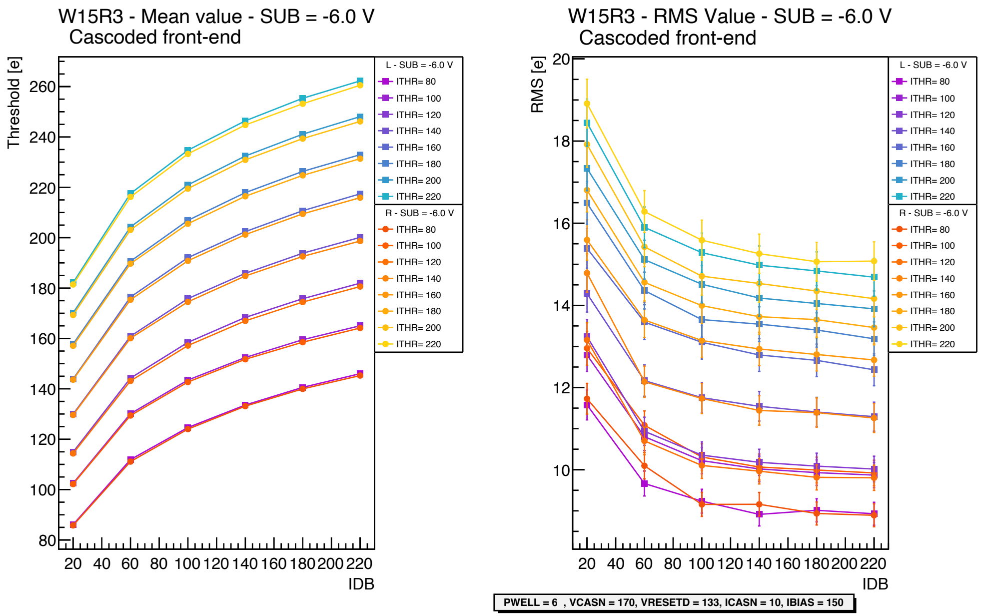
- Introduction of cascoded front-end, allows to reach thresholds below 100e$^-$
- Improvements in front-end control and threshold
- Additionally, more consistent values between enlarged and standard transistors

Standard front-end



Cascoded front-end

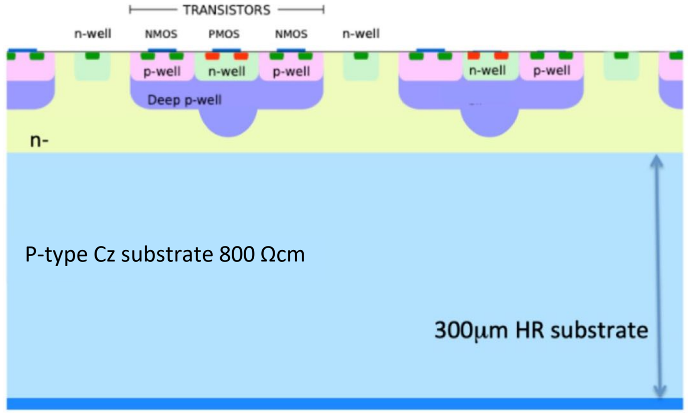


- Cascoded front-end threshold range changes from 80 to 180e$^-$ whereas standard is up to 1200e$^-$
- Strong improvement in threshold RMS from 40-80e$^-$ down to about 10-15e$^-$

The MALTA Czochralski (Cz)

Processed with high resistivity Cz substrate material
- Larger depletion voltage and signal
- Higher radiation hardness
- High operational voltage up to 50V

Efficiency measured at DESY using 4 GeV electron beam



MALTA Cz unirradiated

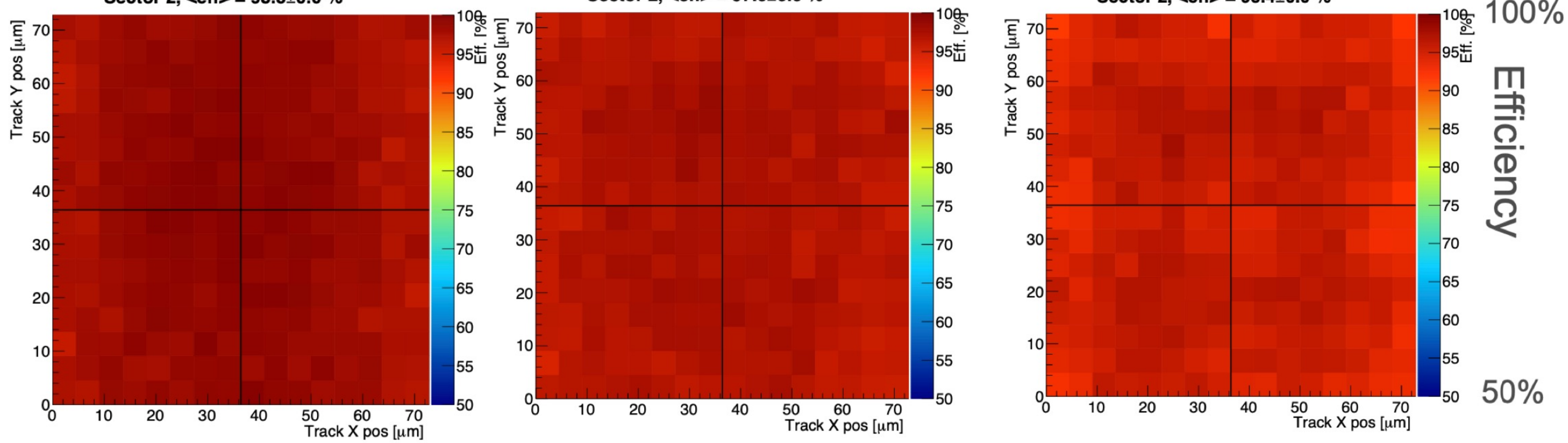
ε = 98.5%

MALTA Cz n-gap $1x10^{15}$ n_{eq}/cm^2

ε = 97.0%

MALTA Cz n-gap $2x10^{15}$ n_{eq}/cm^2

ε = 95.4%



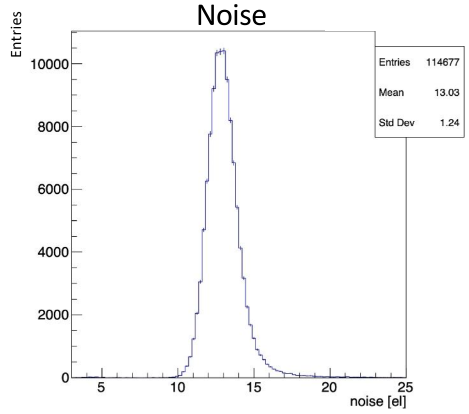
- Radiation hardness of full size MALTA with Cz
- From 98.5 (un-irradiated) to 95.4 % efficiency after 2E15 n_{eq}/cm^2

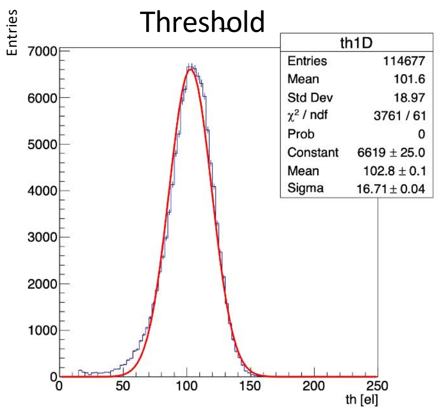
10.1016/j.nima.2020.164381

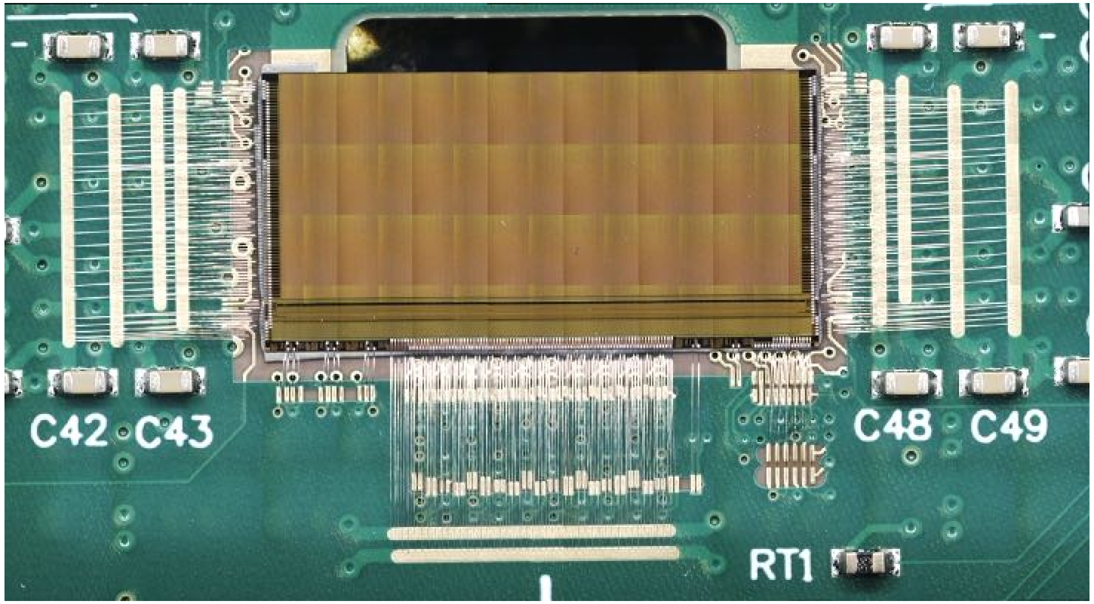
The MALTA2

- Returned from foundry in Jan 2021
- 20.2x10.1 mm² sensor. About half size of MALTA
- Matrix of 224x512 pixels of 36.4 um² size
- Faster analog front-end improves time resolution
- New SlowControl implemented as 4322 bit shift register
- Enlarged transistors as implemented in Mini-MALTA
- Cascode front-end for higher gain and reduced RTS noise (<10e⁻ in unirradiated samples).
- **Applying all the knowledge learnt from MALTA C, Mini-MALTA, ATTRACT and Czochralski**

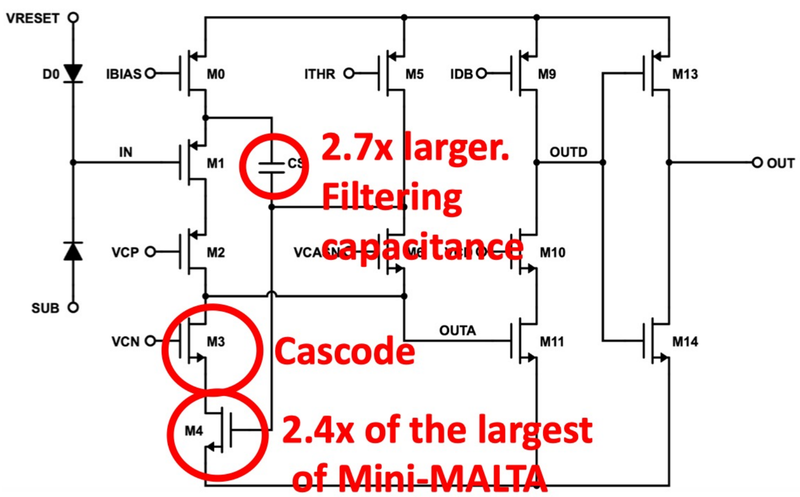
W15R4 2E15 n_{eq}/cm^2, 2 Mrad (ITHR=20)







Analog front end modifications



MALTA daisy chain

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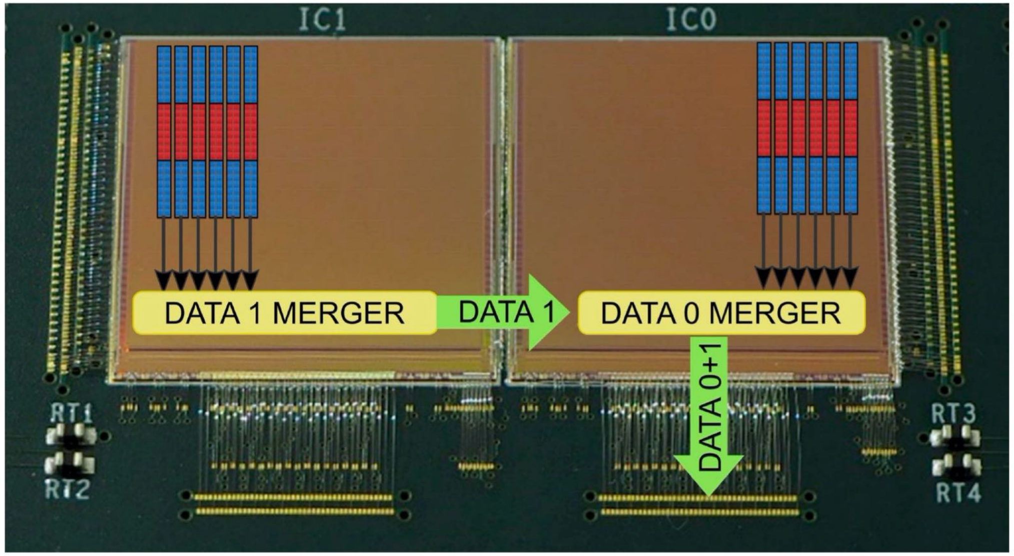
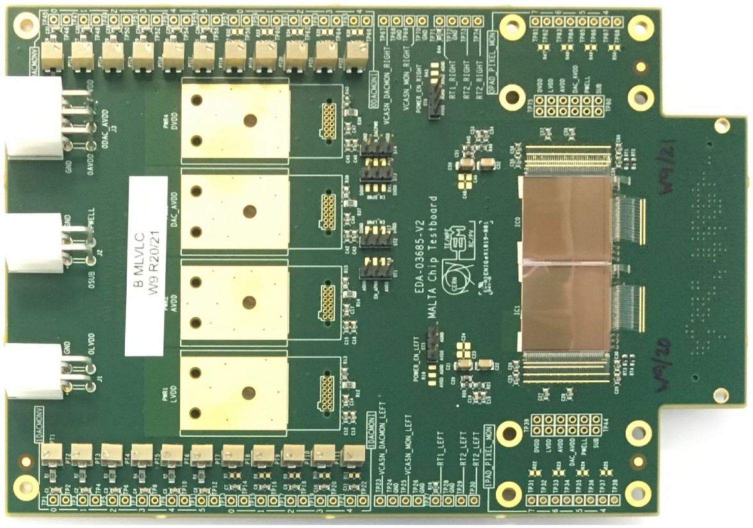
- MALTA1 has fast chip to chip data transfer functionality
- Data from MALTA can be routed to another MALTA to the left or to the right through CMOS outputs
- Aim being to target larger sensing surfaces and reduce services

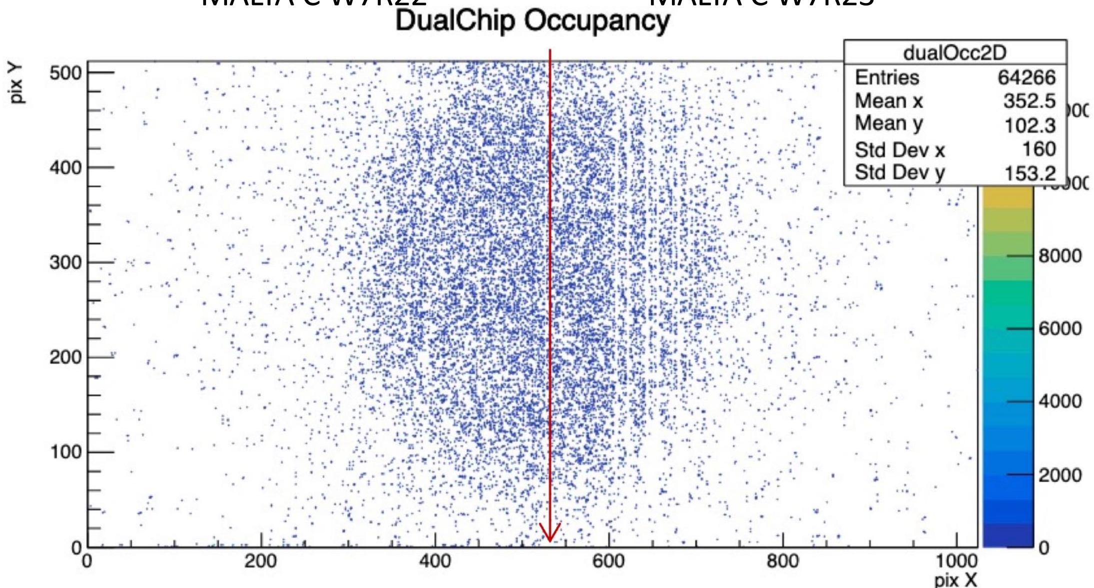


MALTA C W7R22 MALTA C W7R23

Studied in EP R&D WP1.3 activities



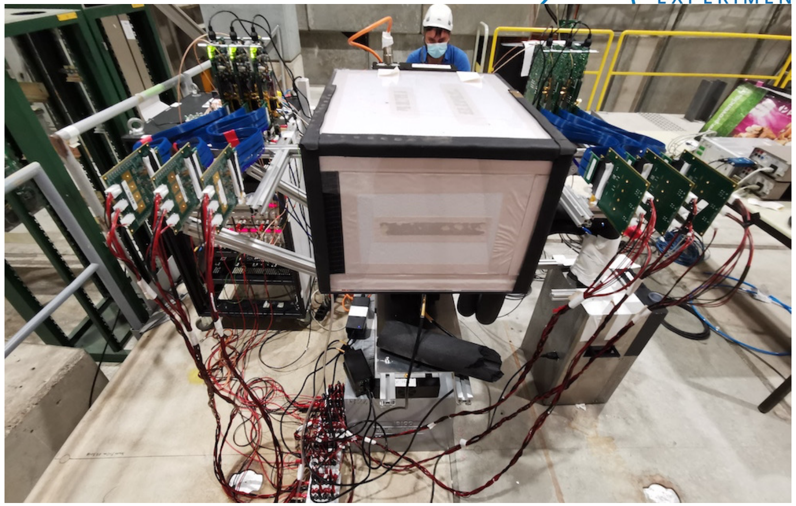
Dual chip carrier board



Occupancy of double chip exposed to Sr-90

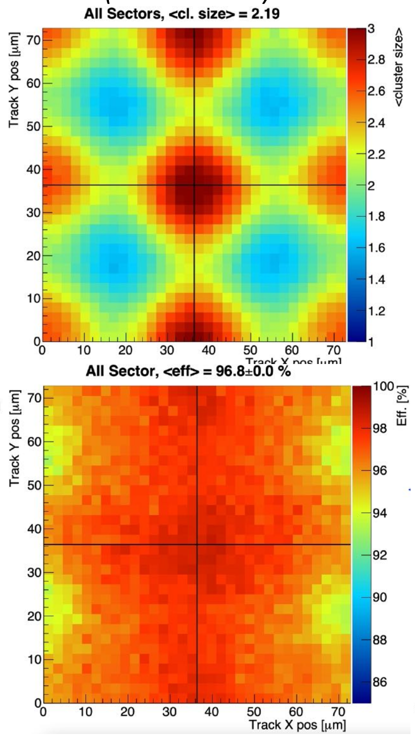
MALTA Telescope

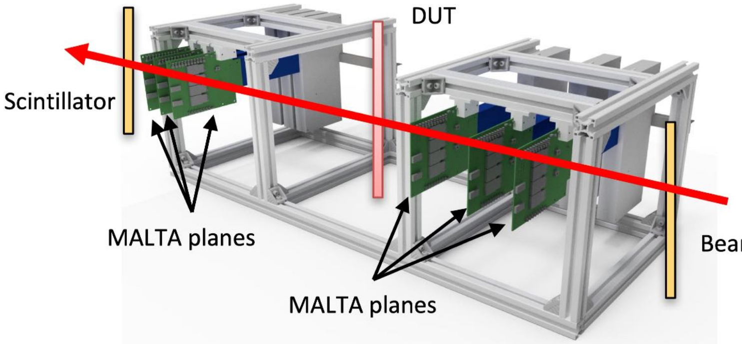
- Using MALTA1 chips to trigger telescope
- Xilinx Virtex-7 FPGA VC707 for readout
- Trigger from MALTA planes as combination reference signals and compatible with AIDA telescopes

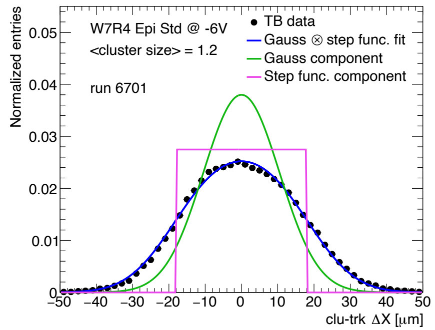


W7R14 (Malta std Cz) SUB=-50 V

*Cluster & efficiency plots from **currently ongoing** SPS campaign*



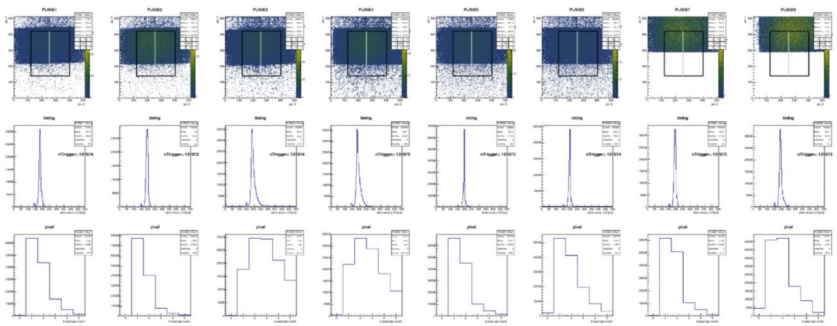




Resolution of ~10.5um as measured at DESY

Key features:

- 4 to 6 MALTA1 reference planes (100 μm thick, 36 μm pitch size)
- Achieving 14 μm track-hit resolution using only 3 tracking planes and General Broken Line (GBL) algorithm in Proteus with 4 GeV e⁻ beam in DESY
- Portable, versatile and flexible telescope essential for continued test-beam during LS2
- Based on custom multi-threaded application



6 plane + 2 DUT DAQ @SPS (currently ongoing)

Conclusions & Outlook

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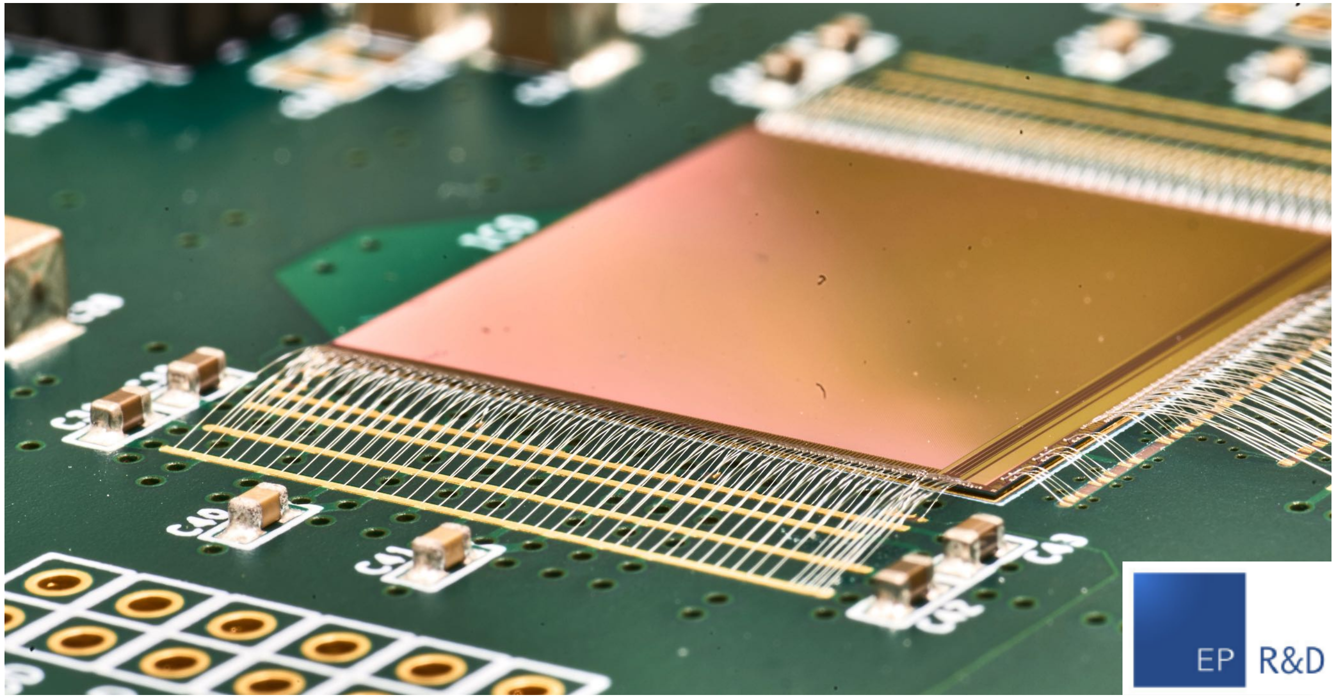
- Large area monolithic chip with chip-to-chip data transfer and routinely thinned to 100 um.
- Portable self-contained telescope system used in multiple placed SPS/DESY.
- MALTA monolithic CMOS sensors continuously improved with excellent performance of Mini-MALTA and Cz iterations.
- Modifications such as the n-gap and extra deep p-well show full efficiency after 100 Mrad and 1E15 n_{eq}/cm^2.
- Many improvements applied to the design of MALTA2 and early measurements show very promising results.

- MALTA3 design already underway and will incorporate latest process modifications, FE design with improved time resolution and asynchronous read-out in a large device.



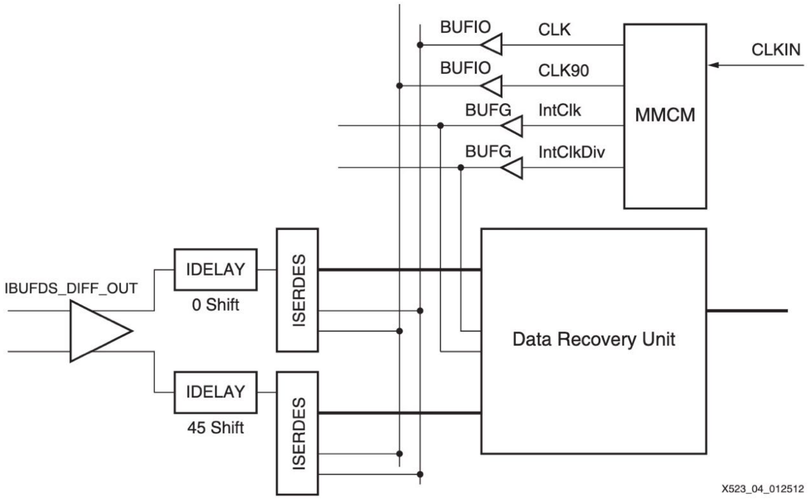
Acknowledgements

- Part of the measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).
- Part of the measurements leading to these results have been performed at the E3 beam-line at the electron accelerator ELSA operated by the university of Bonn in Nordrhein-Westfalen, Germany.
- This project has received funding from the European Union's Horizon 2020 Research and Innovation program under Grant Agreement no. 654168.(IJS, Ljubljana, Slovenia)
- Thanks to Dr. Ben Phoenix, Prof. David Parker and the operators at the MC40 cyclotron in Birmingham (UK) for their support with the irradiations.

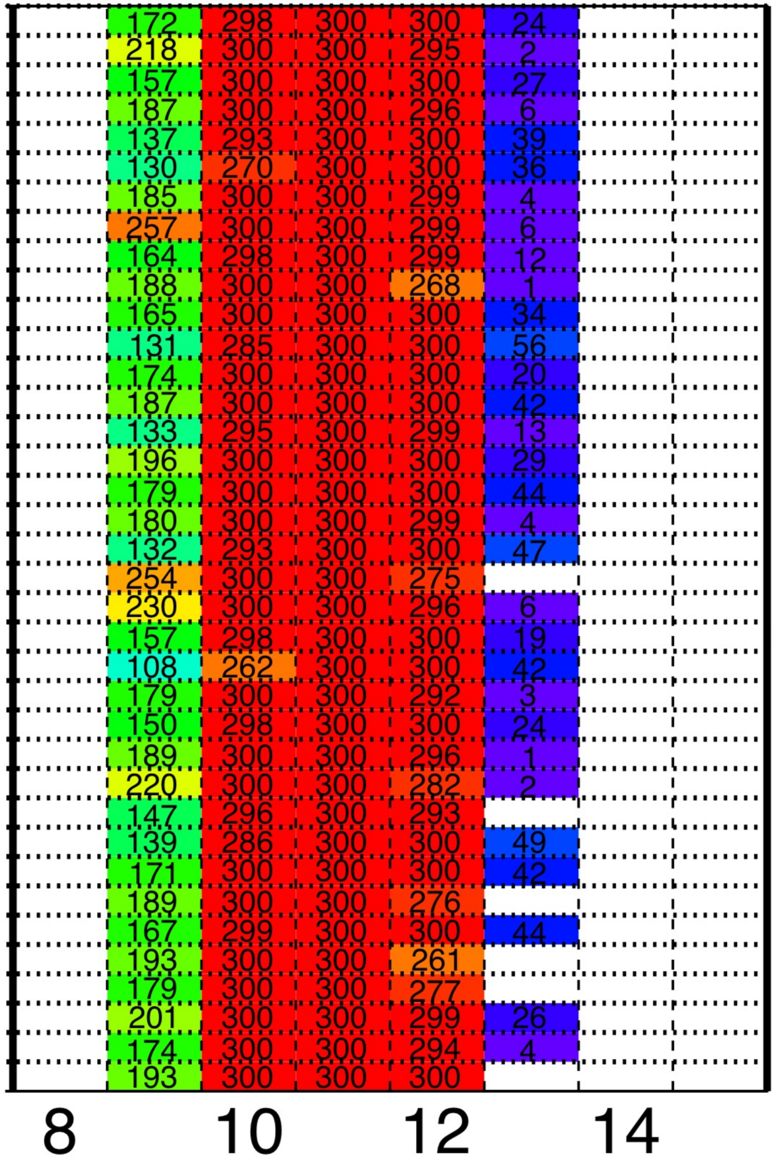
Backup

Asynchronous oversampling

- Read-out on Xilinx 7-series VC707
- Implemented asynchronous oversampling of the data
  - 2 copies of the data (0,45)
  - 2 clock buffers (0,90)
  - 2 samplings per clock (0,180)
  - 8 samples per signal
  - 320 MHz clock domain
  - 4 GHz effective sampling
  - 3 to 4 samples per pulse



Xilinx application note XAPP523



MALTA1 Performance - Effect of the p-well structures

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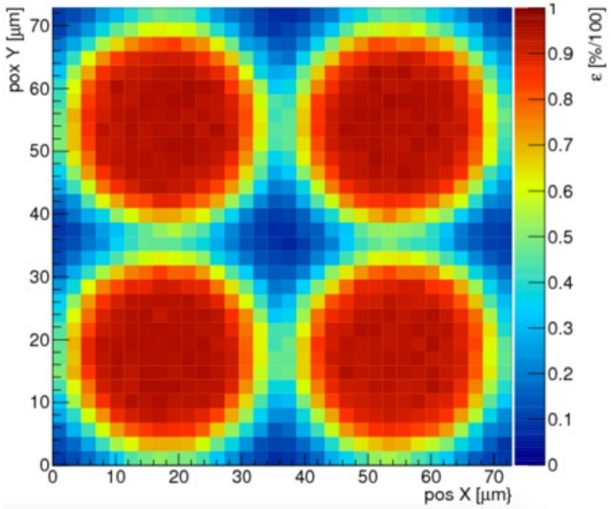
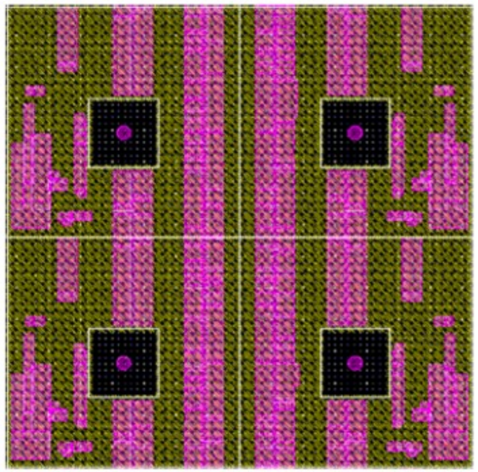
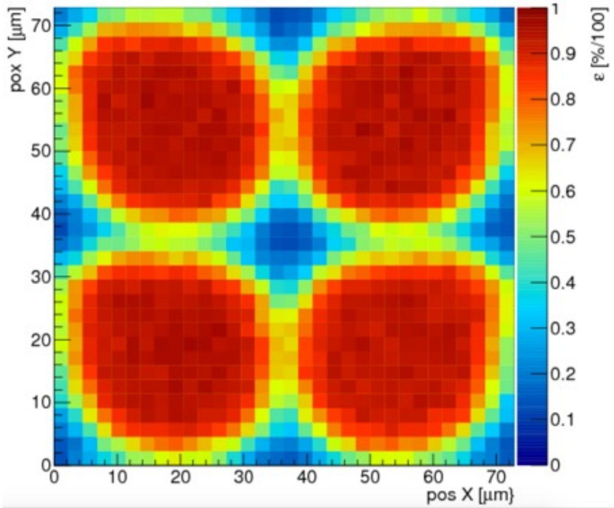
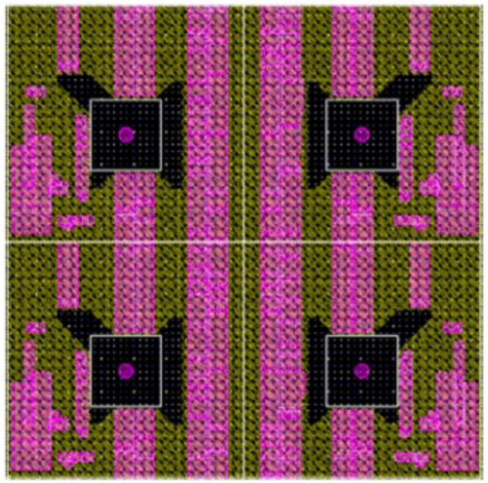
Sector 3
Med deep p-well





Sector 4
Max deep p-well

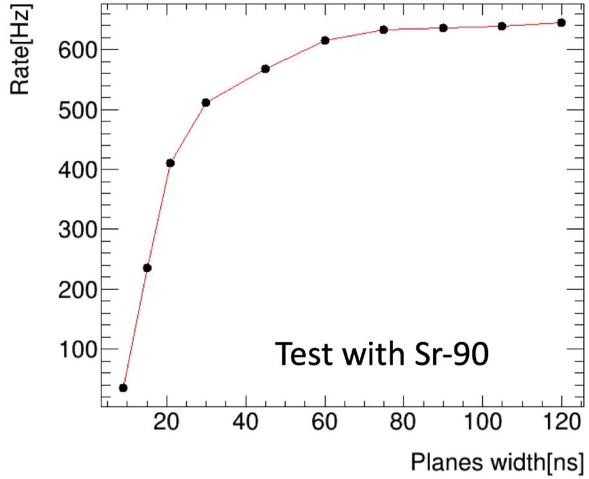


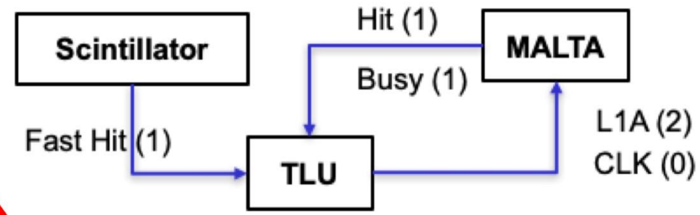


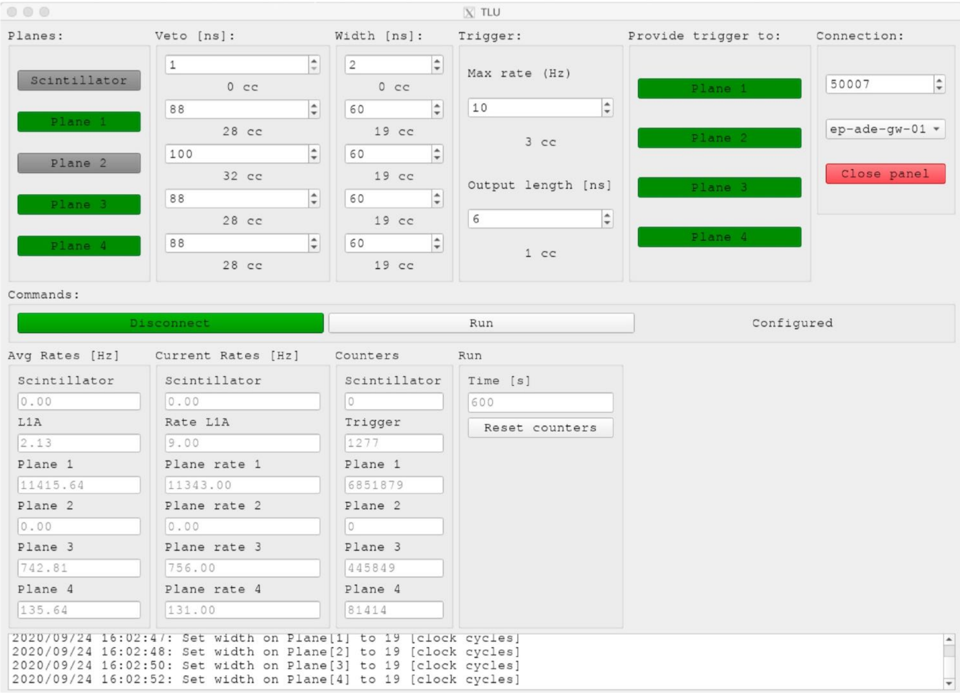
MALTA telescope TLU

Custom Kintex based Trigger Logic Unit (TLU)

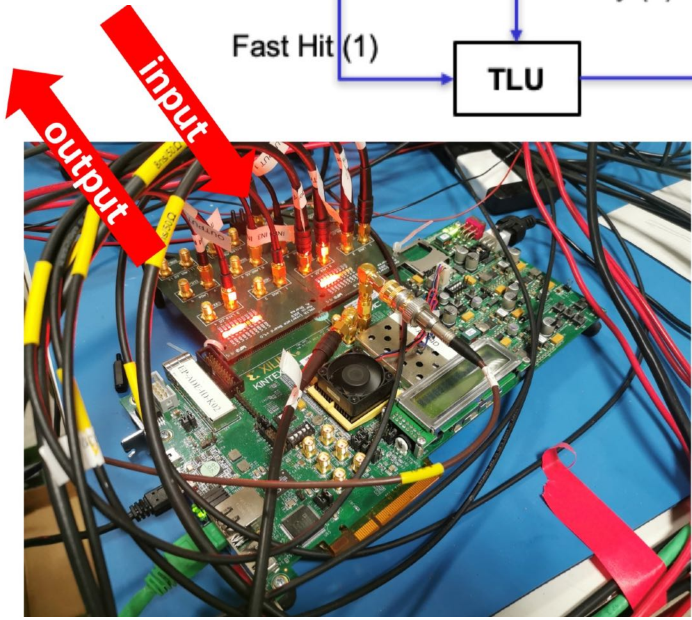
- VHDL FW, CMS IPbus and C++/python driven
- Veto, signals width and combination logic configurable from GUI
- Support for scintillator and up to 6 planes





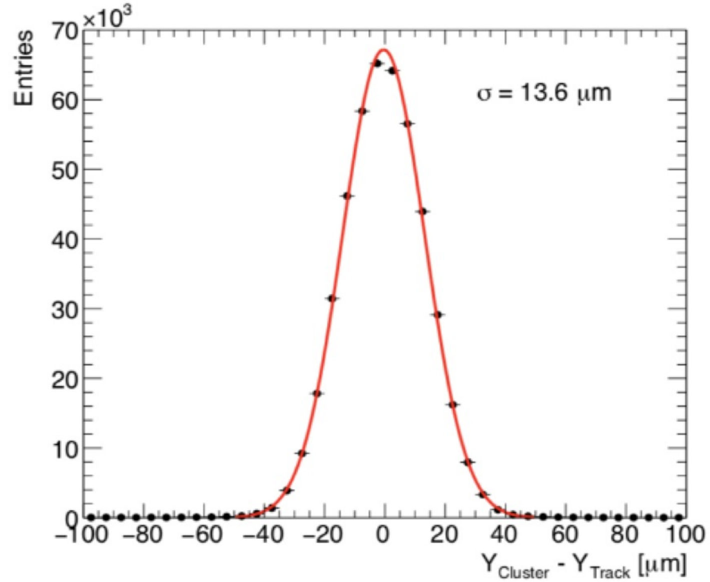


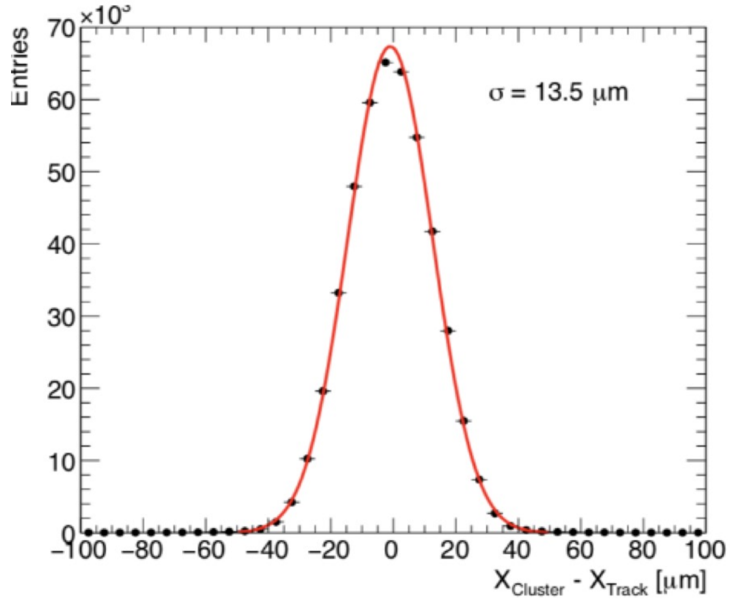
TLU GUI operating and monitoring telescope



MALTA telescope tracking

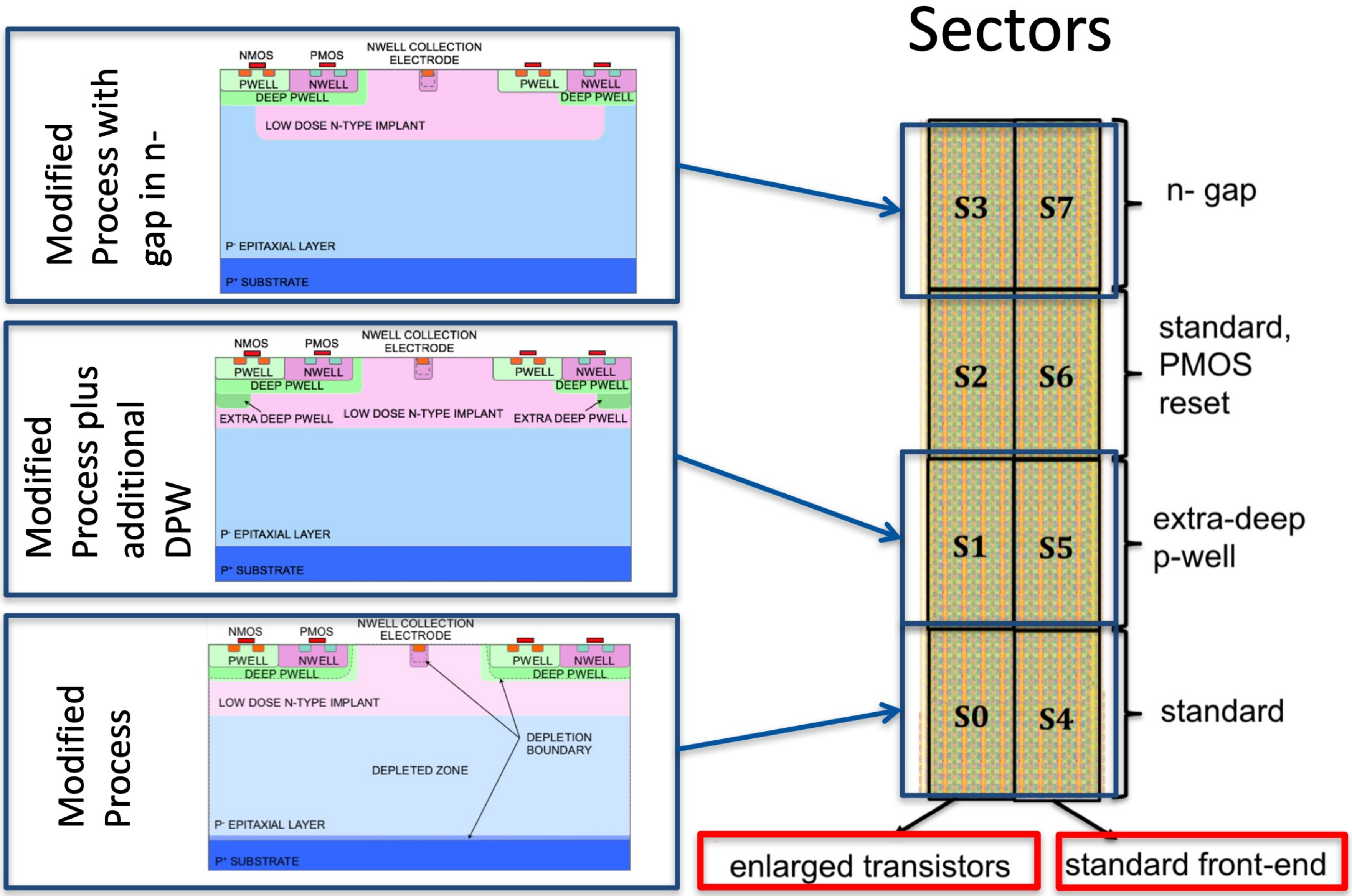
- Using General Broken Lines (GBL) algorithm to mitigate multiple scattering effects
- Tracking resolution
- Distance from the cluster barycenter to the track intercept using a clusterizer algorithm
- Embedded in Proteus software
- Using MALTA Cz un-irradiated



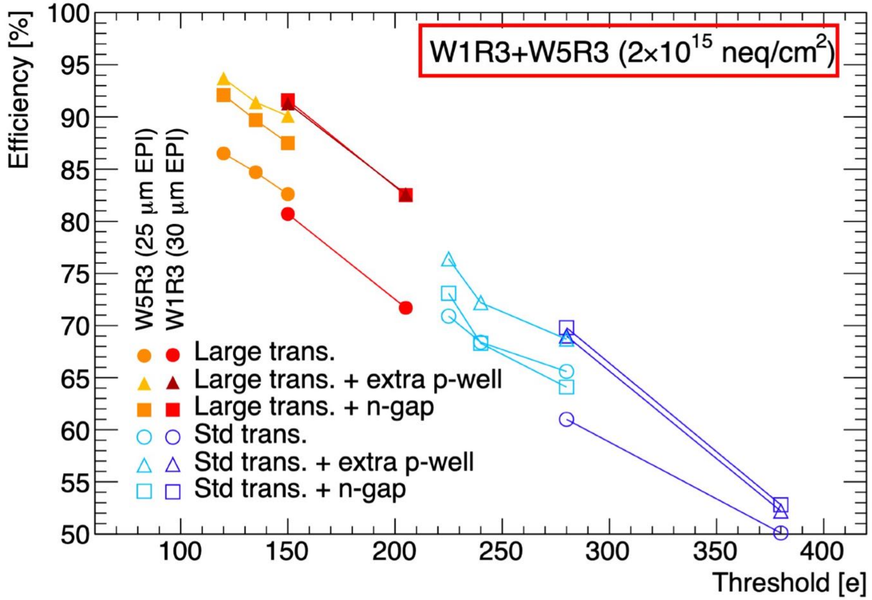


From ELSA test beam Apr 2019

Mini-MALTA


Sectors
Modified Process with gap in n-
NMOS
PMOS
NWELL COLLECTION ELECTRODE
PWELL
NWELL
DEEP PWELL
LOW DOSE N-TYPE IMPLANT
P- EPITAXIAL LAYER
P+ SUBSTRATE
Modified Process plus additional DPW
EXTRA DEEP PWELL
Modified Process
DEPLETION BOUNDARY
DEPLETED ZONE
S3
S7
S2
S6
S1
S5
S0
S4
n- gap
standard, PMOS reset
extra-deep p-well
standard
enlarged transistors
standard front-end

Mini-MALTA efficiency vs threshold



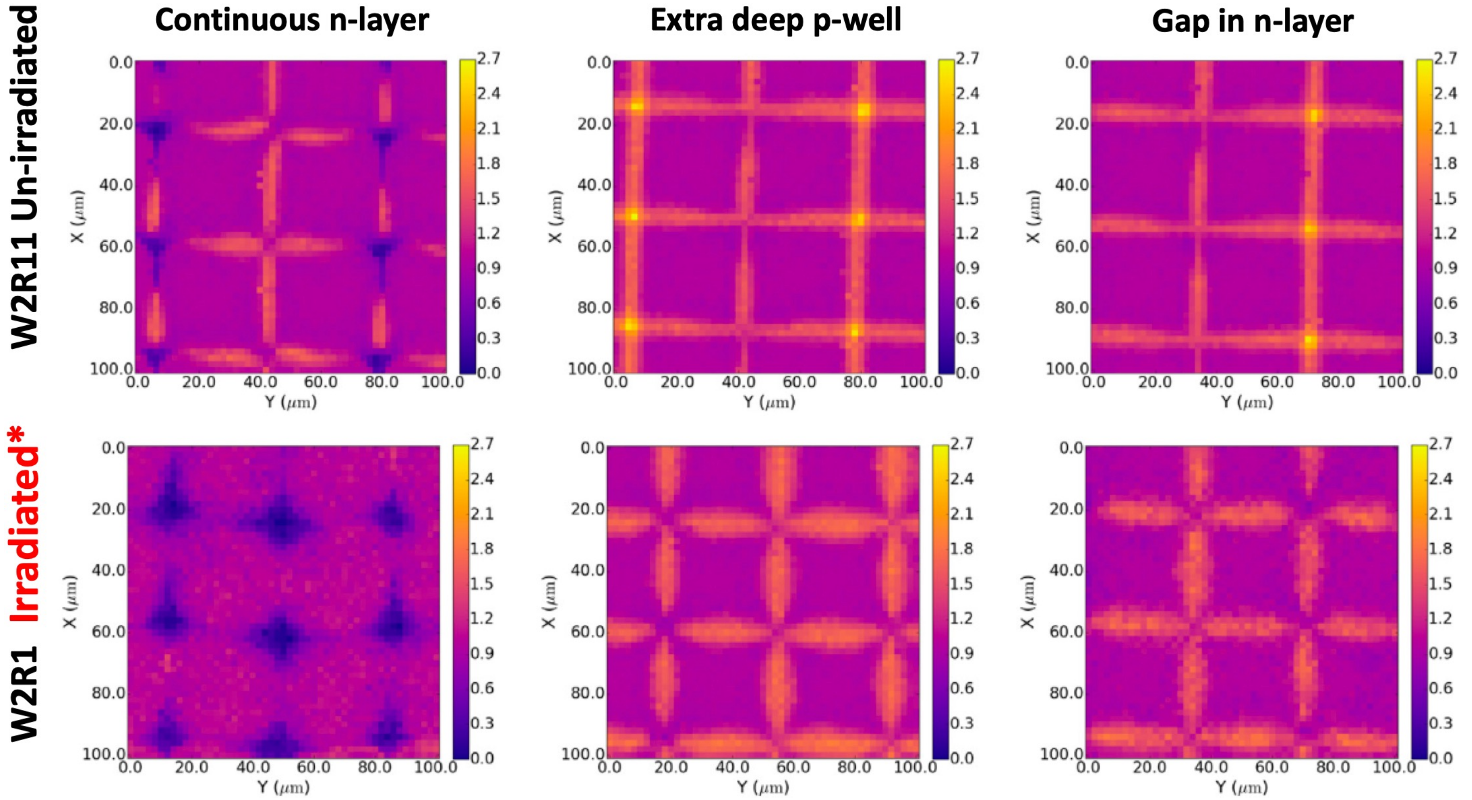
- Efficiency above 97% sensor modification with enlarged transitions
- Higher efficiency for enlarged transistors
- Efficiency above 90% after 2e15 neq /cm2 irradiation

Efficiency versus threshold for two different Mini-MALTA samples, neutron irradiated to 2e15 neq /cm2 , and measured with 2 GeV electron beam at ELSA, with 6 V bias voltage

Mini-MALTA Performance - Pixel response

Photon pixel response as function of dose

- Reduction of pixel response in continuous n-layer of 10%
- Almost no reduction on extra deep p-well and n-gap



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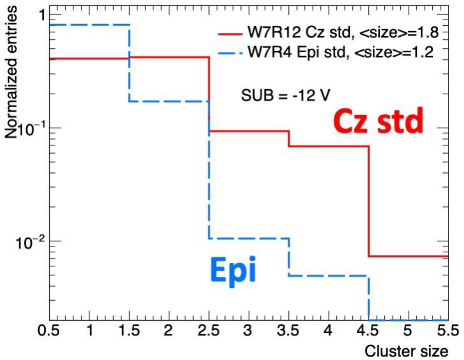
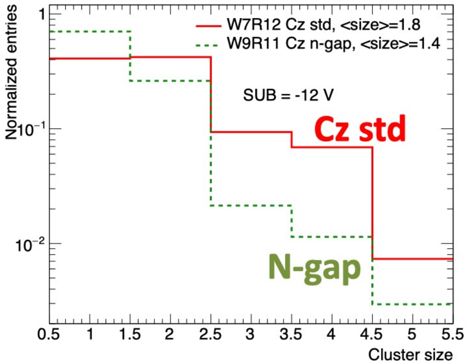
*Neutron-irradiated to 1e15 n_{eq}/cm^2

MALTA Performance - Epi vs Cz std & n-gap

Cluster size before irradiation at -12V:

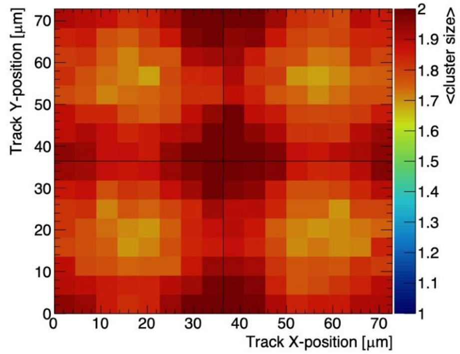
- Cz has a higher cluster size (1.8)
- Greater charge sharing
- Modified N-gap performs worse





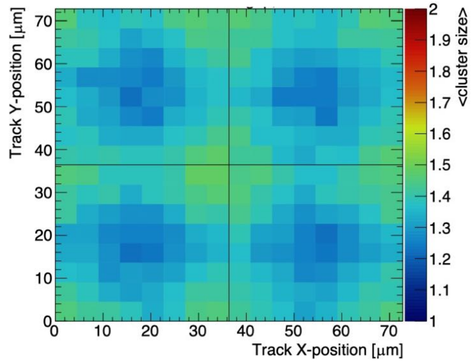
W7R12 Cz std, SUB=-12V

Cluster size 1.8



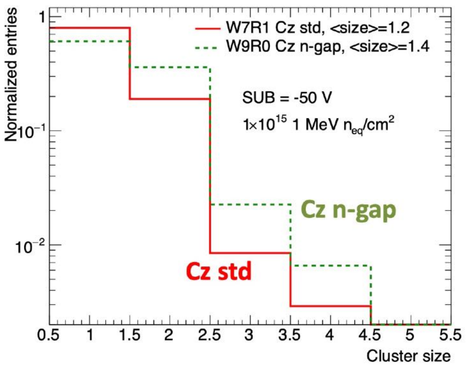
W9R11 Cz n-gap, SUB=-12V

Cluster size 1.4



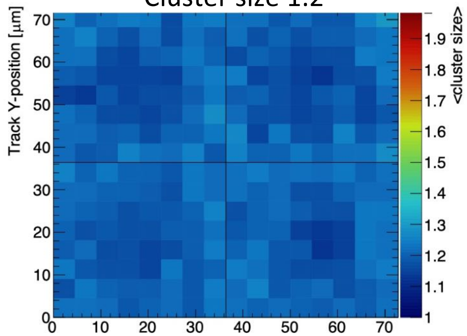
Cluster size after irradiation at -50V:

- 1E15 MeV n_{eq}/cm^2 at DESY with 4 GeV electron beam
- Cz standard more affected by irradiation : From 1.8 to 1.2
- Cz n-gap modification less affected: From 1.4 to 1.2



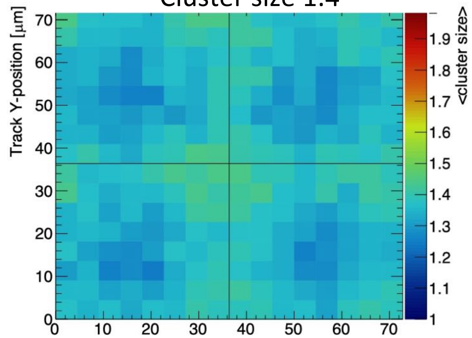
W7R1 Cz std, SUB=-50V

Cluster size 1.2



W9R0 Cz n-gap, SUB=-50V

Cluster size 1.4



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