Overview of the HL-LHC Upgrade for the CMS Level-1 Trigger

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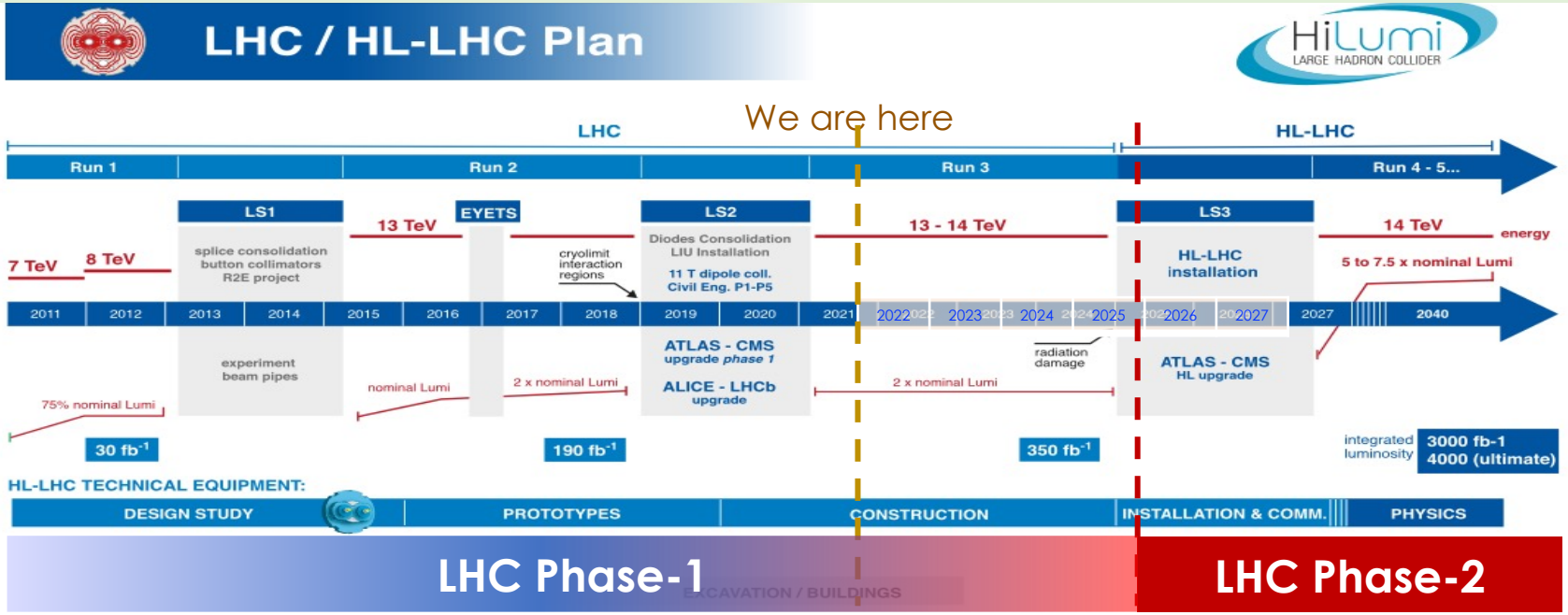
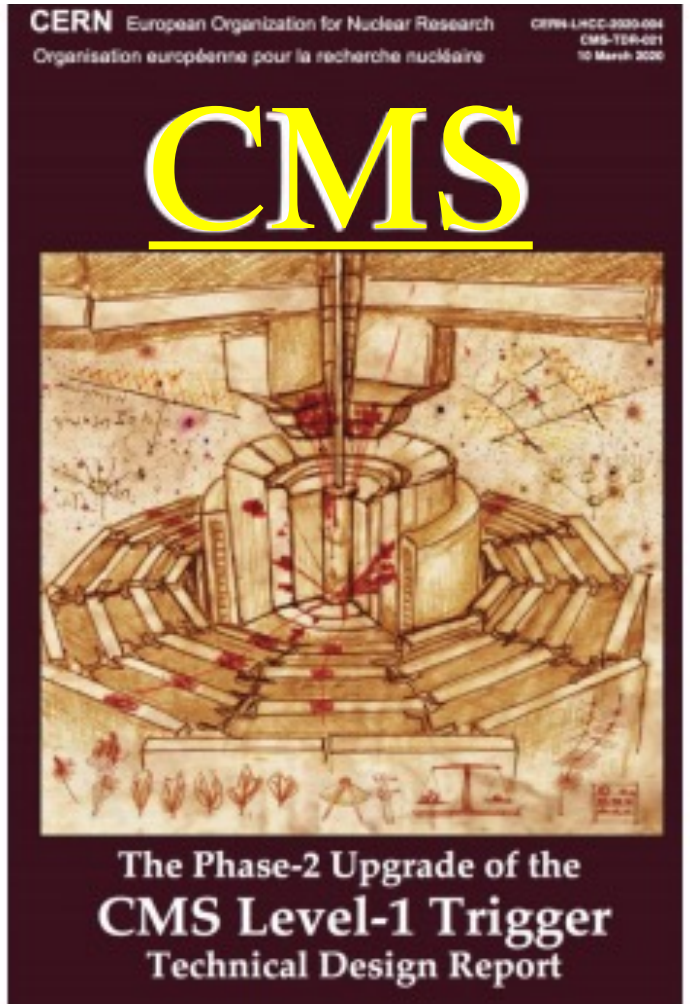
on behalf of the CMS Collaboration

High Luminosity LHC

- Rich & Ambitious Physics Program @ 13 TeV
- Luminosity: Nominal $5x10^{34}$ $cm^{-2}s^{-1}$ & 140 PU, Integrated = 3 ab^{-1}
- *Ultimate:* $7.5x10^{34}$ & 200 PU, Int. Lumi = 4 ab^{-1} (TDR studies)





Harsh Environment at HL-LHC:

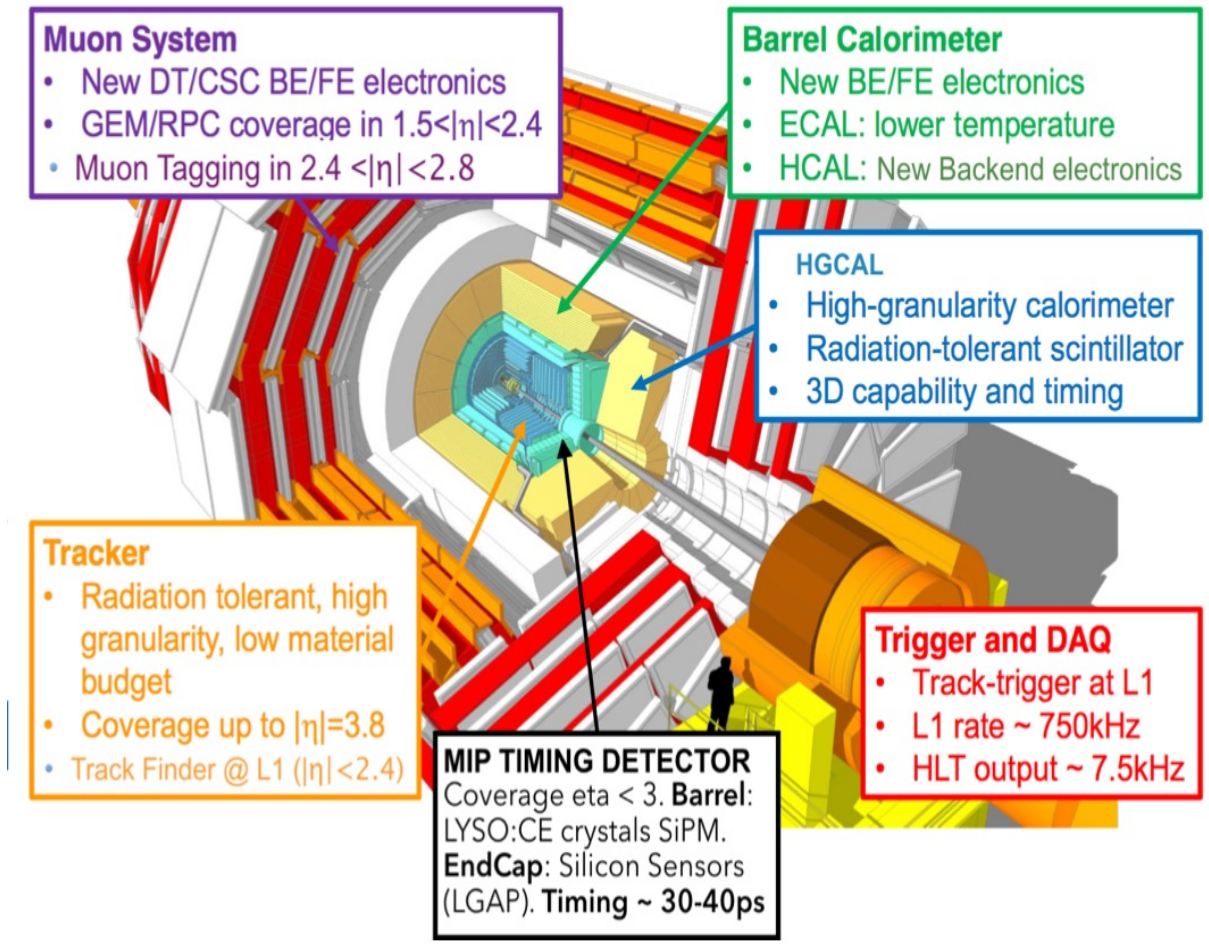
- 200 simultaneous interactions in a single bunch crossing (pileup)

Why HL-LHC ?

L1 Trigger TDR

- ***Unprecedented opportunity to explore uncharted territory***
  - High precision measurements in SM
  - Improved characterization of Higgs Sector
  - Unravel the blind spots and unconventional signatures in BSM scenarios

- ***How to address***
  - ✓ Large data sample
  - ✓ Upgraded detector (extended coverage)
  - ✓ Advanced selection algorithms
  - ✓ Sophisticated triggers to select specific topologies such as VBS/VBF, rare B-meson decay, etc.
  - ✓ Scouting system



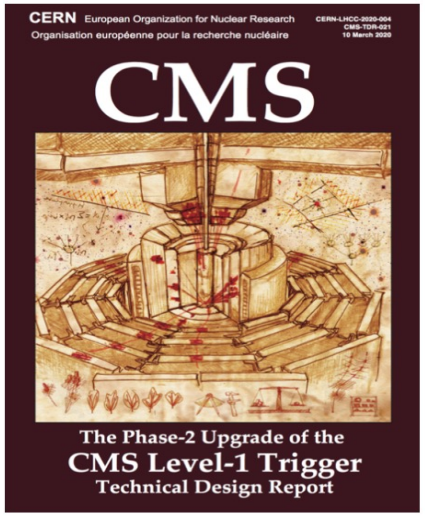
Phase-2 Trigger Upgrade

L1 Trigger TDR

CMS Phase-2 will keep two-level of triggering system: L1 & HLT

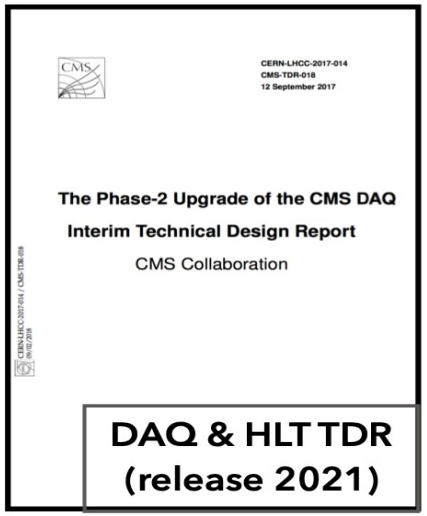
➢ *Level-1 (hardware based) Trigger*

- Extensive use of state-of-the-art FPGAs
- Increase bandwidth: 100 kHz ⇒ 750 kHz
- Increase Latency: 3.8 μs ⇒ 12.5 μs
- Higher granularity (calorimeters & muon systems) and tracking information
- Sophisticated object reconstruction and correlation
- Enhanced physics selection & Scouting system



➢ *High Level (software) Trigger*

- Optimize reconstruction: Improve physics reach, maintain thresholds while increasing efficiency and stay within computing resources.
- Reduction rate (100:1) 1 kHz ⇒ 7.5 kHz
- Data throughput: 2.5 Gb/s ⇒ 61 Gb/s
- Heterogenous architecture – CPU/GPU



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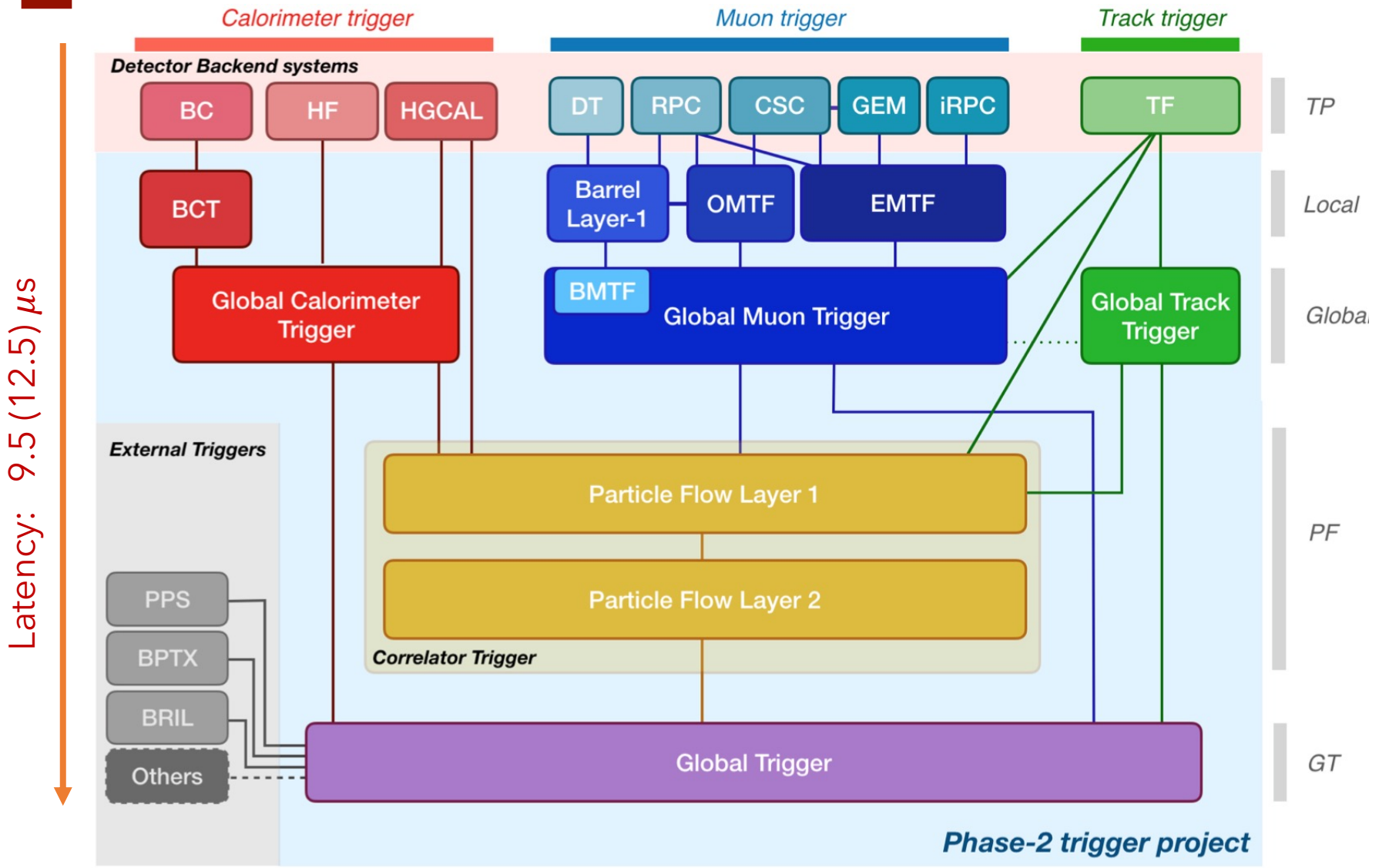
Phase-2: Level-1 Trigger

Level-1 Trigger TDR

L1 Phase-2 Upgrade: Conceptual Design



Designed to benefit from upgraded detectors to sustain a high efficiency of physics event selection

Some key features:

- Introduction of correlator layer – sophisticated algos
- Optimum flexibility of design – robustness
- Four independent data processing paths: tracking, calorimeter, muon systems, particle flow techniques

L1 Phase-2 Upgrade: Key Features

- *Calorimeter Trigger Path*
  - BCT and HGCAL backend to process high-granularity information from calorimeters to produce high-resolution clusters and identification variables
  - HGCAL – completely new calorimeter to cope with high radiations in the forward region
  - 3D granularity allows particle flow reconstructions and helps reduce pile-up
  - Crystal level granularity in BCT to give better position resolution and thus better distinction between jets, electrons and photons
  - Build calorimeter based objects - e/γ, τ_{hadronic}, jets, energy sums

- *Muon Trigger Path:*
  - Additonal muon stations to be installed to extend coverage up to $|\eta| = 2.8$ (2.4)
  - Muon track finders organized in three regions: Barrel, Endcap and Overlap

L1 Phase-2 Upgrade: Key Features

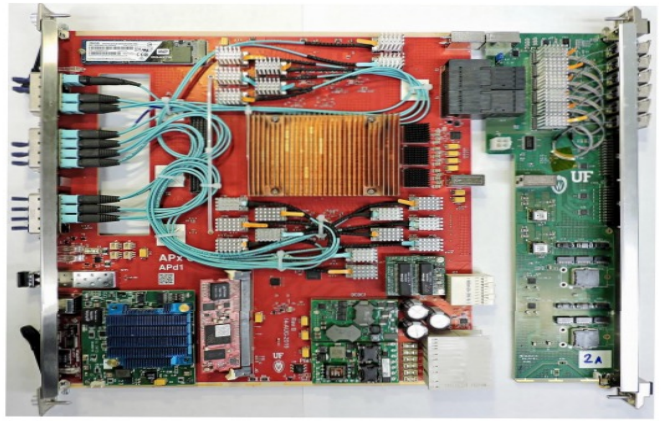
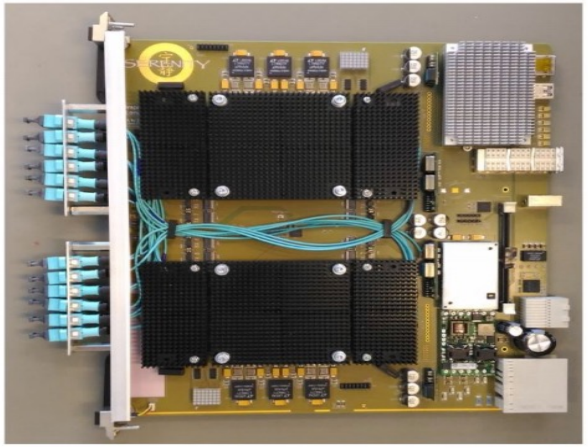
- *Track Trigger Path*
  - Inclusion of data from outer tracker, made possible by readout rate of silicon tracking info @ 40 MHz
  - Reconstruction quality flag helps to achieve precise vertex reconstruction and matching to calo and muon systems
  - This key feature maximizes the trigger efficiency while keeping the trigger rate within the allowed budget

- *Particle Flow Trigger Path (Correlator Trigger)*
  - Sophisticated algorithms (e.g. particle flow) with information from all sub-detectors
  - Significant improvements for complex objects
    - PF MET has a rate twice as low as the track-based MET and ~6 times as low as calorimeter-based MET
  - Lower HT trigger threshold than with track- or calo-only information

L1 Phase-2 Upgrade: Hardware

L1 Trigger TDR

Large efforts to upgrade the L1 system to extend Physics capabilities

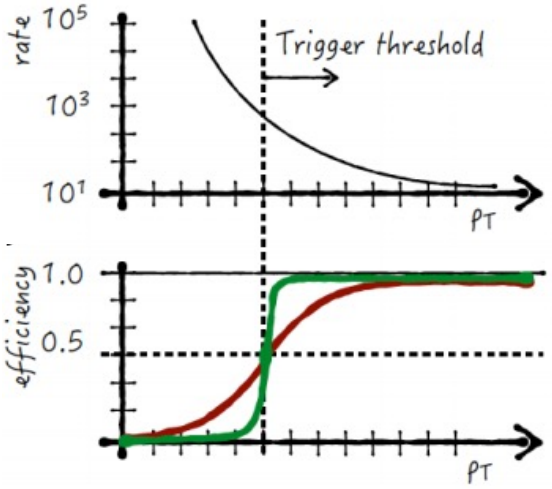
- Four family of boards (digital processors) based on cutting-edge hardware technology
  - Xilinx's Ultra Scale Plus family (VU9P, VU13P) FPGA
- Generic processing engines
  - High speed optical links (28 Gbps)
  - Allows for more complex algorithms and more I/O per boards
  - Huge input data bandwidths (63 TB/s)

- High-Level-Synthesis: Vivaldo-HLS being used successfully, novel techniques based on ML also being implemented
- Advanced Architecture: Platform and interconnections (ATCA) → robust, flexible & modular design

L1 Phase-2 Upgrade: Algorithm

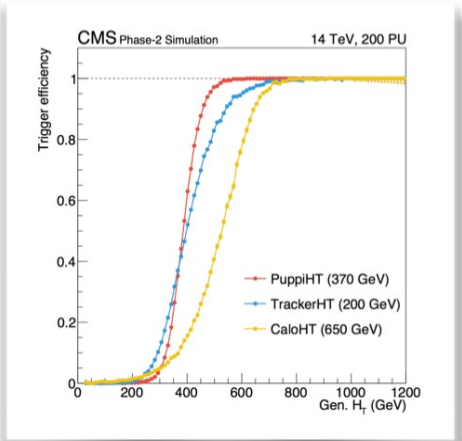
L1 Trigger TDR

- Exploit tracking information to reach offline performance & reconstruction of primary vertex
- Maintain flexibity and robustness:
  - Standalone objects: based on individual sub-detector
  - Track-matched objects: tracking information used to verify standalone Muon & Calo objects
  - Particle Flow objects: Combine all info to match offline algorithms, require most processing time & resources for calculation but yields best performance

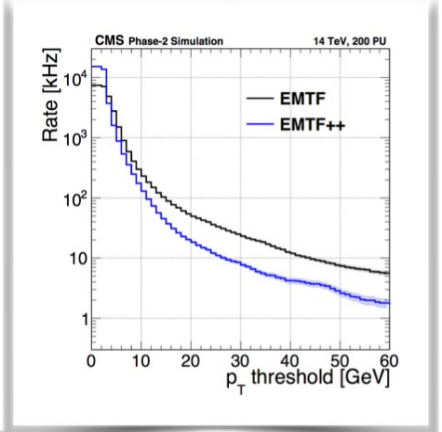


Level-1 Menu:
Simplified: Phase-1 physics built from Run-2 L1 menu (~350 kHz)

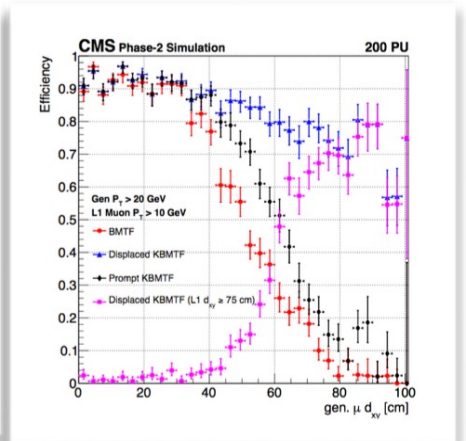
Extended: New trigger strategies to expand physics reach (+~100 kHz)



Particle-flow/PUPPI HT



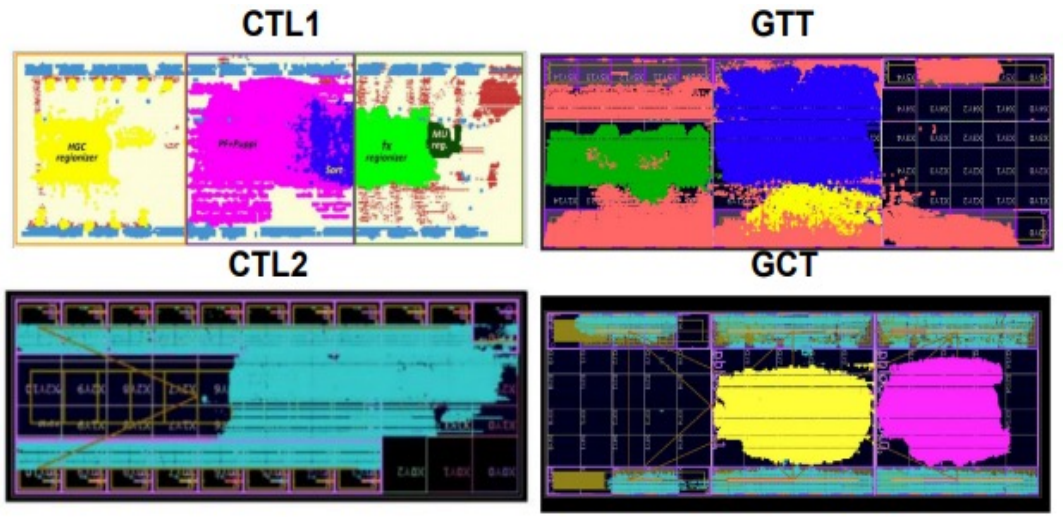
Standalone forward Muon reconstruction

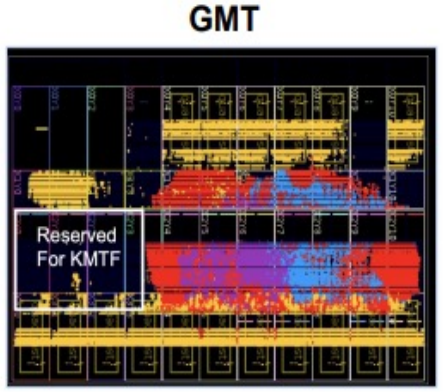


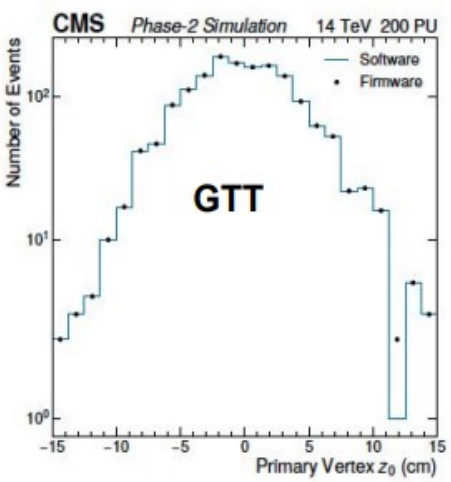
Displaced barrel muon trigger (Kalman Filter)

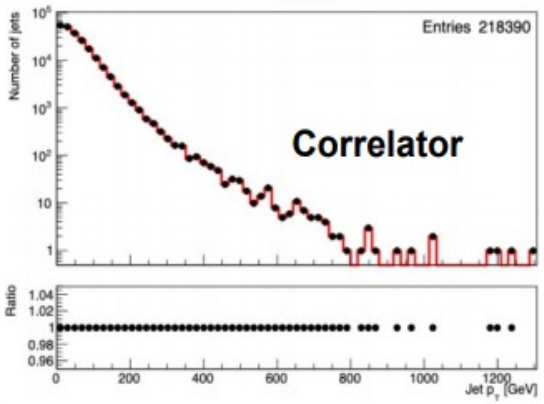
L1 Phase 2 Upgrade: FW Integration

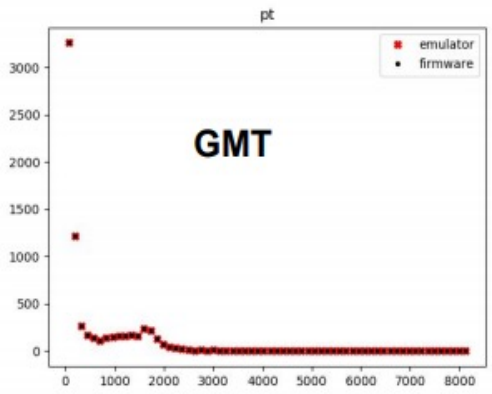
- Integration of a version of all algorithms in different boards has been implemented
- All families of boards have infrastructure ready for integration and testing
- Pre-productions/testing/integration going relatively smoothly despite COVID challenges











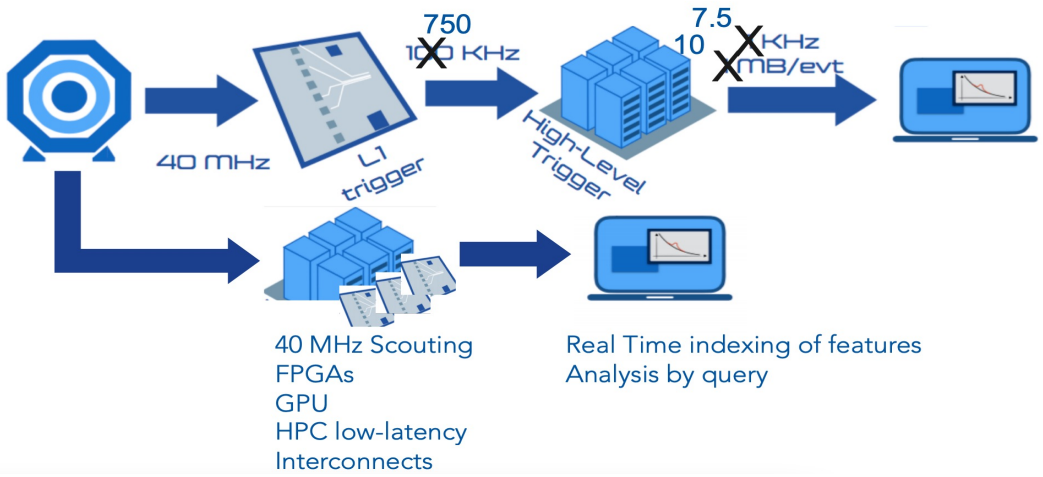
- Very good agreement between emulator and firmware for many complex algorithms
- Boosted by the High level Synthesis paradigm

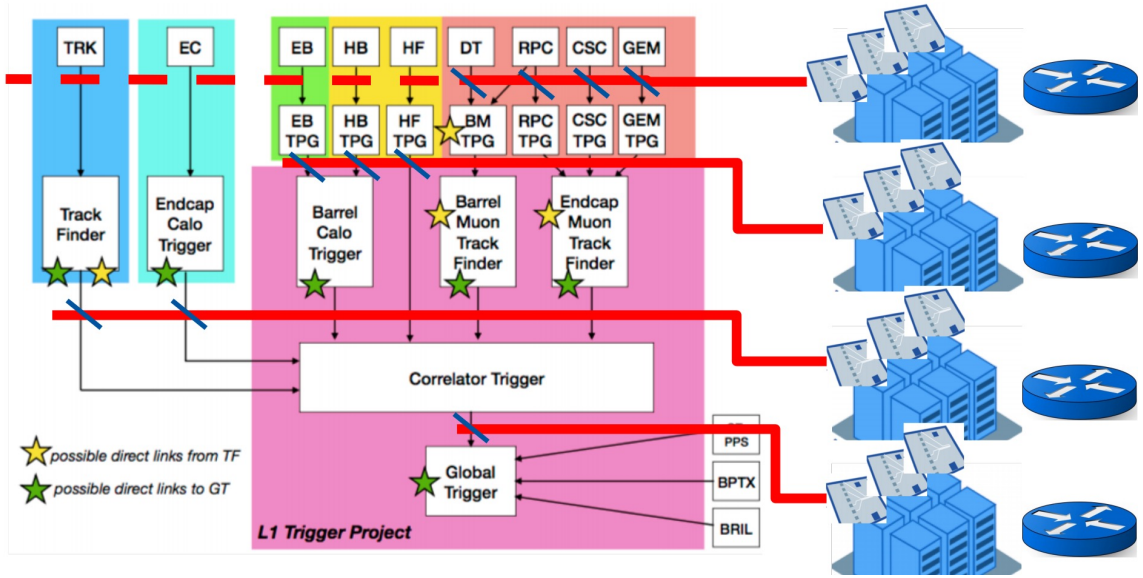
40 MHz Scouting

L1 Trigger TDR

Store subset of raw data or pre-processed HLT by products

- Make use of spare optical outputs of different sub-systems
- Timely and virtually unlimited-statistics diagnostics
- Potential window on interesting physics, where
  - Signature too common to be within L1 budget
  - Have no model to drive trigger design
  - Can do with or without full detector resolution





Analyse multiple contiguous BX, identify signatures unreachable through standard trigger techniques

Physics case:

- Higgs Rare decays (very limited statistics)
- Dark Sector (Zero or short lifetime)
- More Exotic Searches
  - Displaced particles
  - Slow moving/appearing/disappearing

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Summary

Level-1 Trigger TDR

Summary

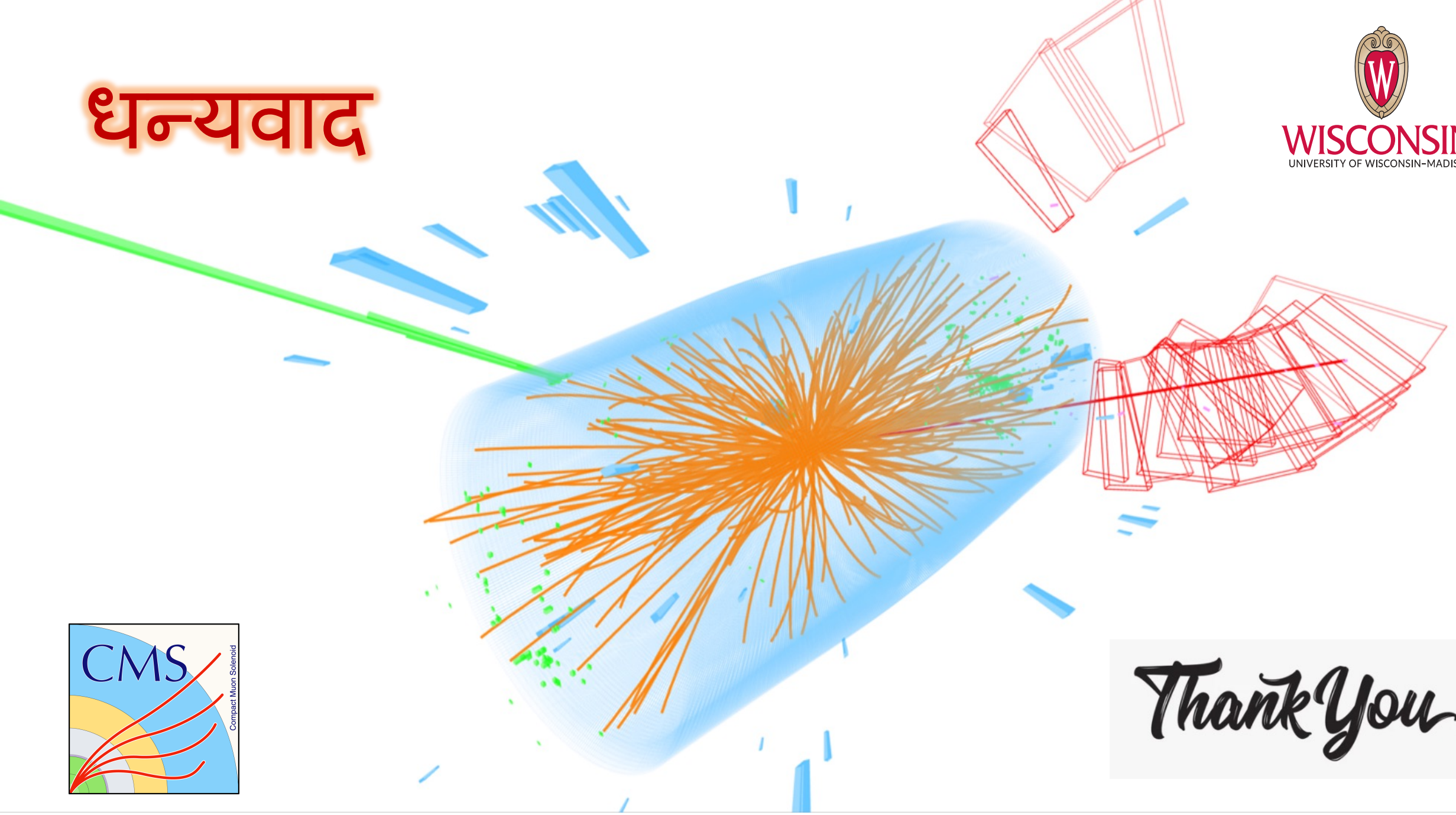
L1 Trigger TDR

- Rich & Ambitious physics program possible due to upgrades to the L1 Trigger system
- CMS working towards firm solution to triggering & DAQ challenges @ HL-LHC

- *Major improvements expected in Level-1 Trigger:*
  - Tracking based trigger, Higher granularity in the barrel ECAL, Extended coverage in the muon systems, New calorimeter in endcaps (3D granularity)
  - Sophisticated algorithms are prototyped in FPGAs (Xilinx's UltraScalePlus/28 Gbps Links)
  - Modular and flexible architecture
  - Hardware demonstrations performed, board-to-board testing planned for different sub-systems
  - Project moving forward with construction

- HLT Trigger
  - Innovative heterogeneous architecture (CPU/GPU)
  - TDR due in few months

धन्यवाद



Thank You

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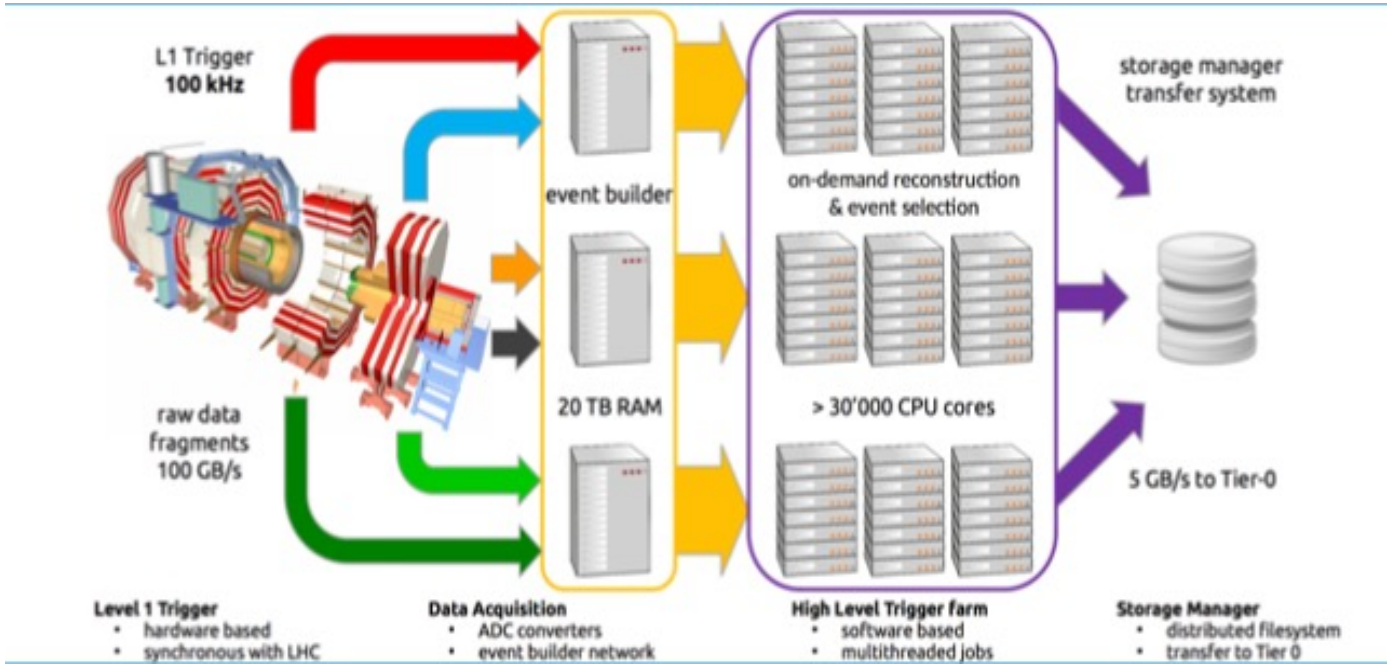
Additional material

HLT Phase-2 Upgrade

- Software algorithms running asynchronously on commercial computing hardware
- Make use of full detector data to select events for offline storage and analysis
- **Goal:** Attain rejection factor 100:1 (while tracking available @L1), keeping timing < 500 ms
  - *Reconstruction:* More complex detector (HGCAL, tracking, timing layer, etc.)
  - *Timing:* Increase with inst luminosity (7.5x input event rate), but also with pile-up

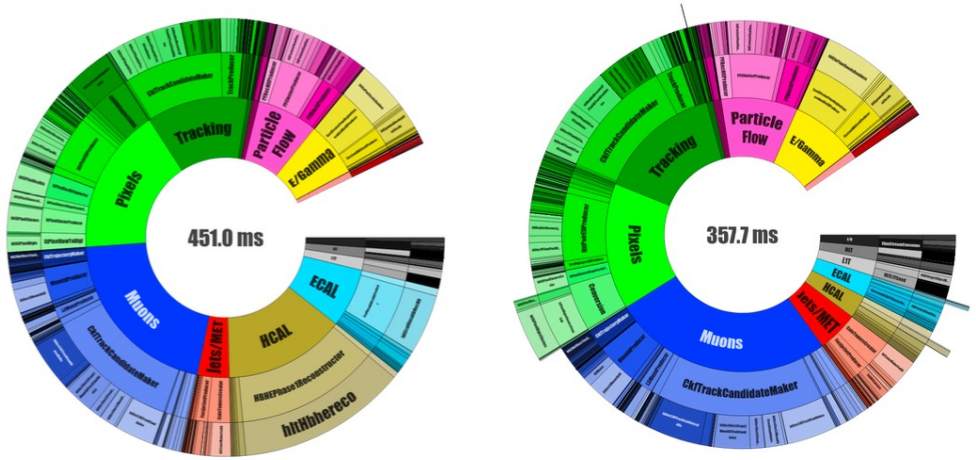
CMS detector Peak <PU>	LHC Phase-1 <60>	HL LHC <200>
Event size at HLT input	2 MB	10 MB
Evt network Throughput	1.6 Tb/s	60 Tb/s
Evt networ buffer	12 TB	445 TB
HLT accept rate	1 kHz	7.5 kHz
Evt size at HLT output	1.4 MB	6.9MB



HLT Phase-2 Upgrade

Heterogeneous Architecture

- Same framework & algorithm as used in offline reconstruction
  - Rapid deployment of new triggers (based on physics needs), reproducibility, trigger efficiency
- Run-1 & 2 used general purpose CPUs
- The adoption of heterogeneous architectures for the HLT, using GPUs is foreseen as a strategy for the deployment of the necessary computing power at an affordable price
- Current HLT R&D: Coprocessors and GPUs as offload engines for specific algos
- Plan to implement during Run-3 (gaining experience on running with GPUs and heterogeneous architectures.



(a) CPU-only (b) CPU and GPU

CPU time profile of Run-3 HLT menu w/ & w/o GPU acceleration. Timing has been measured on pileup 50 events from Run2018D on a full HLT node (2x Intel Skylake Gold 6130) with HT enabled, running 16 jobs in parallel, with four threads each. In the right plot, a NVIDIA Tesla T4 was also used.